SY2A21731 Series
Automotive Camera PMIC

General Description

The SY2A21731 is a highly integrated PMIC that consists of one primary DC-DC buck regulator (Buck 1), two secondary DC-DC buck regulators (Buck 2 and Buck 3), and one secondary LDO. It is designed to power automotive camera modules and can operate across a wide input voltage range from 4V to 16V (absolute maximum of 18V).

All three DC-DC converters use fixed frequency peak current control. The operating frequency is set to 2.2MHz (typ) in order to avoid generating noise in the AM radio band. A spread-spectrum function for the internal clock is integrated to achieve good EMI performance. The low voltage BUCK converters operate out of phase (180 degrees phase shift) to reduce crosstalk between channels.

The SY2A21731 features protection against input overvoltage (OVP), buck and LDO output overvoltage, buck overcurrent (OCP), and overtemperature (OTP).

The SY2A21731 is available in a QFN3×3 -16 package.

Applications

- Automotive Camera Modules

Key Features

- 4V to 16V Input Voltage Range
- 2.2MHz Fixed Switching Frequency
- Primary Synchronous Buck Converter (Buck 1)
  - Fixed Output Voltage: 3.3V/3.8V (optional)
  - Maximum Continuous Output Current: 1.5A
  - Low $R_{DS(ON)}$ Switches: 220mΩ High Side/120mΩ Low Side
- Secondary Synchronous Buck Converter (Buck 2)
  - Fixed Output Voltage: 1.1V/1.2V (optional)
  - Maximum Continuous Output Current: 1.5A
  - Low $R_{DS(ON)}$ Switches: 220mΩ High Side/180mΩ Low Side
- Secondary Synchronous Buck Converter (Buck 3)
  - Fixed Output Voltage: 1.8V
  - Maximum Continuous Output Current: 1A
  - Low $R_{DS(ON)}$ Switches: 320mΩ High Side/220mΩ Low Side
- Secondary LDO
  - Output Voltage: 2.8V/2.9V/3.3V (optional)
  - Maximum Output Current: 300mA
- Spread Spectrum Frequency Modulation
- AEC-Q100 Grade 1 Qualified
- Compact Package: QFN3mm×3mm-16, Wettable Flank

Typical Application

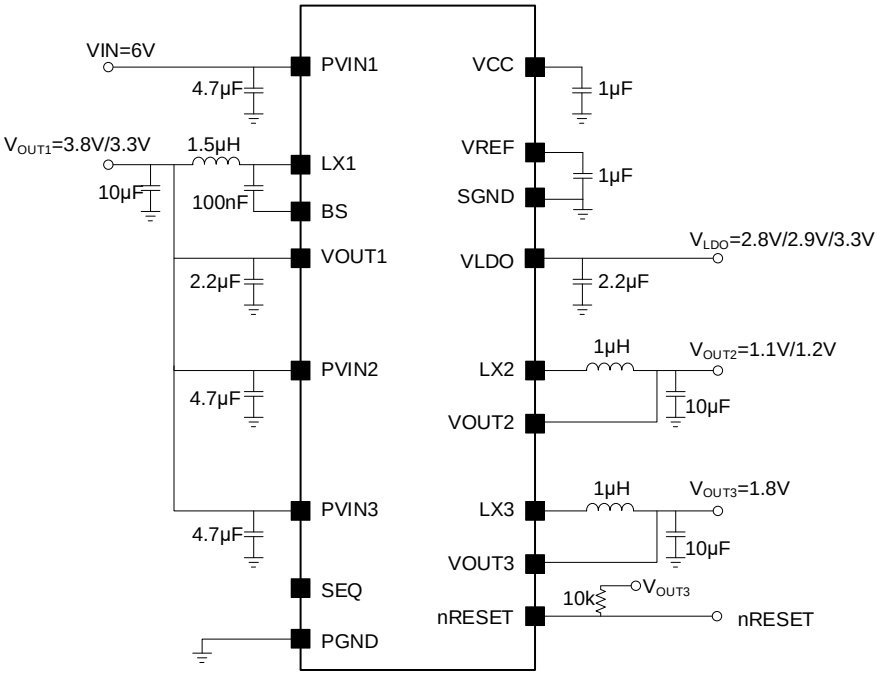


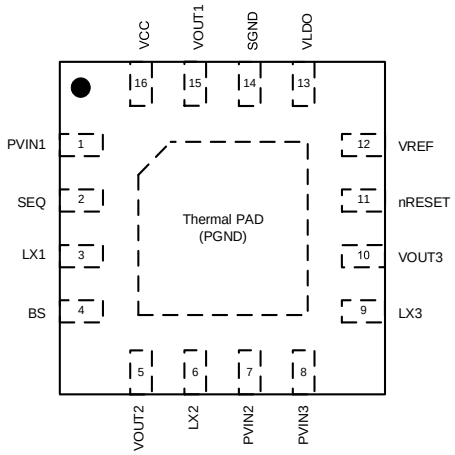
Figure 1. Application Circuit

Ordering Information

Ordering Number	Top Mark	Buck 1	Buck 2	Buck 3	LDO	nRESET Delay Time	Package Type
SY2A21731QDQ	**GCT*xyz***	3.8V	1.1V	1.8V	3.3V	2ms	QFN3×3-16 RoHS-Compliant and Halogen-Free
SY2A21731BQDQ	**HGH*xyz***	3.3V	1.2V	1.8V	2.8V	2ms	
SY2A21731CQDQ	**HGJ*xyz***	3.8V	1.2V	1.8V	3.3V	2ms	
SY2A21731DQDQ	**HKRxyz**	3.3V	1.1V	1.8V	2.8V	2ms	
SA47302FQDQ	**HNKxyz**	3.3V	1.1V	1.8V	2.9V	2ms	
SA47302JQDQ	**AALYxyz**	3.3V	1.2V	1.8V	2.8V	8ms	
SA47302HQDQ	**AAKYxyz**	3.8V	1.1V	1.8V	3.3V	8ms	

x = year code, y = week code, z = lot number code

Pinout (top view)



(QFN3×3-16)

Pin Description

Pin No	Pin Name	Pin Description
1	PVIN1	Power supply of primary buck converter (Buck 1)
2	SEQ	Sequence control pin
3	LX1	Switch node of primary buck converter (Buck 1)
4	BS	Bootstrap pin of primary buck converter (Buck 1) high side switch. Connect a typical 100nF capacitor from this pin to the LX1 pin to supply the high side switch driving voltage.
5	VOUT2	Output feedback pin of secondary buck converter Buck 2
6	LX2	Switch node of secondary buck converter Buck 2
7	PVIN2	Power supply of Buck 2. This pin is internally connected to PVIN3.
8	PVIN3	Power supply of Buck 3. This pin is internally connected to PVIN2.
9	LX3	Switch node of secondary buck converter Buck 3
10	VOUT3	Output feedback pin of secondary buck converter Buck 3
11	nRESET	Open-drain reset output. nRESET at high state indicates all outputs operate correctly.
12	VREF	Internal reference pin. Connect a 1μF capacitor from this pin to SGND.
13	VLDO	LDO output
14	SGND	Analog ground
15	VOUT1	LDO input pin and primary buck converter (Buck 1) output feedback pin
16	VCC	Gate drive LDO output for primary buck converter (Buck 1)
Thermal PAD	–	Device thermal PAD and PGND connection. Connect to main ground plane for proper operation.

Block Diagram

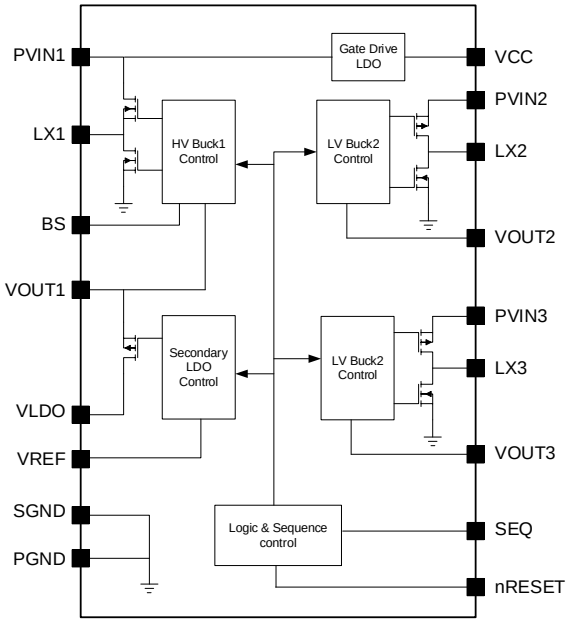


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
PVIN1, LX1 to GND	-0.3	18	V
BS to LX1	-0.3	6	
PVIN2, PVIN3, LX2, LX3, VOUT1, VOUT2, VOUT3 to GND	-0.3	6	
VCC, VREF, VLDO to GND	-0.3	6	
SEQ, nRESET to GND	-0.3	6	
Junction Temperature Range		150	°C
Lead Temperature (Soldering, 10 sec.)		260	
Storage Temperature	-65	150	
ESD Susceptibility			
HBM (Human Body Mode)	±2000		V
CDM (Charge Device Mode) All Pins	±500		

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	34	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	5.4	
Continuous Power Dissipation	3.53	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Supply Voltage PVIN1	4	16	V
Supply Voltage PVIN2，PVIN3	2.7	5	
Junction Temperature Range	-40	150	°C
Ambient Temperature Range	-40	125	

Electrical Characteristics

(V_{IN} = 8V, V_{OUT1} = 3.3V/3.8V, V_{OUT2} = 1.1V/1.2V, V_{OUT3} = 1.8V, V_{LDO} = 2.8V/2.9V/3.3V, T_A = 25°C for Typ value, Min-Max covers from -40°C to 125°C, unless otherwise specified. (Note 4))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
System	Undervoltage Lockout Threshold	UVLO_H	V_{IN} rising	3.9	4.05	4.2	V
		UVLO_L	V_{IN} falling	3.68	3.8	3.92	
	Input Undervoltage Lockout Deglitch Time	UVLO_DT	V_{IN} UVLO deglitch time		32		μs
	Maximum Input Voltage	PVIN1_MAX			16		V
	Input Overvoltage Protection	V_{IN_OV}		18	18.5	19	
CH1 HV Buck 1	Power Supply Voltage Range	V_{VIN}		4.0	8.0	16.0	V
	Output Voltage Range	V_{OUT1}	See Ordering Information		3.3		V
			See Ordering Information		3.8		
	Output Feedback Voltage Accuracy			-2		2	%
	Switching Frequency	F_{SW_HV1}	PVIN1 > 6V	1.98	2.2	2.42	MHz
	Spread-Spectrum Range	SS_{HV1}		+4	+6	+8	%
	Switching Minimum On-Time	$T_{ON\_MIN\_HV1}$			60	80	ns
	Maximum Duty Cycle	D_{MAX}		95			%
	High Side MOSFET On-Resistance	$R_{ON\_HS\_HV1}$	From PVIN1 pin to LX1 pin	120	220	390	mΩ
	Low Side MOSFET On-Resistance	$R_{ON\_LS\_HV1}$	From LX1 pin to PGND pad	20	120	210	mΩ
	Inductor Peak Current Limit	$I_{CL\_PK\_HV1}$		2.125	2.5	2.875	A
	Inductor Valley Current Limit	$I_{CL\_VL\_HV1}$			3		A
	Negative Inductor Peak Current Limit	$I_{CL\_NPK\_HV1}$			1.5		A
	Output Discharge Resistor	R_{DIS_HV1}		135	270	405	Ω
	Output Undervoltage Falling Threshold	UVP_{F_HV1}		40	50	60	%
	Output Undervoltage Deglitch Time	$T_{UVP\_D\_LV1}$		15	30	45	μs
	Output Feedback Overvoltage Rising Threshold	OVP_{R_HV1}		115	120	125	%
CH2 LV Buck 2	Output Voltage	V_{OUT2}	See Ordering Information		1.1		V
			See Ordering Information		1.2		
	Output Voltage Accuracy	$V_{OUT\_ACC\_LV2}$		-1.5		1.5	%
	Switching Frequency	F_{SW_LV2}		1.98	2.2	2.42	MHz
	Spread-Spectrum Range	SS_{LV2}		+4	+6	+8	%
	Switching Minimum On-Time	$T_{ON\_MIN\_LV2}$			60	80	ns
	High-Side MOSFET On-Resistance	$R_{ON\_HS\_LV2}$	From PVIN2 pin to LX2 pin	120	220	390	mΩ
	Low-Side MOSFET On-Resistance	$R_{ON\_LS\_LV2}$	From LX2 pin to PGND pad	50	180	290	mΩ
	Inductor Peak Current Limit	$I_{CL\_PK\_LV2}$		1.785	2.1	2.415	A
	Inductor Valley Current Limit	$I_{CL\_VL\_LV2}$			2.4		A
	Negative Inductor Peak Current Limit	$I_{CL\_NPK\_LV2}$			0.8		A
	Output Discharge Resistor	R_{DIS_LV2}		50	100	150	Ω
	Output Undervoltage Falling Threshold	UVP_{F_LV2}		40	50	60	%
	Output Undervoltage Deglitch Time	$T_{UVP\_D\_LV2}$		15	30	45	μs

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
	Output Overvoltage Rising Threshold	OVP_{LV2}		115	120	125	%
	Input Overvoltage Threshold	$OVP_{IN\_R\_LV2}$		4.9	5.2	5.5	V
CH3 LV Buck 3	Output Voltage	V_{OUT3}			1.8		V
	Output Voltage Accuracy	$V_{OUT\_ACC\_LV3}$		-1.5		1.5	%
	Switching Frequency	F_{SW_LV3}		1.98	2.2	2.42	MHz
	Spread-Spectrum Range	SS_{LV3}		+4	+6	+8	%
	Switching Minimum On-Time	$T_{ON\_MIN\_LV3}$			60	80	ns
	High Side MOSFET On-Resistance	$R_{ON\_HS\_LV3}$	From PVIN3 pin to LX3 pin	170	320	520	mΩ
	Low Side MOSFET On-Resistance	$R_{ON\_LS\_LV3}$	From LX3 pin to PGND pad	80	220	350	mΩ
	Inductor Peak Current Limit	$I_{CL\_PK\_LV3}$		1.3	1.53	1.76	A
	Inductor Valley Current Limit	$I_{CL\_VL\_LV3}$			1.8		A
	Negative inductor Peak Current Limit	$I_{CL\_NPK\_LV3}$			0.8		A
	Output Discharge Resistor	R_{DIS_LV3}		50	100	150	Ω
	Output Undervoltage Falling Threshold	UVP_{F_LV3}		40	50	60	%
	Output Undervoltage Deglitch Time	$T_{UVP\_D\_LV3}$		15	30	45	μs
	Output Overvoltage Threshold	OVP_{LV3}		115	120	125	%
	Input Overvoltage Threshold	$OVP_{IN\_R\_LV3}$		4.9	5.2	5.5	V
CH4 LDO	Output Voltage	V_{LDO}	See Ordering Information		2.8		V
			See Ordering Information		2.9		
			See Ordering Information		3.3		
	Output Voltage Accuracy	$V_{OUT\_ACC\_LDO}$		-1.5		1.5	%
	Maximum Output Current	$I_{OUT\_MAX\_LDO}$		300			mA
	Dropout Voltage	V_{DROP_300}	I_{OUT_LDO} = 300mA			300	mV
		V_{DROP_150}	I_{OUT_LDO} = 150mA			150	
	Output Current Limit	I_{CL_LDO}		345	450	555	mA
	Output Discharge Resistor	R_{DIS_LDO}		40	80	120	Ω
	Output Undervoltage Falling Threshold	UVP_{F_LDO}		30	40	50	%
	Output Undervoltage Deglitch Time	$T_{UVP\_D\_LDO}$		15	30	45	μs
	Output Overvoltage Threshold	OVP_{R_LDO}		115	120	125	%
	Input Overvoltage Threshold	OVP_{IN_LDO}				5.5	V
	Power Supply Rejection Ratio	PSRR	I_{OUT_LDO} = 100mA, f = 100kHz		60		dB
			I_{OUT_LDO} = 100mA, f = 1MHz		50		
	Output Noise Voltage	eN_{LDO}	I_{OUT_LDO} = 100mA, f = 100Hz to 100kHz		18		μV
VCC	Internal Regulator Output Voltage	V_{OUT_VCC}		4.5	5	5.5	V
	SEQ Pull-Low Resistor	R_{SEQ}			400		kΩ
	SEQ Low Level Input Voltage	V_{SEQ_L}				0.4	V
	SEQ High Level Input Voltage	V_{SEQ_H}		1.5			V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
	nRESET Pulldown Voltage	$V_{OUT\_L\_PG}$	Current into nRESET pin equal to 5mA			200	mV
	nRESET input Leakage Current	I_{LEAK_PG}	1.8V applied on nRESET pin			1	μA
OTP	Overtemperature Protection	OTP			160		°C
	Overtemperature Protection Hysteresis	OTP_H			20		°C
Timing	Soft-Start Time	T_{SS_LV1}	V_{OUT1} 0% to 90%, no load	500	1000	1500	μs
		T_{SS_LV2}	V_{OUT2} 0% to 90%, no load	500	1000	1500	
		T_{SS_LV3}	V_{OUT3}0% to 90%, no load	500	1000	1500	
		T_{SS_LDO}	VLDO 0% to 90%, no load	300	750	1200	
	nReset Delay Time	t_{nReset}	For SY2A21731QDQ, SY2A21731BQDQ, SY2A21731CQDQ, SY2A21731DQDQ, SA47302FQDQ	1.5	2	3.5	ms
			For SA47302JQDQ SA47302HQDQ	6	8	10.5	

System Characteristics

(V_{IN} = 8V, V_{OUT1} = 3.8V, V_{OUT2} = 1.1V, V_{OUT3} = 1.8V, V_{LDO} = 3.3V, T_A = 25°C for Typ value, Min-Max covers from -40°C to 125°C, unless otherwise specified. (Note 5))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
CH1 HV Buck 1	Maximum Output Current	$I_{OUT\_MAX\_HV1}$		1.5			A
	Load Regulation	$V_{LOAD\_REG\_HV1}$	I_{OUT_HV1} =0A to 1.5A			0.1	%/ A
	Line Regulation	$V_{LINE\_REG\_HV1}$	V_{IN} = 5V to 14V, I_{OUT_HV1} =1.5A			1	%
	Load Transient	$V_{LOAD\_TRAIN\_HV1}$	I_{OUT_HV1} = 10mA to 500mA to10mA, 1μs	-150		+150	mV
	Line Transient	$V_{LINE\_TRAIN\_HV1}$	V_{IN} = 5V to 14V to 5V, 100μs, I_{OUT_HV1} = 10mA/500mA	-50		50	mV
	Output Ripple	V_{RIPPLE_HV1}	Peak to peak in one switching cycle			20	mV_{p-p}
CH2 LV Buck 2 (PVIN2 = 3.3V/3.8V)	Maximum Output Current	$I_{OUT\_MAX\_LV2}$		1.5			A
	Load Regulation	$V_{LOAD\_REG\_LV2}$	I_{OUT_HV1} = 0A to 1.5A			0.1	%/A
	Line Regulation	$V_{LINE\_REG\_LV2}$	V_{IN} = 2.7V to 5V, I_{OUT_LV2} = 1.5A			1	%
	Load Transient	$V_{LOAD\_TRAIN\_LV2}$	I_{OUT_LV2} = 10mA to 500mA to10mA, 1μs	-65		65	mV
	Line Transient	$V_{LINE\_TRAIN\_LV2}$	V_{IN_PVIN23} = 3V to 5V to 3V, 50μs, I_{OUT_LV2} = 10mA/1A	-10		10	mV
	Output Ripple	V_{RIPPLE_LV2}	Peak-to-peak in one switching cycle			10	mV_{p-p}
CH3 LV Buck 3 (PVIN3 = 3.3V/3.8V)	Maximum Output Current	$I_{OUT\_MAX\_LV3}$		1			A
	Load Regulation	$V_{LOAD\_REG\_LV3}$	I_{OUT_LV3} = 0A to 1A			0.1	%/A
	Line Regulation	$V_{LINE\_REG\_LV3}$	V_{IN} = 2.7V to 5V, I_{OUT_LV3} =1A			1	%
	Load Transient	$V_{LOAD\_TRAIN\_LV3}$	I_{OUT_LV2} = 10mA to 300mA to10mA, 1μs	-65		65	mV
	Line Transient	$V_{LINE\_TRAIN\_LV3}$	V_{IN_PVD23} = 3V to 5V to 3V,50μs, I_{OUT_LV3} = 10 mA/300mA	-10		10	mV
	Output Ripple	V_{RIPPLE_LV3}	Peak-to-peak in one switching cycle			10	mV_{p-p}
CH4 LDO (V_{OUT1} = 3.8V,	Load Transient	$V_{LOAD\_TRAN\_LDO}$	I_{OUT_LDO} = 10mA to 200mA to10mA, 1μs	-25		25	mV

V_{LDO} = 3.3V)	Line Transient	$V_{LINE\_TRAIN\_LDO}$	All V_{OUT_LDO}, V_{IN_LDO} step 600mV, LDO not in dropout condition, 10μs, I_{OUT_LDO} = 1mA/300mA	-25		25	mV
Required Components	Effective Input Capacitance	C_{PVIN1}		3	4.7	10	μF
		C_{VOUT1_IN}		1.1	2.2	10	
		C_{PVIN2}		2	4.7	10	
		C_{PVIN3}		2	4.7	10	
	Effective Output Capacitance	C_{VCC}		0.3	1	1.4	
		C_{VREF}		0.38	1	2.2	
		C_{VLDO}		1.1	2.2	10	
		C_{VOUT1}		3.7	10	14	
		C_{VOUT2}		5	10	14	
		C_{VOUT3}		5	10	14	
	Effective Boot Capacitance	C_{BS}		70	100	130	nF
	Inductance	L_1		1	1.5	2	μH
		L_2		0.68	1	1.2	
		L_3		0.68	1	1.2	

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective 4-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. The exposed pad of the QFN3×3-16 package is used for θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

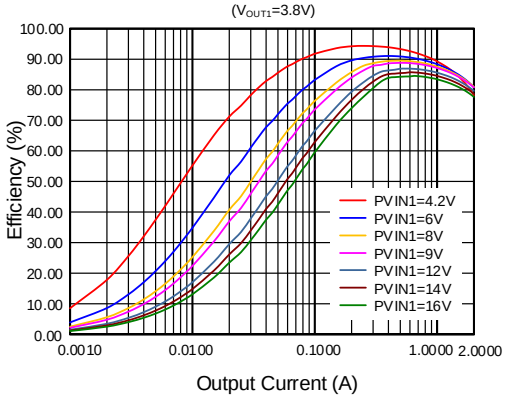
Note 5: The specifications are guaranteed by design and are not performed in production testing.

Typical Performance Characteristics

(T_A = 25°C)

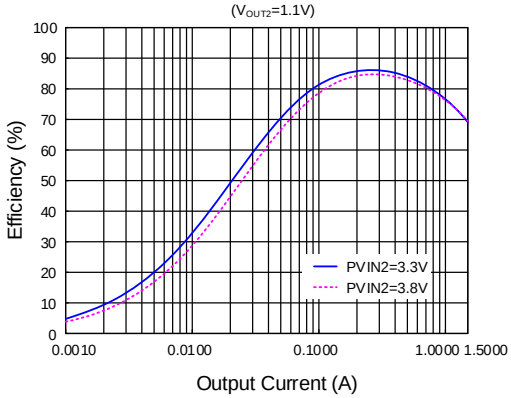
Efficiency vs Output Current

(V_{OUT1}=3.8V)



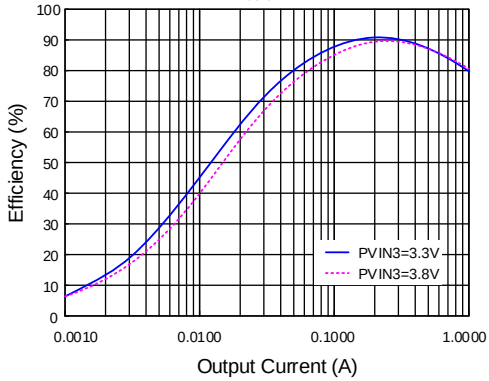
Efficiency vs Output Current

(V_{OUT2}=1.1V)



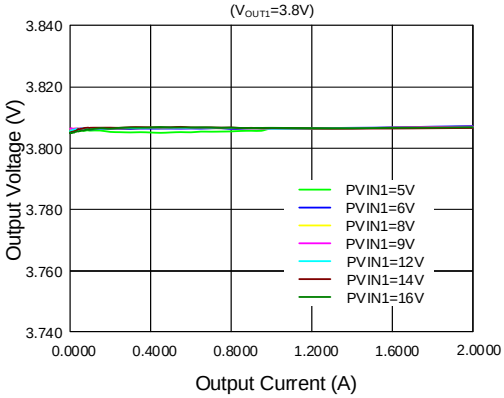
Efficiency vs Output Current

(V_{OUT3}=1.8V)



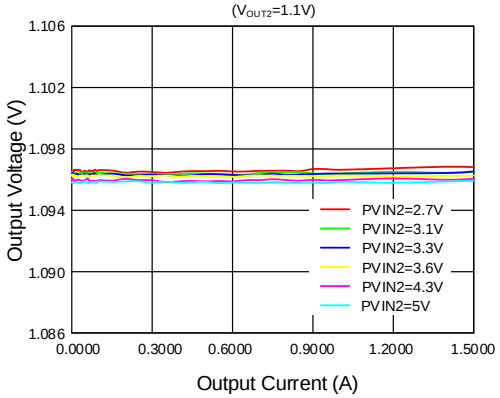
Output Voltage vs Output Current

(V_{OUT1}=3.8V)



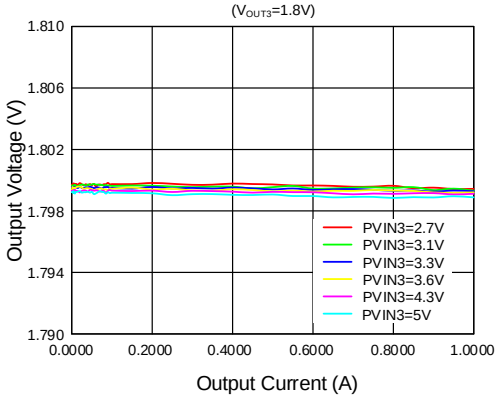
Output Voltage vs Output Current

(V_{OUT2}=1.1V)



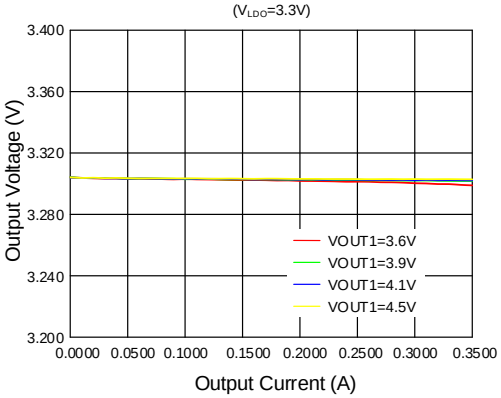
Output Voltage vs Output Current

(V_{OUT3}=1.8V)



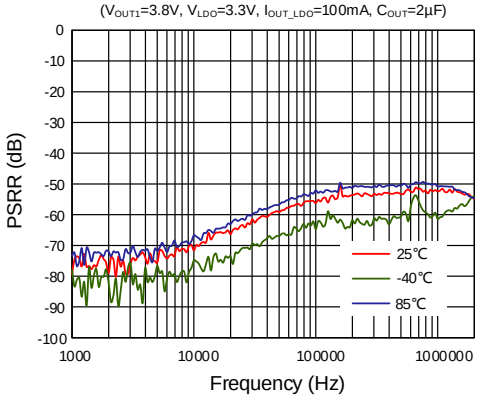
Output Voltage vs Output Current

(V_{LDO}=3.3V)



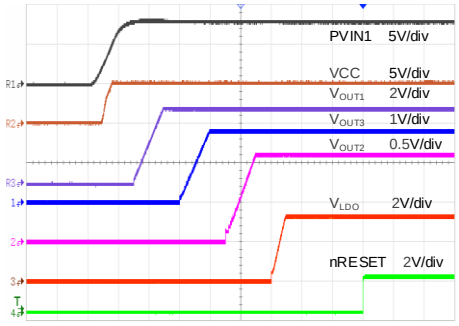
LDO PSRR

(V_{OUT1}=3.8V, V_{LDO}=3.3V, I_{OUT_LDO}=100mA, C_{OUT}=2μF)



Power On Sequence

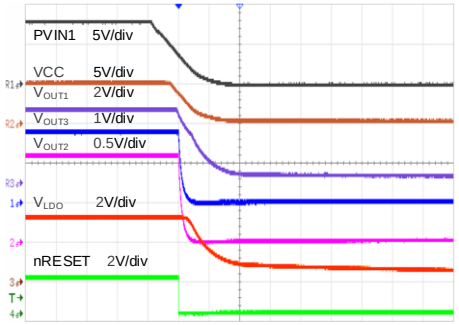
(PVIN1=8V, VCC=5V, V_{OUT1}=3.8V, V_{OUT2}=1.1V,
V_{OUT3}=1.8V , V_{LDO}=3.3V, SEQ=Low)



Time (1ms/div)

Power Off Sequence

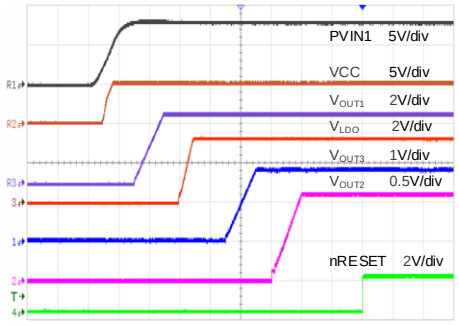
(PVIN1=8V, VCC=5V, V_{OUT1}=3.8V, V_{OUT2}=1.1V,
V_{OUT3}=1.8V , V_{LDO}=3.3V, SEQ=Low)



Time (10ms/div)

Power On Sequence

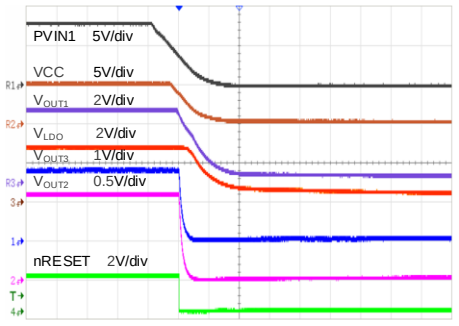
(PVIN1=8V, VCC=5V, V_{OUT1}=3.8V, V_{OUT2}=1.1V,
V_{OUT3}=1.8V , V_{LDO}=3.3V, SEQ=High)



Time (1ms/div)

Power Off Sequence

(PVIN1=8V, VCC=5V, V_{OUT1}=3.8V, V_{OUT2}=1.1V,
V_{OUT3}=1.8V , V_{LDO}=3.3V, SEQ=High)



Time (10ms/div)

Detailed Description

The SY2A21731 is a highly integrated PMIC that consists of one primary DC-DC buck regulator (Buck 1), two secondary DC-DC buck regulators (Buck 2 and Buck 3), and one secondary LDO. It is designed to power automotive camera modules and can operate across a wide input voltage range from 4V to 16V (absolute maximum of 18V).

All three DC-DC converters use fixed frequency peak current control. The operating frequency is set to 2.2MHz (typ) in order to avoid generating noise in the AM radio band. A spread-spectrum function for the internal clock is integrated to achieve good EMI performance. The low voltage buck converters operate out of phase (180 degrees phase shift) to reduce crosstalk between channels.

Primary Synchronous Buck Converter (Buck 1)

The primary buck converter Buck 1 starts working after V_{IN} voltage rises above the POR level. It is designed to supply a stable voltage for the secondary regulators, and operates at 2.2MHz using fixed frequency peak current control. Buck 1 operates with a fixed 3.3V or 3.8V output voltage (based on different options) with a 1.5A load capacity. It's suitable for POC power supply scenarios with a 4V–16V input voltage range.

The SY2A21731 integrates both high side and low side power MOSFETs. Buck 1 operates in Forced Continuous Current Mode (FCCM) in light load conditions. Spread spectrum with a spread range of +6% is applied to Buck 1. It requires an output filter capacitor with at least 20μF total capacitance.

Secondary Synchronous Buck Converters (Buck 2, 3)

Secondary buck converter Buck 2 operates with a fixed 1.1V or 1.2V output voltage (based on different options) with ±1.5% accuracy and 1.5A load capacity, which can meet the core power supply (DVDD) of the CIS.

Secondary buck converter Buck 3 operates with a fixed 1.8V output voltage with 1A load capacity, which is suited for the core power supply (VDD) of the serializer and logic power supply (IOVDD) of CIS in the camera module.

Both secondary buck converters feature internal power MOSFETs with low on-resistance to enable high efficiency power conversions. They operate at 2.2MHz using constant frequency peak current mode control to achieve stable loop control and fast dynamic response. Both secondary buck converters operate in forced current continuous mode (FCCM) to reduce low frequency noise and improve EMI performance. Both secondary buck converters use spread-spectrum technology to improve system EMC performance, and operate 180 degrees out of phase to further promote radiation quantity of simultaneous switching energy and automotive EMI compliance.

Secondary LDO

The secondary LDO of the PMIC features internal power MOSFETs to provide an output voltage of 2.8V or 3.3V (based on different options). The secondary LDO input power supply pin VOUT1 is also the primary buck converter output feedback pin. The secondary LDO operates with ±1.5% output voltage accuracy and more than 300mA output current capability. It features high PSRR and ultra-low noise, making it ideal for analog power supply (AVDD) of camera sensors.

Power Sequence Control

The SY2A21731 supports two power-on sequences for the step-down converters and LDO, selected by the SEQ pin. All outputs are powered down simultaneously during the power-down sequence. Power sequences and timing information are shown in Figure 3 and Figure 4.

When VIN(PVIN1) powers on and VIN is higher than the VIN UVLO_H threshold, the primary buck converter gate drive LDO (VCC) turns on and the SEQ voltage level is sampled to select the power-on sequence. The nReset output is driven low until all channels have completed the soft-start sequence and their outputs are within the regulation range.

When VIN falls below the UVLO_F threshold for a duration longer than UVLO_DT, all outputs power off simultaneously except for the VCC LDO. In this state, VCC is kept in the active state to power the internal gate drivers and internal logic until VIN falls below 3.6V.

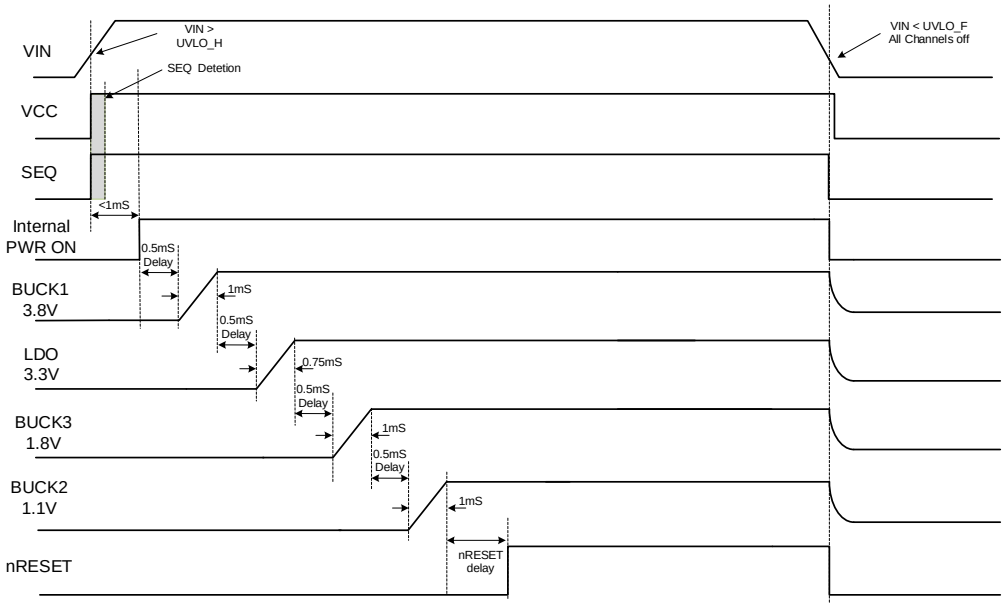


Figure 3. SEQ High Power On/Off Sequence

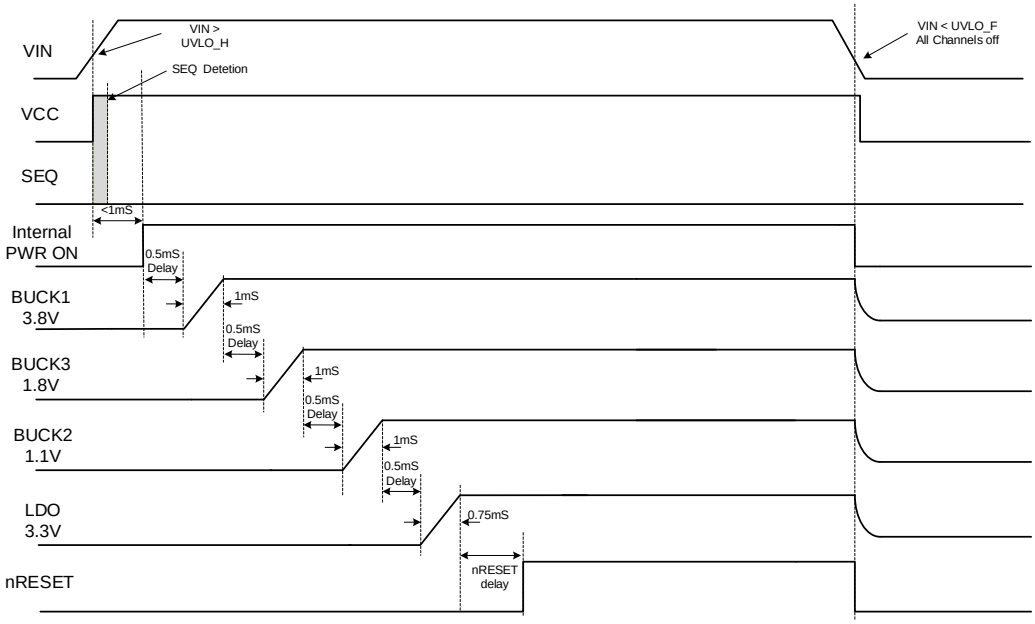


Figure 4. SEQ Low Power On/Off Sequence

Fault Protection

VIN Overvoltage (OVP) Protection

When VIN reaches the VIN_OV_R threshold, the buck converters, LDO, and nRESET block are disabled immediately. The device exits the OVP state only when VIN falls below VIN_OV_F. When returning to normal operation, all channels restart as enabled by the sequencer configuration (determined by the SEQ pin setting).

Buck and LDO Output Overvoltage (OVP) and Undervoltage (UVP) Protection

When any of the three buck converters or LDO outputs reach their respective overvoltage (OVP) or undervoltage (UVP) protection thresholds, the operation of all buck converters stops immediately and the nReset output is driven low. The device then attempts a restart after an 8ms delay (hiccup time). If any channel triggers OVP or UVP after the soft-start period is completed, the power process is terminated and a restart sequence is initiated after the 8ms hiccup time.

Buck Overcurrent (OCP) Protection

The inductor current for each of the three bucks is monitored cycle by cycle. When the value exceeds the peak current protection threshold, an internal counter increments. When the counter records 256 overcurrent events within a 500µs time period, a T1 event is recorded and a second counter increments. When 16 consecutive T1 events are recorded by the second counter, the load is considered abnormal and the device shuts down and switches to hiccup mode, where it will attempt a restart after an 8 ms delay.

If the current returns to values below the protection threshold and less than 256 overcurrent events are recorded in a 500µs interval, it is considered that the load returned to normal, all the counter values are reset and the device continues normal operation.

Spread-Spectrum Operation

A spread-spectrum function is used to modulate the internal clock of the SY2A21731 to meet the CISPR standard for automotive EMI compliance. By using +6% spread of the switching frequency, the design guarantees that the minimum switching frequency is higher than 1.8MHz.

Frequency Foldback Operation

In order to prevent the Buck 1 output voltage from dropping due to the duty cycle limitation when PVIN1 is too low, a built-in frequency foldback logic circuit is enabled when PVIN1 falls below 5.8V. The frequency foldback point is dependent on the output voltage of Buck 1 and load conditions, and allows the device to operate at PVIN1 = 4V while still maintaining VOUT1 = 3.8V under full load operation.

During power up, PVIN1 must rise above 6V to ensure the chip operates at the 2.2MHz target switching frequency. Figure 5 and Figure 6 illustrate the frequency foldback operation.

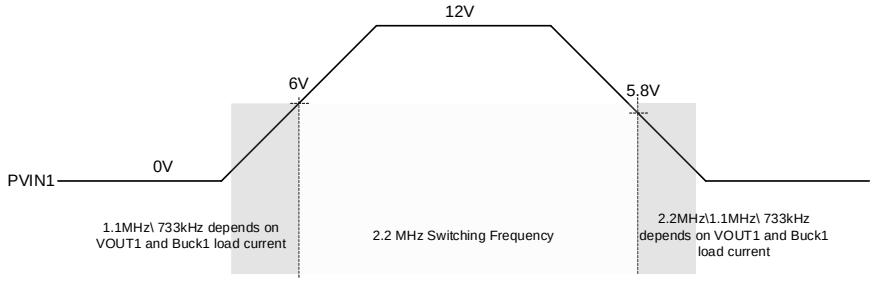


Figure 5. Frequency Foldback when PVIN1 is Low

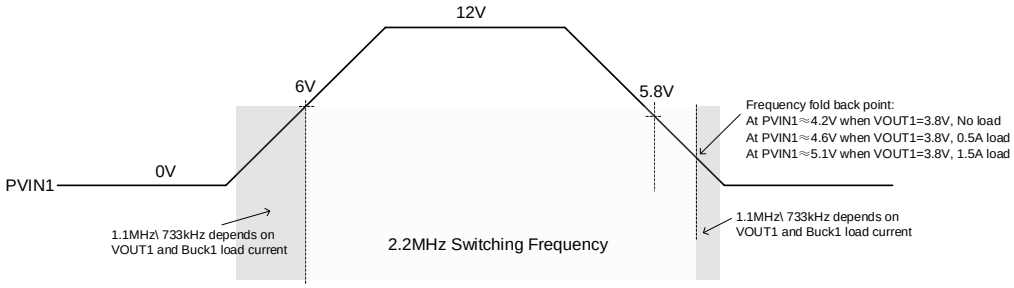


Figure 6. Examples of Frequency Foldback Point

Protection Modes Table

Channel	Protection Type	Protection Condition (Typ.)	Deglitch Time (Typ)	Device Operation	Protection release
System	UVP	PVIN1 ≤ 3.75V (after IC Operation)	32μs	Disable all channels	PVIN1 ≥ 4.05V
	OVP	PVIN1 ≥ 17V		Disable all channels	PVIN1 ≤ 16.5V, then all channel restart
	OTP	T_J ≥ 160°C		Disable all channels	Tj ≤ 140°C, then all channel restart
Buck 1	UVP	VOUT1 ≤ 50% V_{SET}	30μs	Disable all channels, then try to restart after 8ms hiccup time	VOUT1 ≥ 50% V_{SET}
	OVP	VOUT1 ≥ 120% V_{SET}		Disable all channels, then try to restart after 8ms hiccup time	VOUT1 ≤ 110% V_{SET}
	OCP	IL1_PEAK ≥ 2.5A		OC detected 256 times within 500μs is recorded as T1; if T1 triggered 16 times consecutively, disable all channels, then try to restart after 8ms hiccup time	IL1_PEAK ≤ 2.5A
Buck 2	UVP	VOUT2 ≤ 50% V_{SET}	30μs	Disable all channels, then try to restart after 8ms hiccup time	VOUT2 ≥ 50% V_{SET}
	OVP	VOUT2 ≥ 120% V_{SET}		Disable all channels, then try to restart after 8ms hiccup time	VOUT2 ≤ 110% V_{SET}
	OCP	IL2_PEAK ≥ 2.1A		OC detected 256 times within 500μs is recorded as T1; if T1 triggers 16 times consecutively, disable all channels, then try to restart after 8ms hiccup time	IL2_PEAK ≤ 2.1A
	Input OVP	PVIN2 ≥ 5.2V		Disable all channels	PVIN2 ≤ 4.9V, then all channels restart
Buck 3	UVP	VOUT3 ≤ 50% V_{SET}	30μs	Disable all channels, then try to restart after 8ms hiccup time	VOUT3 ≥ 50% V_{SET}
	OVP	VOUT3 ≥ 120% V_{SET}		Disable all channels, then try to restart after 8ms hiccup time	VOUT3 ≤ 110% V_{SET}
	OCP	IL3_PEAK ≥1.53A		OC detected 256 times within 500μs is recorded as T1; if T1 triggers 16 times consecutively, disable all channels, then try to restart after 8ms hiccup time	IL3_PEAK ≤ 1.53A
	Input OVP	PVIN2 ≥ 5.2V		Disable all channels	PVIN3 ≤ 4.9V, then all channel restart
LDO	UVP	VLDO ≤ 40% V_{SET}	30μs	Disable all channels, then try to restart after 8ms hiccup time	VLDO ≥ 40% V_{SET}
	OVP	VLDO ≥ 120% V_{SET}		Disable all channels, then try to restart after 8ms hiccup time	VLDO ≤ 110% V_{SET}
	OCP	IOUT_LDO ≥ 450mA	10ms	Disable all channels, then try to restart after 8ms hiccup time	IOUT_LDO ≤ 450mA

Note 6: The nRESET output is driven low when any protection mode is entered.

Component Selection

Input Capacitor for Buck 1, Buck 2, and Buck 3

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply, and to reduce EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X7R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability, and high RMS current ratings over a wide temperature and voltage range. Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated as follows:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1 - D)$$

where D is the convertor duty cycle. The worst-case condition occurs at D = 0.5, where

$$V_{CIN\_RIPPLE,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The typical recommended values for Buck1, Buck2, and Buck3 input capacitors is 4.7μF or higher.

Inductor selection

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. Selecting a low inductor value will help enhance transient response and reduce size and cost, but will increase peak inductor ripple current, which will reduce efficiency and increase output voltage ripple. The low DC resistance (DCR) of these low value inductors may help reduce DC losses and increase efficiency. Higher inductor values, however, tend to have higher DCR and slow the transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a ripple current (ΔIL) approximately 20%–50% of the desired full output load current. Start calculating the approximate inductor value by selecting the input and output voltages, the operating frequency (f_{SW}), and the maximum output current ($I_{OUT,MAX}$), then estimating a ΔI_L as some percentage of that current.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current (ΔI_L) and required peak current inductor current $I_{L,PEAK}$.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L_1}$$

$$I_{L,\,PEAK} = I_{OUT,\,MAX} + \frac{\Delta I_L}{2}$$

Select an inductor with a saturation current and thermal rating in excess of $I_{L,PEAK}$.

For highest efficiency, select an inductor with a low DCR that meets the inductance, size, and cost targets. Consider using low loss ferrite materials.

Output Capacitors for Buck 1, Buck 2, and Buck 3

Select the output capacitor C_{OUT} to handle the output ripple noise requirements. Both steady-state ripple and transient requirements must be taken into consideration when selecting this capacitor. Ceramic and POS types are most often selected due to their small size and low cost. For Buck 1, Buck 2, and Buck 3, it is recommended to use X7R or better grade ceramic capacitors with greater than 10μF capacitance.

Output Ripple

Output ripple at the switching frequency is caused by the inductor ripple (ΔI_L) on the output capacitor's ESR (ESR ripple) as well as the stored charge (capacitive ripple). For estimating the total ripple, both should be considered:

$$V_{RIPPLE,\,ESR} = \Delta I_L \times ESR$$

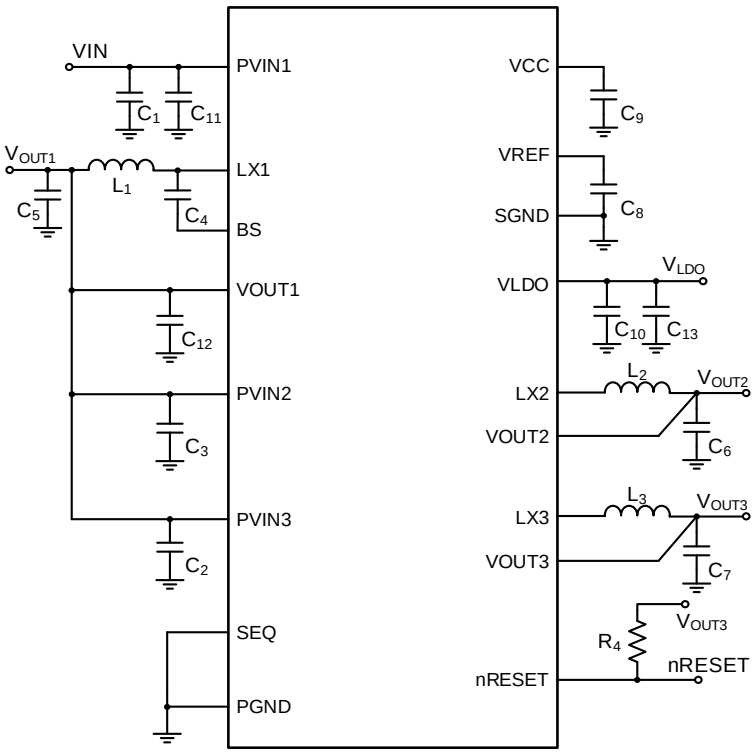
$$V_{RIPPLE,\,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The actual capacitive ripple may be higher than the theoretical value because the capacitance decreases with the voltage across the capacitor. Capacitor datasheets from different manufactures provide voltage derating curves. For accurate estimation, this information should be used to re-calculate the capacitive ripple based on the output voltage.

Bootstrap Capacitor for Buck1

The HV Buck 1 requires a bootstrap capacitor located between the BS and LX1 pins, with recommended capacitance of 0.1μF and rated at 25V or higher. The capacitor must be high quality ceramic type with X7R grade dielectric for temperature stability.

Application Schematic



BOM List

Designator	Description	Part Number	Manufacture
C1, C11	4.7μF/25V/0603	CGA5L1X7R1E475K160AC	TDK
C2, C3	4.7μF/10V/0603	CGA3E1X7T1A475K080AC	TDK
C4	100nF/25V/0603	CGA3E2X7R1E104K080AA	TDK
C12	2.2μF/10V/0603	CGA3E3X7S1A225K080AB	TDK
C5, C6, C7	10μF/10V/0603	GRT188C81A106ME13	MURATA
C8, C9, C10, C13	1μF/16V/0603	CGA3E1X7R1C105K080AC	TDK
L1	1.5μH	TEM201610ALMA1R5MTAA	TDK
L2, L3	1μH	TEM201610ALMA1R0MTAA	TDK
R4	10kΩ, 1%, 0603	AC0603FR-0710KL	YAGEO

Layout Design

Camera sensors are sensitive to the quality of power supplies, so a good PCB layout is important to reduce the ripple and enhance the line and load transients, as well as to reduce noise, and improve EMI and loop stability.

The recommended layout of power lines is shown in Figure 7 and Figure 8. Follow these PCB layout guidelines for optimal performance:

- A four-layer PCB with a common ground plane is recommended.
- Use short, wide switching node traces (LX1, LX2, and LX3).
- Place input capacitors on PVIN1/2/3 and output capacitors on VOUT1/2/3 as close as possible to the device.
- Use short, wide traces to connect the input capacitors on PVIN and the output capacitors.
- Use parallel capacitors for lower ESR.
- In the case where SEQ is pulled down to GND, connect the SEQ pin directly to the exposed pad of the chip to reduce the input capacitance loop area of PVIN1.

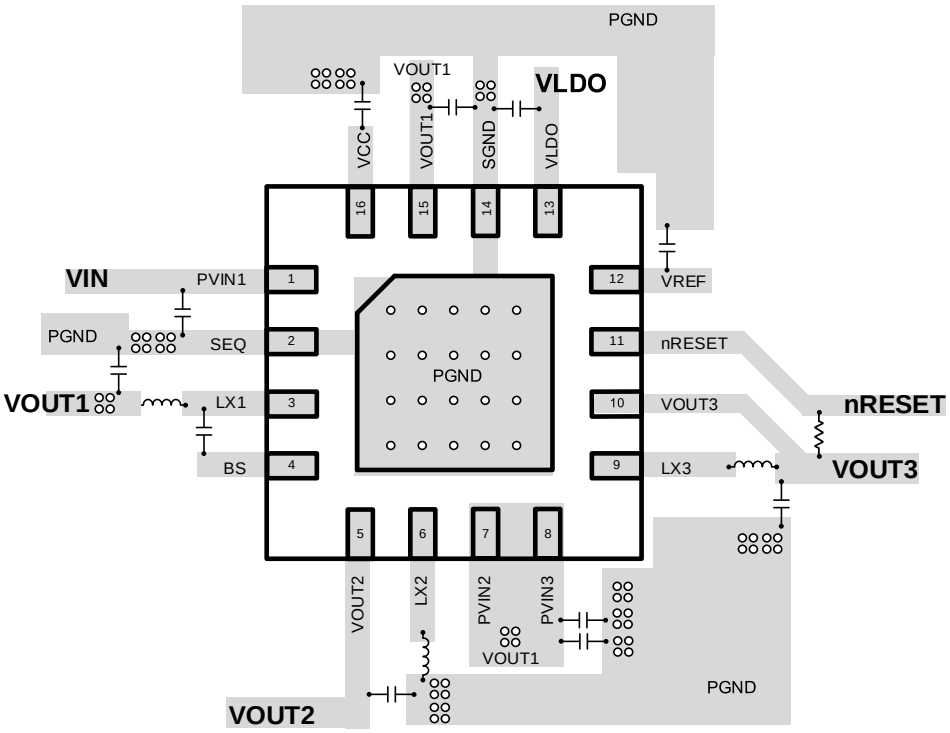


Figure 7. Suggested PCB Layout (SEQ Pin Connected to PGND)

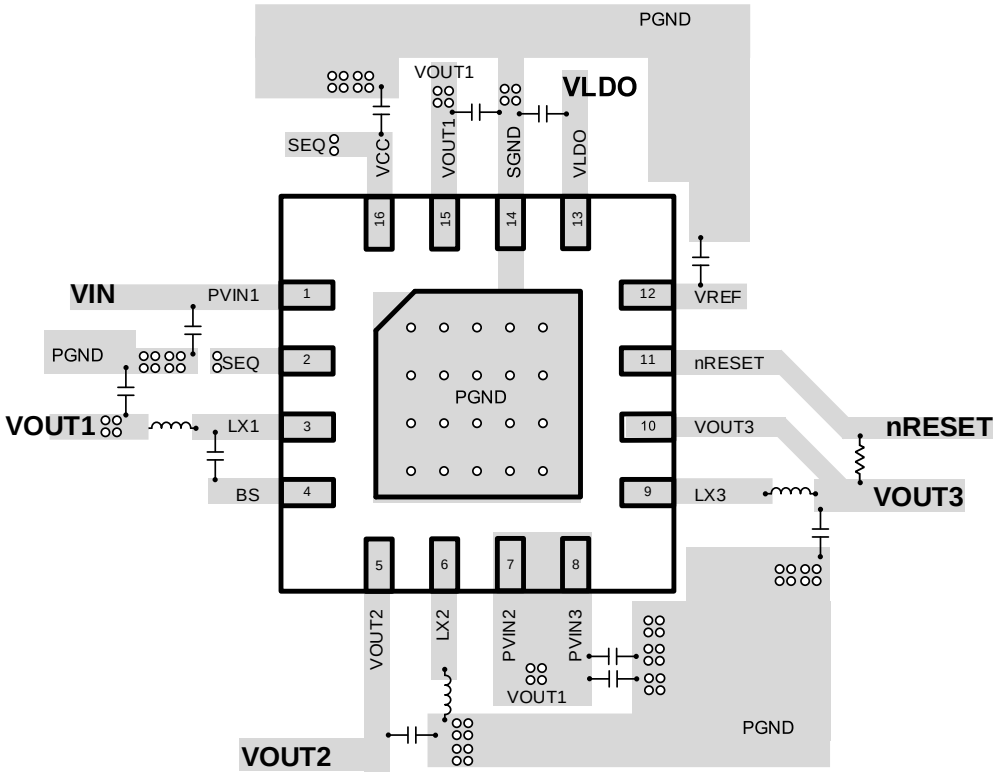
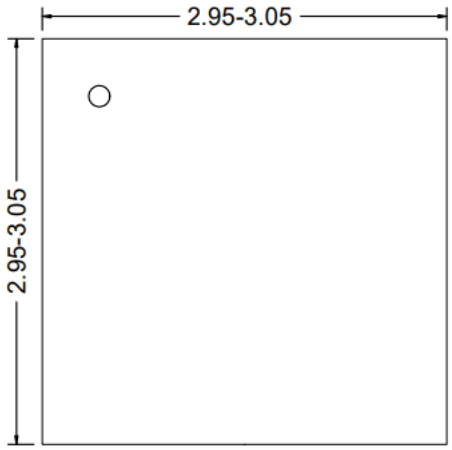
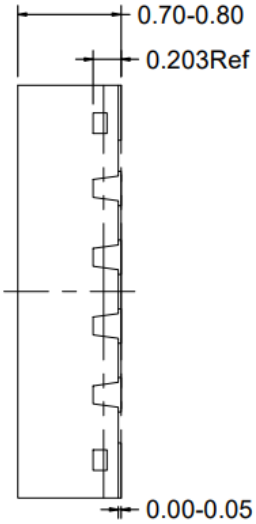


Figure 8. Suggested PCB Layout (SEQ Pin Connected to VCC)

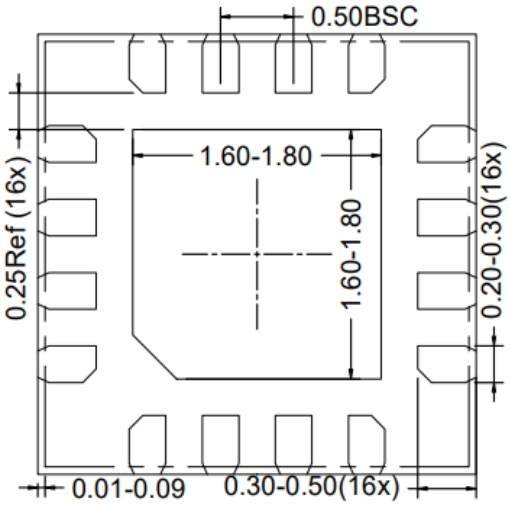
QFN3×3-16 Package Outline Drawing



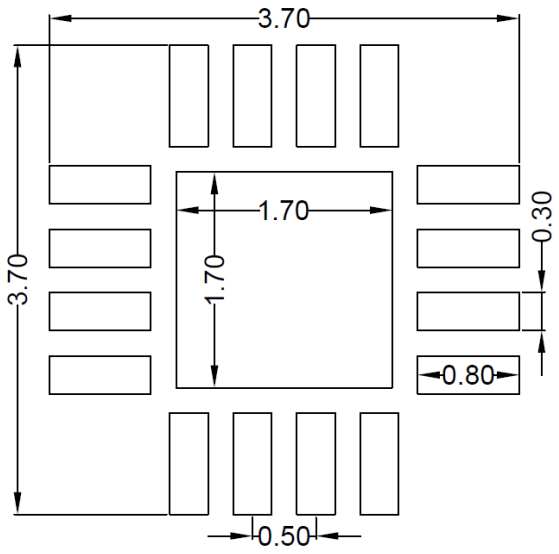
Top View



Side View



Bottom View

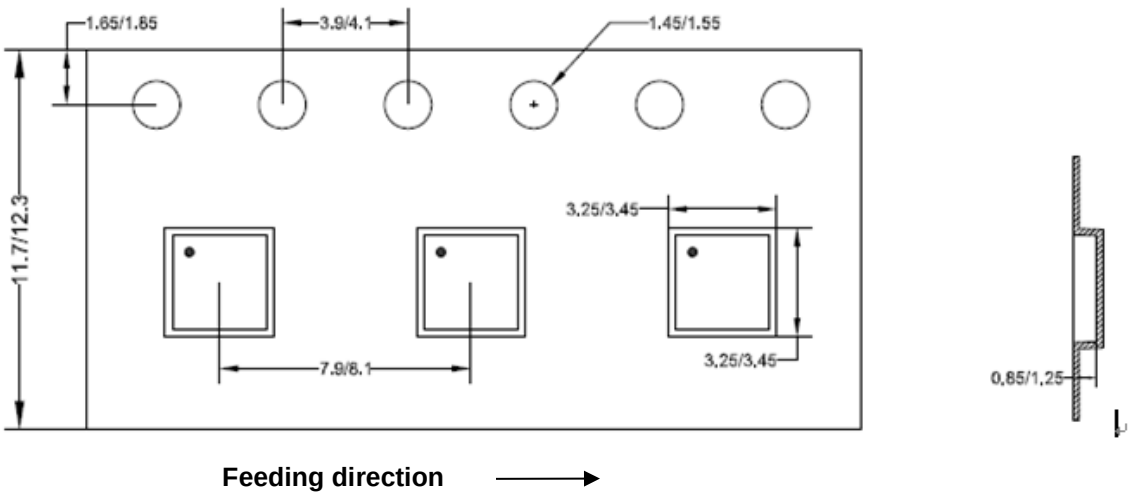


Recommended PCB Layout
(Reference Only)

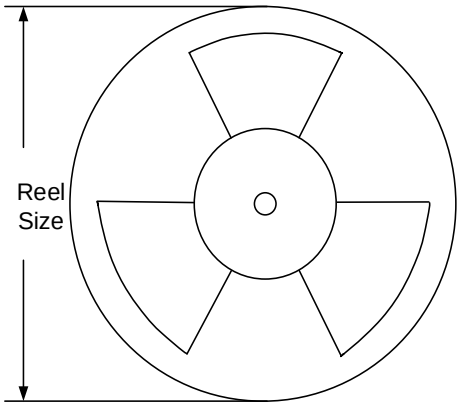
Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

Tape and Reel Information

Taping Dimensions and Orientation



Reel Dimensions



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Trailer Length(mm)	Leader Length (mm)	Qty per Reel
QFN3×3	12	8	13"	400	400	5000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
Aug.12, 2024	Revision 1.0	SY2A21731/B/C initial release.	-
Jun.05, 2025	Revision 1.0	SA47302F initial release.	-
		Add recommended PCB layout.	18
Dec.17, 2025	Revision 1.0a	SY2A21731DQDQ initial release. SA47302J/H initial release.	-
		Update the label on the third graph from 'Vout2=1.1V' to 'Vout3=1.8V in “Typical Performance Characteristics” section.	8

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