



# SY83008

## High Efficiency Fast Response, 8A, 25V Input Synchronous Buck Converter with 100mA 3.3V LDO

### General Description

The SY83008 is a high efficiency synchronous buck converter operating over a wide input voltage range of 4V to 25V and capable of delivering up to 8A current. It integrates low  $R_{DS(ON)}$  top and bottom MOSFETs to minimize the conduction loss. It operates at a pseudo-constant frequency of 600kHz, to enable the use of small size inductor and capacitors.

The SY83008 uses SEL programming to achieve all-in-one main source solution for notebook application. Refer to *Table 1* for more details.

Silergy's constant on-time and ripple-based control strategy supports high input/output voltage ratios (low duty cycles), and fast transient response while maintaining a near constant operating frequency over line, load and output voltage ranges. This control method provides stable operation without complex compensation, including when using low ESR output ceramic capacitors.

The device provides cycle-by-cycle current limit, input under voltage lockout, internal soft-start, output under voltage protection, over voltage protection and over temperature protection, to guarantee safe operation in all operating conditions.

### Applications

- Notebook/PC
- LCD-TV/Net-TV/3D-TV
- Set Top Box
- High Power AP

### Features

- Low  $R_{DS(ON)}$  for Internal MOSFETs: 17m $\Omega$  Top, 8.5m $\Omega$  Bottom
- Wide Input Voltage Range: 4V ~ 25V
- Multiple Identity Selection: Fixed 5.1V, 3.338V or Adjustable Output Voltage
- $\pm 1\%$  0.6V Reference under  $T_J = -40^\circ\text{C} \sim 125^\circ\text{C}$
- 8A Continuous Output Current Capability
- 100mA LDO Current Capability
- Support 98% Duty Cycle Operation
- 25 $\mu\text{A}$  Low Quiescent Current
- 1 $\Omega$  Integrated Bypass Switch
- 600kHz Pseudo-Constant Frequency
- Internal Soft-Start Limits the Inrush Current
- Support Smooth Startup with Pre-Biased Output
- Advanced Constant On-Time and Ripple-Based Control to Achieve Fast Transient Responses
- PFM/PFM+<sup>TM</sup>/USM Selectable Light Load Operation Mode
- Power Good Indicator
- Output Auto-Discharge Function
- Cycle-by-Cycle Valley, Peak and Reverse Over Current Protection (OCP) for Buck
- Latch-off Mode Output Under Voltage Protection (UVP) for Buck
- Latch-off Mode Output Over Voltage Protection (OVP) for Buck
- Latch-off Mode Over Temperature Protection (OTP) for Buck
- Auto-recovery Mode Output Under Voltage (UVP) Protection for LDO
- Auto-recovery Mode Over Temperature Protection (OTP) for LDO
- Input Under Voltage Lockout (UVLO)
- RoHS Compliant and Halogen Free
- Compact Package: QFN2.5x2.5-17

### Typical Application

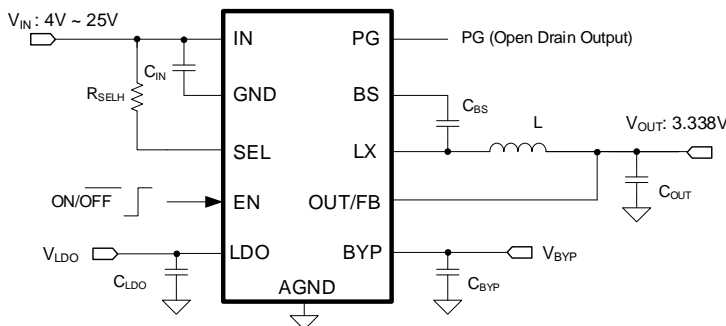


Figure 1. Schematic Diagram (Example: SEL=High)

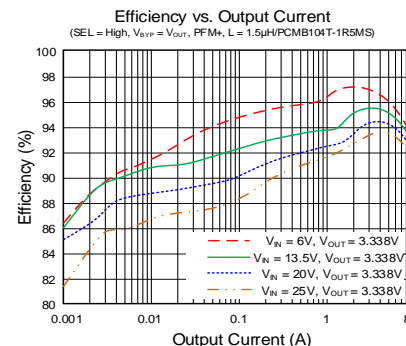


Figure 2. Efficiency vs. Output Current

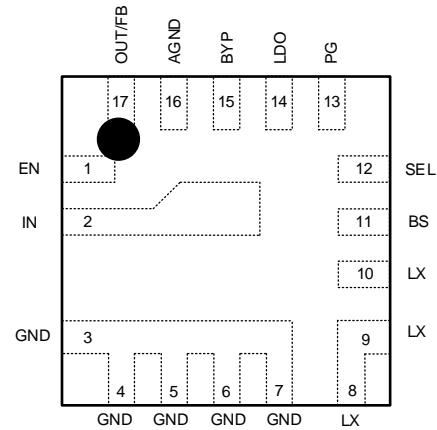


Ordering Information

Ordering Part Number	Package type	Top Mark
SY83008YKQ	QFN2.5x2.5-17 RoHS Compliant and Halogen Free	KMMxyz

x = year code, y = week code, z = lot number code

Pinout (top view)



SEL	V <sub>OUT</sub>	EN	LDO	Buck
High	Fixed 3.338V	< 0.4V	On	Off
		1.0V ~ 1.6V	On	On, USM Mode
		1.9V ~ 2.5V		On, PFM+ Mode
		V <sub>LDO</sub> -0.1V ~ V <sub>IN</sub>		On, PFM Mode
Floating	Fixed 5.1V	< 0.4V	Off	Off
		1.0V ~ 1.6V	On	On, USM Mode
		1.9V ~ 2.5V		On, PFM+ Mode
		V <sub>LDO</sub> -0.1V ~ V <sub>IN</sub>		On, PFM Mode
Low	Adjustable Output Voltage: 0.6~12.5V	< 0.4V	Off	Off
		1.0V ~ 1.6V	On	On, USM Mode
		1.9V ~ 2.5V		On, PFM+ Mode
		V <sub>LDO</sub> -0.1V ~ V <sub>IN</sub>		On, PFM Mode

Table 1. Identity Selection and EN Table

Pin Description

Pin No	Pin Name	Pin Description
1	EN	Enable control pin. Pull high to turn on the device. Pull low to turn off the device. Do not leave this pin floating. The pin is also used for controlling the operation mode of the buck converter under light load condition after its output is within the regulated range. Refer to <i>Table 1</i> for more details.
2	IN	Input pin. Decouple this pin to the GND pin with at least two 10μF ceramic capacitors. A 0.1μF ceramic capacitor placed in parallel is recommended to reduce high frequency noise.
3, 4, 5, 6, 7	GND	Ground pin.
8, 9, 10	LX	Inductor pin. Connect this pin to the switching node of the inductor.
11	BS	Bootstrap pin. Supply top MOSFET gate driver. Connect a 0.1μF ceramic capacitor between the BS pin and the LX pin.
12	SEL	Identity selection pin. Refer to <i>Table 1</i> for more details.
13	PG	Power good indicator pin. PG pin should be connected to V <sub>IN</sub> or another voltage source through a resistor (e.g., 10kΩ ~ 100kΩ). This pin becomes high when the output voltage is within 90% to 120% of regulated value under normal operation.
14	LDO	3.3V LDO output pin. Decouple this pin to ground with at least a 4.7μF ceramic capacitor.
15	BYP	Bypass input pin. This pin provides the bypass input for the 3.3V LDO. Decouple this pin to ground with a 1μF ceramic capacitor. Make one good RC filter for BYP input if the 3.3V external power ripple is large. Leave this pin floating or connect this pin to the ground if it is not used.
16	AGND	Analog ground pin.
17	OUT/FB	Output pin or feedback pin. If SEL = high or SEL = floating, connect this pin with output capacitors where you want to regulate the voltage. If SEL = low, connect this pin to the center point of the output resistor divider. V <sub>OUT</sub> = 0.6 × (1 + R <sub>H</sub> /R <sub>L</sub> ).

## Block Diagram

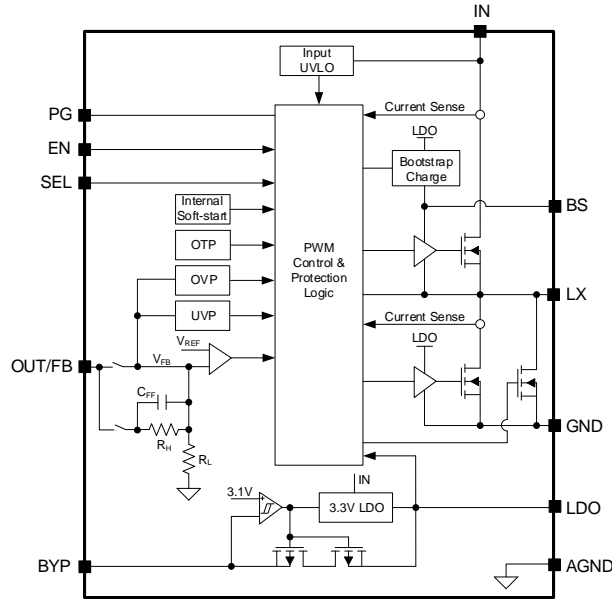


Figure3. Block Diagram

## Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN, IN-LX, LX, PG, EN, SEL	-0.3	30	V
BS-LX, LDO, BYP, AGND	-0.3	4	
OUT/FB	-0.3	6.5	
LX, 10ns Duration	-5	32	
LX, 20ns Duration	-1	31	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature	-65	150	

## Thermal Information

Parameter (Note 2)	Typ	Unit
$\theta_{JA}$ Junction-to-Ambient Thermal Resistance	29	°C/W
$\theta_{JC}$ Junction-to-Case Thermal Resistance	4.5	
$P_D$ Power Dissipation $T_A = 25^\circ\text{C}$	3.4	W

## Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Input Voltage	4	25	V
Buck Output Current		8	A
LDO Output Current		100	mA
Junction Temperature	-40	125	°C

**Electrical Characteristics**

 (V<sub>IN</sub> = 12V, C<sub>OUT</sub> = 88μF, T<sub>J</sub> = 25°C, I<sub>OUT</sub> = 1A unless otherwise specified(Note 4))

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit		
Input	Voltage Range	V <sub>IN</sub>	4		25	V		
	UVLO Rising Threshold	V <sub>IN,UVLO</sub>	V <sub>IN</sub> rising		3.9			
	UVLO Hysteresis	V <sub>IN,HYS</sub>		0.3				
	Quiescent Current	I <sub>Q,IN</sub>	I <sub>OUT</sub> = 0A, V <sub>BYP</sub> = V <sub>OUT</sub> , EN = high, SEL = high, measure input current		25	μA		
	Shutdown Current 1	I <sub>SHDN1</sub>	EN = Low, LDO enable		30			
Shutdown Current 2	I <sub>SHDN2</sub>	EN = Low, LDO disable		4				
Output	Voltage Set-Point	V <sub>SET,1</sub>	CCM, SEL = high	3.305	3.338	3.371	V	
		V <sub>SET,2</sub>	CCM, SEL = floating	5.049	5.1	5.151		
	Feedback Reference Voltage	V <sub>REF</sub>	T <sub>J</sub> = -40°C ~ 125°C	0.594	0.6	0.606		
	Voltage Range	V <sub>OUT</sub>	SEL = low	0.6		12.5		
	Discharge Current	I <sub>DIS</sub>	V <sub>OUT</sub> = 5V		100		mA	
	Soft-Start Time	t <sub>SS</sub>	V <sub>OUT</sub> from 0% to 100% V <sub>SET</sub> , SEL = high		1.2		ms	
			V <sub>OUT</sub> from 0% to 100% V <sub>SET</sub> , SEL = floating		0.8			
			V <sub>OUT</sub> from 0% to 100% V <sub>SET</sub> , SEL = low		0.6			
	OVP Rising Threshold	V <sub>OVPR</sub>	V <sub>FB</sub> rising	117	120	123	%V <sub>REF</sub>	
	OVP Falling Threshold	V <sub>OVPF</sub>	V <sub>FB</sub> falling	112	115	118		
	OVP Delay Time	t <sub>OVPDLY</sub>	(Note 5)		40		μs	
UVP Threshold	V <sub>UVP</sub>	V <sub>FB</sub> falling	55	60	65	%V <sub>REF</sub>		
UVP Delay Time	t <sub>UVPDLY</sub>	(Note 5)		200				
MOSFETs	Top MOSFET R <sub>DS(ON)</sub>	R <sub>DS(ON),TOP</sub>		17		mΩ		
	Bottom MOSFET R <sub>DS(ON)</sub>	R <sub>DS(ON),BOT</sub>		8.5				
	Top MOSFET Current Limit Threshold	I <sub>LMT,TOP</sub>	R <sub>SEL</sub> ≤ 1kΩ to GND	13.5			A	
			R <sub>SEL</sub> = 30kΩ to GND	6				
			R <sub>SEL</sub> = 100kΩ to GND	19				
	Bottom MOSFET Current Limit Threshold	I <sub>LMT,BOT</sub>	R <sub>SEL</sub> ≤ 1kΩ to GND	9				
			R <sub>SEL</sub> = 30kΩ to GND	3.5		5.5		
R <sub>SEL</sub> = 100kΩ to GND			13					
Bottom MOSFET Reverse Current Limit Threshold	I <sub>LMT,RVS</sub>	USM	2.7		5.2			
SEL	Input Voltage High	V <sub>SEL,H</sub>	2.5		V <sub>IN</sub>	V		
	Input Voltage Low	V <sub>SEL,L</sub>	0		0.4			
	Input Current	I <sub>SEL</sub>		0		μA		
Enable (EN)	Voltage for Buck Off	V <sub>EN,OFF</sub>	0		0.4	V		
	Voltage for USM Mode	V <sub>EN,USM</sub>	1.0		1.6			
	Voltage for PFM+ Mode	V <sub>EN,PFM+</sub>	1.9		2.5			
	Voltage for PFM Mode	V <sub>EN,PFM</sub>	V <sub>LDO</sub> -0.1		V <sub>IN</sub>			
	De-Glitch Time	t <sub>EN,DG</sub>	(Note 5)		10	μs		
Frequency	Switching Frequency	f <sub>SW</sub>	CCM	510	600	690	kHz	
	Ultra-Sonic Mode Frequency	f <sub>USM</sub>	USM, I <sub>OUT</sub> = 0A	20				
	Minimum On-Time	t <sub>ON,MIN</sub>	V <sub>IN</sub> = V <sub>IN,MAX</sub> (Note 5)		40		ns	
	Minimum Off-Time	t <sub>OFF,MIN</sub>			150			
Power Good (PG)	Rising Threshold	V <sub>PG,R</sub>	V <sub>FB</sub> rising (good)	87	90	93	%V <sub>REF</sub>	
	Falling Threshold	V <sub>PG,F</sub>	V <sub>FB</sub> falling (not good)	80	83	86		
	Delay Time	t <sub>PG</sub>	t <sub>PG,R</sub>	Low to high (Note 5)		200		μs
			t <sub>PG,F</sub>	EN = High, High to low (Note 5)		40		
t <sub>PG,OFF</sub>			From EN low to PG low (Note 5)			5		
Low Voltage	V <sub>PG,LOW</sub>	V <sub>FB</sub> = 0V, I <sub>PG</sub> = 2mA			0.45			
LDO	Output Voltage	V <sub>LDO</sub>	I <sub>LDO</sub> = 0mA ~ 100mA	3.15	3.3	3.45	V	
	Dropout Voltage	V <sub>DROPOUT</sub>	I <sub>LDO</sub> = 100mA		0.5			
	Output Current Limit Threshold	I <sub>LMT,LDO</sub>		150		310	mA	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
BYP	R <sub>DS(ON)</sub>	R <sub>DS(ON),BYP</sub>		1	1.5	Ω
	Turn on Voltage	V <sub>BYP</sub>	3.1		3.25	V
	Turn on Hysteresis	V <sub>BYP,HYS</sub>		0.2		
	OVP Voltage	V <sub>BYP,OVP</sub>	114	120	126	%V <sub>LDO</sub>
OTP	Buck Thermal Shutdown Temperature	T <sub>OTP,BUCK</sub>	T <sub>J</sub> rising (Note 5)	150		°C
	Buck Thermal Shutdown Temperature Hysteresis	T <sub>BUCK,HYS</sub>	T <sub>J</sub> falling (Note 5)	15		
	LDO Thermal Shutdown Temperature	T <sub>OTP,LDO</sub>	T <sub>J</sub> rising (Note 5)	160		
	LDO Thermal Shutdown Temperature Hysteresis	T <sub>LDO,HYS</sub>	T <sub>J</sub> falling (Note 5)	25		

**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:** Package thermal resistance is measured in the natural convection at T<sub>A</sub> = 25°C on a 8.5cm×8.5cm size, four-layer Silergy Evaluation Board with 2-oz copper.

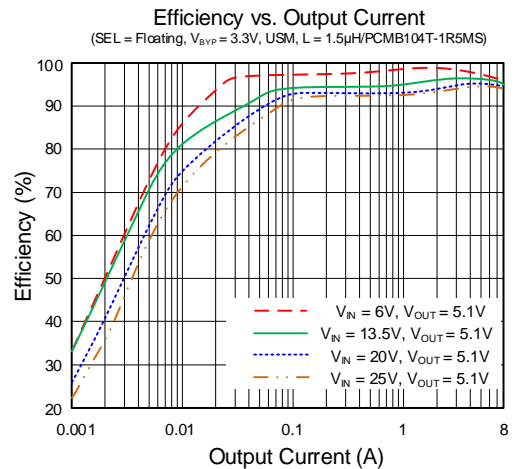
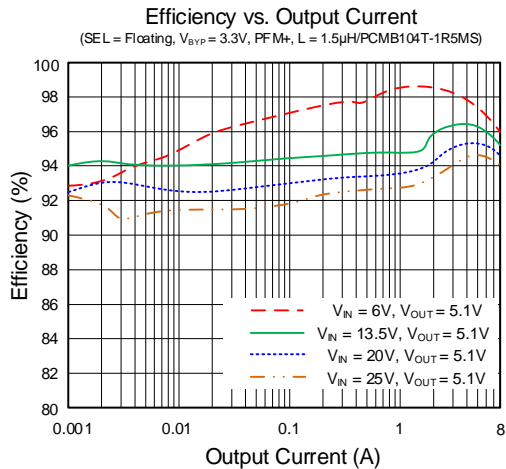
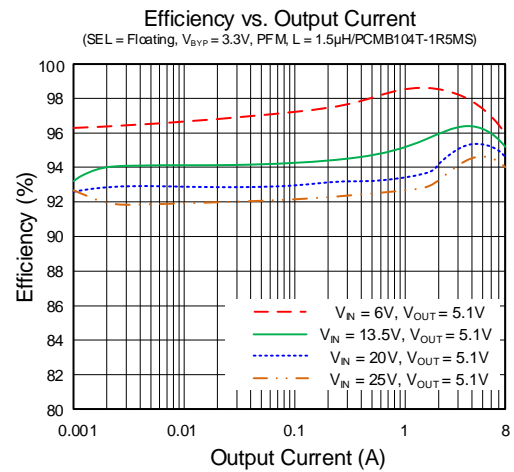
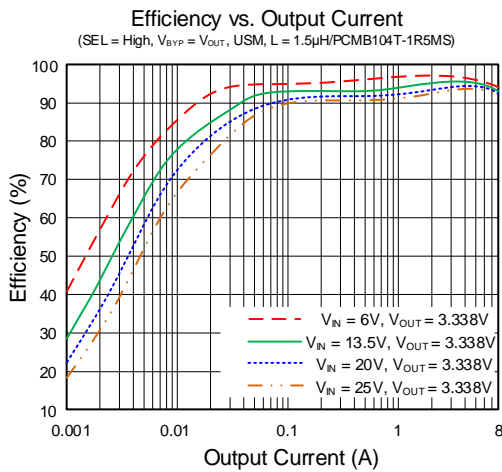
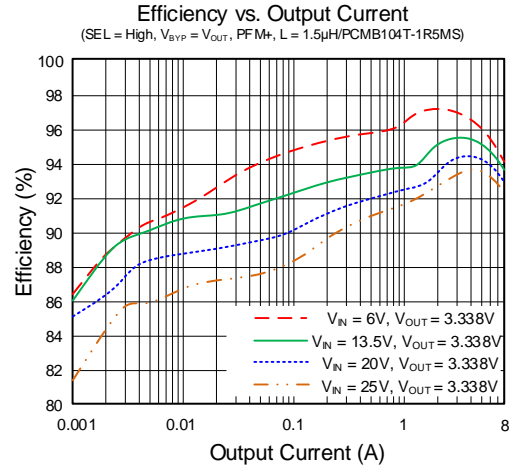
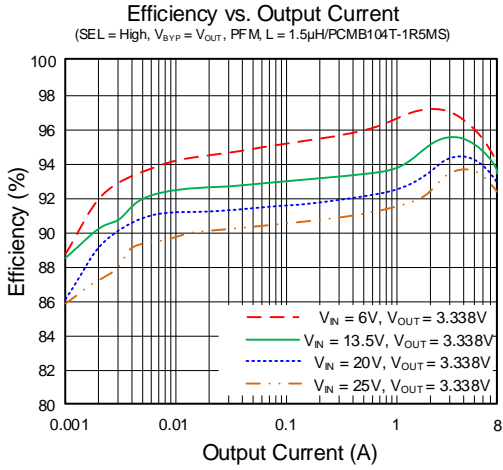
**Note 3:** The device is not guaranteed to function outside its operating conditions.

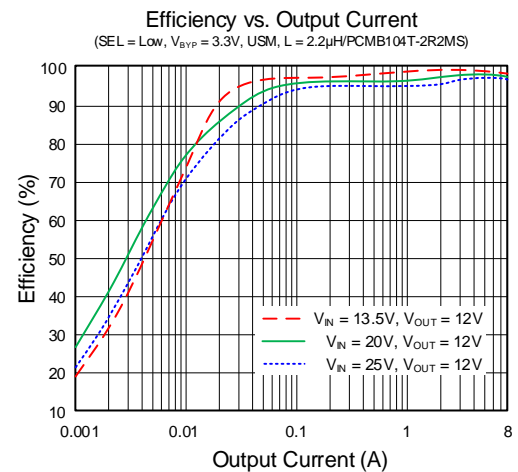
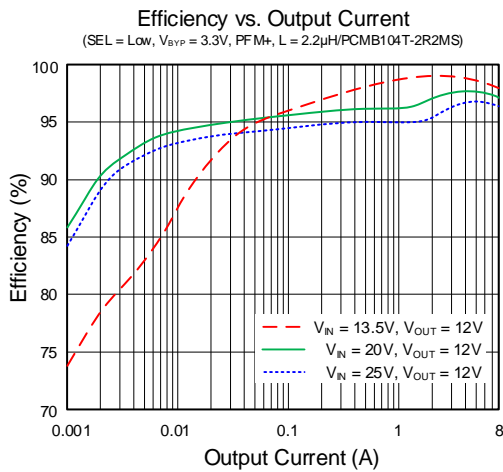
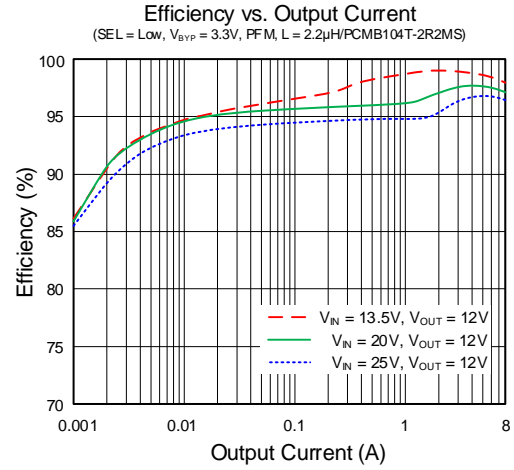
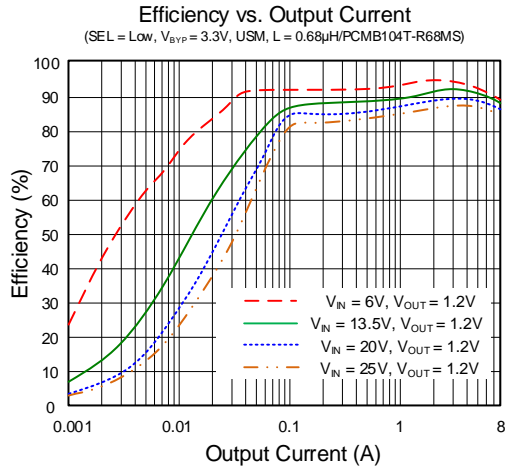
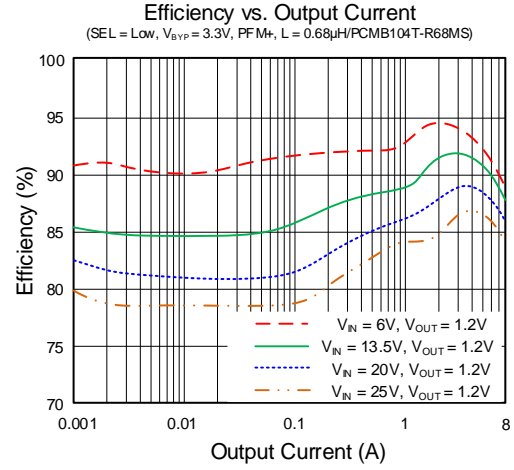
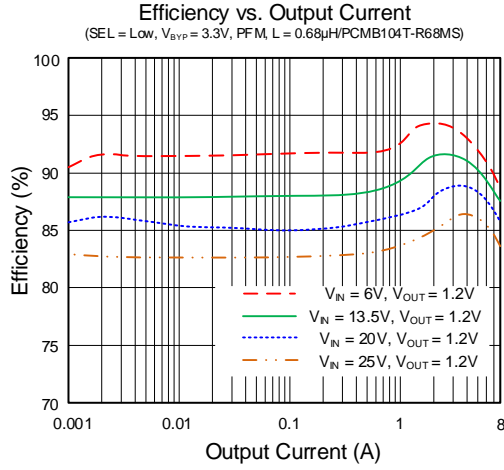
**Note 4:** Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that T<sub>A</sub> ≅ T<sub>J</sub> = 25°C. Limits over the operating temperature range (Refer to recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

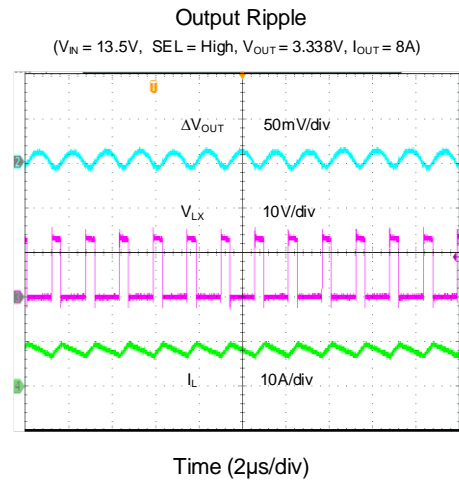
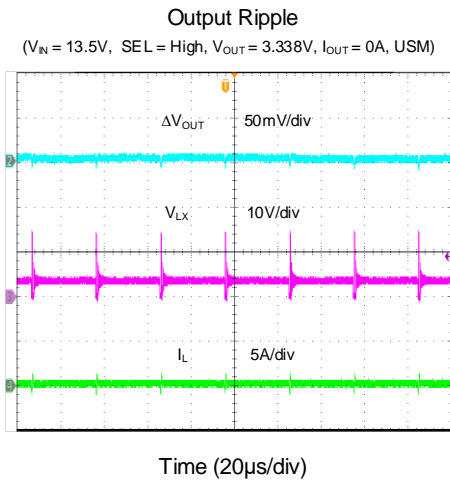
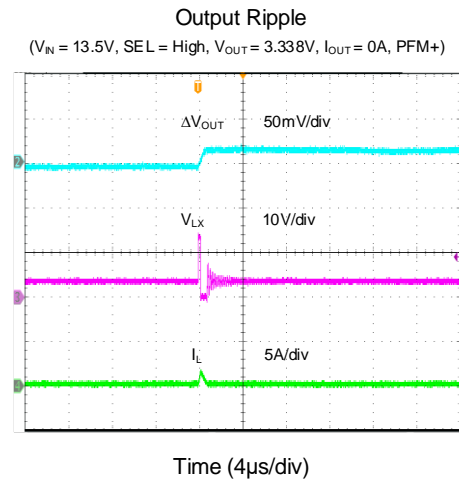
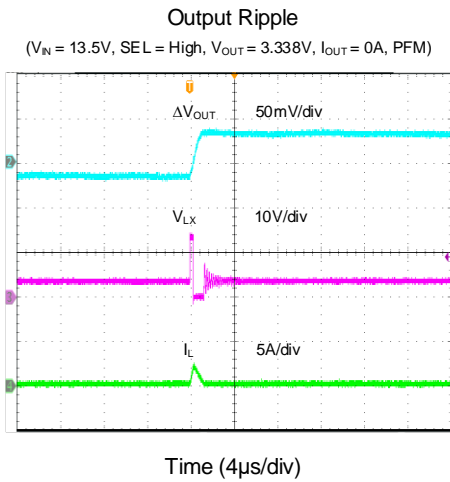
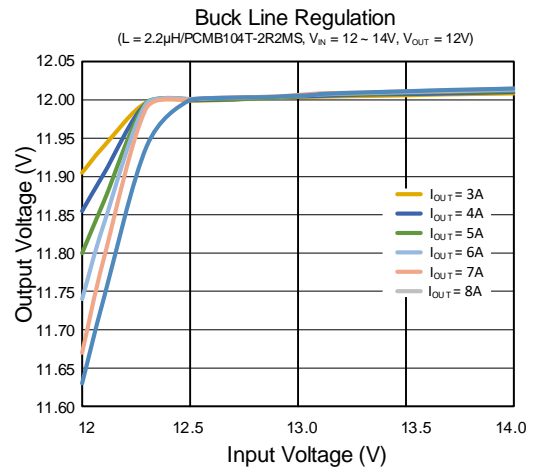
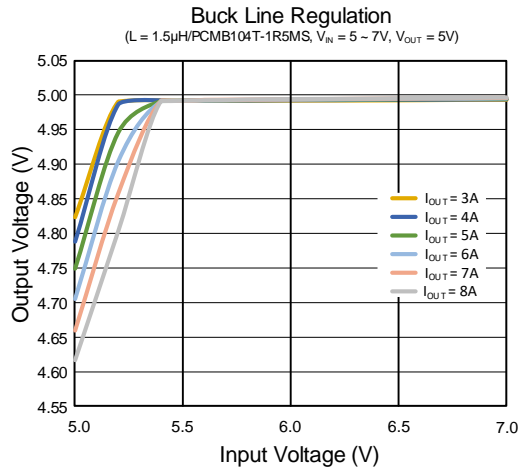
**Note 5:** Guaranteed by design.

## Typical Performance Characteristics

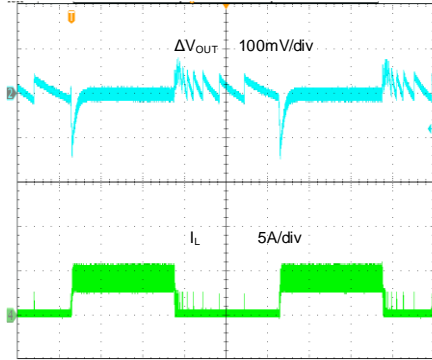
( $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 13.5\text{V}$ , SEL = High,  $L = 1.5\mu\text{H}$ ,  $C_{OUT} = 88\mu\text{F}$ , unless otherwise noted)





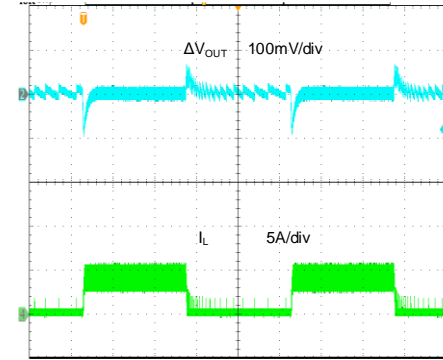


**Load Transient**  
 ( $V_{IN} = 13.5V$ , SEL = High,  $V_{OUT} = 3.338V$ ,  $I_{OUT} = 0 \sim 4A$ , PFM)



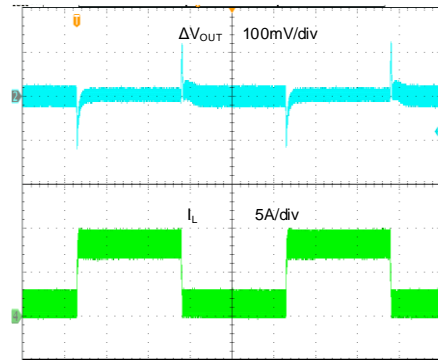
Time (200μs/div)

**Load Transient**  
 ( $V_{IN} = 13.5V$ , SEL = High,  $V_{OUT} = 3.338V$ ,  $I_{OUT} = 0 \sim 4A$ , PFM+)



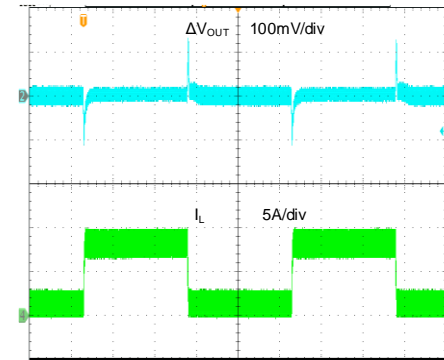
Time (200μs/div)

**Load Transient**  
 ( $V_{IN} = 13.5V$ , SEL = High,  $V_{OUT} = 3.338V$ ,  $I_{OUT} = 0.8 \sim 8A$ , PFM)



Time (200μs/div)

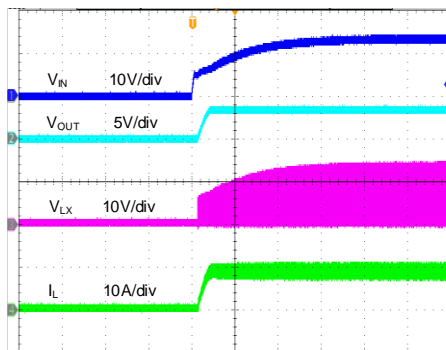
**Load Transient**  
 ( $V_{IN} = 13.5V$ , SEL = High,  $V_{OUT} = 3.338V$ ,  $I_{OUT} = 0.8 \sim 8A$ , PFM+)



Time (200μs/div)

**Startup from  $V_{IN}$**

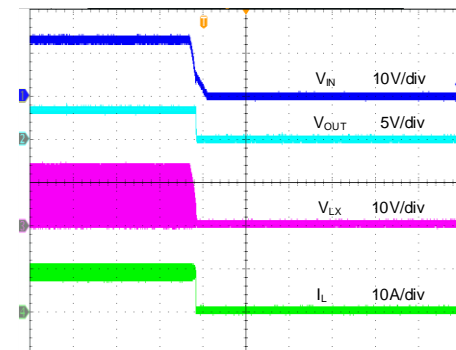
( $V_{IN} = 13.5V$ , SEL = High,  $V_{OUT} = 3.338V$ ,  $I_{OUT} = 8A$ )



Time (4ms/div)

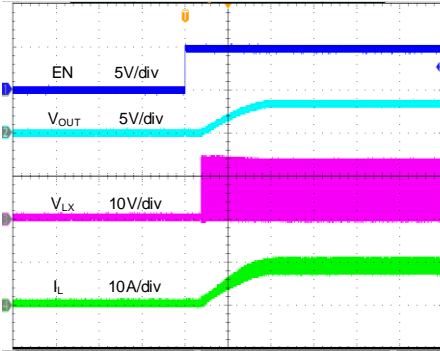
**Shutdown from  $V_{IN}$**

( $V_{IN} = 13.5V$ , SEL = High,  $V_{OUT} = 3.338V$ ,  $I_{OUT} = 8A$ )



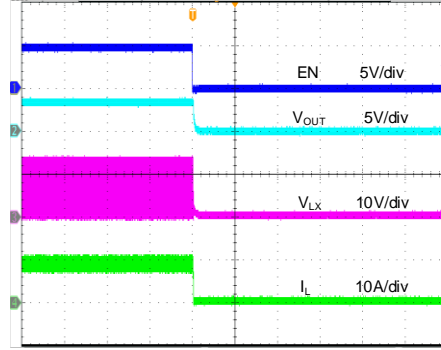
Time (4ms/div)

**Startup from EN**  
 ( $V_{IN} = 13.5V$ , SEL = High,  $V_{OUT} = 3.338V$ ,  $I_{OUT} = 8A$ )



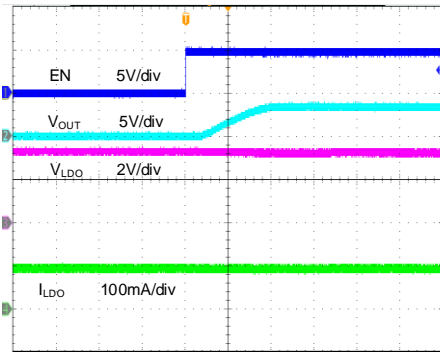
Time (800 $\mu$ s/div)

**Shutdown from EN**  
 ( $V_{IN} = 13.5V$ , SEL = High,  $V_{OUT} = 3.338V$ ,  $I_{OUT} = 8A$ )



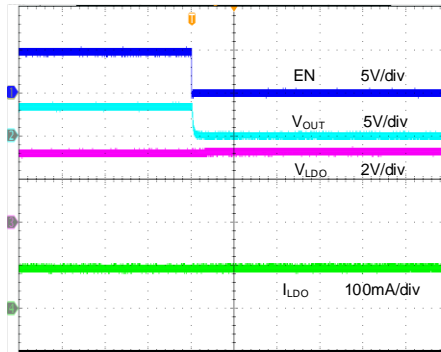
Time (800 $\mu$ s/div)

**LDO Switchover When EN On**  
 ( $V_{IN} = 13.5V$ , SEL = High,  $V_{OUT} = 3.338V$ ,  $I_{OUT} = 8A$ ,  $I_{LDO} = 100mA$ ,  $V_{BYP}$  connects  $V_{OUT}$ )



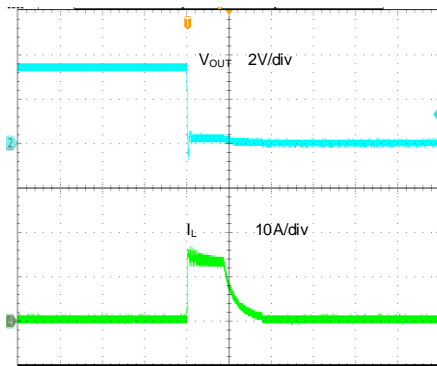
Time (800 $\mu$ s/div)

**LDO Switchover When EN Off**  
 ( $V_{IN} = 13.5V$ , SEL = High,  $V_{OUT} = 3.338V$ ,  $I_{OUT} = 8A$ ,  $I_{LDO} = 100mA$ ,  $V_{BYP}$  connects  $V_{OUT}$ )



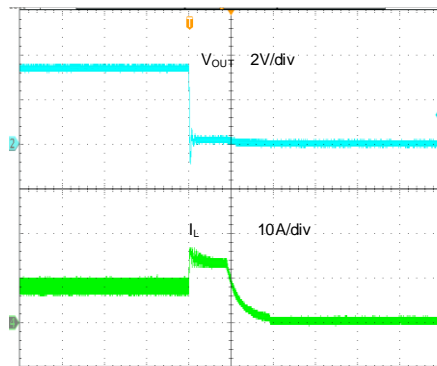
Time (800 $\mu$ s/div)

**Short Circuit Protection**  
 ( $V_{IN} = 13.5V$ , SEL = High,  $V_{OUT} = 3.338V$ ,  $I_{OUT} = 0A$ -short, PFM)



Time (200 $\mu$ s/div)

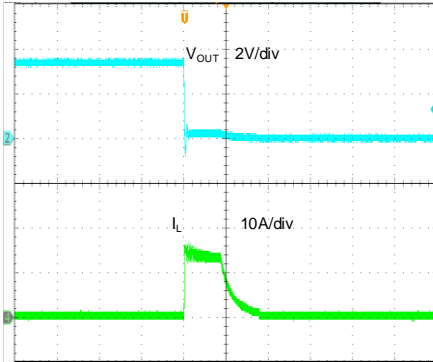
**Short Circuit Protection**  
 ( $V_{IN} = 13.5V$ , SEL = High,  $V_{OUT} = 3.338V$ ,  $I_{OUT} = 8A$ -short)



Time (200 $\mu$ s/div)

### Short Circuit Protection

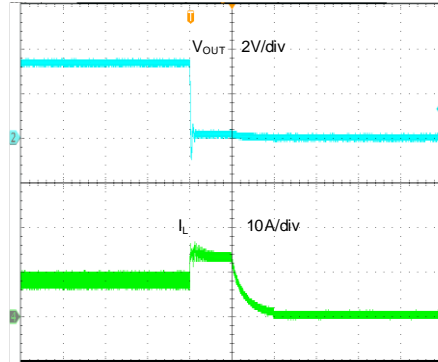
( $V_N = 13.5V$ , SEL = Low,  $V_{OUT} = 3.3V$ ,  $I_{OUT} = 0A$ -short,  $R_{SEL} = 1k\Omega$ , PFM)



Time (200 $\mu$ s/div)

### Short Circuit Protection

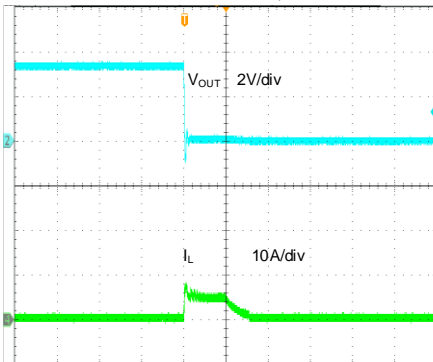
( $V_N = 13.5V$ , SEL = Low,  $V_{OUT} = 3.3V$ ,  $I_{OUT} = 8A$ -short,  $R_{SEL} = 1k\Omega$ )



Time (200 $\mu$ s/div)

### Short Circuit Protection

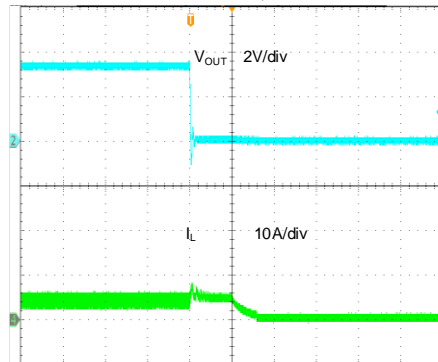
( $V_N = 13.5V$ , SEL = Low,  $V_{OUT} = 3.3V$ ,  $I_{OUT} = 0A$ -short,  $R_{SEL} = 30k\Omega$ , PFM)



Time (200 $\mu$ s/div)

### Short Circuit Protection

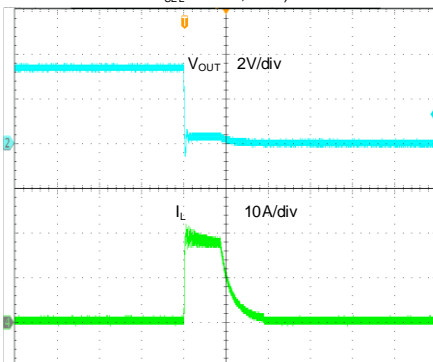
( $V_N = 13.5V$ , SEL = Low,  $V_{OUT} = 3.3V$ ,  $I_{OUT} = 4A$ -short,  $R_{SEL} = 30k\Omega$ )



Time (200 $\mu$ s/div)

### Short Circuit Protection

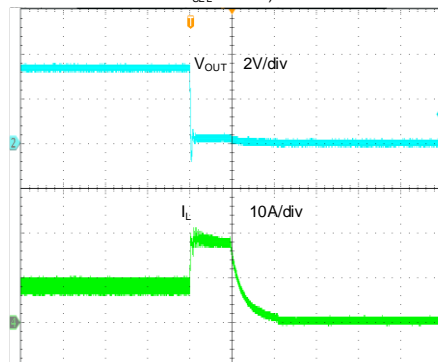
( $V_N = 13.5V$ , SEL = Low,  $V_{OUT} = 3.3V$ ,  $I_{OUT} = 0A$ -short,  $R_{SEL} = 100k\Omega$ , PFM)



Time (200 $\mu$ s/div)

### Short Circuit Protection

( $V_N = 13.5V$ , SEL = Low,  $V_{OUT} = 3.3V$ ,  $I_{OUT} = 8A$ -short,  $R_{SEL} = 100k\Omega$ )



Time (200 $\mu$ s/div)

## Detailed Description

### General Features

#### Constant On-Time Architecture

Fundamental to any constant on-time (COT) architecture is the one-shot circuit or on-time generator, which determines how long to turn on the top MOSFET. Each on-time ( $t_{ON}$ ) is a “fixed” voltage ratio,

$$t_{ON} = \left( \frac{V_{OUT}}{V_{IN}} \right) \times \left( \frac{1}{f_{SW}} \right)$$

For example, considering that a hypothetical converter targets 3.338V output from a 13.5V input at 600kHz, the target on-time is

$$\frac{3.338V}{13.5V} \times \frac{1}{600kHz} = 412.10ns$$

Each  $t_{ON}$  pulse is triggered by the feedback comparator when the output voltage as measured at FB node drops below the regulated value. After one  $t_{ON}$  period, a minimum off-time ( $t_{OFF,MIN}$ ) is imposed before any further switching is initiated, even if the output voltage is lower than the regulated value. This approach avoids making any switching decisions during the noisy periods just after switching events and while the switching node (LX) is rapidly rising or falling.

In a COT architecture, there is no fixed clock, so the top MOSFET can turn on almost immediately after a load transient and subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays.

#### Minimum and Maximum Duty Cycle

In the COT architecture, there is no limitation for operating the part at low duty cycle, since in this case, when the on-time is close to the minimum on-time, the switching frequency is reduced as needed to always ensure a proper operation.

To convert the output voltage during low input voltage operation, the  $t_{ON}$  can be extended to increase the duty cycle as needed. When the device detects that the feedback voltage is lower than the reference voltage during normal on-time operation, the  $t_{ON}$  will be extended. The device can support 98% open loop duty cycle if duty losses caused by MOSFET  $R_{DS(ON)}$  and inductor DCR are not considered.

#### Instant-PWM Operation

Silergy’s COT ripple-based control strategy adds several proprietary improvements to the traditional COT architecture. Whereas most legacy based on COT implementations require a dedicated connection to the output voltage terminal to calculate the  $t_{ON}$  duration, instant-PWM control method derives this signal internally. Another improvement optimizes operation with low ESR

ceramic output capacitors. In many applications it is desirable to utilize very low ESR ceramic output capacitors, but legacy COT converters may become unstable in these cases because the beneficial ramp signal that results from the inductor current flowing into the output capacitor may become too small to maintain stable operation. For this reason, instant-PWM synthesizes a virtual replica of this signal internally. This internal virtual ramp and the feedback voltage are combined and compared to the reference voltage. When the sum is lower than the reference voltage, the  $t_{ON}$  pulse is triggered as long as the minimum off-time has been satisfied and the inductor current as measured in the bottom MOSFET is lower than its current limit threshold. As the  $t_{ON}$  pulse is triggered, the bottom MOSFET turns off and the top MOSFET turns on. The inductor current ramps up linearly during the  $t_{ON}$  period. At the end of the  $t_{ON}$  period, the top MOSFET turns off, the bottom MOSFET turns on, and the inductor current ramps down linearly. This action also initiates the minimum off-time timer to ensure sufficient time for stabilizing any transient conditions and settling the feedback comparator before the next cycle is initiated. This minimum off-time is relatively short so that during fast speed load transients,  $t_{ON}$  can be retriggered with minimal delay, allowing the inductor current to ramp quickly and provide sufficient energy to the load side.

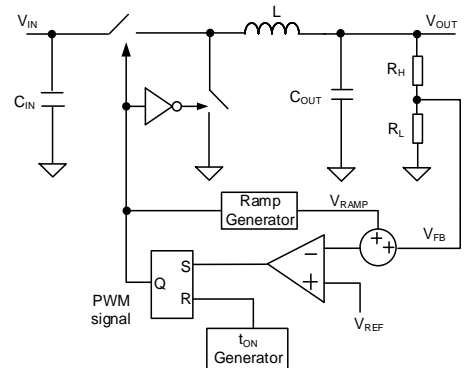


Figure4. Silergy’s COT Ripple-based Control Strategy

In order to avoid shoot-through, a dead time ( $t_{DEAD}$ ) is generated internally between turning the top MOSFET off and the bottom MOSFET on, as well as between turning the bottom MOSFET off and the top MOSFET on.

#### Light Load Operation Mode Selection

EN is a dual purpose input serving as the buck converter enable pin but also as mode selection pin to control operation mode of the buck converter under light load conditions, after its output is within the regulated range.

When identity is selected, PFM, PFM+ or USM light load operation is selected using the EN pin. If the voltage on this pin is lower than 1.6V and higher than 1V, the buck converter operates in ultra-sonic mode (USM). If the voltage on this pin is lower than 2.5V and higher than

1.9V, the buck converter operates using pulse-frequency modulation plus (PFM+) mode. If the voltage on this pin is 0.1V higher than  $V_{LDO}$ , the buck converter operates using pulse-frequency modulation (PFM) mode.

If PFM light load operation is selected, under light load conditions, typically when the load satisfies the following equation,

$$I_{OUT\_CTL} = \frac{\Delta I_L}{2} = \frac{V_{OUT} \times (1 - D)}{2 \times f_{SW} \times L} \quad (1)$$

the current through the bottom MOSFET will ramp to near zero before the next  $t_{ON}$  time. When this occurs, the bottom MOSFET turns off, preventing recirculation current that can seriously reduce efficiency under these light load conditions. As load current is further reduced, the combined feedback and ramp signals remain much higher than the reference voltage, the instant-PWM control loop will not trigger another  $t_{ON}$  until needed, and the apparent operating switching frequency will correspondingly drop, improving efficiency. The switching frequency can be lower than audible frequency area under deep light load or null load conditions. Continuous conduction mode (CCM) resumes smoothly as soon as the load current increases sufficiently for the inductor current to remain above zero at the time of the next  $t_{ON}$  cycle. The buck converter enters CCM once the load current exceeds the threshold shown in (1). Above the threshold, the switching frequency stays fairly constant over the output current range.

If PFM+ light-load operating mode is selected, under discontinuous conduction mode, the conduction time will decrease as the load increases, resulting in lower output voltage ripple that is smaller than that in PFM mode. During the transition from null load to CCM, the output voltage ripple remains constant, thereby reducing the number of output capacitors required. In addition, PFM+ will demonstrate improved dynamic performance compared to PFM.

If USM light load operation is selected, the control loop keeps the switching frequency above the audible frequency range, even under deep light load or null load conditions.

### Input Under Voltage Lockout (UVLO)

To prevent operation before the internal circuitry is ready and to ensure that the top and bottom MOSFETs can be properly driven, the device incorporates an input under voltage lockout protection.

If SEL is high, the device remains in a low current state and LX node switching actions and LDO are inhibited until  $V_{IN}$  exceeds the power-on reset protection (POR) rising threshold ( $V_{IN,POR}$ ). At that time, the LDO starts operating, and if  $V_{IN}$  exceeds the UVLO rising threshold and EN is

also high, the buck converter is enabled and soft-start ramp is initiated. If  $V_{IN}$  falls below  $V_{IN,UVLO}$  less than the input UVLO hysteresis, LX node switching actions will again be suppressed, if  $V_{IN}$  continues to fall below  $V_{IN,POR}$  less than the input POR hysteresis, LDO will also be suppressed.

If SEL is floating or low, the device remains in a low current state and LX node switching actions and LDO are inhibited until  $V_{IN}$  exceeds the POR rising threshold. At that time, if EN is also high, the LDO starts operating, the buck converter is enabled and soft-start ramp is initiated until  $V_{IN}$  exceeds the UVLO rising threshold. If  $V_{IN}$  falls below  $V_{IN,UVLO}$  less than the input UVLO hysteresis, LX node switching actions will again be suppressed, if  $V_{IN}$  continues to fall below  $V_{IN,POR}$  less than the input POR hysteresis, LDO will also be suppressed.

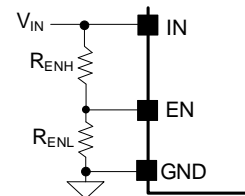


Figure5. Enable Control

Increasing the default input UVLO threshold can be implemented using an external resistor divider connected to EN.

### SEL Selection

The device supports three different identity selections by SEL pin. When the SEL pin is connected to  $V_{IN}$  before startup, LDO starts operating even EN is low, the device provides fixed output 3.338V main supply. When the SEL pin is floating, the device provides fixed output 5.1V main supply. When the SEL pin is low, the device provides adjustable output through external resistor divider programming, along with programmable peak and valley current limit threshold.

### EN Control

The EN input is high-voltage capable inputs with logic-compatible threshold. EN logic high is defined as a voltage higher than 1V, and a logic low as a voltage lower than 0.4V.

EN pin is also used for controlling the light load operation mode of the buck converter after its output is within the regulated range. Refer to *Table 1* for more details.

It is not recommended to connect EN pin to  $V_{IN}$  or another voltage source directly. A resistor in a range of 1k $\Omega$  to 1M $\Omega$  should be used for EN pin in this case.

## Startup and Shutdown

The device incorporates an internal soft-start circuit to smoothly ramp the buck converter output to the desired voltage whenever it is enabled. Internally, the soft-start circuit clamps the output at zero and then allows the output to rise to the desired voltage, which avoids high current flow and transients during startup.

If the SEL pin is floating or low, the startup and shutdown sequence are shown in Figure6. After  $V_{IN}$  exceeds the POR rising threshold, the internal LDO regulator is turned on after the delay time  $t_{DLY1}$  if EN is high. After  $V_{IN}$  exceeds the UVLO rising threshold, the buck converter is turned on after the delay time  $t_{DLY2}$ , once LDO voltage is ready. When the output voltage is 90% of the regulated value, PG is set to the high-impedance state after the delay time  $t_{PG,R}$ . LDO output switches to the BYP if BYP voltage is higher than bypass switch turn on voltage. LDO output will switch to internal LDO when BYP voltage falls below  $V_{BYP}$  less than the BYP turn on hysteresis.

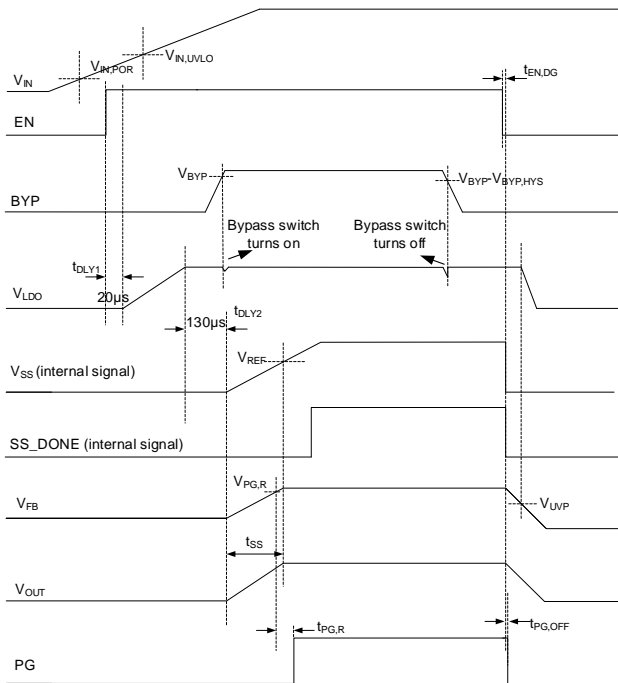


Figure6. Startup and Shutdown Sequence (SEL = Low or Floating)

If the SEL pin is high and the BYP pin is connected to the OUT pin, the startup and shutdown sequence are shown in Figure7. After  $V_{IN}$  exceeds the POR rising threshold, the internal LDO regulator is turned on. After  $V_{IN}$  exceeds the UVLO rising threshold, if EN is high, the buck converter is turned on after the delay time  $t_{DLY2}$ , once LDO voltage is ready. When the output voltage is 90% of the regulated value, PG is set to the high-impedance state after the delay time  $t_{PG,R}$ . After the delay time  $t_{DLY3}$  from SS\_DONE signal becomes high, the LDO output switches to the buck output if the output voltage is higher than

bypass switch turn on voltage. The LDO output will switch to the internal LDO regulator when EN is driven low.

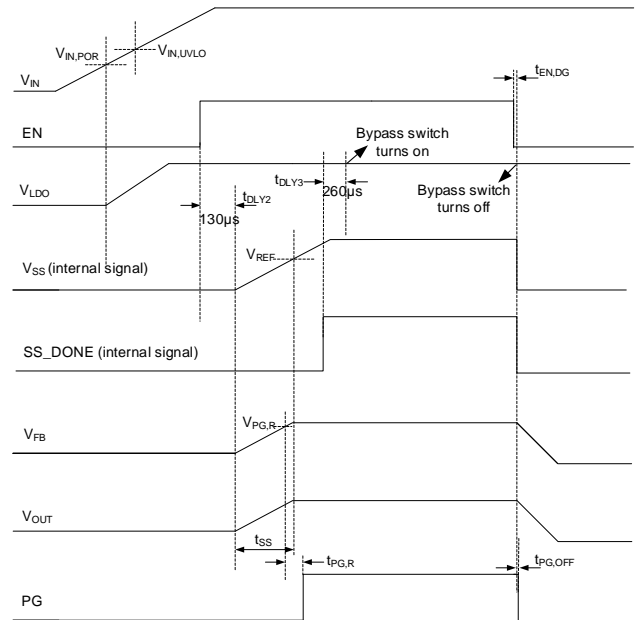


Figure7. Startup and Shutdown Sequence (SEL = High)

The device supports startup with pre-biased output. If the output is pre-biased to a certain voltage before startup, the buck converter disables the switching of both the top MOSFET and the bottom MOSFET until the internal soft-start voltage  $V_{SS}$  exceeds the sensed output voltage at the FB node. The first pulse on-time is internally calculated based the input voltage and pre-biased output voltage.

### PG Power Good Indicator

PG is an open drain output controlled by a window comparator connected to FB node. If the voltage is higher than  $V_{PG,R}$  and less than  $V_{OV,P}$  for at least the power good delay time (low to high), PG will be set to high-impedance state.

PG should be connected to  $V_{IN}$  or another voltage source through a resistor (e.g., 100k $\Omega$ ). After  $V_{IN}$  rises until the internal initial power is ready, the PG internal MOSFET is turned on so that PG is actively driven low before output voltage is ready. After the feedback voltage  $V_{FB}$  reaches  $V_{PG,R}$ , PG is set to high-impedance state after a delay time of 200 $\mu$ s (typ.). When  $V_{FB}$  drops to  $V_{PG,F}$ , or rises above  $V_{OV,P}$  for the OVP delay time, PG is driven low after a delay time of 40 $\mu$ s (typ.).

### Buck Output Auto-Discharge Function

The device discharges the output voltage when the buck converter shuts down due to low  $V_{IN}$  or EN, or caused by a protection function being triggered, so that the output voltage can be discharged in a minimal time, even if the buck output load current is zero. The discharge MOFET

in parallel with the bottom MOSFET turns on after the bottom MOSFET turns off when the shutdown logic is enabled. The output discharge current is typically 100mA for  $V_{OUT} = 5V$ . The discharge MOSFET is not active outside of these shutdown conditions.

### External Bootstrap Capacitor

This device integrates a floating power supply for the gate driver of the top MOSFET. Proper operation requires a  $0.1\mu F$  low ESR ceramic capacitor to be connected between BS and LX. This bootstrap capacitor provides the gate driver supply voltage for the N-channel top MOSFET.

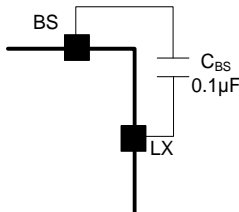


Figure8. Bootstrap Capacitor Connection

### LDO Output

The device integrates a high performance, low drop-out linear regulator 3.3V LDO, which can power the internal gate drivers, PWM logic, analog circuitry and other blocks, but also power the external peripherals with 100mA capability. Connect a  $4.7\mu F$  low ESR ceramic capacitor from LDO to GND.

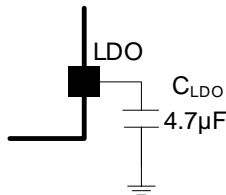


Figure9. LDO Capacitor Connection

### BYP Input

When a 3.3V external power supply is connected to the BYP pin, the internal LDO is automatically turned off. The overall efficiency may be improved by using an external power supply. Connect a  $1.0\mu F$  low ESR ceramic capacitor from BYP pin to GND. When SEL is high, it is recommended to connect the BYP pin to the OUT pin, BYP turn on and off logic is special considering the LDO output should be as equal as the output voltage.

Using an external low pass filter consisting of a small value resistor  $R_{BYP}$  and a ceramic capacitor  $C_{BYP}$  is recommended for applications where the external power rail has significant ripple. Connect the pin to GND or leave floating if not used.

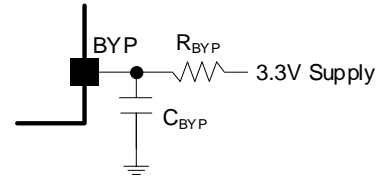


Figure10. BYP Low Pass Filter Connection

## Fault Protection Modes

### Buck Output Current Limit

The buck converter features cycle-by-cycle “valley” current limit (bottom MOSFET current limit). The Inductor current is monitored in the bottom MOSFET when it turns on and as the inductor current ramps down. If the monitored current is higher than current limit threshold,  $t_{ON}$  is inhibited until the current returns back to below the threshold.

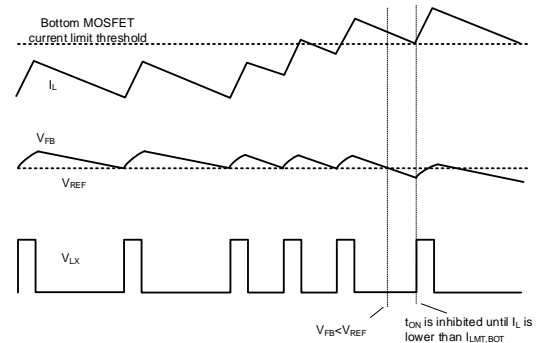


Figure11. Bottom Current Limit Protection

When the valley current limit occurs, the output current limit value is

$$I_{LMT,OUT} = I_{LMT,BOT} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

The valley current limit protection limits the inductor current, but the OCP itself is a non-latched protection. When the load current is higher than the bottom MOSFET current limit threshold by one half of the peak-to-peak inductor ripple current, the output voltage starts to drop. When the feedback voltage falls below the under voltage protection (UVP) threshold, and continues for the UVP delay time, the buck converter will be disabled and enter latch-off state. Independent from this mechanism, the over temperature protection may also be triggered under the over current condition and the buck converter will be disabled and enter latch-off state.

The buck converter also features cycle-by-cycle peak current limit (top MOSFET current limit). During the  $t_{ON}$  time, the top MOSFET current is monitored. If it exceeds the current limit threshold, the MOSFET will be turned off, and the bottom MOSFET will be turned on.  $t_{ON}$  can be not

inhibited when the bottom MOSFET current is lower than the bottom MOSFET current limit threshold.

The device supports programmable peak and valley current limit threshold when SEL is low. The detailed pin configuration is shown in *Table2*.

R <sub>SEL</sub> to GND	I <sub>LMT, TOP</sub>	I <sub>LMT, BOT</sub>
≤ 1kΩ ± 10%	≥ 13.5A	≥ 9A
30kΩ ± 10%	≥ 6A	5.5A ≥ I <sub>LMT, BOT</sub> ≥ 3.5A
100kΩ ± 10%	≥ 19A	≥ 13A

Table2. Programmable Current Limit Threshold

### Buck Output Under Voltage Protection (UVP)

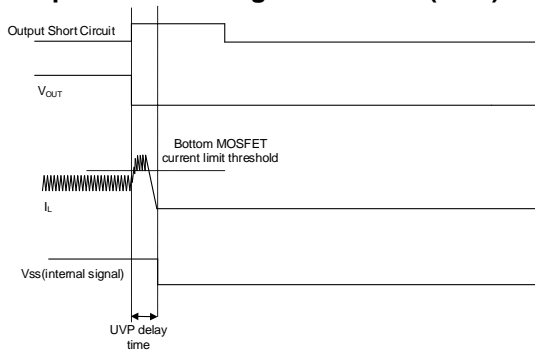


Figure12. Output Under Voltage Protection

If  $V_{OUT} < \sim 60\%$  of the regulated value for approximately 200μs occurring when the output short circuit or the load current is much higher than the maximum current capacity, the output under voltage protection (UVP) will be triggered, and the buck converter will be disabled and set to a latch-off state. Cycle EN input to re-enable the buck converter.

### Buck Output Over Voltage Protection (OVP)

The buck converter includes output over voltage protection (OVP). If the feedback voltage rises above the reference voltage level, the top MOSFET naturally remains off and different actions are taken depending on the operation mode.

When operating in PFM or PFM+ light load mode, if the feedback voltage remains high, the bottom MOSFET remains on until the inductor current reaches zero and the LX node switching actions are suppressed. If the feedback voltage doesn't exceed the over voltage protection threshold, the LX node switching actions will be resumed when the combined feedback and ramp signals become lower than the reference voltage. If the feedback voltage exceeds the over voltage protection threshold for the OVP delay time, the output over voltage protection (OVP) will be triggered, and the buck converter will be disabled and enter latch off state. Cycle EN input to re-enable the buck converter.

When operating in USM light load mode, if the feedback voltage remains high, the bottom MOSFET turn on time will be longer and inductor current average value becomes more and more negative until the reverse current limit is triggered, trying to make output voltage lower. If the feedback voltage exceeds the OVP threshold for the OVP delay time, the protection will be triggered, and the buck converter will be disabled and enter latch off state. Cycle EN input to re-enable the buck converter. False OVP triggers may happen under USM light load conditions, if the inductance value is chosen too low.

### Buck Over Temperature Protection (OTP)

The buck converter includes over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. When the thermal sensor detects a junction temperature exceeding 150°C, the over temperature protection (OTP) will be triggered, and the buck converter will be disabled and enter a latch off state. In this case the LDO is not disabled. Cycle EN to re-enable the buck converter after the junction temperature cools down about 15°C. For continuous operation, provide adequate thermal dissipation so that the junction temperature does not exceed the OTP threshold.

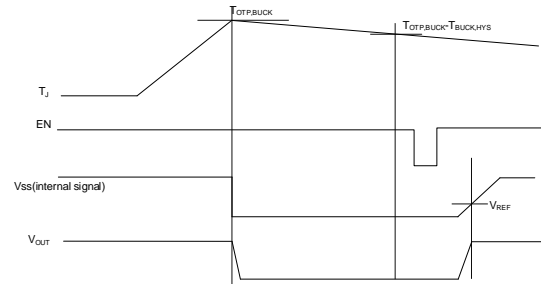


Figure13. Over Temperature Protection

### LDO Output Current Limit

The device features LDO current limit to guarantee LDO safe operation in all operating conditions. When the LDO output voltage is less than the target value after LDO is turned on, the internal LDO regulator or bypass switch will operate in current limit mode until the LDO output voltage is reaches the target. For example, when a LDO output short circuit occurs, the LDO will operate in a current limit mode. The LDO will switch to normal operation after the short circuit condition is removed.

### LDO Over Temperature Protection

The device also features auto-recovery mode LDO over temperature protection to guarantee LDO safe operation when under increased power dissipation. When the LDO thermal sensor detects that the junction temperature exceeds 160°C, the LDO will be turned off. When the junction temperature cools down by approximately 25°C, the LDO will be turned on, and the buck converter will also be recovered as experiencing once EN input re-enabling.

## Design Procedure

### Feedback Resistor Divider Selection

If the SEL pin is low, choose  $R_H$  and  $R_L$  to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both  $R_H$  and  $R_L$ . A value of between 10k $\Omega$  and 1M $\Omega$  is strongly recommended for both resistors. If  $V_{SET}$  is 3.3V,  $R_H = 100k\Omega$  is chosen, then using following equation,  $R_L$  can be calculated to be 22.1k $\Omega$ .

$$R_L = \frac{0.6V}{V_{SET} - 0.6V} \times R_H$$

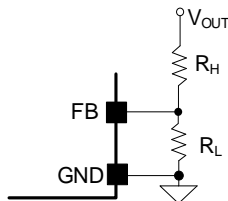


Figure14. Feedback Resistor Divider

### Buck Input Capacitor Selection

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply and to reduce EMI. When selecting the input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X5R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability and high RMS current ratings over a wide temperature and voltage range. However, systems which are powered by a wall adapter or a long inductive cable may be susceptible to significant inductive ringing at the input of the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum or polymer type capacitors. Using a combination of bulk capacitors (to reduce input overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current,

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at  $D = 0.5$ , then

$$I_{CIN\_RMS\_MAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification. Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated by

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1 - D)$$

The worst-case condition occurs at  $D = 0.5$ , then

$$V_{CIN\_RIPPLE,CAP\_MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications two 10 $\mu$ F X5R capacitors are sufficient. Place the ceramic input capacitor as close to the device's IN and GND pin as possible.

### Buck Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the LX node.

The buck converter operates well over a wide range of inductance values. This flexibility allows for optimization to find the best trade-off between efficiency, cost and size for a particular application. Selecting a low inductance value will help reduce size and cost and enhance transient response, but will increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low inductance value inductors may help reduce DC losses and increase efficiency. Choosing higher inductance value inductors tend to have higher DCR and will slow down transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a ripple current ( $\Delta I_L$ ) about 20% ~ 50% of the desired full output load current. Start calculating the approximate inductance value by selecting the input and output voltages, the operating frequency ( $f_{SW}$ ), the maximum output current ( $I_{OUT\_MAX}$ ) and estimating a  $\Delta I_L$  as some percentage of that current.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current ( $\Delta I_L$ ) and required peak current inductor current  $I_{L\_PEAK}$ .

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{\Delta I_L}{2}$$

Select an inductor with a saturation current and thermal rating in excess of  $I_{L,PEAK}$ .

If USM light load operation is selected, make sure the inductance value is high enough to avoid reverse current limit is been triggered just under steady state if the load current is zero.

For highest efficiency, select an inductor with a low DCR that meets the inductance, size and cost targets. Selecting low loss ferrite materials is recommended.

### Buck Inductor Design Example

Consider a typical design for a buck converter providing 3.338V<sub>OUT</sub> at 8A from 13.5V<sub>IN</sub>, operating at 600kHz and using target inductor ripple current ( $\Delta I_L$ ) of 40% or 3.2A.

First, determine the approximate inductance value:

$$L = \frac{3.338V \times (13.5V - 3.338V)}{13.5V \times 600kHz \times 3.2A} = 1.31\mu H$$

Next, select the nearest standard inductance value, in this case 1.5 $\mu$ H, and calculate the resulting inductor ripple current ( $\Delta I_L$ ):

$$\Delta I_L = \frac{3.338V \times (13.5V - 3.338V)}{13.5V \times 600kHz \times 1.5\mu H} = 2.79A$$

$$I_{L,PEAK} = 8A + \frac{2.79A}{2} = 9.395A$$

The resulting 2.79A ripple current is 2.79A/8A is ~34.875%, which is within the 20% ~ 50% target.

$$I_{L,PEAK,RVS} = \frac{2.79A}{2} = 1.395A < I_{LMT,RVS}$$

Finally, select an available inductor with a saturation current higher than the resulting  $I_{L,PEAK}$  of 9.395A.

### Buck Steady State Output Ripple

Steady state output voltage ripple at the switching frequency is caused by the inductor current ripple ( $\Delta I_L$ ) on the output capacitors ESR (ESR ripple) as well as the stored charge (capacitive ripple). When considering total ripple, both should be considered.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Consider a typical application with  $\Delta I_L = 2.79A$  using four 22 $\mu$ F ceramic capacitors under 3.338V<sub>OUT</sub>, each with an ESR of ~2m $\Omega$  for parallel total of 29.49 $\mu$ F (consider the capacitance decreases with the voltage on the capacitor) and 0.5m $\Omega$  ESR.

$$V_{RIPPLE,ESR} = 2.79A \times 0.5m\Omega = 1.395mV$$

$$V_{RIPPLE,CAP} = \frac{2.79A}{8 \times 29.49\mu F \times 600kHz} = 19.71mV$$

Total ripple = 21.105mV.

Using a 150 $\mu$ F 40m $\Omega$  POS cap, the above result is

$$V_{RIPPLE,ESR} = 2.79A \times 40m\Omega = 111.60mV$$

$$V_{RIPPLE,CAP} = \frac{2.79A}{8 \times 150\mu F \times 600kHz} = 3.875mV$$

Total ripple = 115.475mV.

### Buck Output Transient Undershoot/Overshoot

If very fast load transient must be supported, consider the effect of the output capacitor on the output transient undershoot and overshoot. Instant-PWM responds quickly to changing load conditions, however, for good performance specific considerations must be addressed, especially when using small ceramic capacitors which have low capacitance at low output voltages, which results in insufficient stored energy for load transients. Output transient undershoot and overshoot have two causes: voltage changes caused by the ESR of the output capacitor and voltage changes caused by the output capacitance and inductor current slew rate.

ESR undershoot or overshoot may be calculated as

$$V_{ESR} = \Delta I_{OUT} \times ESR$$

Using the ceramic capacitor example above and a fast load transient of +/- 4A,  $V_{ESR} = +/- 4A \times 0.5m\Omega = +/- 2mV$ . The POS capacitor result with the same load transient,  $V_{ESR} = +/- 4A \times 40m\Omega = +/- 160mV$ .

Capacitive undershoot (load increasing) is a function of the output capacitance, the load step, the inductor value and the input-output voltage difference and the maximum duty cycle factor. During a fast load transient, the maximum duty cycle of the buck converter is a function of  $t_{ON}$  and the  $t_{OFF,MIN}$ , as the control scheme is designed to rapidly ramp the inductor current by grouping together many  $t_{ON}$  pulses in this case. The maximum duty factor  $D_{MAX}$  may be calculated by

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF,MIN}}$$

Given this, the capacitive undershoot may be calculated by

$$V_{UNDERSHOOT,CAP} = - \frac{L \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times (V_{IN,MIN} \times D_{MAX} - V_{OUT})}$$

Consider a 4A load increase using the ceramic capacitor case when  $V_{IN} = 13.5V$ . At  $V_{OUT} = 3.338V$ , the result is  $t_{ON} = 412.10ns$ ,  $t_{OFF,MIN} = 150ns$ ,  $D_{MAX} = 412.10 / (412.10 + 150) = 0.733$  and

$$V_{UNDERSHOOT,CAP} = - \frac{1.5\mu H \times (4A)^2}{2 \times 29.49\mu F \times (13.5V \times 0.733 - 3.338V)}$$

$$= -62.05mV$$

Using the POS capacitor in the above example, the result is:

$$V_{UNDERSHOOT,CAP} = -\frac{1.5\mu H \times (4A)^2}{2 \times 150\mu F \times (13.5V \times 0.733 - 3.338V)} = -12.20mV$$

Capacitive overshoot (load decreasing) is a function of the output capacitance, the inductor value and the output voltage.

$$V_{OVERSHOOT,CAP} = \frac{L \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times V_{OUT}}$$

Consider a 4A load decrease using the ceramic capacitor case above. At  $V_{OUT} = 3.338V$  the result is

$$V_{OVERSHOOT,CAP} = \frac{1.5\mu H \times (4A)^2}{2 \times 29.49\mu F \times 3.338V} = 121.90mV$$

Using the POS capacitor case, the above result is

$$V_{OVERSHOOT,CAP} = \frac{1.5\mu H \times (4A)^2}{2 \times 150\mu F \times 3.338V} = 23.97mV$$

Combine the ESR and capacitive undershoot and overshoot to calculate the total overshoot and undershoot for a given application. If the system requirements are not met, recalculate with a different configuration.

### Load Transient Considerations

The device uses the COT ripple-based control strategy to achieve good stability and fast transient response. When SEL is low, in applications with high step load current, adding an RC network  $R_{FF}$  and  $C_{FF}$  between the OUT capacitors and the FB pin may further speed up the load transient response.  $R_{FF} = 1k\Omega$  and  $C_{FF} = 220pF$  have been shown to perform well in most applications. Increasing  $C_{FF}$  will speed up the load transient response if there is no stability issue.

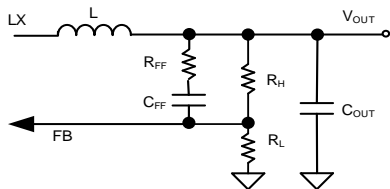


Figure15. Feedforward Network (SEL = Low)

Note: For  $C_{OUT} > 500\mu F$  and when the minimum load current is low, use PFM mode and feedforward values of  $R_{FF} = 1k\Omega$  and  $C_{FF} = 2.2nF$  to provide sufficient ripple to FB node for low output ripple and good transient behavior.

### Buck Output Capacitor Selection

The buck converter provides excellent performance with a wide variety of output capacitor types. Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the transient response and output voltage ripple requirements

of the system. When the SEL pin is low, recommend output capacitor values are shown in Table3.

$V_{OUT}(V)$	$L(\mu H)$	$C_{FF}(pF)$	$C_{OUT}(\mu F)$
1.2	0.47	220	88~286
	0.68	220	88~220
	1.0	220	88~176
3.3	1.0	220	88~330
	1.0	100	330~500
	1.5	220	88~176
	1.5	100	176~500
	2.2	220	88~132
	2.2	100	132~286
5	1.0	220	88~500
	1.5	220	88~500
	2.2	220	88~500
12	1.5	220	66~500
	2.2	220	66~500
	3.3	220	66~500

Table3. Recommended Output Capacitor Values

### Thermal Design Considerations

Maximum power dissipation depends on the thermal resistance of the device package, the PCB layout, the surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation may be calculated by:

$$P_{D,MAX} = \frac{T_{J,MAX} - T_A}{\theta_{JA}}$$

Where,  $T_{J,MAX}$  is the maximum junction temperature,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the junction to ambient thermal resistance.

To comply with the recommended operating conditions, the maximum junction temperature is  $125^\circ C$ . The junction to ambient thermal resistance  $\theta_{JA}$  is layout dependent. For the QFN2.5x2.5-17 package the thermal resistance  $\theta_{JA}$  is  $29^\circ C/W$  when measured on a standard Silergy four-layer thermal test board. These standard thermal test layouts have a very large area with long 2-oz. copper traces connected to each IC pin and very large, unbroken 1-oz. internal power and ground planes.

Meeting the performance of the standard thermal test board in a typical tiny evaluation board area requires wide copper traces well-connected to the device backside pads leading to exposed copper areas on the component side of the board as well as good thermal via from the exposed pad connecting to a wide middle-layer ground plane and, perhaps, to an exposed copper area on the board's solder side.

The maximum power dissipation at  $T_A=25^\circ C$  may be calculated by the following formula:

$$P_{D,MAX} = \frac{125^{\circ}\text{C} - 25^{\circ}\text{C}}{29^{\circ}\text{C}/\text{W}} = 3.4\text{W}$$

The maximum power dissipation depends on operating ambient temperature for fixed  $T_{J,MAX}$  and thermal resistance  $\theta_{JA}$ . Use the derating curve in figure below to calculate the effect of rising ambient temperature on the maximum power dissipation.

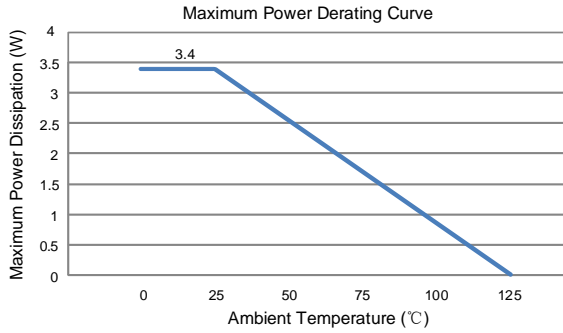
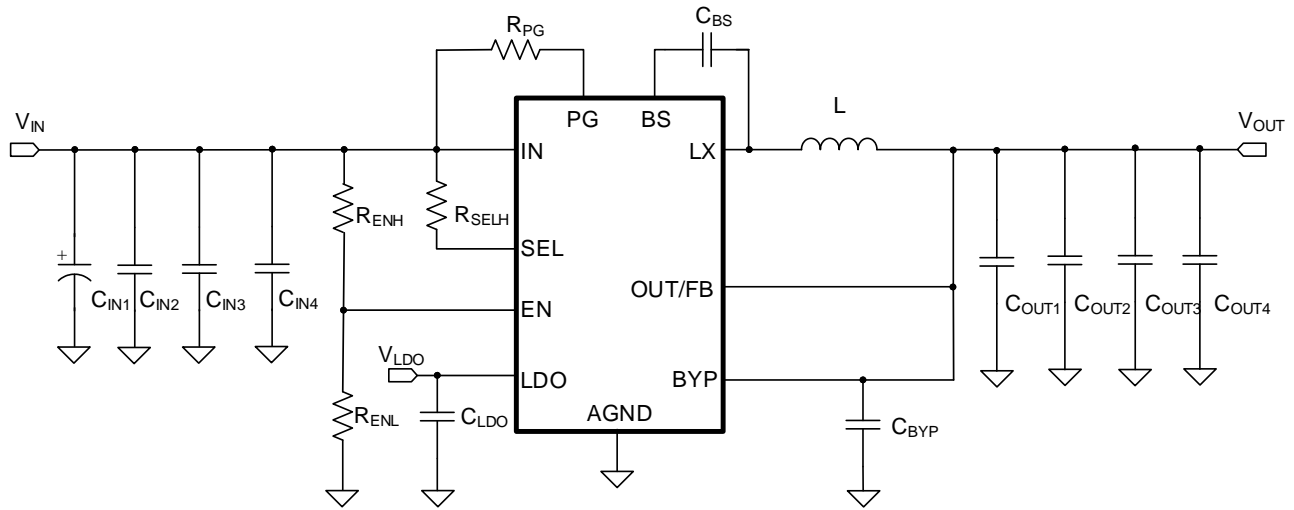


Figure 16. Maximum Power Derating Curve

**Recommended Application Schematic and BOM List**
**SEL = High**

*Figure17. Recommended Schematic Diagram (SEL = High)*

Reference Designator	Description	Part Number	Manufacturer
C <sub>IN1</sub>	47μF/50V, Electrolytic Capacitor		
C <sub>IN2</sub> , C <sub>IN3</sub>	10μF/50V/X5R, 0805	GRM21BR61H106KE43L	mμRata
C <sub>IN4</sub> , C <sub>BS</sub>	0.1μF/50V/X5R, 0603	GRM188R61H104KA93D	mμRata
C <sub>OUT1</sub> , C <sub>OUT2</sub> , C <sub>OUT3</sub> , C <sub>OUT4</sub>	22μF/6.3V/X5R, 0603	GRM188R60J226ME15D	mμRata
C <sub>LDO</sub>	4.7μF/16V/X5R, 0603	GRM185R61C475KE11D	mμRata
C <sub>BYB</sub>	1.0μF/25V/X5R, 0603	GRM188R61E105KA12D	mμRata
L	1.5μH/16A, inductor	PCMB104T-1R5MS	CYNTEC
R <sub>SELH</sub>	1kΩ, 1%, 0603		
R <sub>ENH</sub>	10kΩ, 1%, 0603		
R <sub>ENL</sub>	1MΩ, 1%, 0603		
R <sub>PG</sub>	100kΩ, 1%, 0603		

*Table4: Recommended BOM List (SEL = High)*



SEL = Floating

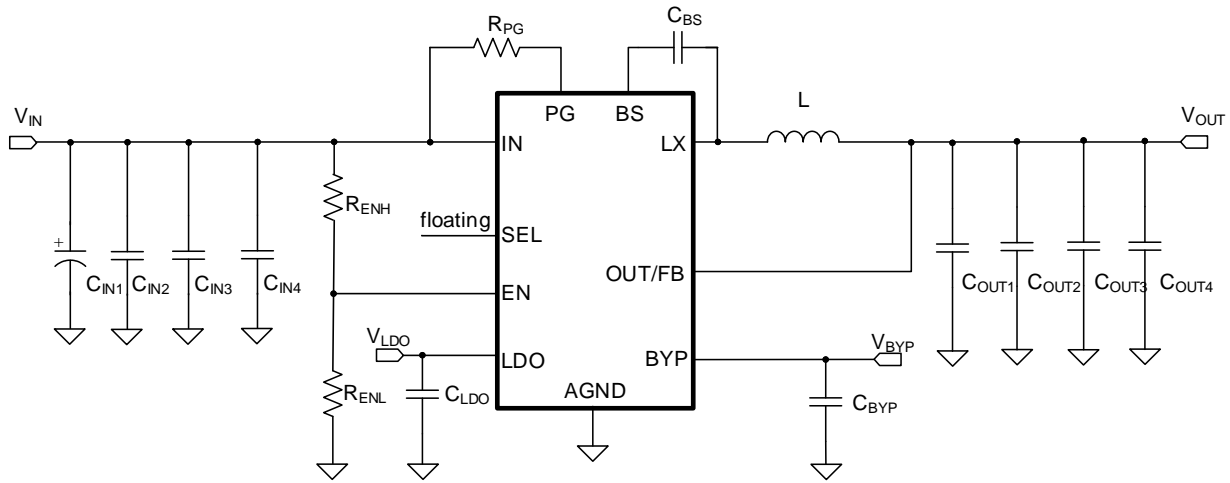


Figure 18. Recommended Schematic Diagram (SEL = Floating)

Reference Designator	Description	Part Number	Manufacturer
$C_{IN1}$	47 $\mu$ F/50V, Electrolytic Capacitor		
$C_{IN2}, C_{IN3}$	10 $\mu$ F/50V/X5R, 0805	GRM21BR61H106KE43L	m $\mu$ Rata
$C_{IN4}, C_{BS}$	0.1 $\mu$ F/50V/X5R, 0603	GRM188R61H104KA93D	m $\mu$ Rata
$C_{OUT1}, C_{OUT2}, C_{OUT3}, C_{OUT4}$	22 $\mu$ F/6.3V/X5R, 0603	GRM188R60J226ME15D	m $\mu$ Rata
$C_{LDO}$	4.7 $\mu$ F/16V/X5R, 0603	GRM185R61C475KE11D	m $\mu$ Rata
$C_{BYVP}$	1.0 $\mu$ F/25V/X5R, 0603	GRM188R61E105KA12D	m $\mu$ Rata
$L$	1.5 $\mu$ H/16A, inductor	PCMB104T-1R5MS	CYNTEC
$R_{ENH}$	10k $\Omega$ , 1%, 0603		
$R_{ENL}$	1M $\Omega$ , 1%, 0603		
$R_{PG}$	100k $\Omega$ , 1%, 0603		

Table 5. Recommended BOM List (SEL = Floating)

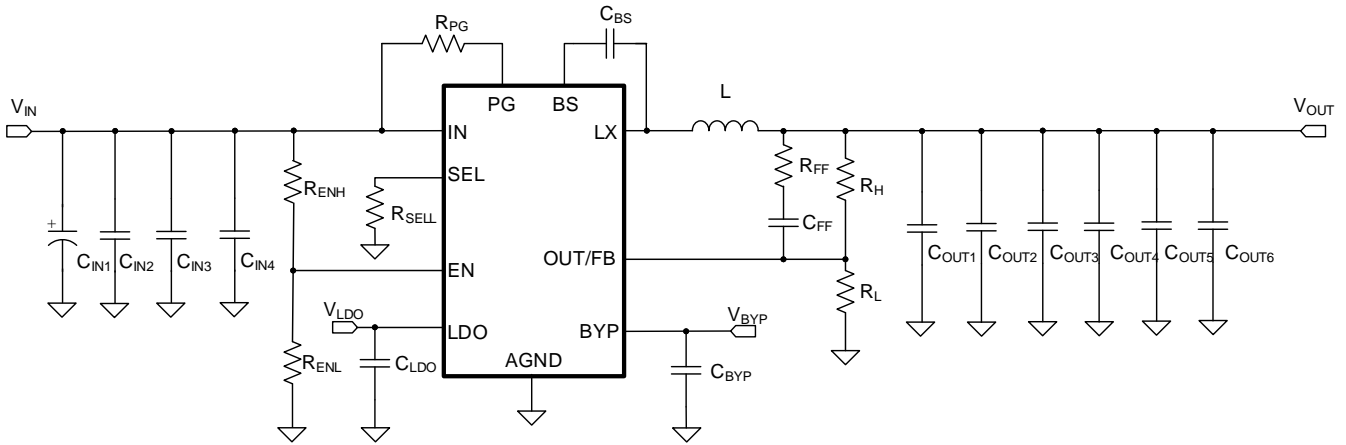


Figure19. Recommended Schematic Diagram (SEL = Low,  $V_{OUT} = 1.2V$ )

Reference Designator	Description	Part Number	Manufacturer
$C_{IN1}$	47 $\mu$ F/50V, Electrolytic Capacitor		
$C_{IN2}, C_{IN3}$	10 $\mu$ F/50V/X5R, 0805	GRM21BR61H106KE43L	m $\mu$ Rata
$C_{IN4}, C_{BS}$	0.1 $\mu$ F/50V/X5R, 0603	GRM188R61H104KA93D	m $\mu$ Rata
$C_{OUT1}, C_{OUT2}, C_{OUT3}, C_{OUT4}, C_{OUT5}, C_{OUT6}$	22 $\mu$ F/6.3V/X5R, 0603	GRM188R60J226ME15D	m $\mu$ Rata
$C_{LDO}$	4.7 $\mu$ F/16V/X5R, 0603	GRM185R61C475KE11D	m $\mu$ Rata
$C_{BYP}$	1.0 $\mu$ F/25V/X5R, 0603	GRM188R61E105KA12D	m $\mu$ Rata
$C_{FF}$	220pF/50V/C0G, 0603	GRM1885C1H221JA01D	m $\mu$ Rata
L	0.68 $\mu$ H/23A, inductor	PCMB104T-R68MS	CYNTEC
$R_{SELL}, R_{FF}$	1k $\Omega$ , 1%, 0603		
$R_{ENH}$	10k $\Omega$ , 1%, 0603		
$R_{ENL}$	1M $\Omega$ , 1%, 0603		
$R_{PG}, R_H, R_L$	100k $\Omega$ , 1%, 0603		

Table6. Recommended BOM List (SEL = Low,  $V_{OUT} = 1.2V$ )

$V_{OUT}(V)$	$R_H(k\Omega)$	$R_L(k\Omega)$	$C_{FF}(pF)$	L/Part Number	$C_{OUT}$
1.2	100	100	220	0.68 $\mu$ H/PCMB104T-R68MS	6pcs 22 $\mu$ F/6.3V/X5R, 0603
3.3	100	22.1	220	1.5 $\mu$ H/PCMB104T-1R5MS	4pcs 22 $\mu$ F/6.3V/X5R, 0603
5	100	13.7	220	1.5 $\mu$ H/PCMB104T-1R5MS	4pcs 22 $\mu$ F/6.3V/X5R, 0603
12	100	5.26	220	2.2 $\mu$ H/PCMB104T-2R2MS	3pcs 22 $\mu$ F/16V/X5R, 1206

Table7. Recommended Table (SEL = Low)

## Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation.

**Input Capacitors:** Place the input capacitor very near IN and GND, minimizing the loop formed by these connections. And the input capacitor should be connected to the IN and GND by wide copper plane. A 0.1 $\mu$ F input ceramic capacitor is recommended to reduce the input noise.

**Output Capacitors:** Guarantee the C<sub>OUT</sub> negative sides are connected with GND pin by wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.

**LDO Capacitor:** Place the LDO capacitor close to LDO pin using short, direct copper trace to AGND pin (pin 16).

**BYP Capacitor:** Place the BYP capacitor close to BYP pin using short, direct copper trace to AGND pin (pin 16) if bypass function is used. Keep bypass line width at least 20mil as it is also the 100mA LDO's bypass input.

**Feedback Network and Output Line:** Place the feedback components (R<sub>FF</sub> and C<sub>FF</sub>, and R<sub>H</sub> and R<sub>L</sub> if necessary) as close to FB pin as possible. Avoid routing the feedback line near LX, BS or other high frequency signal as it is noise sensitive. Make the feedback

sampling point Kelvin connect with C<sub>OUT</sub> rather than the inductor output terminal.

**LX Connection:** Keep LX area small to prevent excessive EMI, while providing wide copper traces to minimize parasitic resistance and inductance.

**BS Capacitor:** Place the BS capacitor on the same layer as the device, keep the BS voltage path (BS, LX and C<sub>BS</sub>) as short as possible.

**Control Signals:** It is not recommended to connect control signals and IN directly. A resistor in a range of 1k $\Omega$  to 1M $\Omega$  should be used if they are pulled high by IN.

**GND Vias:** Place adequate number of vias on the GND layer around the device for better thermal performance. Especially, make one good thermal heating GND copper trace and add several GND vias around pin 3,4,5,6,7.

**PCB Board:** A four-layer layout with 2-oz copper is strongly recommended to achieve better thermal performance. The top layer and bottom layer should place power IN and GND copper plane as wide as possible. Middle1 layer should place all GND layer for conducting heat and shielding middle2 layer signal line from top layer crosstalk. Place signal lines on middle2 layer instead of the other layers, so that the other layers' GND plane not be cut apart by these signal lines.

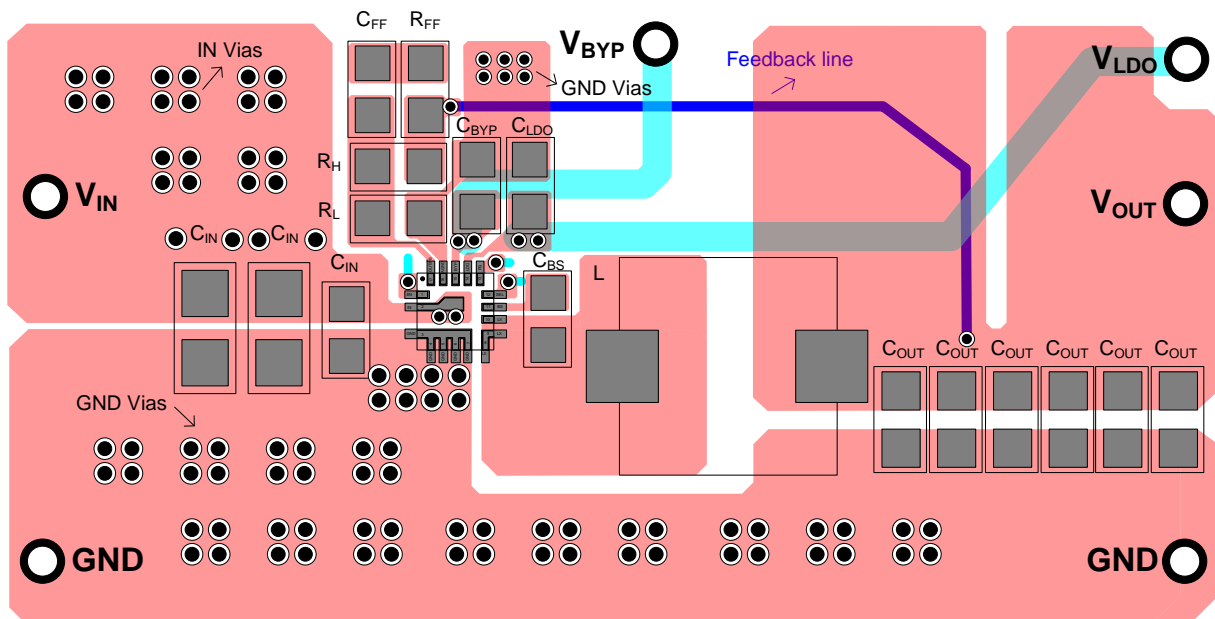
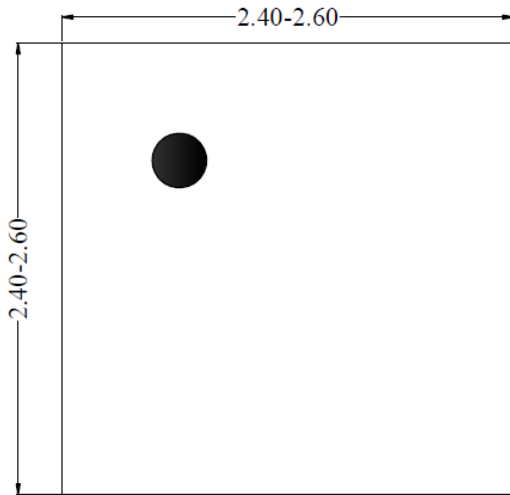
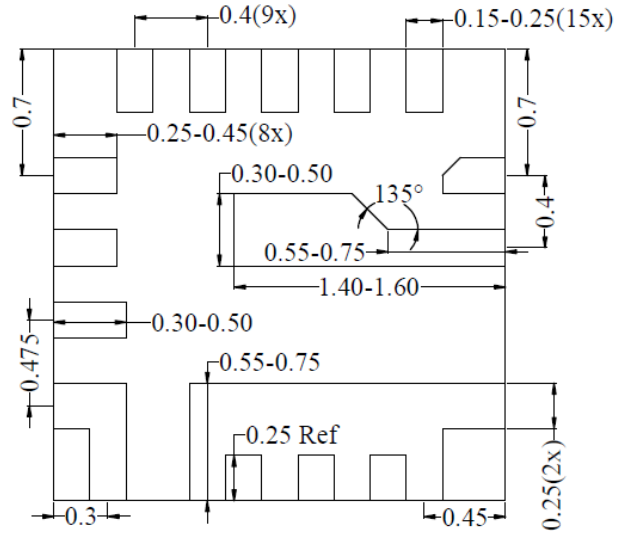


Figure20. PCB Layout Suggestion

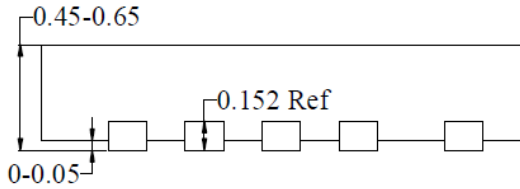
**QFN2.5x2.5-17 Package Outline Drawing**



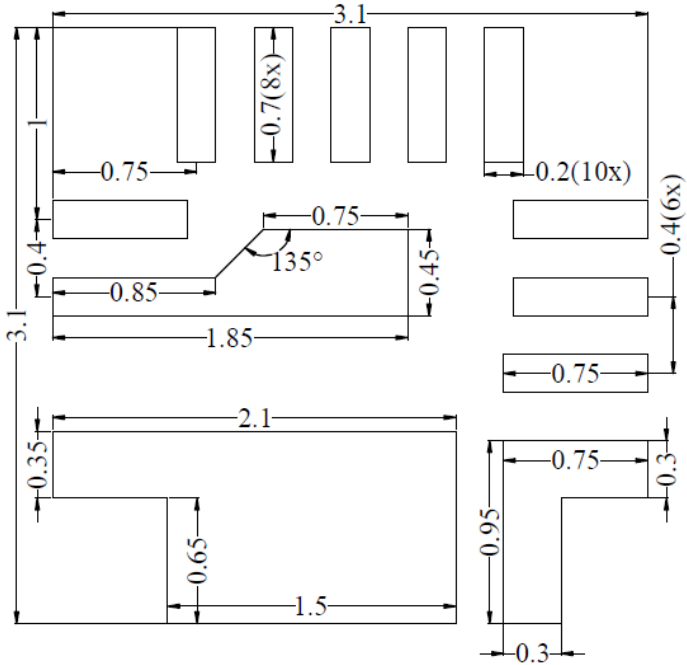
**Top View**



**Bottom View**



**Front View**

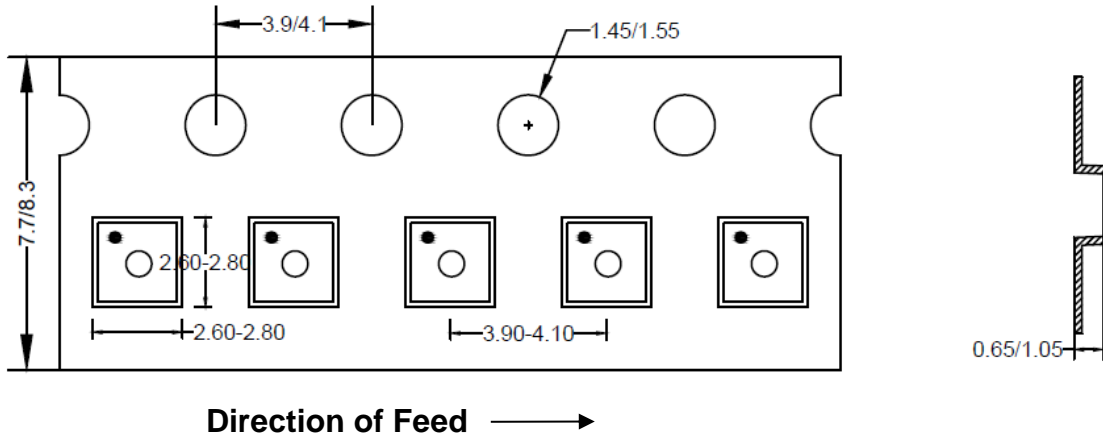


**Recommended PCB Layout  
(Reference only)**

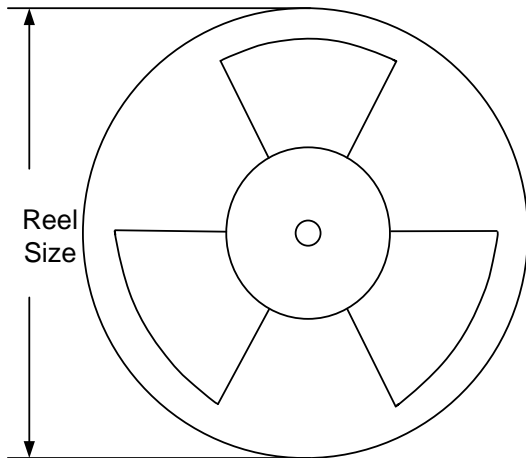
**Notes:** All dimension in millimeter and exclude mold flash & metal burr.

## Tape and Reel Information

### 1. Tape Dimensions and Pin1 Orientation QFN2.5x2.5



### 2. Reel Dimensions



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN2.5x2.5	8	4	7	400	160	3000

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## Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
Dec 23, 2025	1.0	Initial Release	-

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