

General Description

The SY89456 develops a high efficiency synchronous Buck converter capable of delivering 6A continuous. The device integrates top FET and bottom FET with very low $R_{DS(ON)}$ to minimize the conduction loss. In addition, it operates at pseudo-constant frequency of 500kHz under CCM condition to minimize the size of inductor and capacitor. The SY89456 also integrates a bypass switch which allows the VCC to be powered by external 3.3V power supply, further reduce the power consumption of the entire system.

Silergy's constant on-time and ripple-based control strategy supports high input/output voltage ratios (low duty cycles), and fast transient response while maintaining a near constant operating frequency over line, load and output voltage ranges. This control method provides stable operation without complex compensation and even with low ESR ceramic capacitors.

The SY89456 operates over a wide input voltage range from 4V to 40V. Cycle-by-cycle current limit, input under voltage lockout, internal soft-start, output under voltage protection, over voltage protection and over temperature protection provide safe operation in all operating conditions.

Features

- Low $R_{DS(ON)}$ for Internal MOSFET: 38mΩ Top, 19mΩ Bottom
- Wide Input Voltage Range: 4V ~ 40V
- Wide Output Voltage Range: 0.6V ~ 24V
- Support 99% Duty Cycle Operation
- $\pm 1.5\%$ 0.6V Reference under $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$
- 6A Continuous Output Current Capability
- Pseudo-Constant Frequency: 500kHz
- Constant On-time and Ripple-Based Control to Achieve Fast Transient Responses
- Internal Soft-start Limits the Inrush Current
- PFM/FCCM Selectable Light Load Operation
- Selectable Peak and Valley Current Limit Threshold
- Optional BYP Input for Reducing Power Consumption
- Power Good Indicator
- Output Auto-Discharge Function
- Cycle-by-Cycle Valley, Peak and Reverse Current Limit Protection
- Hic-cup Mode Output Under Voltage Protection
- Auto-Recovery Mode Output Over Voltage Protection
- Auto-Recovery Mode Over Temperature Protection
- Input Under Voltage Lockout (UVLO)
- RoHS Compliant and Halogen Free
- Compact Package: QFN2x3-14

Applications

- LCD-TV/Net-TV/3DTV
- Set Top Box
- Monitor
- High Power AP

Typical Application

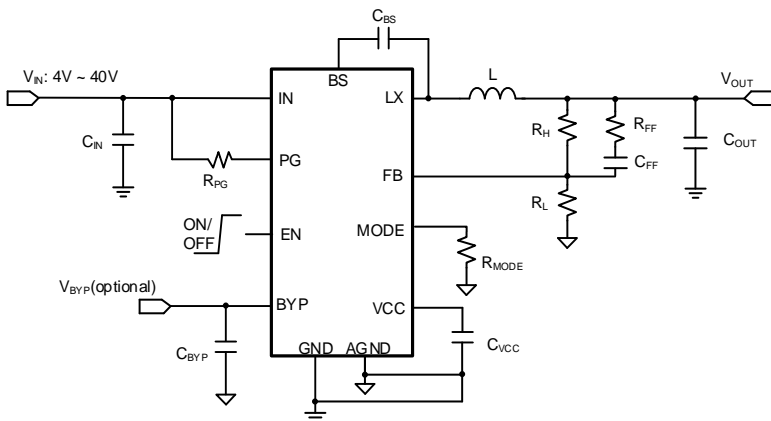


Figure1. Schematic Diagram

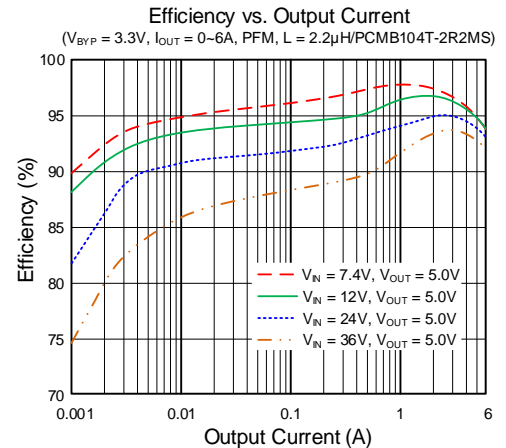


Figure2. Efficiency vs. Output Current

Ordering Information

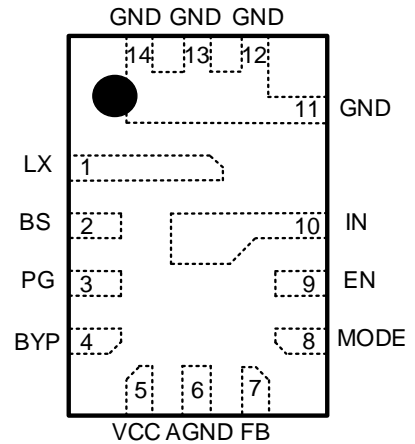
Ordering Part Number	Package type	Top Mark
SY89456WYQ	QFN2x3 -14 RoHS Compliant and Halogen Free	KDNxyz

x=year code, y=week code, z= lot number code

MODE Connection	MODE	Valley Current Limit Threshold	Peak Current Limit Threshold
VCC	PFM	4A	6A
240kΩ ±15% to GND	PFM	6A	9A
120kΩ ±15% to GND	PFM	9A	14A
GND	FCCM	4A	6A
30kΩ ±15% to GND	FCCM	6A	9A
60kΩ ±15% to GND	FCCM	9A	14A

Table 1. MODE Selection

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	LX	Inductor pin. Connect this pin to the switching node of the inductor.
2	BS	Bootstrap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between the BS pin and the LX pin.
3	PG	Power good indicator. Open drain output when the output voltage is within 90% to 120% of regulated value.
4	BYP	External 3.3V bypass power supply input. Decouple this pin to the GND with a 1μF ceramic capacitor. Leave this pin floating or connect this pin to the GND if not used.
5	VCC	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuit. Decouple this pin to GND with a 2.2μF ceramic capacitor.
6	AGND	Analog ground pin.
7	FB	Output feedback pin. Connect to the center point of resistor divider.
8	MODE	Operation mode selection. Program MODE to select FCCM/PFM, and the valley and peak current limit thresholds. Refer to Table 1 for more details.
9	EN	Enable control of the Buck regulator. Pull high to turn on the Buck regulator and pull low to turn off the Buck regulator. Do not leave this pin floating.
10	IN	Input pin. Decouple this pin to GND pin with at least a 10μF ceramic capacitor. A 0.1μF ceramic capacitor placed in parallel is recommended to reduce high frequency noise.
11, 12, 13, 14	GND	Ground pin.

Block Diagram

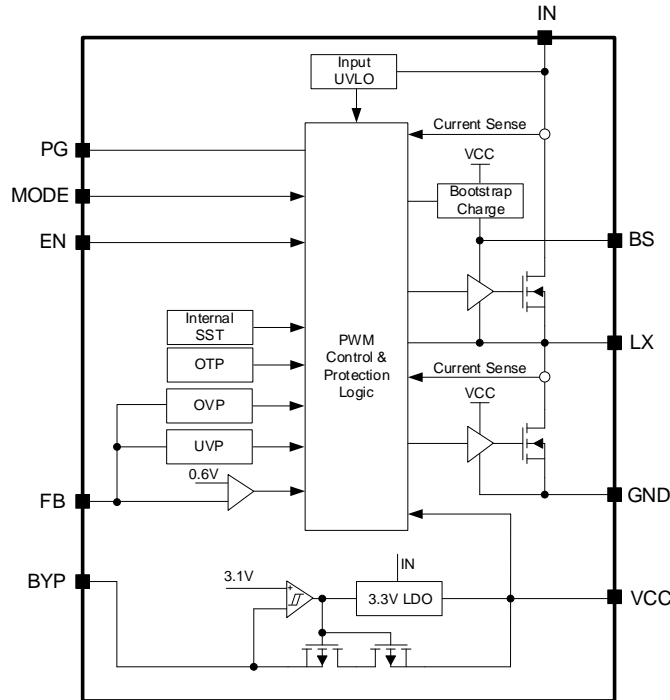


Figure3. Block Diagram

Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
IN	-0.3	40	V
LX, PG, EN, MODE	-0.3	IN + 0.3	
BS-LX, VCC, AGND, BYP	-0.3	4	
FB	-0.3	4	
Dynamic LX Voltage in 10ns Duration	GND - 5	IN + 3	
Dynamic LX Voltage in 20ns Duration	GND - 1	IN + 2	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10sec.)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	22	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	3	
P_D Power Dissipation $T_A = 25^\circ\text{C}$	4.5	W

Recommended Operating Conditions

Parameter (Note3)	Min	Max	Unit
IN	4	40	V
Output Voltage	0.6	24	
Continuous Output Current		6	A
Junction Temperature	-40	125	°C

Electrical Characteristics

 (V_{IN} = 12V, V_{OUT} = 5V, L = 2.2μH, C_{OUT} = 66μF, T_A = 25°C, I_{OUT} = 1A, unless otherwise specified (Note4))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage Range	V _{IN}		4		40	V
	UVLO Threshold	V _{IN,UVLO}	V _{IN} rising	3.4		3.95	
	UVLO Hysteresis	V _{IN,HYS}			0.3		
	Quiescent Current	I _Q	I _{OUT} = 0A, EN = High, V _{FB} = V _{REF} × 105%		60		μA
	Shutdown Current	I _{SHDN}	EN = Low		6	10	
Output	Voltage Range	V _{OUT}		0.6		24	V
	Feedback Reference Voltage	V _{REF}	T _J = -40°C ~ 125°C	0.591	0.6	0.609	
	Discharge Current	I _{DIS}	V _{OUT} = 5V		80		mA
	Soft-start Time	t _{SS}	V _{OUT} from 0% to 100% V _{SET}	0.7	1	1.3	ms
	Maximum Duty Cycle	D _{MAX}	Without inductor	99			%
	FB Input Current	I _{FB}	V _{FB} = 1V	-50		50	nA
	OVP Threshold	V _{OVP}	V _{FB} rising	115	120	125	%V _{REF}
	OVP Hysteresis	V _{OVP,HYS}			5		
	OVP Delay	t _{OVP,DLY}	(Note5)		40		μs
	UVP Threshold	V _{UVP}		45	50	55	%V _{REF}
	UVP Delay	t _{UVP,DLY}	(Note5)		50		
	UVP Hic-cup On Time	t _{HICCU,ON}	(Note5)		2		ms
	UVP Hic-cup Off Time	t _{HICCU,OFF}	(Note5)		6		
MOSFET	Top FET R _{DS(ON)}	R _{DS(ON)1}			38		mΩ
	Bottom FET R _{DS(ON)}	R _{DS(ON)2}			19		
	Top FET Current Limit Threshold	I _{LMT,TOP1}	V _{MODE} = 0V or V _{CC}	6			A
		I _{LMT,TOP2}	R _{MODE} = 30kΩ or 240kΩ	9			
		I _{LMT,TOP3}	R _{MODE} = 60kΩ or 120kΩ	14			
	Bottom FET Current Limit Threshold	I _{LMT,BOT1}	V _{MODE} = 0V or V _{CC}	4			
		I _{LMT,BOT2}	R _{MODE} = 30kΩ or 240kΩ	6			
I _{LMT,BOT3}		R _{MODE} = 60kΩ or 120kΩ	9				
Bottom FET Reverse Current Limit Threshold	I _{LMT,RVS}	FCCM Mode	2.5	4	5		
Enable (EN)	Rising Threshold	V _{EN,R}		1.08	1.2	1.32	V
	Falling Threshold	V _{EN,F}		0.9	1.0	1.1	
Frequency	Switching Frequency	f _{SW}	V _{OUT} = 5V, CCM	425	500	575	kHz
	Min On-Time	t _{ON,MIN}			50		
	Min Off-Time	t _{OFF,MIN}				150	ns
Power Good	Rising Threshold	V _{PG,R}	V _{FB} rising (good)	86	90	94	%V _{REF}
	Hysteresis	V _{PG,HYS}			5		
	Delay Time	t _{PG,R}	Low to high (Note5)		200		μs
		t _{PG,F}	High to low (Note5)		40		
Low Voltage	V _{PG,LOW}	V _{FB} = 0V, I _{PG} = 5mA			0.4	V	
VCC	Output Voltage	V _{CC}	V _{CC} adds 1mA load	3.2	3.3	3.4	V
BYP	R _{DS(ON)}	R _{DS(ON),BYP}			5		Ω
	Turn on Voltage	V _{BYP}		3.05	3.15	3.25	V
	Turn on Hysteresis	V _{BYP,HYS}			0.2		
	OVP Voltage	V _{BYP,OVP}			120		%V _{CC}
OTP	Temperature	T _{OTP}	(Note5)		150		°C
	Temperature Hysteresis	T _{OTP,HYS}	(Note5)		15		



Note 1: Stresses beyond “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: Package thermal resistance is measured in the natural convection at $T_A = 25^\circ\text{C}$ on a 8.5cm×8.5cm size, four-layer Silergy Evaluation Board with 2-oz copper.

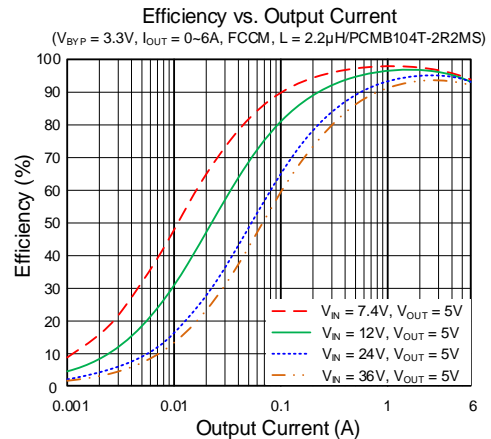
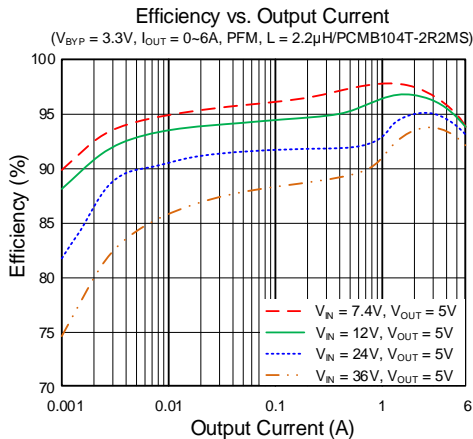
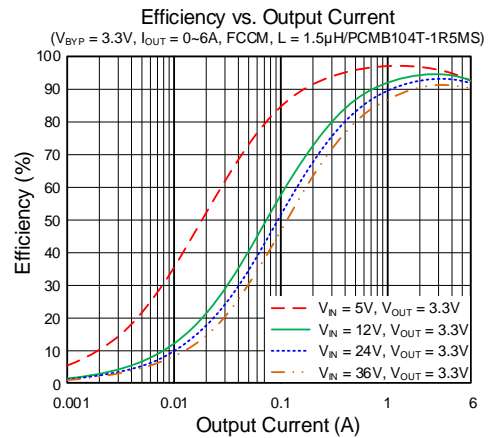
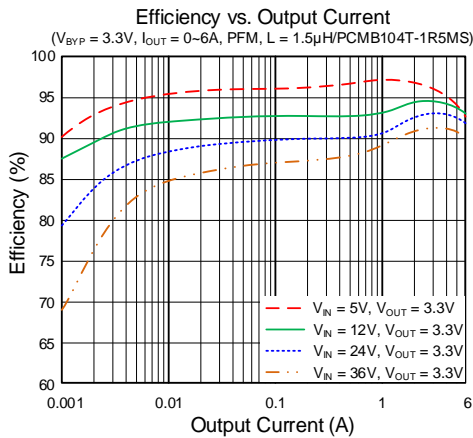
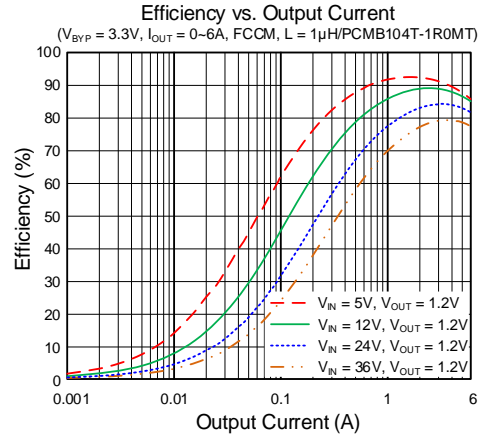
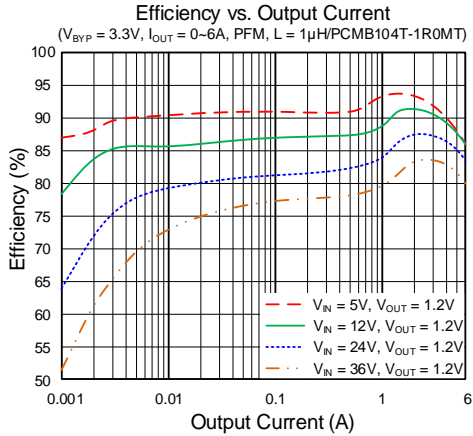
Note 3: The device is not guaranteed to function outside its operating conditions.

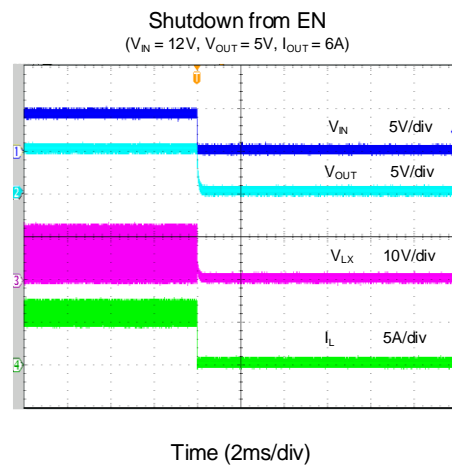
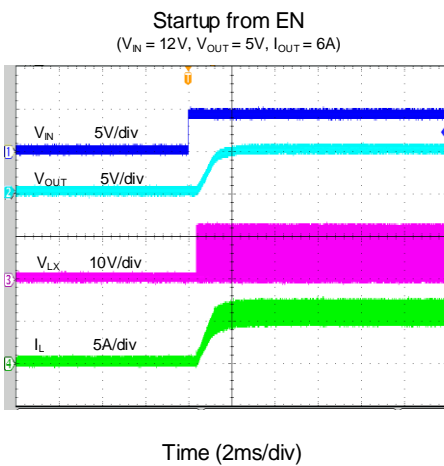
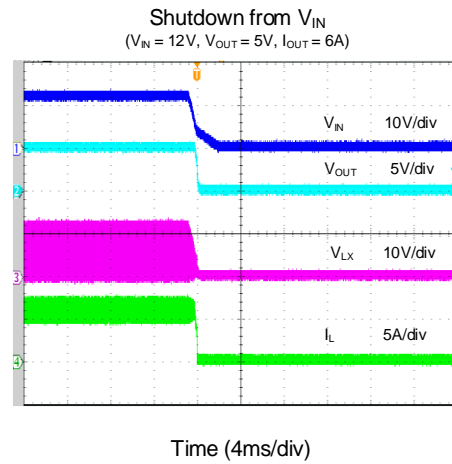
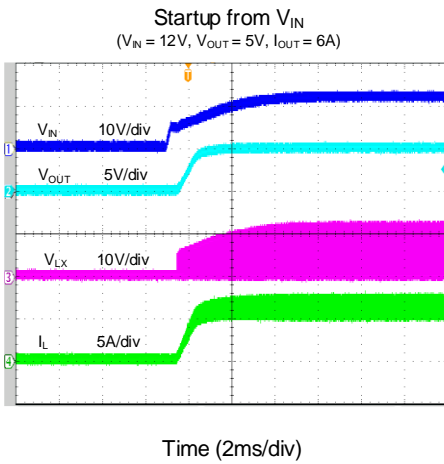
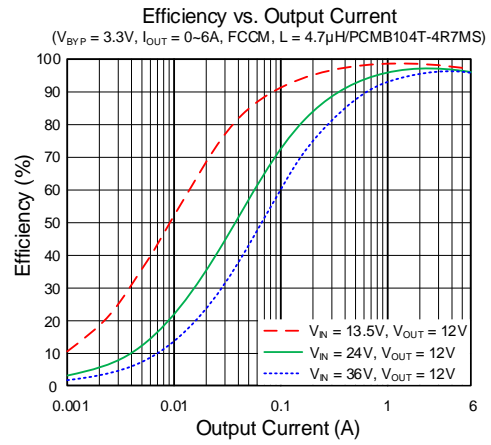
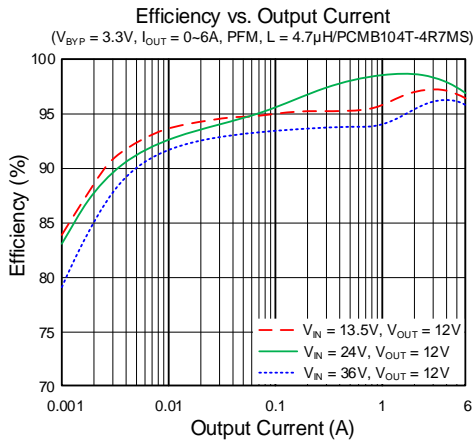
Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J = 25^\circ\text{C}$. Limits over the operating temperature range (Refer to recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design.

Typical Performance Characteristics

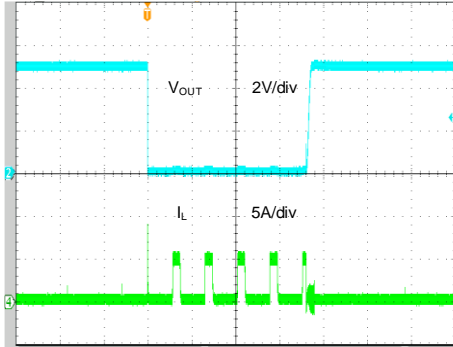
($T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $V_{OUT} = 5\text{V}$, $L = 2.2\mu\text{H}$, $C_{OUT} = 66\mu\text{F}$, $C_{FF} = 470\text{pF}$, $R_{FF} = 1\text{k}\Omega$, unless otherwise noted)





Output Short Circuit Protection

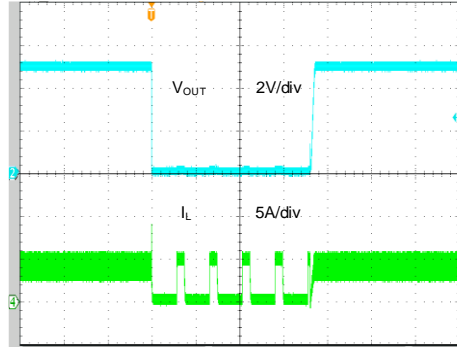
($V_N = 12V$, $V_{OUT} = 5V$, $I_{OUT} = 0A \sim \text{Short}$, $V_{MODE} = V_{CC}$)



Time (10ms/div)

Output Short Circuit Protection

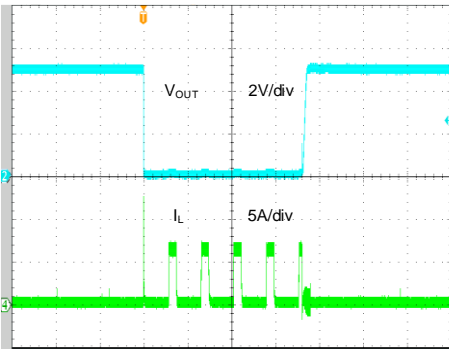
($V_N = 12V$, $V_{OUT} = 5V$, $I_{OUT} = 4A \sim \text{Short}$, $V_{MODE} = V_{CC}$)



Time (10ms/div)

Output Short Circuit Protection

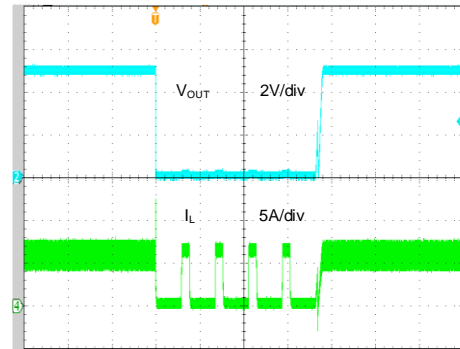
($V_N = 12V$, $V_{OUT} = 5V$, $I_{OUT} = 0A \sim \text{Short}$, $R_{MODE} = 240k\Omega$)



Time (10ms/div)

Output Short Circuit Protection

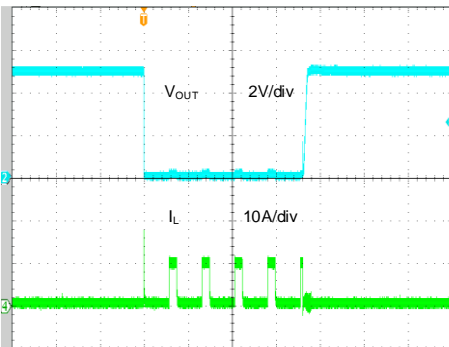
($V_N = 12V$, $V_{OUT} = 5V$, $I_{OUT} = 6A \sim \text{Short}$, $R_{MODE} = 240k\Omega$)



Time (10ms/div)

Output Short Circuit Protection

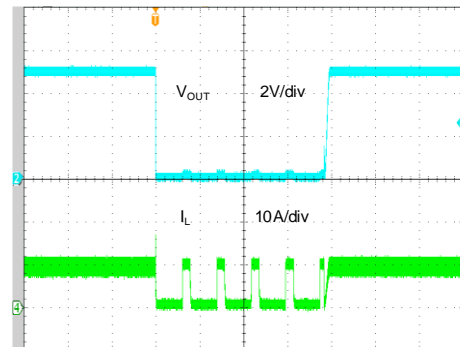
($V_N = 12V$, $V_{OUT} = 5V$, $I_{OUT} = 0A \sim \text{Short}$, $R_{MODE} = 120k\Omega$)



Time (10ms/div)

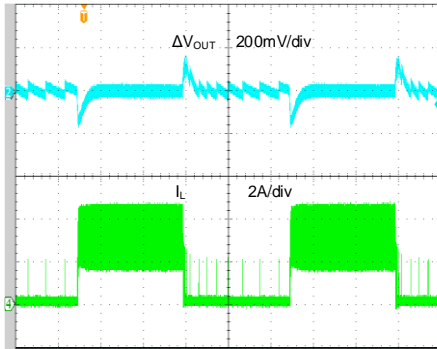
Output Short Circuit Protection

($V_N = 12V$, $V_{OUT} = 5V$, $I_{OUT} = 9A \sim \text{Short}$, $R_{MODE} = 120k\Omega$)



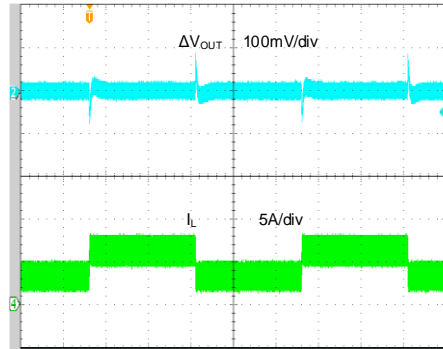
Time (10ms/div)

Load Transient
 ($V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0 - 3A, PFM$)



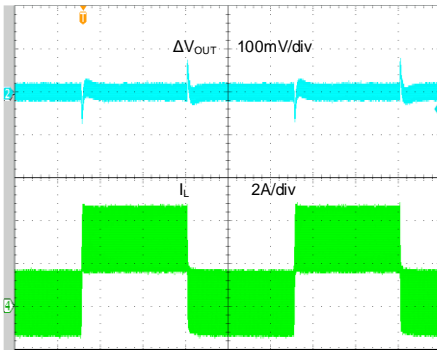
Time (400μs/div)

Load Transient
 ($V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0.6 - 6A, PFM$)



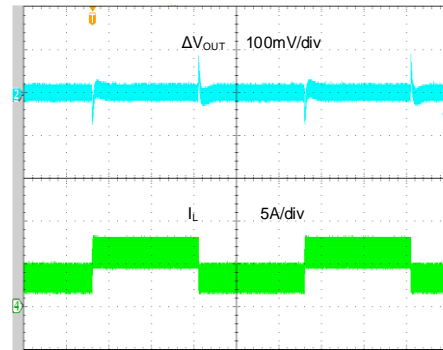
Time (400μs/div)

Load Transient
 ($V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0 - 3A, FCCM$)



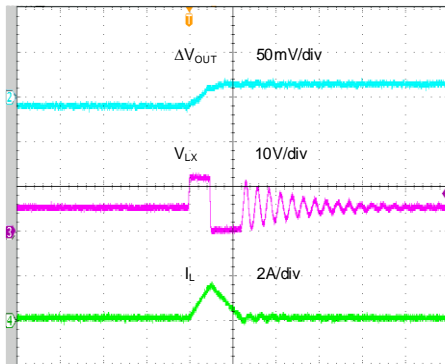
Time (400μs/div)

Load Transient
 ($V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0.6 - 6A, FCCM$)



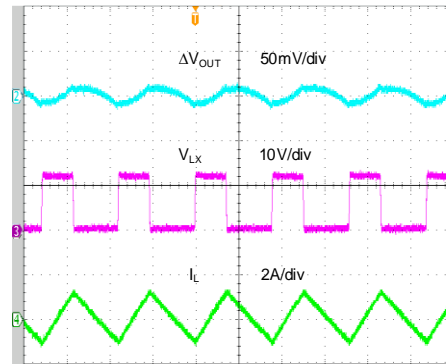
Time (400μs/div)

Output Ripple
 ($V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A, PFM$)



Time (1μs/div)

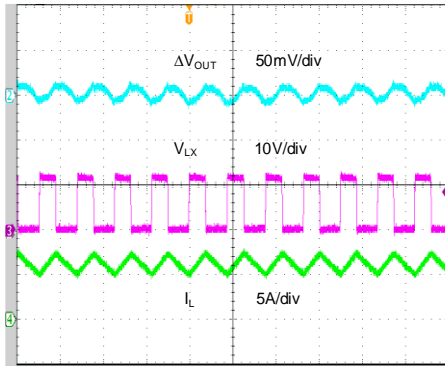
Output Ripple
 ($V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A, FCCM$)



Time (1μs/div)

Output Ripple

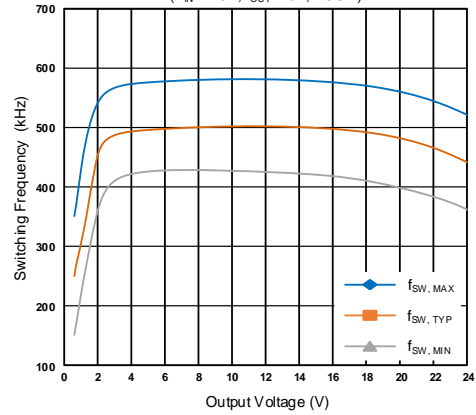
($V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A$)



Time (2 μ s/div)

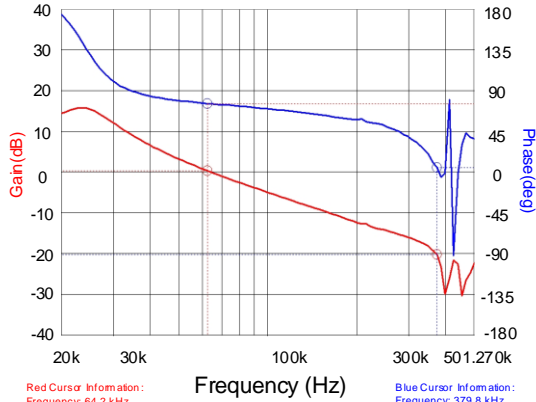
Switching Frequency vs. Output Voltage

($V_{IN} = 40V, I_{OUT} = 0A, FCCM$)



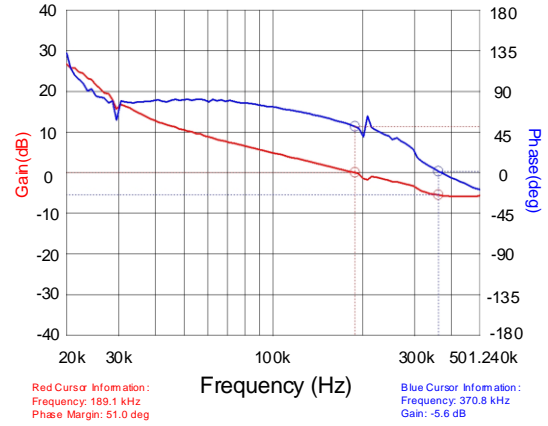
Bode Plot

($V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 3A, L = 1\mu H, PFM$)



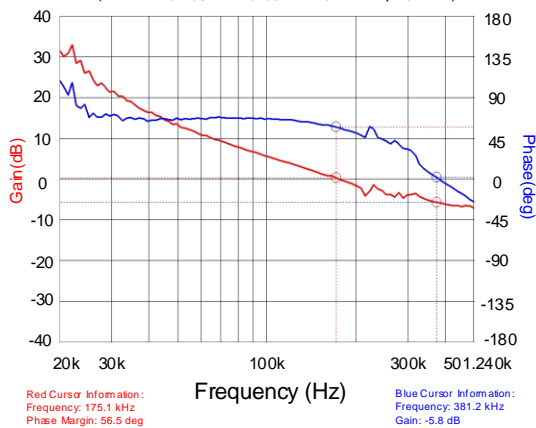
Bode Plot

($V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A, L = 1.5\mu H, PFM$)



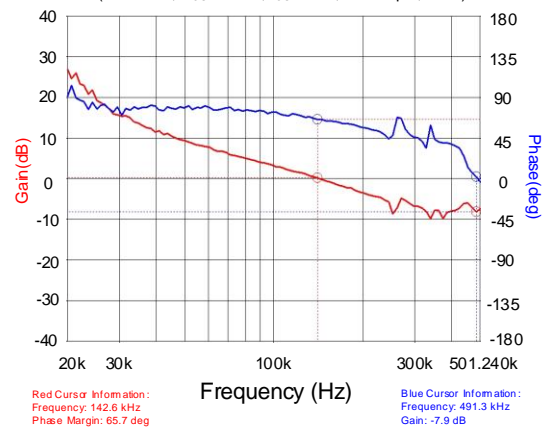
Bode Plot

($V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, L = 2.2\mu H, PFM$)



Bode Plot

($V_{IN} = 24V, V_{OUT} = 12V, I_{OUT} = 3A, L = 4.7\mu H, PFM$)



Detailed Description

General Features

Constant On-Time Architecture

Fundamental to any constant on-time (COT) architecture is the one-shot circuit or on-time generator, which determines how long to turn on the top MOSFET. Each on-time (t_{ON}) is a “fixed” voltage ratio,

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}}$$

For example, considering that a hypothetical converter targets 5V output from a 28V input at 500kHz, the target on-time is

$$\frac{5V}{28V} \times \frac{1}{500kHz} = 357.14ns$$

Each t_{ON} pulse is triggered by the feedback comparator when the output voltage as measured at FB node drops below the regulated value. After one t_{ON} period, a minimum off-time ($t_{OFF,MIN}$) is imposed before any further switching is initiated, even if the output voltage is lower than the regulated value. This approach avoids making any switching decisions during the noisy periods just after switching events and while the switching node (LX) is rapidly rising or falling.

In a COT architecture, there is no fixed clock, so the top MOSFET can turn on almost immediately after a load transient and subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays.

Minimum Duty Cycle and Maximum Duty Cycle

In the COT architecture, there is no limitation for operating the device at low duty cycle, since in this case, when the on-time is close to the minimum on-time, the switching frequency is reduced as needed to always ensure a proper operation.

To convert the output voltage during low input voltage operation, the t_{ON} can be extended to increase the duty cycle as needed. When the device detects that the feedback voltage is lower than the reference voltage during normal on-time operation, the t_{ON} will be extended. The device can support 99% open loop duty cycle if duty losses caused by MOSFET $R_{DS(ON)}$ and inductor DCR are not considered. The device can also support 100% duty cycle operation if an external voltage source greater than 2.1V is added to the BS-LX voltage.

Instant-PWM Operation

Silergy’s COT ripple-based control strategy adds several proprietary improvements to the traditional COT

architecture. Whereas most legacy based on COT implementations require a dedicated connection to the output voltage terminal to calculate the t_{ON} duration, instant-PWM control method derives this signal internally. Another improvement optimizes operation with low ESR ceramic output capacitors. In many applications it is desirable to utilize very low ESR ceramic output capacitors, but legacy COT converters may become unstable in these cases because the beneficial ramp signal that results from the inductor current flowing into the output capacitor may become too small to maintain stable operation. For this reason, instant-PWM synthesizes a virtual replica of this signal internally. This internal virtual ramp and the feedback voltage are combined and compared to the reference voltage. When the sum is lower than the reference voltage, the t_{ON} pulse is triggered as long as the minimum off-time has been satisfied and the inductor current as measured in the bottom MOSFET is lower than its current limit threshold. As the t_{ON} pulse is triggered, the bottom MOSFET turns off and the top MOSFET turns on. The inductor current ramps up linearly during the t_{ON} period. At the end of the t_{ON} period, the top MOSFET turns off, the bottom MOSFET turns on, and the inductor current ramps down linearly. This action also initiates the minimum off-time timer to ensure sufficient time for stabilizing any transient conditions and settling the feedback comparator before the next cycle is initiated. This minimum off-time is relatively short so that during fast speed load transients, t_{ON} can be retriggered with minimal delay, allowing the inductor current to ramp quickly and provide sufficient energy to the load side.

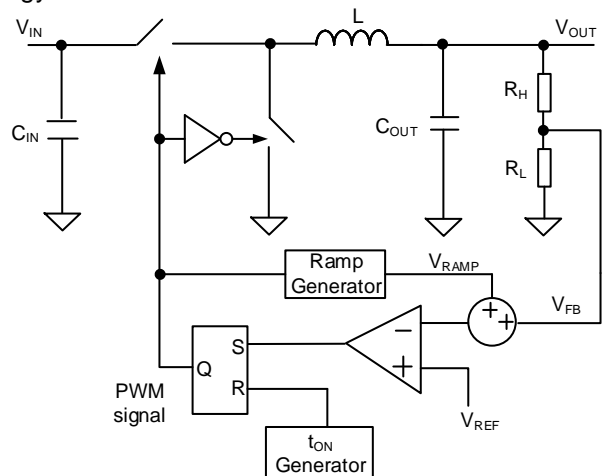


Figure4. Silergy’s COT Ripple-based Control Strategy

In order to avoid shoot-through, a dead time (t_{DEAD}) is generated internally between turning the top MOSFET off and the bottom MOSFET on, as well as between turning the bottom MOSFET off and the top MOSFET on.

Light Load Operation Mode Selection

PFM or FCCM light load operation is selected using the MODE pin. The detailed MODE pin configuration is shown in the table 1.

If PFM light load operation is selected, under light load conditions, typically when the load satisfies the following equation,

$$I_{OUT_CTL} = \frac{\Delta I_L}{2} = \frac{V_{OUT} \times (1 - D)}{2 \times f_{SW} \times L} \quad (1)$$

The current through the bottom MOSFET will ramp to near zero before the next t_{ON} time. When this occurs, the bottom MOSFET turns off, preventing recirculation current that can seriously reduce efficiency under these light load conditions. As load current is further reduced, the combined feedback and ramp signals remain much higher than the reference voltage, the instant-PWM control loop will not trigger another t_{ON} until needed, and the apparent operating switching frequency will correspondingly drop, improving efficiency. The switching frequency can be lower than audible frequency area under deep light load or null load conditions. Continuous conduction mode (CCM) resumes smoothly as soon as the load current increases sufficiently for the inductor current to remain above zero at the time of the next t_{ON} cycle. The buck converter enters CCM once the load current exceeds the threshold shown in (1). Above the threshold, the switching frequency stays fairly constant over the output current range.

If FCCM light load operation is selected, under light load conditions, the bottom MOSFET still turns on even when the inductor current crosses zero. Current flow will continue until the next t_{ON} cycle appears. The buck converter always operates under continuous conditions mode and keeps fairly constant switching frequency over all the output current range.

Input Under Voltage Lockout (UVLO)

To prevent operation before the internal circuitry is ready and to ensure that the top and bottom MOSFETs can be properly driven, the device incorporates an input under voltage lockout protection.

The device remains in a low current state and LX node switching actions are inhibited until V_{IN} exceeds the UVLO rising threshold. At that time, if EN is high, the device is enabled and soft-start ramp is initiated. If V_{IN} falls below $V_{IN,UVLO}$ less than the input UVLO hysteresis, LX node switching actions will again be suppressed.

Precise EN Threshold

The EN pin uses precise rising and falling thresholds to provide programmable ON/OFF control. The device will be turned on when the EN pin voltage exceeds the rising

threshold. The device will be turned off while the EN pin voltage falls below the falling threshold. Increasing the UVLO startup voltage threshold is possible using an external resistor divider as shown below:

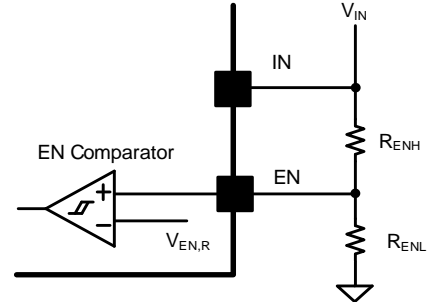


Figure5. Enable Control

It is not recommended to connect EN pin to the V_{IN} or another voltage source directly. A resistor in a range of $1k\Omega$ to $1M\Omega$ should be used for EN pin in this case.

Soft-Start and Startup with Pre-Biased Output

The device incorporates an internal soft-start circuit to ramp the output to the desired voltage whenever the device is enabled. Internally, the soft-start circuit clamps the output at a low voltage and then allows the output to rise to the desired voltage over approximately 1ms, which avoids high current flow and transients during startup. The device operates in FCCM mode during soft-start no matter which mode it selects.

The device supports startup with pre-biased output. If the output is pre-biased to a certain voltage before startup, the buck converter disables the switching of both the top MOSFET and the bottom MOSFET until the internal soft-start voltage V_{SS} exceeds the sensed output voltage at the FB node. The first pulse on-time is internally calculated based the input voltage and pre-biased output voltage.

PG Power Good Indicator

PG is an open drain output controlled by a window comparator connected to the feedback signal. If the voltage is higher than $V_{PG,R}$ and less than V_{OVP} for at least the power good delay time (low to high), PG will be set to high-impedance state.

PG should be connected to V_{IN} or another voltage source through a resistor (e.g., $100k\Omega$). After V_{IN} rises until the internal initial power is ready, the PG internal MOSFET is turned on so that PG is actively driven low before output voltage is ready. After the feedback voltage V_{FB} reaches $V_{PG,R}$, PG is set to high-impedance state after a delay time of $200\mu s$ (typ.). When V_{FB} drops to $V_{PG,F}$, or rises above V_{OVP} for the OVP delay time, PG is driven low after a delay time of $40\mu s$ (typ.).

Output Auto-Discharge Function

The device discharges the output voltage when the buck converter shuts down due to low V_{IN} or EN, or caused by a protection function being triggered, so that the output voltage can be discharged in a minimal time, even if the buck output load current is zero. The discharge MOSFET in parallel with the bottom MOSFET turns on after the bottom MOSFET turns off when the shutdown logic is enabled. The output discharge current is typically 80mA for $V_{OUT} = 5V$. The discharge MOSFET is not active outside of these shutdown conditions.

External Bootstrap Capacitor

This device integrates a floating power supply for the gate driver of the top MOSFET. Proper operation requires a $0.1\mu F$ low ESR ceramic capacitor to be connected between BS and LX. This bootstrap capacitor provides the gate driver supply voltage for the N-channel top MOSFET.

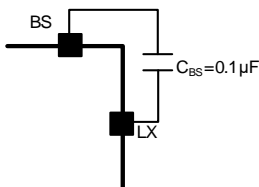


Figure6. Bootstrap Capacitor Connection

VCC Output

The device integrates a high performance, low drop-out linear regulator 3.3V VCC, which can power the internal gate drivers, PWM logic, analog circuitry and other blocks. Once the input voltage exceeds its own UVLO (rising) threshold, and EN is high, VCC is turned on and supplied power by V_{IN} . After the BYP voltage exceeds BYP turn on voltage, the internal LDO regulator will be turned off and the bypass switch will be turned on so that VCC output can switch to BYP voltage to reduce power consumption. Connect a $2.2\mu F$ low ESR ceramic capacitor from VCC to GND. Make sure the loop formed by the VCC capacitor is shorter than the loop for the BYP capacitor, if there is placement conflict between them.

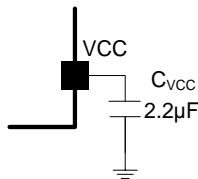


Figure7. VCC Capacitor Connection

BYP Input

When a 3.3V external power supply is connected to the BYP, the internal LDO is automatically turned off. The overall efficiency may be improved by using an external power supply. Connect a $1\mu F$ low ESR ceramic

capacitor from BYP pin to GND. Using an external low pass filter consisting of a small value resistor R_{BYP} and a ceramic capacitor C_{BYP} is recommended for applications where the external power rail has significant ripple. Connect the pin to GND or leave floating if not used.

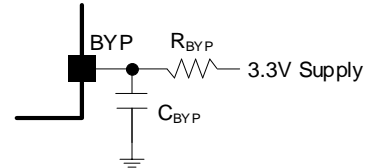


Figure8. BYP Low Pass Filter Connection

Fault Protection Modes

Output Current Limit

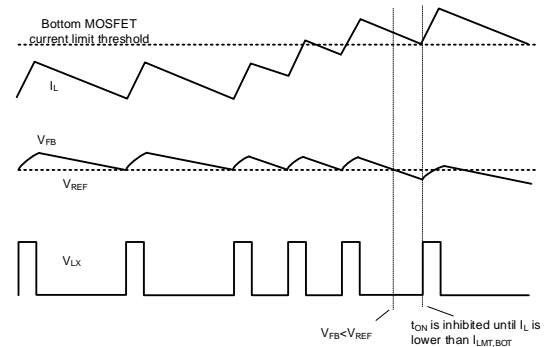


Figure9. Bottom Current Limit Protection

The buck converter features cycle-by-cycle “valley” current limit (bottom MOSFET current limit). The Inductor current is monitored in the bottom MOSFET when it turns on and as the inductor current ramps down. If the monitored current is higher than current limit threshold, t_{ON} is inhibited until the current returns back to below the threshold.

The device supports programmable peak and valley current limit threshold using MODE pin. The detailed MODE pin configuration is shown in the table 1. When the valley current limit occurs, the output current limit value is

$$I_{LMT,OUT} = I_{LMT,BOT} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

The buck converter also features cycle-by-cycle peak current limit (top MOSFET current limit). During the t_{ON} time, the top MOSFET current is monitored. If it exceeds the current limit threshold, the MOSFET will be turned off, and the bottom MOSFET will be turned on. t_{ON} can be not inhibited when the bottom MOSFET current is lower than the bottom MOSFET current limit threshold.

Output Under Voltage Protection (UVP)

If $V_{OUT} < \sim 50\%$ of the regulated value for approximately $50\mu s$ occurring when the output short circuit or the load current is much heavier than the maximum current capacity, the output under voltage protection (UVP) will be triggered, and the device will enter into hic-cup protection mode. The hic-cup on time is 2ms (typ.), and the hic-cup off time is 6ms (typ.). If the output fault conditions are removed, the buck converter will go back to normal operation in the nearest hic-cup on time.

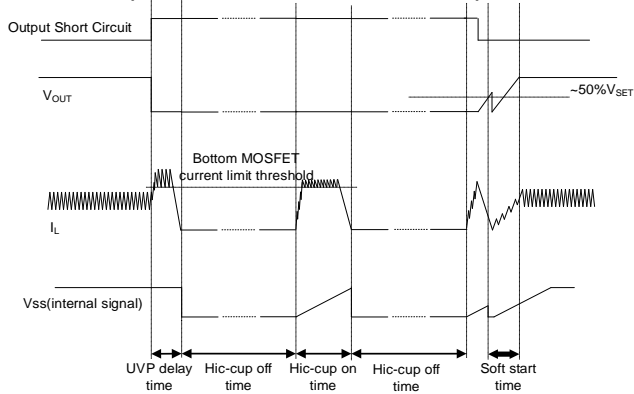


Figure 10. Output Under Voltage Protection

To avoid output overshoot, the internal soft-start circuit voltage V_{SS} should be pull low for a while when V_{FB} exceeds UVP threshold if the output fault conditions are removed during hic-cup on time, then the V_{SS} rises smoothly to ramp the output to the desired voltage during a new soft-start cycle.

Output Over Voltage Protection (OVP)

The buck converter includes output over voltage protection (OVP). If the feedback voltage rises above the feedback regulation level, the top MOSFET naturally remains off and different actions are adopted in different operation mode.

When operating in PFM light load mode, if the output voltage remains high, the bottom MOSFET remains on until the inductor current reaches zero and the LX node switching actions are suppressed. LX node switching actions will be recovered once the combined feedback and ramp signals become lower than the reference voltage.

When operating in FCCM light load mode, if the feedback voltage remains high, the bottom MOSFET turn on time will be longer and inductor current average value becomes more and more negative until the reverse current limit is triggered, trying to make output voltage lower. If the feedback voltage exceeds the OVP threshold for the OVP delay time, the protection will be triggered, and LX node switching actions will be suppressed. LX

node switching actions will be recovered once the combined feedback and ramp signals become lower than the reference voltage. False OVP triggers may happen under FCCM light load condition, if the inductance value is chosen too low.

Over Temperature Protection (OTP)

The buck converter includes over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. When the thermal sensor detects the junction temperature exceeds $150^{\circ}C$, the over temperature protection (OTP) will be triggered, and the buck converter will be disabled, once the junction temperature cools down by approximately $15^{\circ}C$, the buck converter will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature will not exceed the OTP threshold.

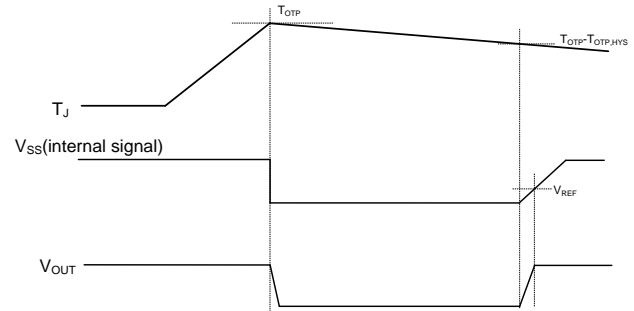


Figure 11. Over Temperature Protection

Design Procedure

The following paragraphs provide information on the selection of the external components needed to meet the targeted application specifications.

Feedback Resistor Divider R_H and R_L

Choose R_H and R_L to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_H and R_L . A value of between $1k\Omega$ and $1M\Omega$ is recommended for both resistors. As an example, if $V_{SET} = 5V$ and R_H selected value is $100k\Omega$, R_L can be calculated as follows:

$$R_L = \frac{0.6V}{V_{SET} - 0.6V} \times R_H$$

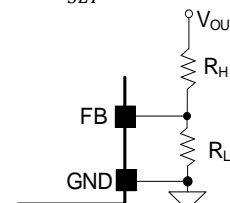


Figure 12. Feedback Resistor Divider

With a calculated value of 13.7kΩ for R_L, a standard 1% 13.7kΩ resistor is selected.

Input Capacitor C_{IN}

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply and to reduce EMI. When selecting the input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X5R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability and high RMS current ratings over a wide temperature and voltage range. However, systems which are powered by a wall adapter or a long inductive cable may be susceptible to significant inductive ringing at the input of the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum or polymer type capacitors. Using a combination of bulk capacitors (to reduce input overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN_RMS_MAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification. Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1 - D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN_RIPPLE,CAP_MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications a single 10μF X5R capacitor is sufficient. Place the ceramic input capacitor as close to the device's IN and GND pin as possible.

Output Inductor L

Consider the following when choosing this inductor:

- 1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 0.4}$$

Where f_{SW} is the switching frequency and I_{OUT,MAX} is the maximum load current.

The device has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

- 2) Make sure the inductance value is high enough to avoid reverse current limit threshold is been triggered just under steady state if the load current is zero.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L,PEAK,RVS} = \frac{\Delta I_L}{2} < I_{LMT,RVS}$$

- 3) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

- 4) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Use an inductor with DCR less than 20mΩ to achieve good overall efficiency.

Output Capacitor C_{OUT}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting C_{OUT}. For the best performance, use a X5R or better grade ceramic capacitor with a 16V rating, and capacitance of at least 10μF.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed.

The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, consider both.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The measured capacitive ripple might be higher than the theoretical value because the effective capacitance for ceramic capacitors decreases with the voltage across its terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Load Transient Considerations

The device integrates the compensation components to achieve good stability and fast transient responses.

For most applications, adding the RC network R_{FF} and C_{FF} in parallel with R_H may further enhance the transient response of the load, as shown in Figure 13. $R_{FF} = 1k\Omega$ and $C_{FF} = 220pF$ is recommended for most applications. Note that when the output LC parameter is large, the feedforward capacitor can be increased to provide sufficient ripple to FB for small output ripple and good transient behavior.

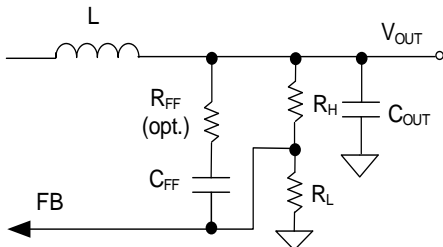


Figure 13. Feedforward Network without LX compensation

For $C_{OUT} > 500\mu F$ and when the minimum load current is low, use feedforward values of $R_{FF} = 1k\Omega$ and $C_{FF} = 2.2nF$ to provide sufficient ripple to FB node for low output ripple and good transient behavior.

For small duty cycle applications (generally less than 20%), additional compensation is recommended, as shown in Figure 14. An RC network (specifically R_{LX} and C_{FF}) should be added between the LX and OUT terminals to achieve a ripple that is in phase with the inductor current. This ripple can then be fed forward to the FB through the capacitor C_{COUPLE} . The recommended values for R_{LX} , C_{FF} , and C_{COUPLE} should consider both good stability and fast transient responses. For 1.2V output, it is recommended to use $C_{FF} = 220pF$, $C_{COUPLE} = 470pF$, and $R_{LX} = 100k\Omega$.

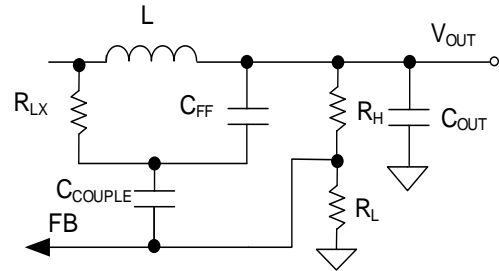


Figure 14. Feedforward Network with LX compensation

Thermal Design Considerations

Maximum power dissipation depends on the thermal resistance of the device package, the PCB layout, the surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation may be calculated by:

$$P_{D,MAX} = \frac{T_{J,MAX} - T_A}{\theta_{JA}}$$

Where, $T_{J,MAX}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

To comply with the recommended operating conditions, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For the QFN2x3-14 package the thermal resistance θ_{JA} is 22°C/W when measured on a standard Silergy 8.5cmx8.5cm size four-layer thermal test board. These standard thermal test layouts have a very large area with long 2-oz copper traces connected to each device pin and very large, unbroken 1-oz internal power and ground planes.

Meeting the performance of the standard thermal test board in a typical tiny evaluation board area requires wide copper traces well-connected to the device backside pads leading to exposed copper areas on the component side of the board as well as good thermal via from the exposed pad connecting to a wide middle-layer ground plane and, perhaps, to an exposed copper area on the board's solder side.

The maximum power dissipation at $T_A = 25^\circ C$ may be calculated by the following formula:

$$P_{D,MAX} = \frac{125^\circ C - 25^\circ C}{22^\circ C/W} = 4.55W$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J,MAX}$ and thermal resistance θ_{JA} . Use the derating curve in figure below to calculate the effect of rising ambient temperature on the maximum power dissipation.

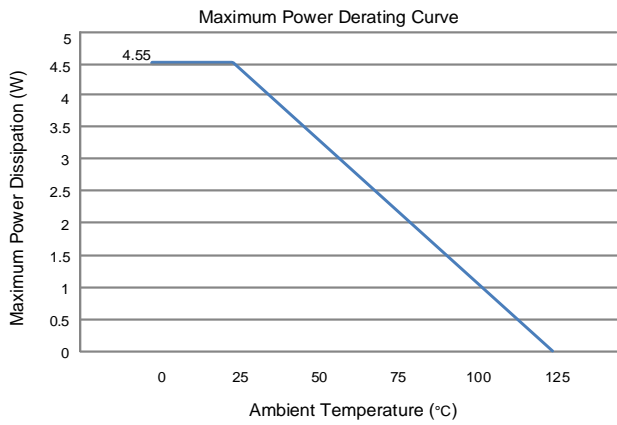


Figure15. Maximum Power Derating Curve

Recommended Application Schematic and BOM List

$V_{OUT} = 1.2V$

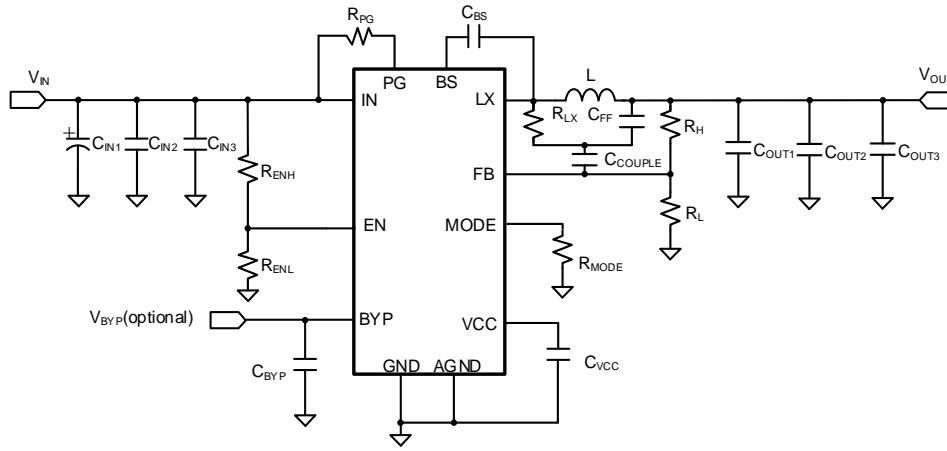


Figure16. Recommended Schematic Diagram ($V_{OUT} = 1.2V$)

Designator	Description	Part Number	Manufacturer
C _{IN1}	47 μ F/50V, Electrolytic Capacitor		
C _{IN2}	10 μ F/50V/X5R, 1206	GRM31CR61H106KA12L	m μ Rata
C _{IN3} , C _{BS}	0.1 μ F/50V/X5R, 0603	GRM188R61H104KA93D	m μ Rata
C _{OUT1} , C _{OUT2} , C _{OUT3}	22 μ F/16V/X5R, 1206	GRM31CR61C226ME15L	m μ Rata
C _{VCC}	2.2 μ F/16V/X5R, 0603	GRM188R61C225KE15D	m μ Rata
C _{BY_P}	1.0 μ F/25V/X5R, 0603	GRM155R61E105KE11D	m μ Rata
C _{FF}	220pF/50V/C0G, 0603	GRM1885C1H221JA01D	m μ Rata
C _{COUPLE}	470pF/50V/C0G, 0603	GRM1885C1H471JA01D	m μ Rata
L	1.0 μ H/18A, inductor	PCMB104T-1R0MT	CYNTEC
R _{ENH}	10k Ω , 1%, 0603		
R _{ENL}	1M Ω , 1%, 0603		
R _H , R _L , R _{PG} , R _{LX}	100k Ω , 1%, 0603		
R _{MODE}	240k Ω , 1%, 0603		

Table2. Recommended BOM List ($V_{OUT} = 1.2V$)

$V_{OUT} = 3.3V$

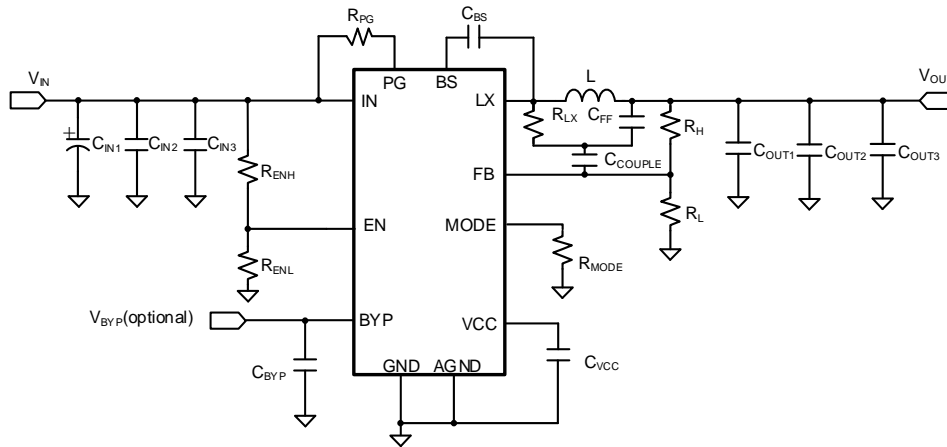


Figure17. Recommended Schematic Diagram ($V_{OUT} = 3.3V$)

Designator	Description	Part Number	Manufacturer
C _{IN1}	47μF/50V, Electrolytic Capacitor		
C _{IN2}	10μF/50V/X5R, 1206	GRM31CR61H106KA12L	mμRata
C _{IN3} , C _{BS}	0.1μF/50V/X5R, 0603	GRM188R61H104KA93D	mμRata
C _{OUT1} , C _{OUT2} , C _{OUT3}	22μF/16V/X5R, 1206	GRM31CR61C226ME15L	mμRata
C _{VCC}	2.2μF/16V/X5R, 0603	GRM188R61C225KE15D	mμRata
C _{BYP}	1.0μF/25V/X5R, 0603	GRM155R61E105KE11D	mμRata
C _{FF}	220pF/50V/C0G, 0603	GRM1885C1H221JA01D	mμRata
C _{COUPLE}	470pF/50V/C0G, 0603	GRM1885C1H471JA01D	mμRata
L	1.5μH/16A, inductor	PCMB104T-1R5MS	CYNTEC
R _{ENH}	10kΩ, 1%, 0603		
R _{ENL}	1MΩ, 1%, 0603		
R _H , R _{PG} , R _{LX}	100kΩ, 1%, 0603		
R _L	22.1kΩ, 1%, 0603		
R _{MODE}	240kΩ, 1%, 0603		

Table3. Recommended BOM List ($V_{OUT} = 3.3V$)

$V_{OUT} = 5V$

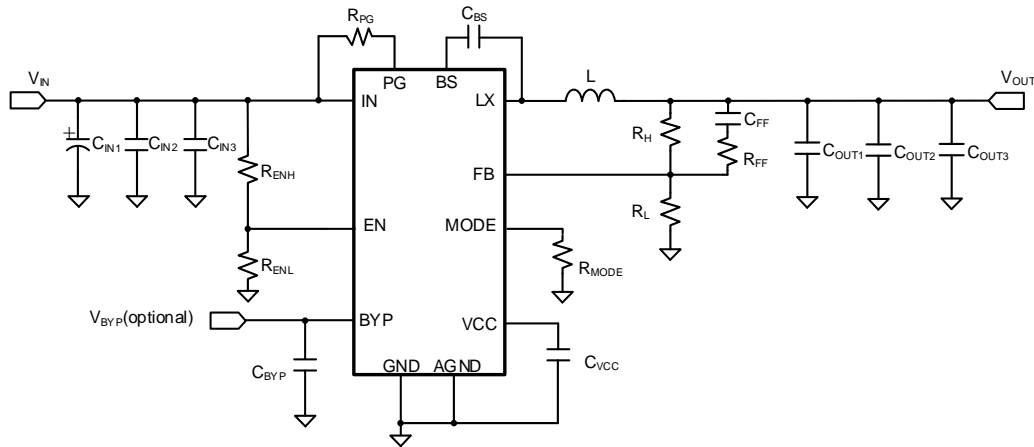


Figure 18. Recommended Schematic Diagram ($V_{OUT} = 5V$)

Designator	Description	Part Number	Manufacturer
C _{IN1}	47 μ F/50V, Electrolytic Capacitor		
C _{IN2}	10 μ F/50V/X5R, 1206	GRM31CR61H106KA12L	m μ Rata
C _{IN3} , C _{BS}	0.1 μ F/50V/X5R, 0603	GRM188R61H104KA93D	m μ Rata
C _{OUT1} , C _{OUT2} , C _{OUT3}	22 μ F/16V/X5R, 1206	GRM31CR61C226ME15L	m μ Rata
C _{VCC}	2.2 μ F/16V/X5R, 0603	GRM188R61C225KE15D	m μ Rata
C _{BYP}	1.0 μ F/25V/X5R, 0603	GRM155R61E105KE11D	m μ Rata
C _{FF}	470pF/50V/C0G, 0603	GRM1885C1H471JA01D	m μ Rata
L	2.2 μ H/12A, inductor	PCMB104T-2R2MS	CYNTEC
R _{ENH}	10k Ω , 1%, 0603		
R _{ENL}	1M Ω , 1%, 0603		
R _H , R _{PG}	100k Ω , 1%, 0603		
R _L	13.7k Ω , 1%, 0603		
R _{FF}	1k Ω , 1%, 0603		
R _{MODE}	240k Ω , 1%, 0603		

Table 4. Recommended BOM List ($V_{OUT} = 5V$)

$V_{OUT} = 12V$

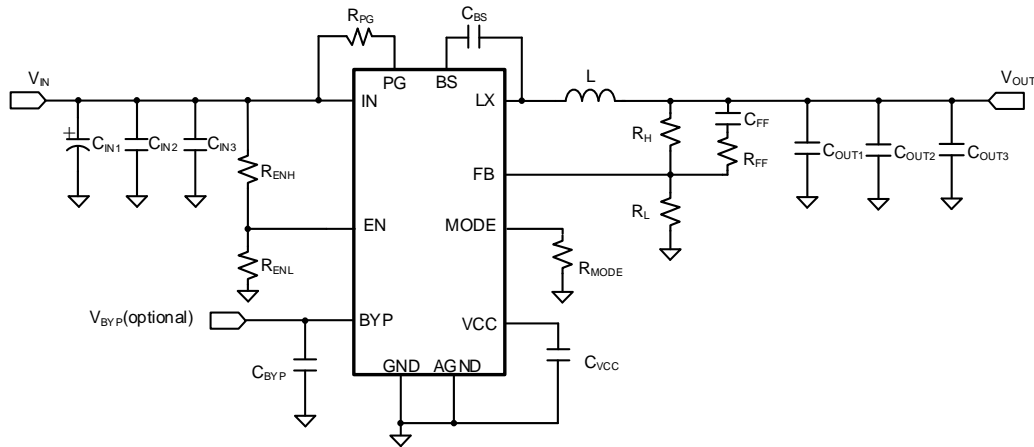


Figure19. Recommended Schematic Diagram ($V_{OUT} = 12V$)

Designator	Description	Part Number	Manufacturer
CIN1	47 μ F/50V, Electrolytic Capacitor		
CIN2	10 μ F/50V/X5R, 1206	GRM31CR61H106KA12L	m μ Rata
CIN3, CBS	0.1 μ F/50V/X5R, 0603	GRM188R61H104KA93D	m μ Rata
COUT1, COUT2, COUT3	22 μ F/25V/X5R, 1206	GRM31CR61E226ME15K	m μ Rata
CVCC	2.2 μ F/16V/X5R, 0603	GRM188R61C225KE15D	m μ Rata
CBYP	1.0 μ F/25V/X5R, 0603	GRM155R61E105KE11D	m μ Rata
CFF	680pF/50V/C0G, 0603	GRM1885C1H681JA01D	m μ Rata
L	4.7 μ H/8.5A, inductor	PCMB104T-4R7MS	CYNTEC
RENH	10k Ω , 1%, 0603		
RENL	1M Ω , 1%, 0603		
RH, RPG	100k Ω , 1%, 0603		
RL	5.23k Ω , 1%, 0603		
RFF	1k Ω , 1%, 0603		
RMODE	240k Ω , 1%, 0603		

Table5. Recommended BOM List ($V_{OUT} = 12V$)

Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation.

Input Capacitors: Place the input capacitor close to IN and GND pins, minimizing the loop formed by these connections. The capacitor should be connected to the IN and GND using a wide copper pour. A 0.1μF input ceramic capacitor is recommended to reduce the high-frequency noise.

Output Capacitors: Ensure that the C_{OUT} negative sides are connected to GND using wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.

VCC Capacitor: Place the VCC capacitor close to VCC pin using a short, direct copper trace to the nearest AGND pin (pin 6). Make one Kelvin connection between AGND and GND at the C_{VCC} negative side by multiple vias.

BYP Capacitor: Place the BYP capacitor close to BYP using short, direct copper trace to one nearest AGND pin (pin 6) if bypass function is used. It is recommended to make one good RC filter for BYP input if the 3.3V external power ripple is large.

Feedback Network: Place the feedback components (R_H, R_L, R_{FF} and C_{FF}) as close to FB pin as possible. Avoid routing the feedback line near LX, BS or other high frequency signal as it is noise sensitive. Use a Kelvin

connection for the feedback sampling point at C_{OUT} rather than the inductor output terminal.

LX Connection: Keep LX area small to prevent excessive EMI, while using a wide copper trace to minimize parasitic resistance and inductance.

BS Capacitor: Place the BS capacitor on the same layer as the device, keep the BS voltage path (BS, LX and C_{BS}) as short as possible.

EN Signal: It is not recommended to connect EN pin directly to V_{IN} or another voltage source. A resistor in a range of 1kΩ to 1MΩ should be used if EN pin is pulled high.

GND Vias: Place an adequate number of vias on the GND layer around the device for better thermal performance. The exposed GND pad should be connected to a copper area larger than its size. Place multiple GND vias on it for heat dissipation.

PCB Board: A four-layer layout with 2-oz copper is strongly recommended to achieve better thermal performance. The top layer and bottom layer should place power IN and GND copper area as wide as possible. Middle1 layer should be used as a GND layer for conducting heat and shielding the middle2 layer signal lines from top layer crosstalk. Place signal lines on middle2 layer instead of the other layers, so that the other layers' GND plane is not cut by signal lines.

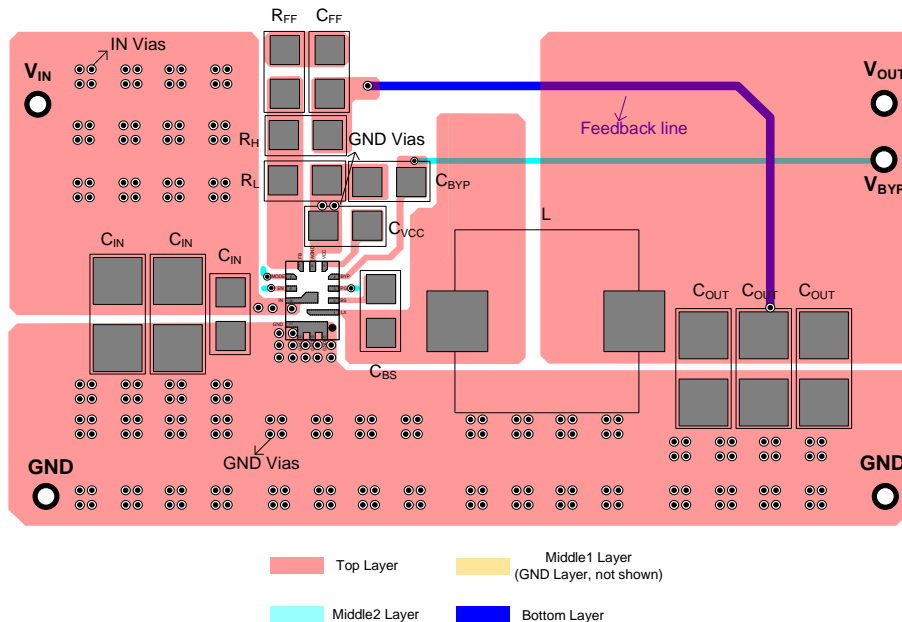
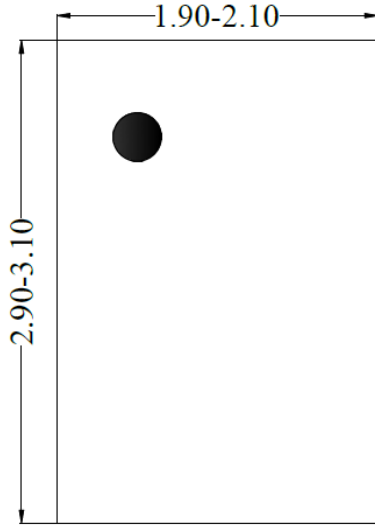
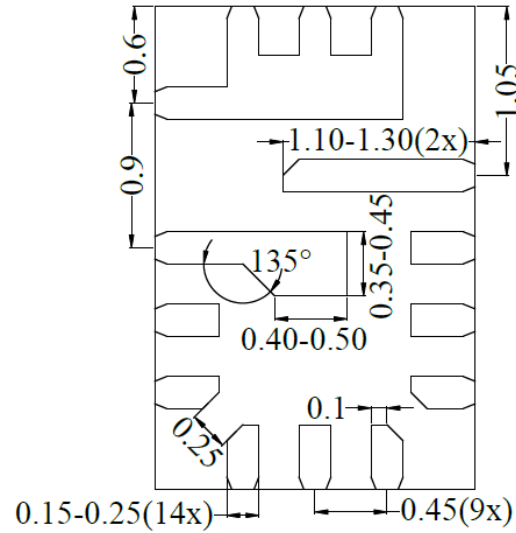


Figure20. PCB Layout Suggestion

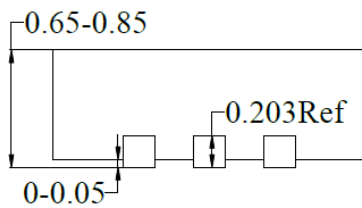
QFN2x3-14 Package Outline Drawing



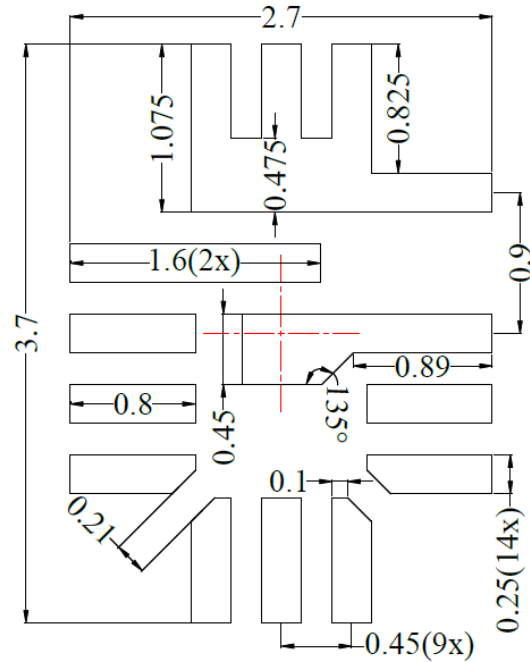
Top View



Bottom view



Front View

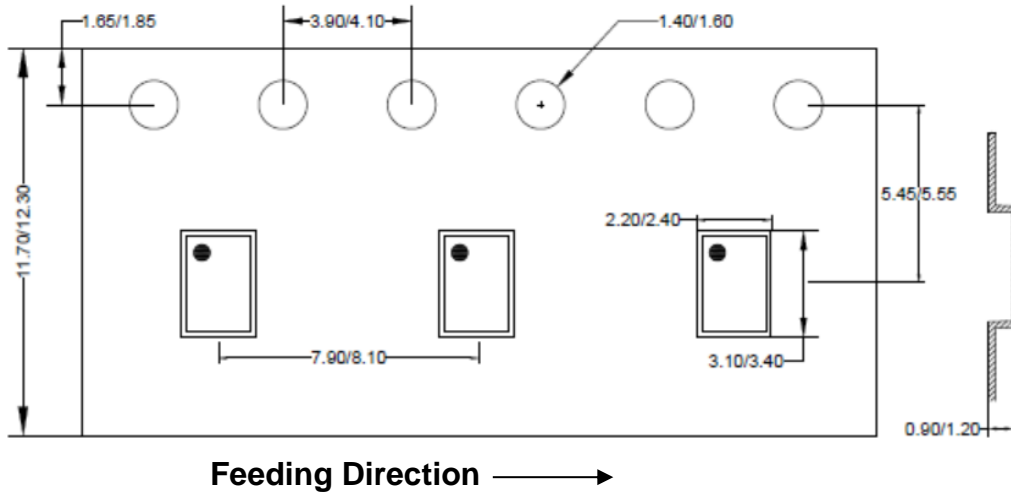


**Recommended PCB layout
(Reference only)**

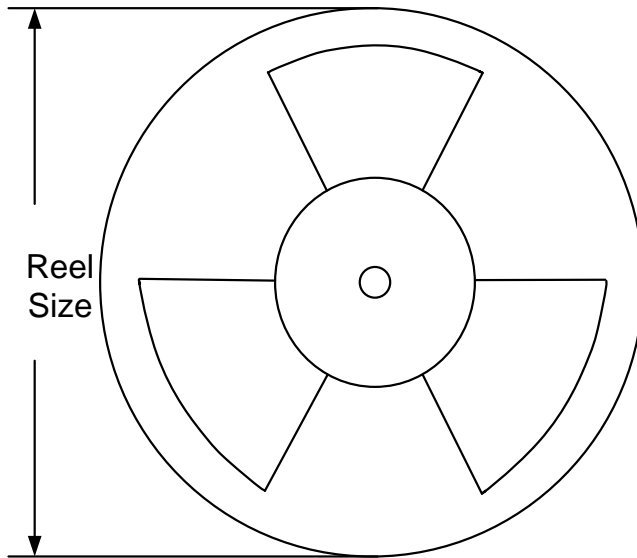
Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

1. Taping Orientation
QFN2x3-14



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel
						(pcs)
QFN2x3-14	12	8	13	400	400	5000



Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
Sep.28, 2025	1.0	Initial Release	-



IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.
2. **Applications.** Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.
3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.
4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.
5. **Terms and conditions of commercial sale.** Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at <http://www.silergy.com/stdterms>, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.
6. **No offer to sell or license.** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com

© 2025 Silergy Corp.

All Rights Reserved.