

General Description

The SY6813C is an ultra-low $R_{DS(ON)}$ load switch. The controlled ramp up speed avoids the inrush current during turn on. The device works under a wide input voltage range from 1.2V to 5.5V.

Ordering Information

SY6813□(□□□)

Package Code

Optional Spec Code

Ordering Number	Package type	Note
SY6813CPES	CSP1.5×1-6	----

Features

- 1.2V to 5.5V Input Voltage Range with 6V Absolute Maximum Rating
- Low $R_{DS(ON)}$ for Internal Pass Switch: 22mΩ at $V_{IN}=5V$
- 3A Continuous Load Current Capability
- ON/OFF Control Input
- Controlled Turn on Delay and Slew Rate: $t_R=550\mu s$ at $V_{IN}=3.6V$
- Quick Output Discharge
- RoHS Compliant and Halogen Free
- Ultra-Small CSP-6 Package 1.5mm×1.0mm, 0.5mm Pitch, 0.5mm Height

Applications

- Smart Phone
- MID
- E-Book
- Storage, DSLR, and Portable Device

Typical Applications

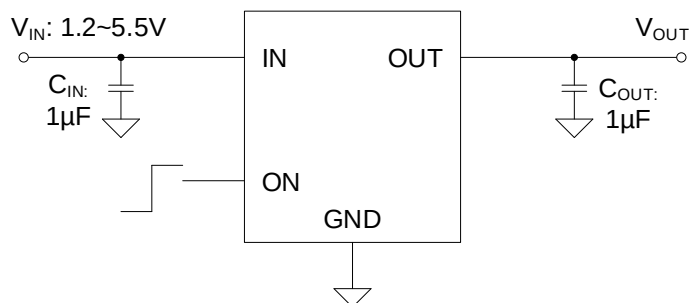


Figure 1. Schematic Diagram

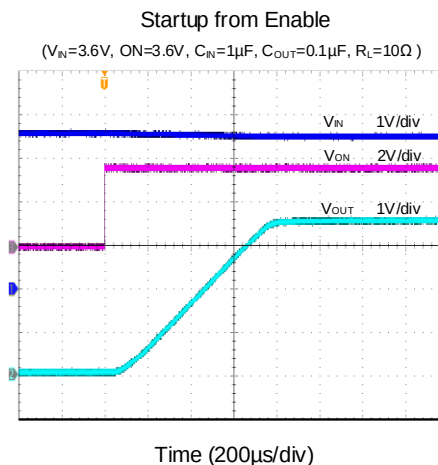
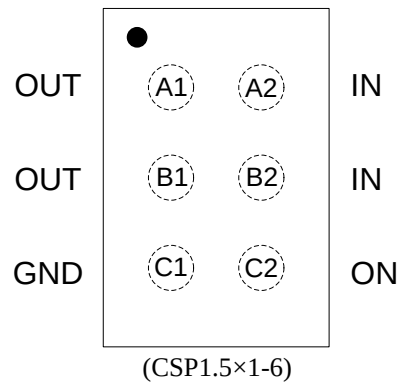


Figure 2. Startup Figure

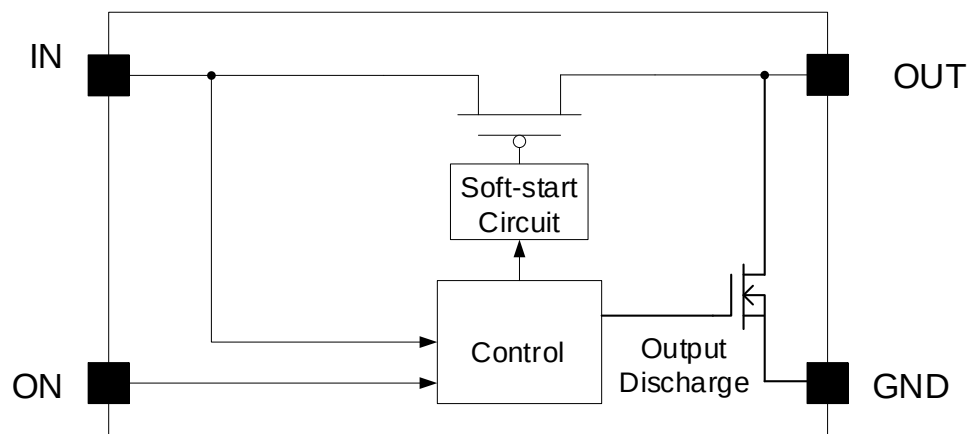
Pinout (Top view)



Top Mark: d5xyz (Device code: d5, x=*year code*, y=*week code*, z= *lot number code*)

Pin Name	Pin Number	Pin Description
IN	A2, B2	Input pin.
OUT	A1, B1	Output pin.
GND	C1	Ground pin.
ON	C2	ON/OFF control. Active high. Do not leave it floating.

Block Diagram



Absolute Maximum Ratings (Note 1)

All Pins	6V
Power Dissipation, P_D @ $T_A = 25^\circ\text{C}$	1.0W
Package Thermal Resistance (Note 2)	
θ_{JA}	123°C/W
θ_{JC}	17°C/W
Junction Temperature Range	-40°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	-65°C to 150°C
ESD Susceptibility (Note 2)	
HBM (Human Body Mode)	8kV
CDM (Charged Device Mode)	1.5kV

Recommended Operating Conditions (Note 3)

IN, OUT	1.2V to 5.5V
ON	-0.3V to $V_{IN}+0.3V$
Junction Temperature Range	-40°C to 125°C
Ambient Temperature Range	-40°C to 85°C

Electrical Characteristics

($V_{IN} = 5.0V$, $T_A = 25^\circ\text{C}$, unless otherwise specified.)

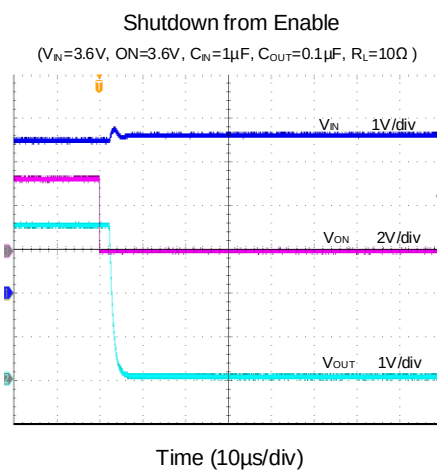
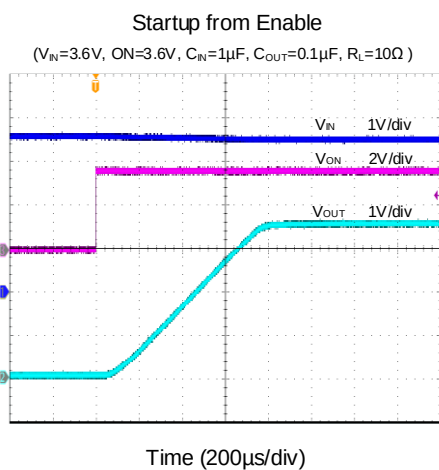
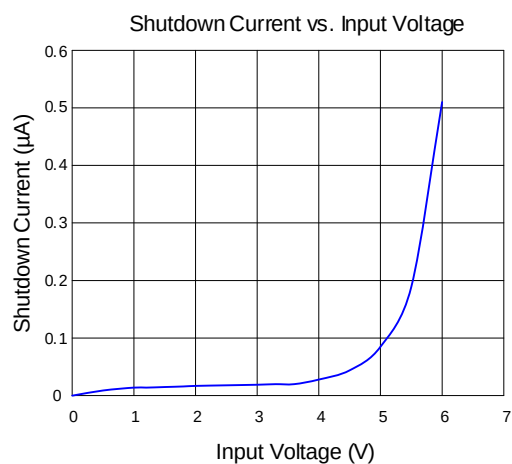
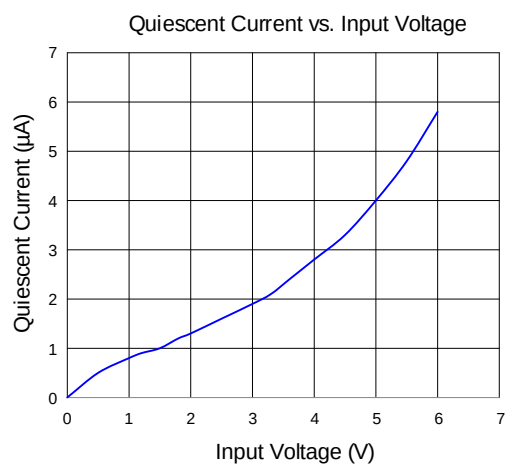
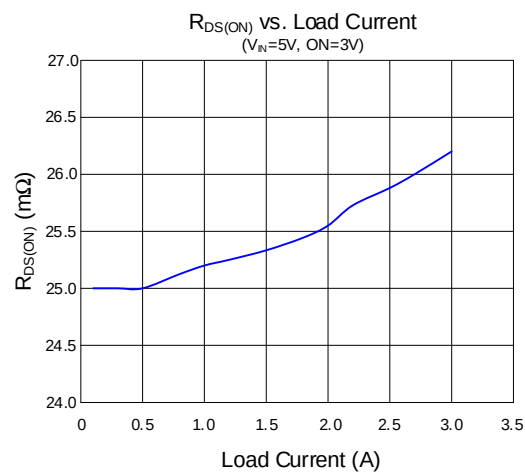
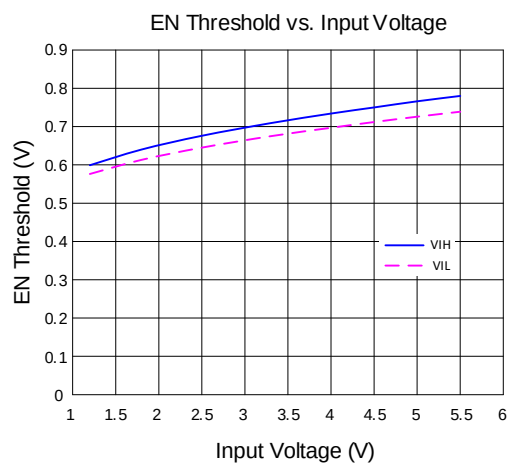
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		1.2		5.5	V
Shutdown Current	I_{SHDN}	ON=Low, $V_{OUT}=\text{GND}$			1	μA
Quiescent Current	I_Q	$I_{OUT}=0$		4	8	μA
FET R_{ON}	$R_{DS(ON)}$			22	30	$\text{m}\Omega$
ON Input Logic High	V_{IH}		1			V
ON Input Logic Low	V_{IL}				0.4	V
Turn On Rise Time	t_r	$V_{IN}=V_{ON}=3.6V$, $R_L=10\Omega$, $C_{IN}=1\mu\text{F}$, $C_L=0.1\mu\text{F}$, $T_A=25^\circ\text{C}$		550		μs
		$V_{IN}=1.8V$, $V_{ON}=3.6V$, $R_L=10\Omega$, $C_{IN}=1\mu\text{F}$, $C_L=0.1\mu\text{F}$, $T_A=25^\circ\text{C}$		280		μs
Output discharge resistor	R_{DSC}		35	50	70	Ω

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at $T_A=25^\circ\text{C}$ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics



Operation

The SY6813C develops an ultra-low $R_{DS(ON)}$ load switch. The controlled ramp up speed avoids the inrush current during turn on. The device works under a wide input voltage range from 1.2V to 5.5V.

Applications Information

Input Capacitor

To reduce device inrush current, a $1\mu F$ ceramic capacitor, C_{IN} , is recommended. A higher value of C_{IN} can be used to reduce the voltage drop experienced as the switch is turned on into large capacitive load. To minimize the potential noise problem, place C_{IN} really close to the IN and GND pins.

Output Capacitor

A $1\mu F$ ceramic output cap is recommended to prevent parasitic board inductance from forcing V_{OUT} below GND when switching off.

Output Discharge

The SY6813C integrates a 50Ω pull-down resistor for quick output discharge. The resistor is activated when the switch is turned off.

PCB Layout Guide

For best performance of the SY6813C, the following guidelines must be strictly followed:

- Keep all power traces as short and wide as possible and use at least 2-ounce copper for all power traces.
- Place a ground plane under all circuitry to lower both resistance and inductance and improve DC and transient performance.
- Locate the output capacitors as close to the connectors as possible to lower the impedance (mainly inductance) between the port and the capacitor and improve transient performance.
- Input and output capacitors should be placed close to the IC and connected to the ground plane to reduce noise coupling.

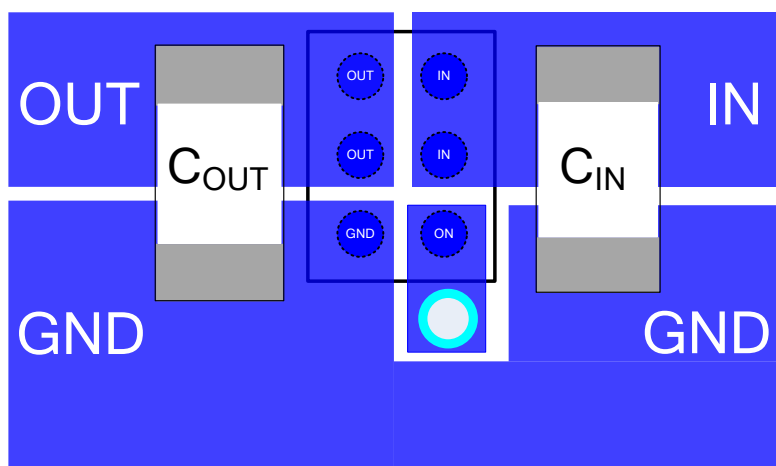
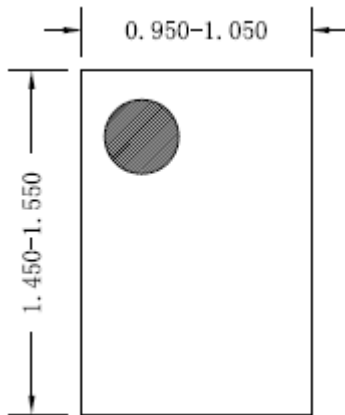
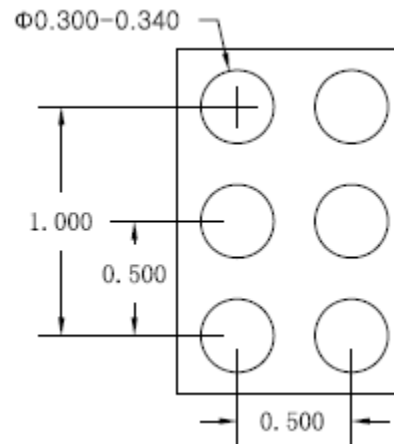


Figure3. PCB Layout Suggestion

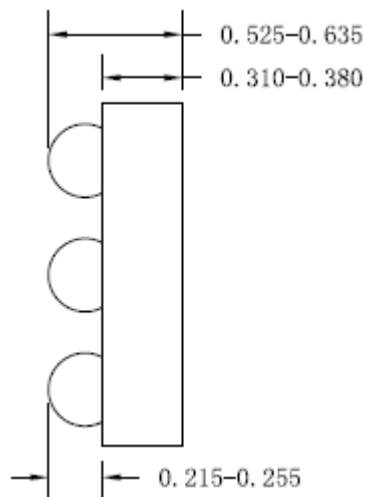
CSP1.5×1 -6 Outline Drawing



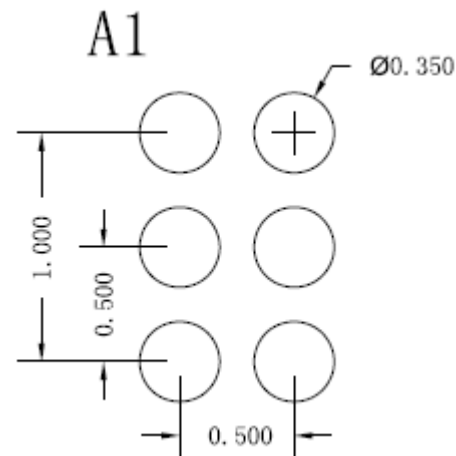
Top View



Bottom View



Side View

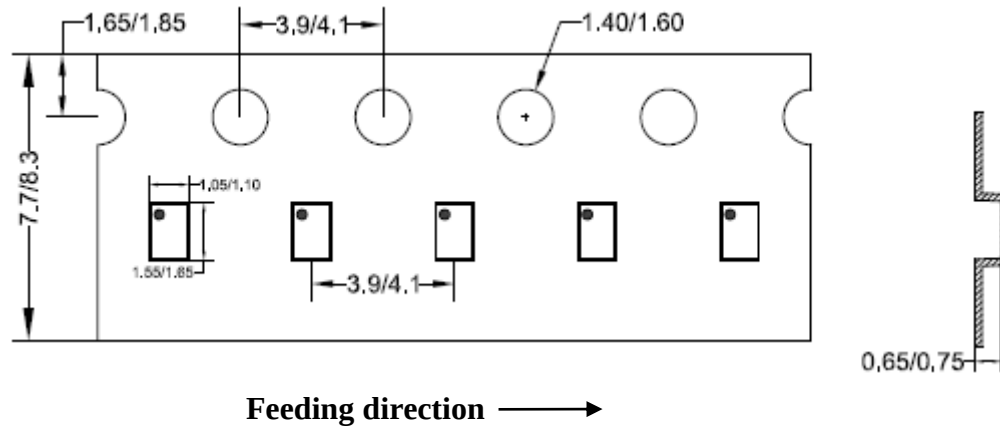


**Recommended PCB layout
(Reference Only)**

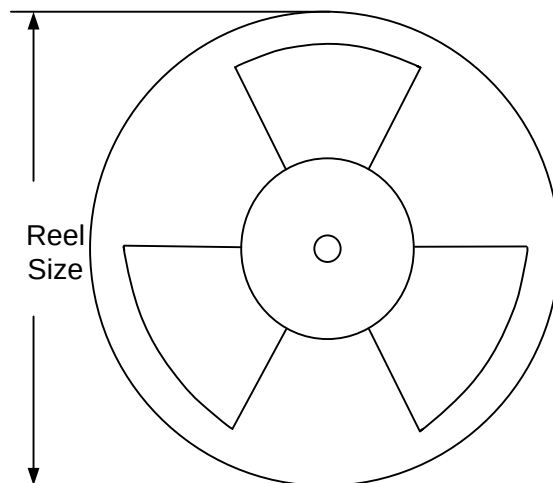
Notes: All dimension in millimeter and exclude mold flash & metal burr

Taping & Reel Specification

1. CSP1.5×1 taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
CSP1.5×1.0	8	4	7"	400	400	3000

3. Others: NA



SY6813C

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Jan.07, 2023	Revision 1.0	Production Release
Jan.07, 2022	Revision 0.9	Initial Release



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