SQ76030A/A1

High-Efficiency 5.5V Input 25A step-down Module Power Module with Integrated Inductor

General Description

The SQ76030A/A1 is PMBus 1.3 compliant. The SQ76030A/A1 is a high efficiency synchronous step-down DC/DC module capable of delivering up to 25A current. The device integrates main switch and synchronous switch with very low $R_{DS\ (ON)}$ to minimize the conduction loss, as well as inductor to minimize package size. It provides accurate regulation for a variety of loads with an accurate voltage reference over T_J= -40°C to 125°C.

The DC/DC regulator adopts COT architecture to achieve fast transient responses for high step-down applications.

Applications

- Optical Module
- PDAs and Pocket PCs
- FPGA System
- General POL

Features

- Input Voltage Range: 2.9V to 5.5V
- Output Voltage Range: 0.35V to 1.25V
- PMBus 1.3 Compliant
- 25A Continuous Output Current
- Switching Frequency of 400kHz / 600kHz / 800kHz / 1MHz
- Differential Remote Sensing
- Startup with Pre-biased Voltage
- Cycle-by-cycle Valley, Peak and Negative Current Limit
- Hiccup Mode Short-Circuit Protection
- Auto Recovery Mode for Output Over-voltage protection (OVP) and Over Temperature Protection (OTP)
- Power Good Indicator
- Compact package: MLGA5.1x6-48 (Height=2.3mm max)

Typical Application

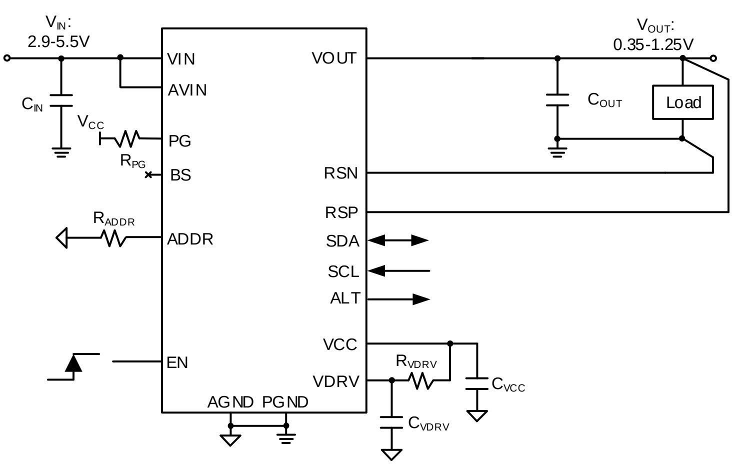


Figure 1: Application circuit

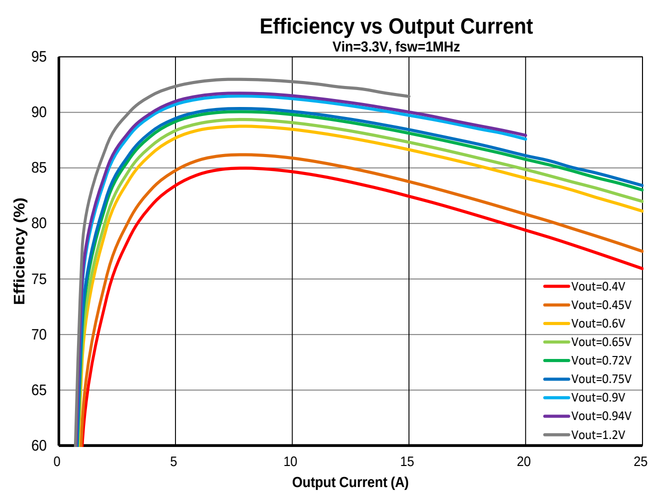


Figure 2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Register OPERATION (01h) default value	Register VOUT_COMMAND(21h) default value	Top Mark
SQ76030AALG	0x00 (Software EN off)	0x00E6 (V_{OUT}=0.45V)	**LRJxyz**
SQ76030A1ALG	0x80 (Software EN on)	0x01D8 (V_{OUT}=0.92V)	**MEBxyz**

SQ76030AALG:Device code :LRJ; x=year code;y=week code;z=lot number code

SQ76030A1ALG:Device code: MEB; x=year code;y=week code;z=lot number code

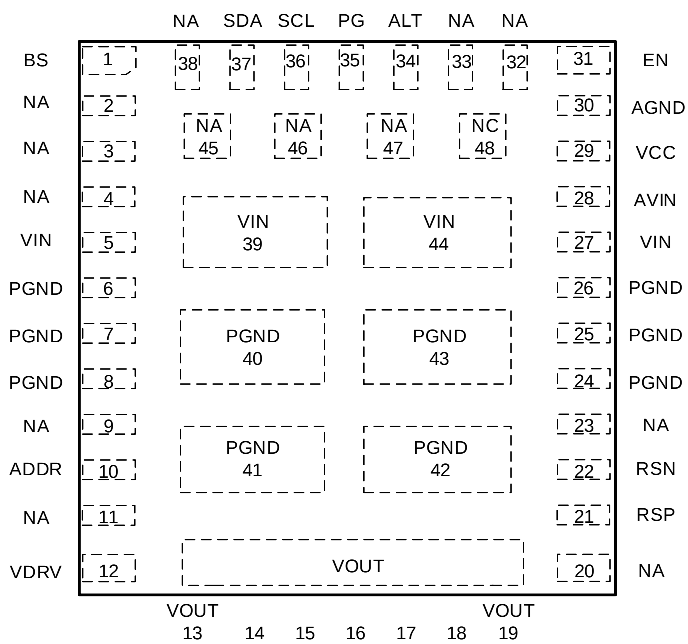
QR Code Information

AAAAAAAAAAAAMMMMMM

AAAAAAAAAAAA: assembly lot

MMMMMM: manufacturing information

Pinout (top view)



Pin No	Pin Name	Pin Description
1	BS	Boot-strap pin.
5,27,39,44	VIN	Input pins.
6-8,24-26,	PGND	Power Ground pins.

40-43		
10	ADDR	PMBus address configure pin. Please refer to Table 3 to choose RADDR for corresponding PMBus address.
12	VDRV	Decoupling input pin for 3.3V driver power supply. Decouple VDRV with a minimum 1uF ceramic capacitor as close to VDRV as possible. VDRV accepts an external 3.3V bias. If no external 3.3V bias is provided, connect VDRV to VCC through a 1Ω resistor.
13-19	VOUT	Output pins.
21	RSP	The positive input of the remote sense amplifier.
22	RSN	The negative input of the remote sense amplifier.
28	AVIN	Analog input. Connect this pin to VIN.
29	VCC	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuit.
30	AGND	Analog ground, should be electrically connected to PGND close to the device.
31	EN	Enable pin. Pull this pin low to shut down the device, or pull this pin high to enable the device. Do not leave this pin floating.
34	ALT	PMBus ALERT pin.
35	PG	Power good output. The output of PG is an open-drain signal.
36	SCL	PMBus CLK pin.
37	SDA	PMBus DATA pin.
2-4,9,11,20, 23,32-33,38, 45-47	NA	These pins have no internal electrical connection.
48	NC	Not connected. Keep this pin floating.

Block Diagram

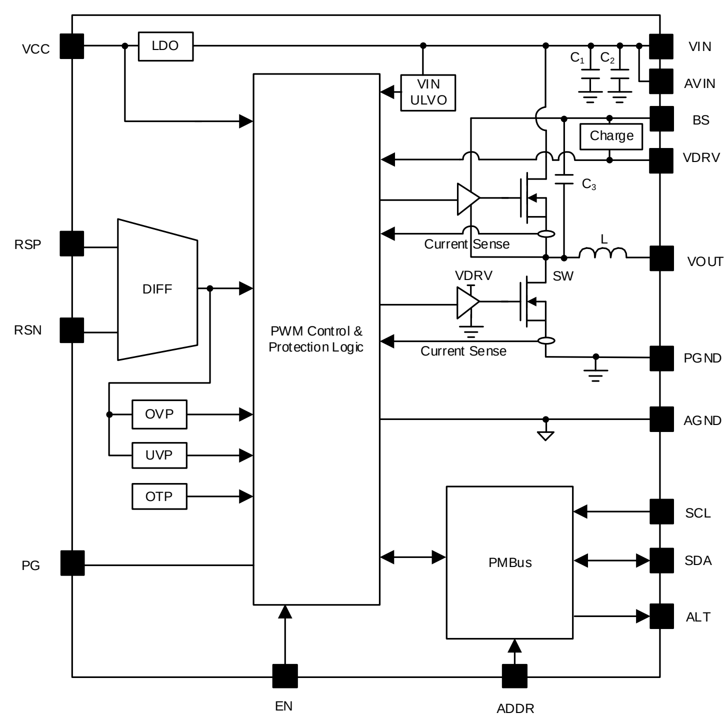


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VIN, AVIN	-0.3	6	V
BS-SW, VCC, VDRV, ADDR, PG	-0.3	4	
EN, SCL, SDA, ALT	-0.3	V_{IN}+0.3	
RSN	-0.3	3.3	
RSP	-0.3	6	
Operation Internal Temperature	-40	150	°C
Lead Temperature (Soldering, 10sec.)		260	
Storage Temperature	-55	150	
ESD Rating HBM(Human Body Model)		2000	V
CDM(Charged Device Model)		500	V

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	11.68	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	0.03	
Ψ_{JB} Junction-to-Board Thermal Resistance	3.88	
P_D Power Dissipation T_A = 25°C	8.56	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Input Voltage	2.9	5.5	V
Output Voltage	0.35	1.25	
Output Current (Note5)	0	25	A
VCC,VDRV	2.8	3.6	V
Internal Die Temperature	-40	125	°C

Electrical Characteristics

(V_{IN} = 3.3V, -40°C < T_J < 125°C, typical values are at T_J = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage Range	V_{IN}		2.9		5.5	V
Input UVLO Rising Threshold	$V_{UVLO\_RISING\_F}$	VCC floating	2.7	2.8	2.9	V
Input UVLO Falling Threshold	$V_{UVLO\_FALLING\_F}$	VCC floating	2.45	2.7	2.85	V
Supply Current (Quiescent)	I_q	EN =0V		2.5	4.0	mA
EN						
EN Input Voltage High	V_{ENH}		1.35			V
EN Input Voltage Low	V_{ENL}				0.4	V
Output						
Feedback Reference Accuracy	V_{FB}	V_{RSN}=0V, 350mV≤V_{RSP}<600mV			±2	%
		V_{RSN}=0V, 600mV≤V_{RSP}≤1250mV			±1	%
OUT step size	V_{STEP}			1.95		mV
Switching frequency	f_{SW}	D2h[2:1]=11	900	1000	1100	kHz
Load regulation(Note4)	ΔV_{LNR}	V_{IN}=3.3V, V_{OUT}=0.6V, T_A=25°C, I_{OUT}=0-25A			±1	%
Line regulation(Note4)	ΔV_{LTR}	V_{IN}=2.9-5.5V, V_{OUT}=0.6V, T_A=25°C, I_{OUT}=12.5A			±1	%
Temperature regulation(Note4)	ΔV_{TR}	V_{IN} =3.3V, V_{OUT}=0.6V T_A=-40°C to 85°C, I_{OUT} =12.5A			±1	%
Power Good						
PG Sink Current Capability	V_{PG}	I_{PG}=10mA			0.3	V
PG Leakage Current	I_{PG_LKG}	V_{PG}=3.3V		3	5	µA
PG High Threshold	$V_{PG\_H\_RISING}$	V_{RSP} rising, PG from low to high	85	90	94	%VREF
	$V_{PG\_H\_FALLING}$	V_{RSP} falling, PG from low to high	100.5	105	109	
PG Low Threshold	$V_{PG\_L\_FALLING}$	V_{RSP} falling, PG from high to low	70.5	75	78	
	$V_{PG\_L\_RISING}$	V_{RSP} rising, PG from high to low	111	115	118	
Protection						
Default Output OVP Threshold	$V_{OVP\_DEFAULT}$		111	115	118	%VREF
Default Output UVP Threshold	$V_{UVP\_DEFAULT}$		70.5	75	78	%VREF
Over Temperature Fault Limit (Note 4)	T_{OT_FAULT}			145		°C
Over Temperature Fault Hysteresis (Note 4)	T_{OT_HYS}			20		°C
Power Switch						
Min On Time(Note4)	T_{ON_MIN}	V_{IN} =3.3V		100	135	ns
Min Off Time(Note4)	T_{OFF_MIN}			250	280	ns
Soft Start						
Soft Start Time	t_{SS}	from 10% to 90% V_{OUT}		2	3	ms
Turn-on Delay Time (Note 4)	t_{ON_DELAY}			0.4	0.5	ms
PMBus Interface (ALT, SDA, SCL) (Note 4)						
Input High Voltage	V_{PMB_IH}	SCL, SDA	1.35			V

Input Low Voltage	V_{PMB_IL}	SCL, SDA			0.8	V
Input Leakage Current	$I_{PMB\_IH,}$	SCL, SDA, ALT	-10		10	μA
Output Low Voltage	V_{PMB_OL}	Sink 4mA			0.4	V
PMBus Operation Frequency Range	f_{PMB}		10		400	kHz
PMBus Free Time between Stop and Start	t_{BUF}		1300			ns
Repeated Start Condition Hold Time	t_{HD_STA}		600			ns
Repeated Start Condition Set-up Tme	t_{SU_STA}		600			ns
Stop Condition Set-up Time	t_{SU_STO}		600			ns
Data Hold Time	t_{HD_DAT}		0			ns
Data Set-up Time	t_{SU_DAT}		100			ns
Clock Low Timeout	$t_{TIMEOUT}$		25		35	ms
Clock Low Period	t_{LOW}		1300			ns
Clock High Period	t_{HIGH}		600			ns
Clock/Data Falling Time	t_F	100kHz Class			300	ns
		400kHz Class			300	ns
Clock/Data Rising Time	t_R	100kHz Class			1000	ns
		400kHz Class			300	ns

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} ,Ψ_{JB} and θ_{JC} are based on a four-layer 8cm×8cm Silergy Evaluation Board in the natural convection at T_A = 25°C. Board thickness: 1.6mm, copper thickness: 2 oz, copper coverage: 95%. Junction temperature (T_J) refers to the die temperature. Ambient temperature (T_A) refers to the air temperature 0.5 inch above the module. Board temperature (T_B) refers to the PCB Temperature 1mm away from the hottest module pin on the PCB top layer. The top case temperature (T_C) refers to the inductor top surface.

Note 3: The device is not guaranteed to function outside its operating conditions.

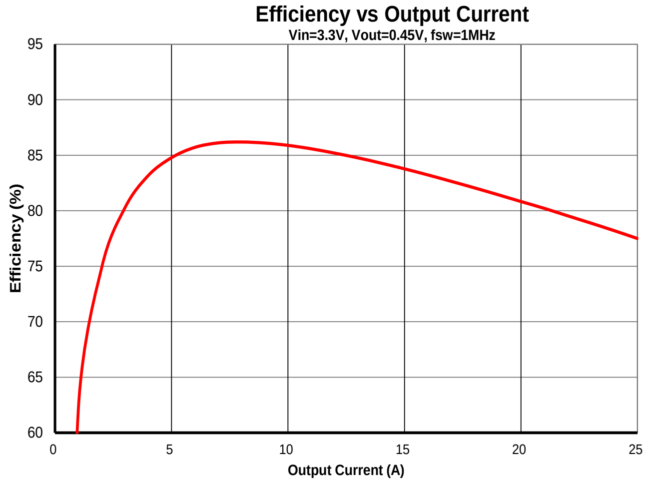
Note 4: The values are guaranteed by design, statistical correlation, not production tested.

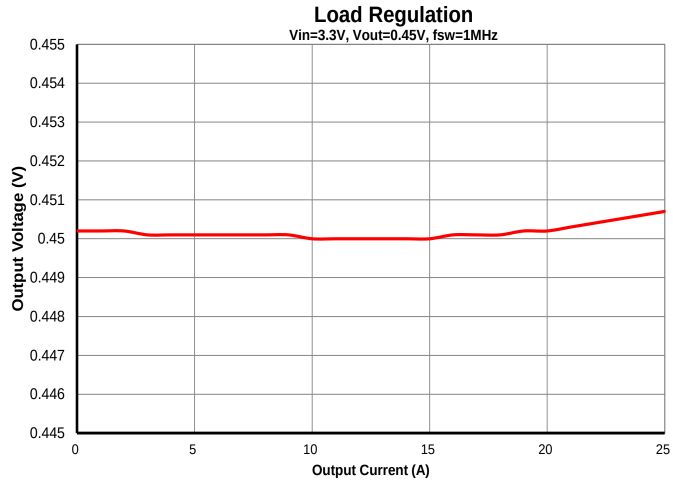
Note 5: Please refer to the Thermal Derating Curve to get the maximum output current under different ambient temperatures.

Typical Performance Characteristics

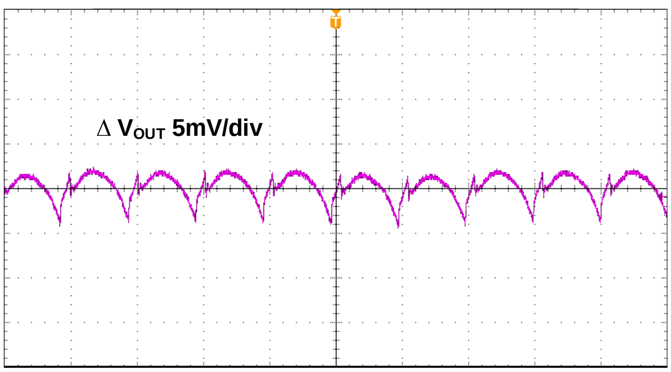
C_{OUT} = (2×47+2×22) μF, T_A = 25 ˚C, unless otherwise noted.

V_{OUT}=0.45V



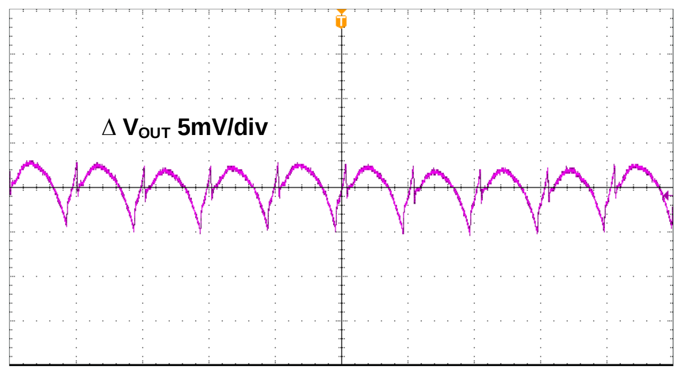


Output Ripple
(V_{IN}=3.3V,V_{OUT}=0.45V,I_O=0A)



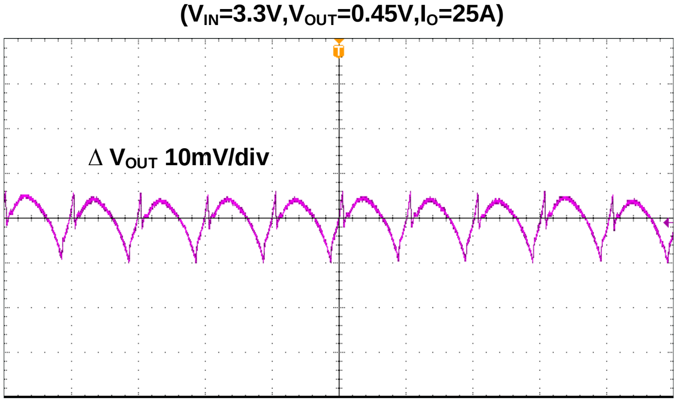
Time 1μs/div

Output Ripple
(V_{IN}=3.3V,V_{OUT}=0.45V,I_O=10A)



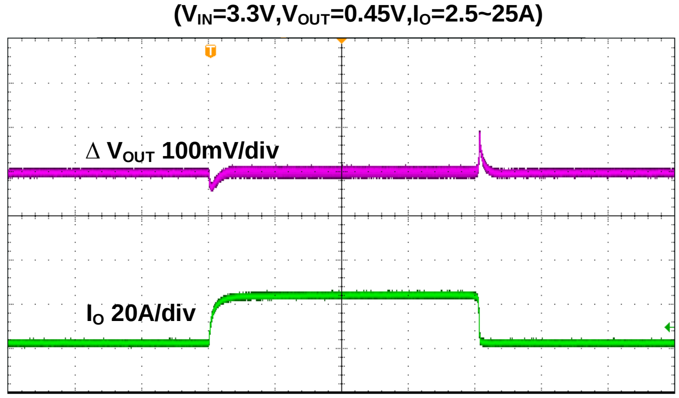
Time 1μs/div

Output Ripple
(V_{IN}=3.3V,V_{OUT}=0.45V,I_O=25A)



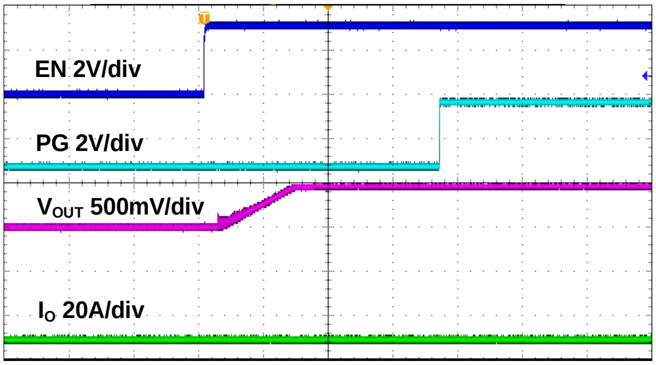
Time 1μs/div

Load Transient
(V_{IN}=3.3V,V_{OUT}=0.45V,I_O=2.5~25A)



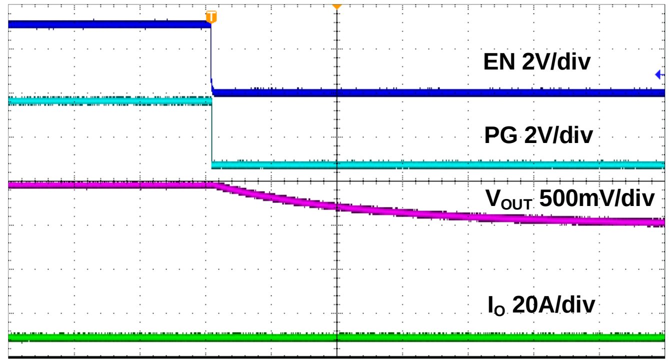
Time 400μs/div

Startup from EN
(V_{IN}=3.3V,V_{OUT}=0.45V,I_O=0A)



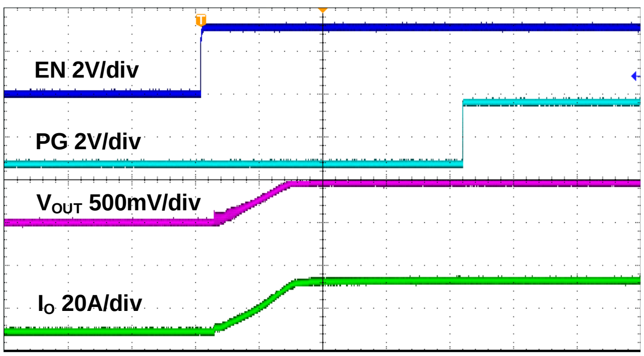
Time 2ms/div

Shutdown from EN
(V_{IN}=3.3V,V_{OUT}=0.45V,I_O=0A)



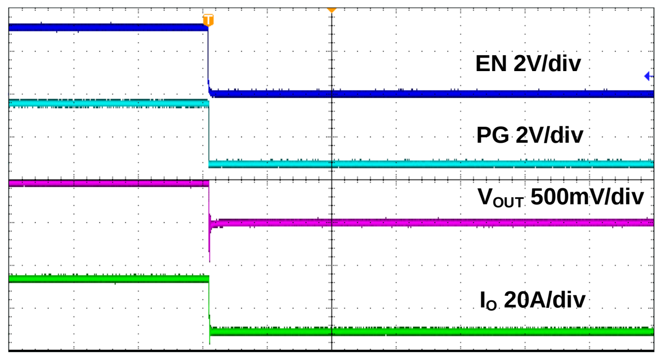
Time 2ms/div

Startup from EN
(V_{IN}=3.3V,V_{OUT}=0.45V,I_O=25A)



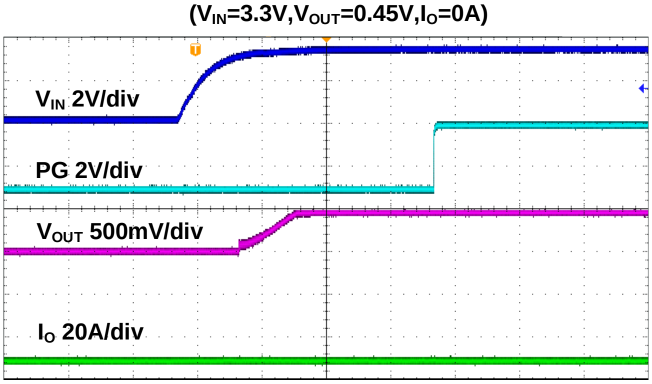
Time 2ms/div

Shutdown from EN
(V_{IN}=3.3V,V_{OUT}=0.45V,I_O=25A)



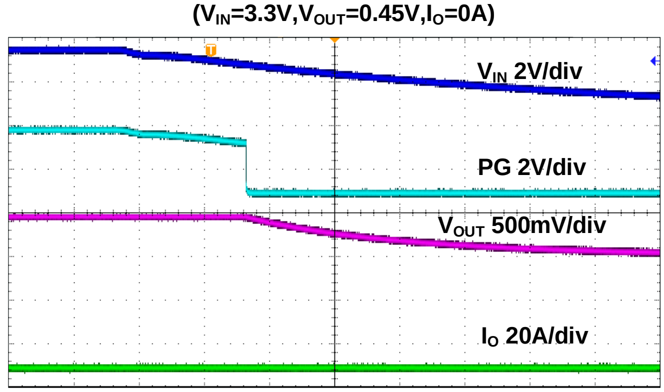
Time 2ms/div

Startup from V_{IN}
(V_{IN}=3.3V,V_{OUT}=0.45V,I_O=0A)



Time 2ms/div

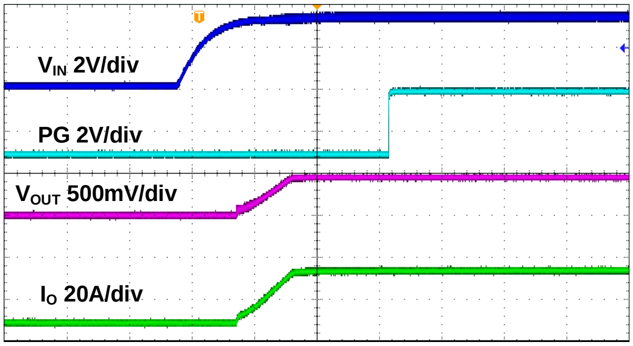
Shutdown from V_{IN}
(V_{IN}=3.3V,V_{OUT}=0.45V,I_O=0A)



Time 2ms/div

Startup from V_{IN}

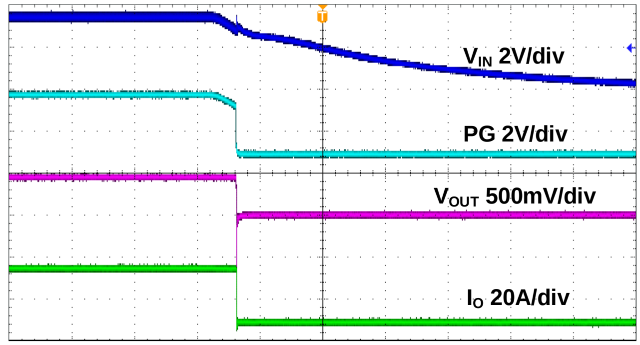
(V_{IN}=3.3V,V_{OUT}=0.45V,I_O=25A)



Time 2ms/div

Shutdown from V_{IN}

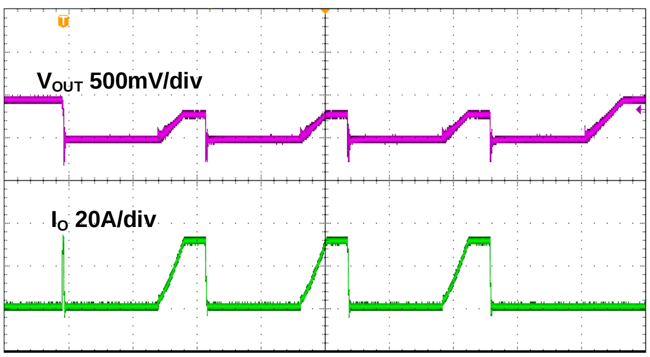
(V_{IN}=3.3V,V_{OUT}=0.45V,I_O=25A)



Time 2ms/div

Short Circuit Protection

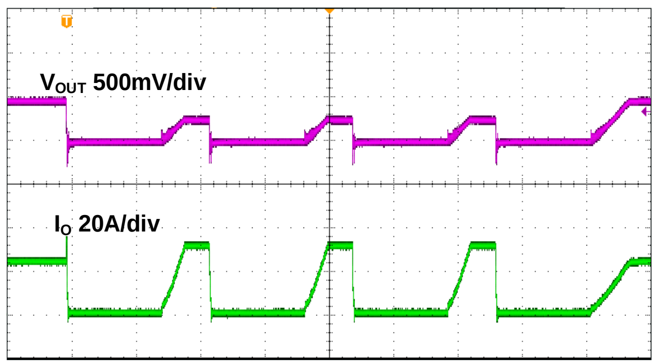
(V_{IN}=3.3V,V_{OUT}=0.45V,I_O=0A)



Time 4ms/div

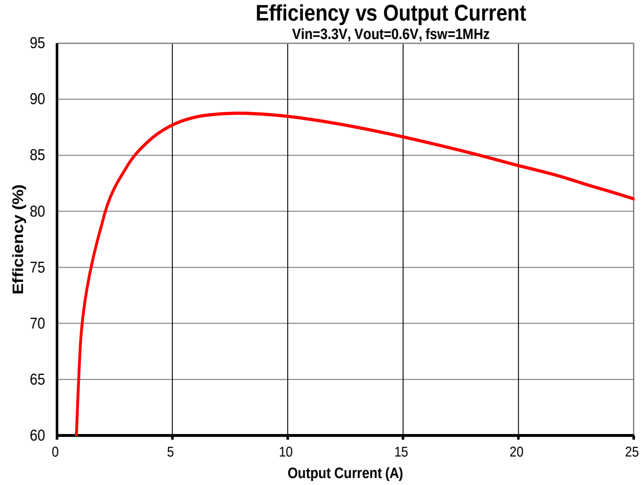
Short Circuit Protection

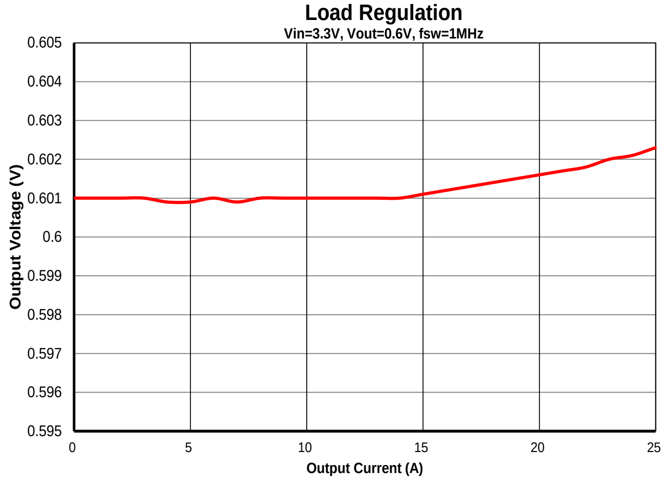
(V_{IN}=3.3V,V_{OUT}=0.45V,I_O=25A)



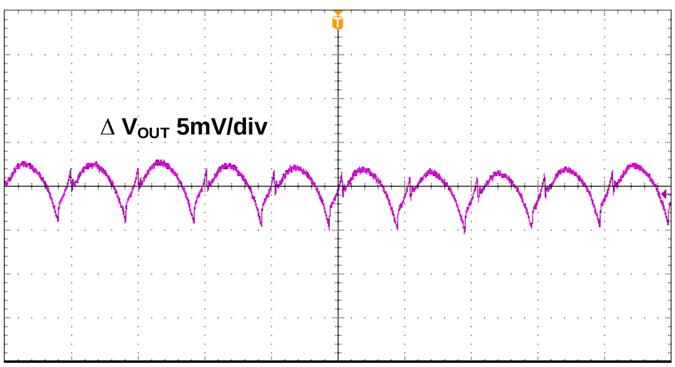
Time 4ms/div

V_{OUT}=0.6V



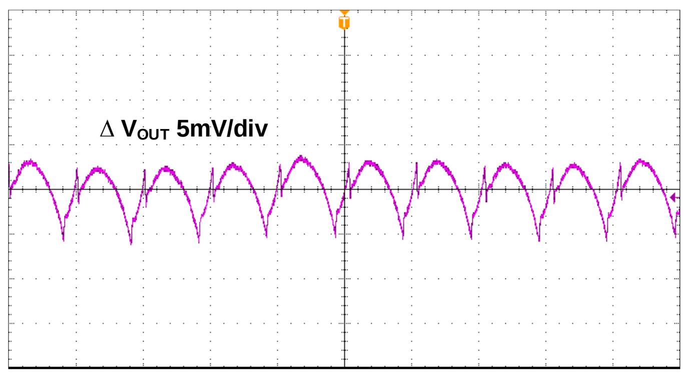


Output Ripple
(V_{IN}=3.3V,V_{OUT}=0.6V,I_O=0A)



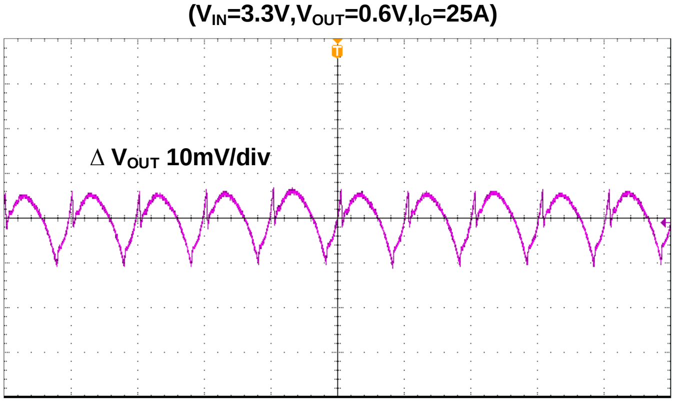
Time 1μs/div

Output Ripple
(V_{IN}=3.3V,V_{OUT}=0.6V,I_O=10A)



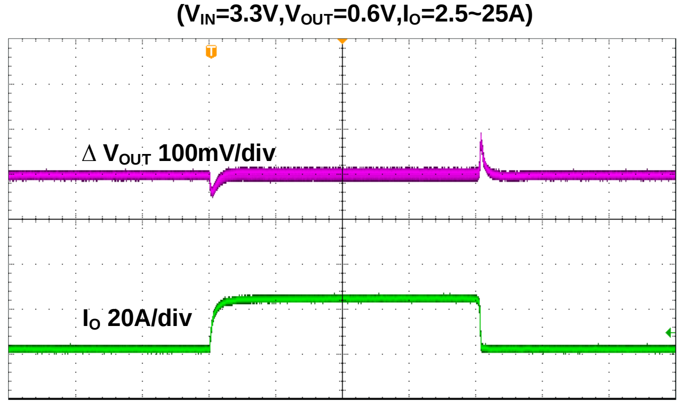
Time 1μs/div

Output Ripple
(V_{IN}=3.3V,V_{OUT}=0.6V,I_O=25A)



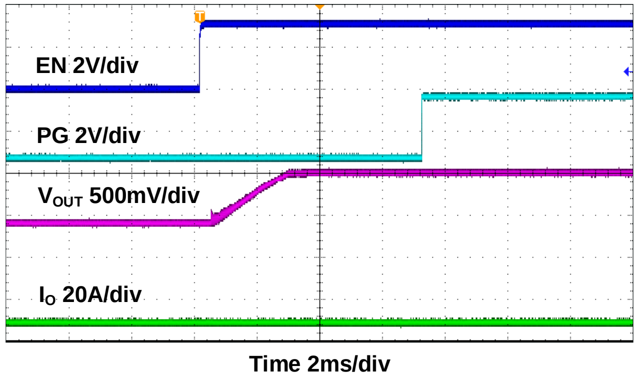
Time 1μs/div

Load Transient
(V_{IN}=3.3V,V_{OUT}=0.6V,I_O=2.5~25A)

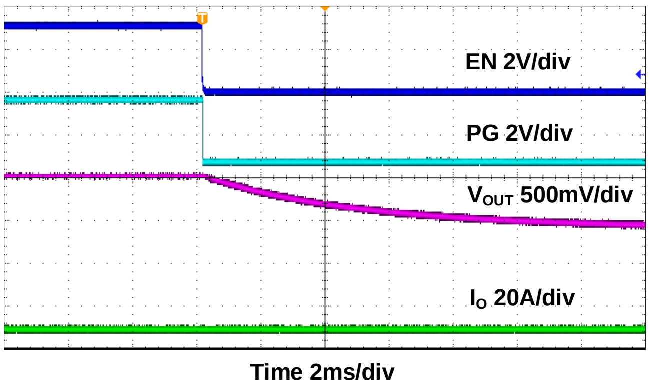


Time 400μs/div

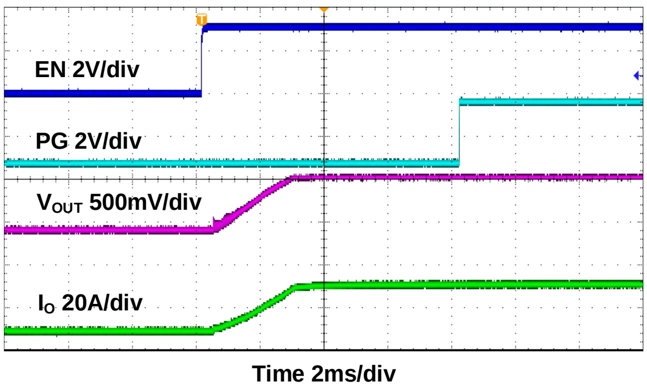
Startup from EN
(V_{IN}=3.3V,V_{OUT}=0.6V,I_O=0A)



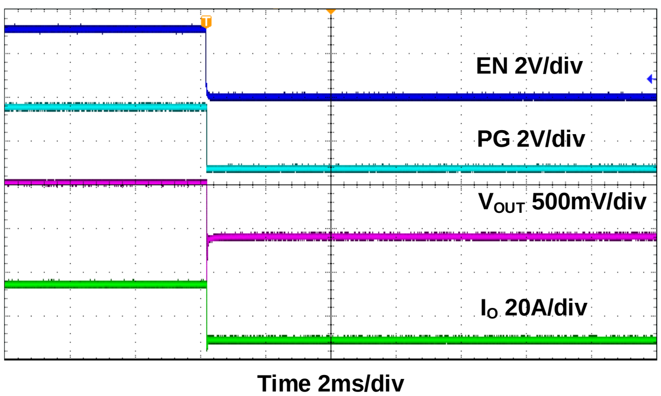
Shutdown from EN
(V_{IN}=3.3V,V_{OUT}=0.6V,I_O=0A)



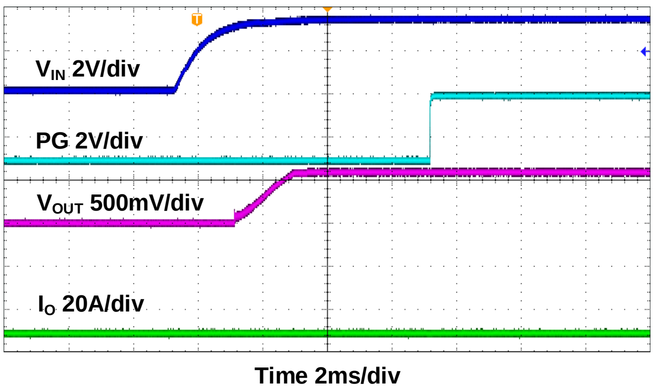
Startup from EN
(V_{IN}=3.3V,V_{OUT}=0.6V,I_O=25A)



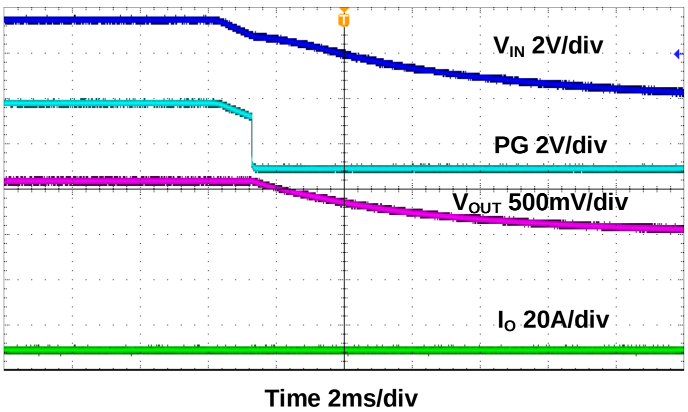
Shutdown from EN
(V_{IN}=3.3V,V_{OUT}=0.6V,I_O=25A)



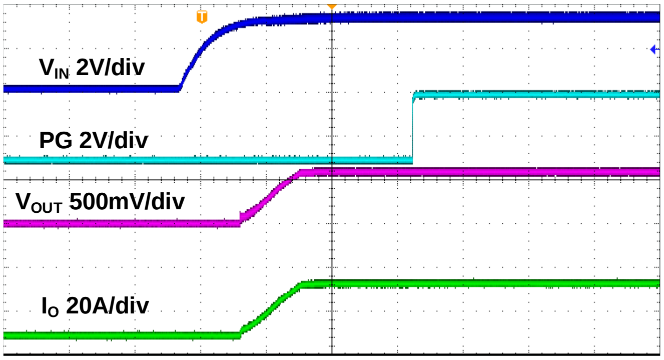
Startup from V_{IN}
(V_{IN}=3.3V,V_{OUT}=0.6V,I_O=0A)



Shutdown from V_{IN}
(V_{IN}=3.3V,V_{OUT}=0.6V,I_O=0A)

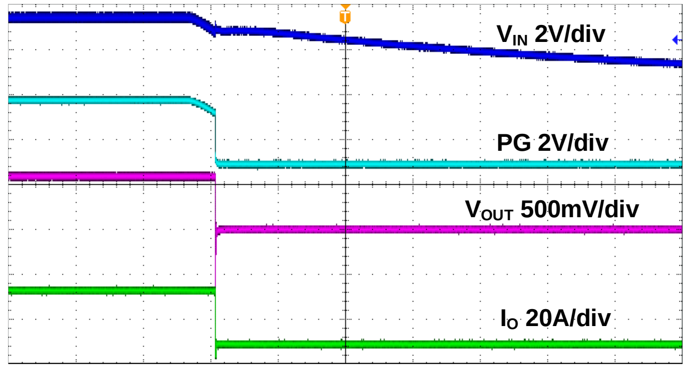


Startup from V_{IN}
(V_{IN}=3.3V,V_{OUT}=0.6V,I_O=25A)



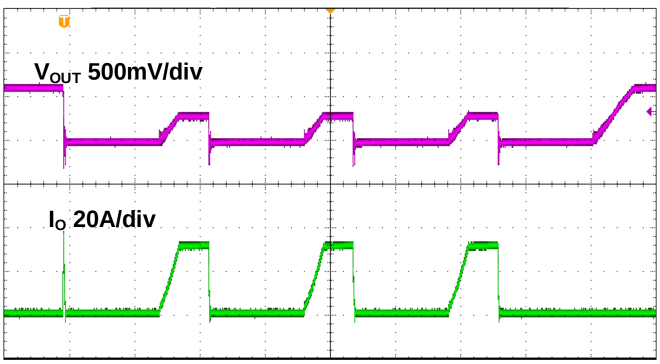
Time 2ms/div

Shutdown from V_{IN}
(V_{IN}=3.3V,V_{OUT}=0.6V,I_O=25A)



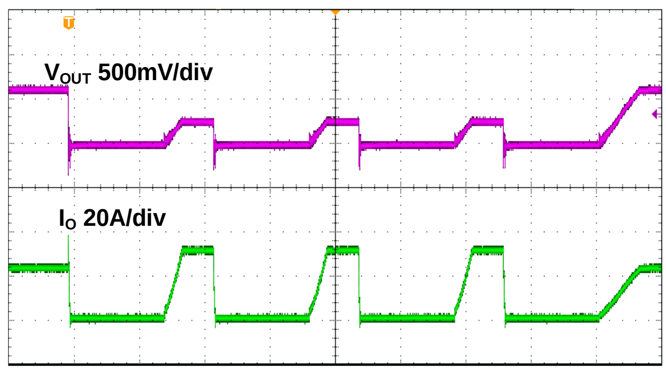
Time 2ms/div

Short Circuit Protection
(V_{IN}=3.3V,V_{OUT}=0.6V,I_O=0A)



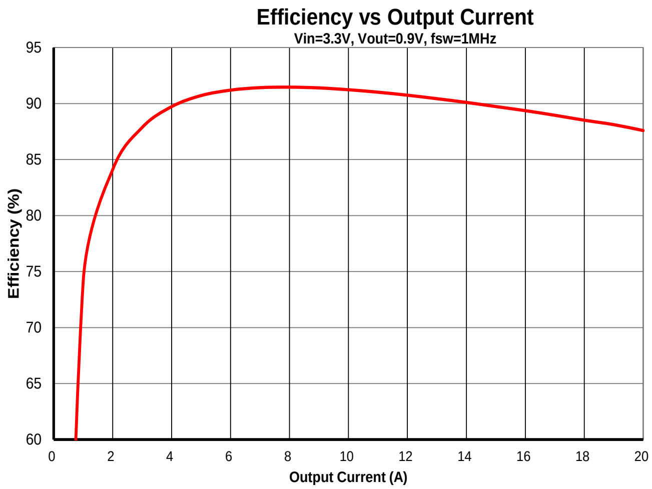
Time 4ms/div

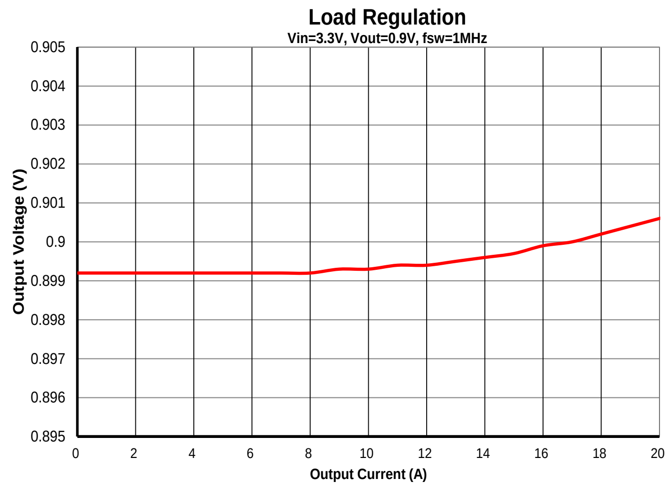
Short Circuit Protection
(V_{IN}=3.3V,V_{OUT}=0.6V,I_O=25A)



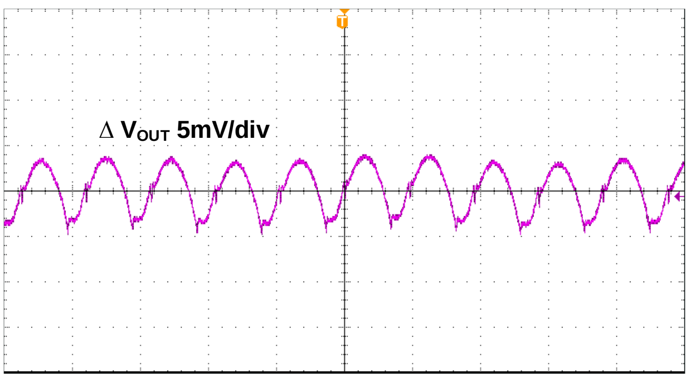
Time 4ms/div

V_{OUT}=0.9V



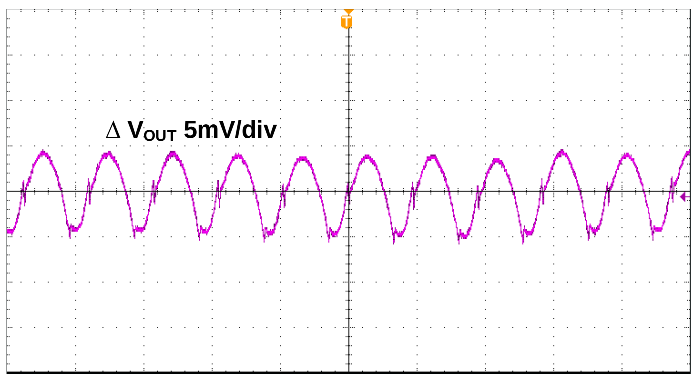


Output Ripple
(V_{IN}=3.3V,V_{OUT}=0.9V,I_O=0A)



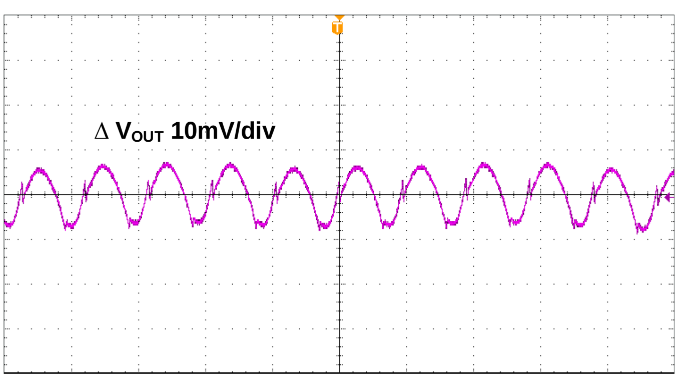
Time 1μs/div

Output Ripple
(V_{IN}=3.3V,V_{OUT}=0.9V,I_O=10A)



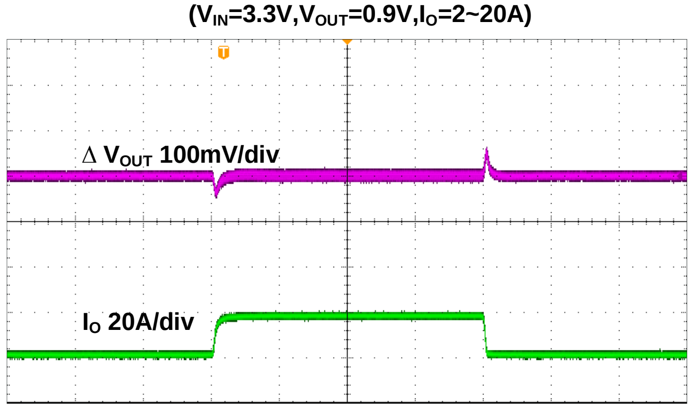
Time 1μs/div

Output Ripple
(V_{IN}=3.3V,V_{OUT}=0.9V,I_O=20A)



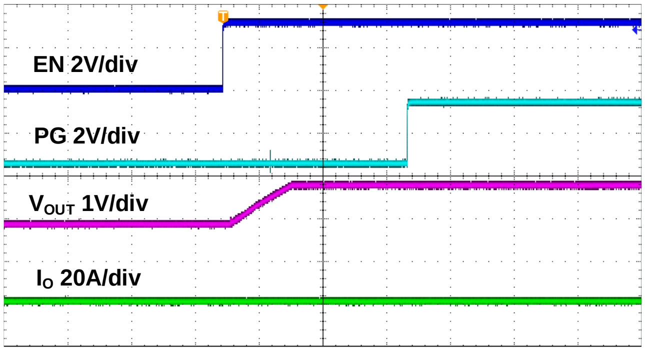
Time 1μs/div

Load Transient
(V_{IN}=3.3V,V_{OUT}=0.9V,I_O=2~20A)



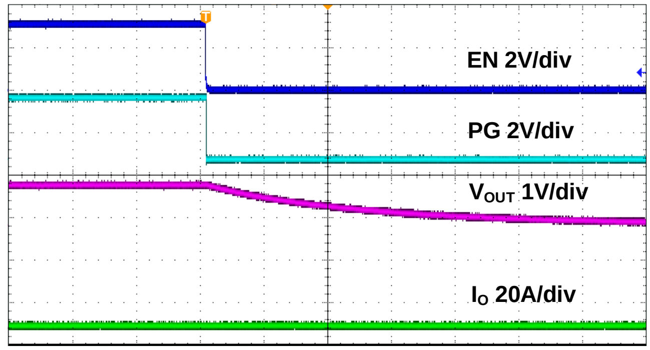
Time 400μs/div

Startup from EN
(V_{IN}=3.3V,V_{OUT}=0.9V,I_O=0A)



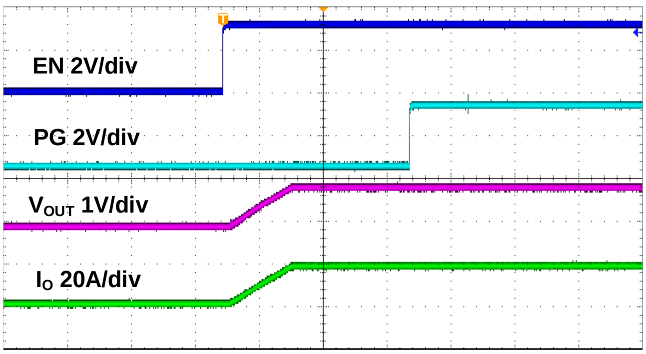
Time 2ms/div

Shutdown from EN
(V_{IN}=3.3V,V_{OUT}=0.9V,I_O=0A)



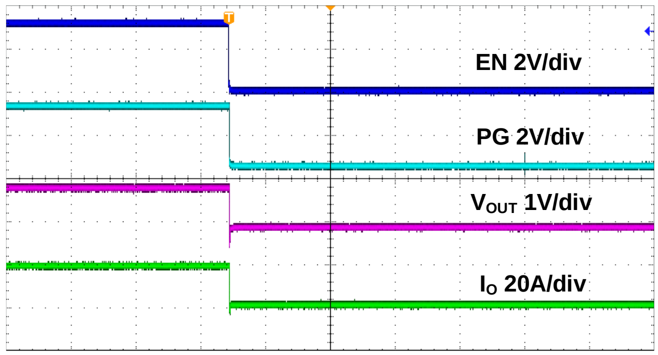
Time 2ms/div

Startup from EN
(V_{IN}=3.3V,V_{OUT}=0.9V,I_O=20A)



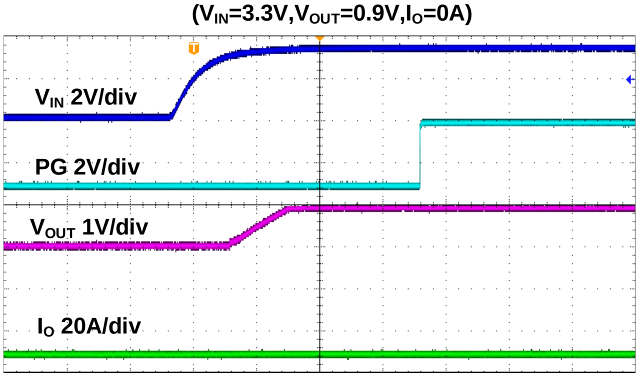
Time 2ms/div

Shutdown from EN
(V_{IN}=3.3V,V_{OUT}=0.9V,I_O=20A)



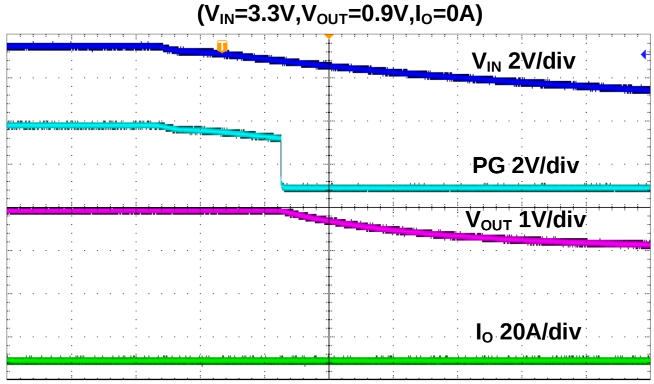
Time 2ms/div

Startup from V_{IN}
(V_{IN}=3.3V,V_{OUT}=0.9V,I_O=0A)



Time 2ms/div

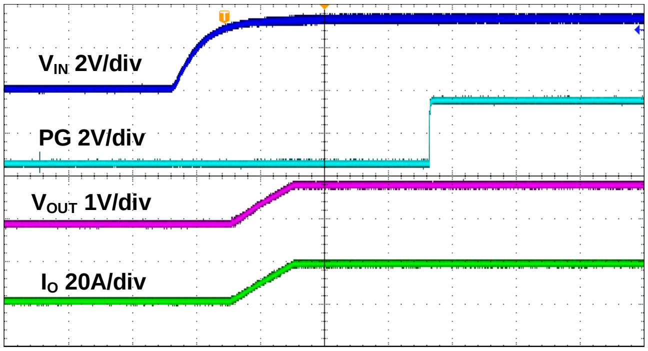
Shutdown from V_{IN}
(V_{IN}=3.3V,V_{OUT}=0.9V,I_O=0A)



Time 2ms/div

Startup from V_{IN}

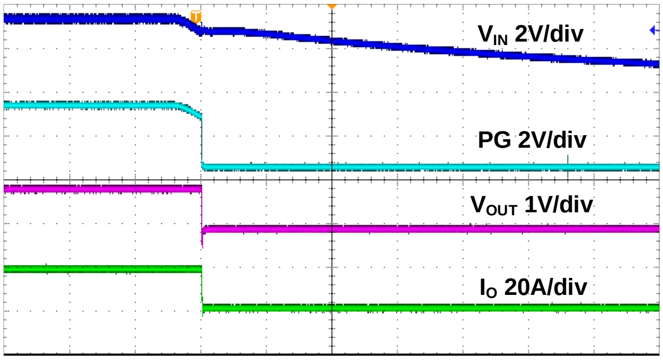
(V_{IN}=3.3V,V_{OUT}=0.9V,I_O=20A)



Time 2ms/div

Shutdown from V_{IN}

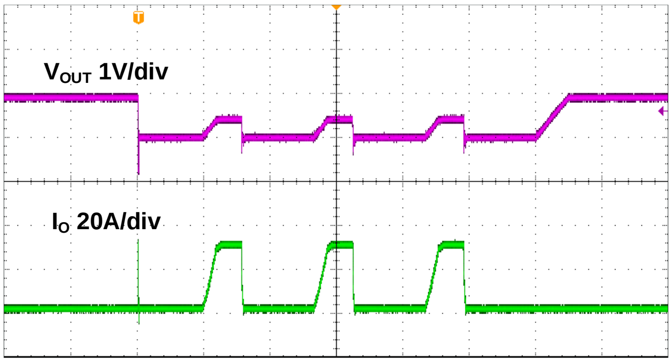
(V_{IN}=3.3V,V_{OUT}=0.9V,I_O=20A)



Time 2ms/div

Short Circuit Protection

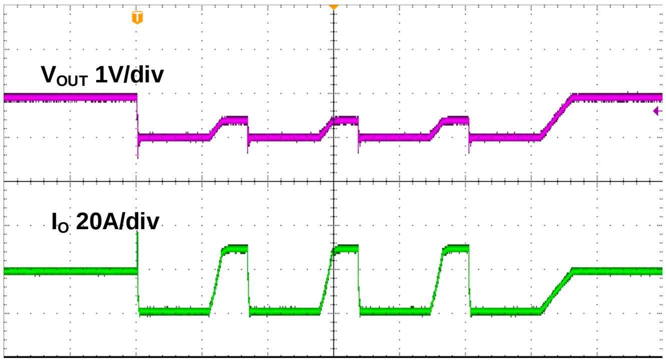
(V_{IN}=3.3V,V_{OUT}=0.9V,I_O=0A)



Time 4ms/div

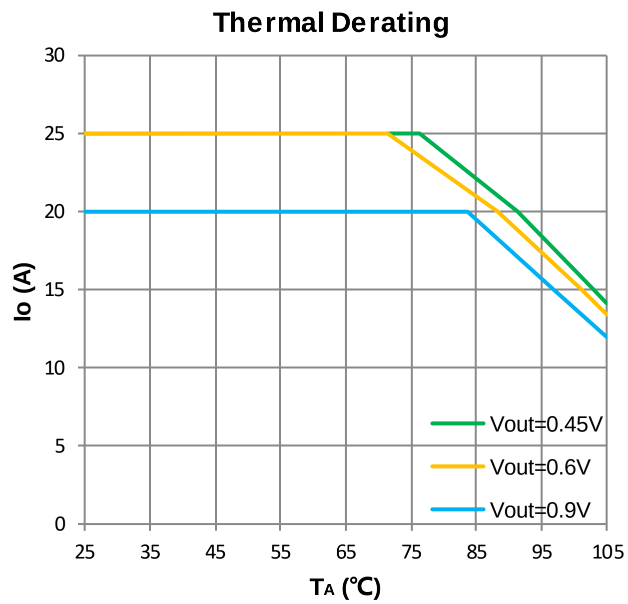
Short Circuit Protection

(V_{IN}=3.3V,V_{OUT}=0.9V,I_O=20A)



Time 4ms/div

Thermal Derating (V_{IN}=3.3V)



- T_A: Ambient temperature, 0.5 inch above IC.
- Based on a four-layer 8cm×8cm Silergy Evaluation Board in the natural convection. Board thickness: 1.6mm, copper thickness: 2 oz, copper coverage: 95%. No heat sink, natural convection.
- The die temperature is not beyond 125℃ under this TD curve.
- The inductor is exposed and the IC case is the inductor top surface.

Detailed Description

The SQ76030A/A1 is a high efficiency synchronous step-down DC/DC module which is PMBus 1.3 compliant. The SQ76030A/A1 is capable of delivering up to 25A current. It provides accurate regulation for a variety of loads with an accurate voltage reference over T_J= -40°C to 125°C.

The SQ76030A/A1 adopts COT architecture to achieve fast transient responses for high step-down applications. The module is also equipped with cycle-by-cycle current limit, hiccup over current protection and thermal shutdown protection.

Constant-on-time Architecture and Frequency Lock Loop (PLL)

Fundamental to any constant-on-time (COT) architecture is the one-shot circuit or on-time generator, which determines how long to turn on the high-side power switch. Each on-time (t_{ON}) is a “fixed” period internally calculated to operate the step down regulator at the desired switching frequency considering the input and output voltage ration, $t_{ON}=(V_{OUT}/V_{IN})\times(1/f_{SW})$. Each t_{ON} pulse is triggered by the feedback comparator when the output voltage as measured at internal feedback point drops below the target value. After a t_{ON} period, a minimum off time ($t_{OFF,MIN}$) is imposed before any further switching is initiated, even if the output voltage is less than the target. This approach avoids making any switching decisions during the noisy periods when the switching node (SW) is rapidly rising or falling.

In a COT architecture, there is no fixed clock, so the high side power switch can turn on almost immediately after a load transient and subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays.

Once the on-time calculated by the constant on-time architecture deviates from the accurate on-time value, especially in the case of low duty cycle operation, the actual switching frequency will deviate significantly from the setting value. When the load is close to full load, the duty cycle loss will also cause switching frequency deviation. In order to keep the switching frequency relatively constant under different application conditions, the constant on-time architecture needs a frequency lock loop (FLL). In the FLL, the reference frequency is a fixed clock, keeps the same as the setting frequency, and the switching frequency is compared with it cycle by cycle. This loop will adjust the actual on-time, let the switching frequency follow the reference frequency until there is no deviation between them.

Instant-PWM Operation

Silergy’s instant-PWM control method adds several proprietary improvements to the traditional COT architecture. Whereas most legacy based on COT implementations require a dedicated connection to the output voltage terminal to calculate the t_{ON} duration, instant-PWM derives this signal internally.

Additionally, it optimizes operation with low ESR ceramic output capacitors. In many applications it is desirable to utilize very low ESR ceramic output capacitors, but legacy COT regulators become unstable in these cases because the beneficial ramp signal that results from the inductor current flowing into the output capacitor may be too small to maintain smooth operation. For this reason, instant PWM synthesizes a virtual replica of this signal internally. This internal virtual ramp and the feedback voltage are combined and compared to the reference voltage. When the sum is lower than the reference voltage, the t_{ON} pulse is triggered as long as the minimum t_{OFF} has been satisfied and the inductor current as measured in the low side synchronous rectifier is lower than the bottom FET current limit. As the t_{ON} pulse is triggered, the low-side synchronous rectifier is turned off if necessary and the high-side power switch is turned on. Inductor current then ramps up linearly during t_{ON}. At the conclusion of t_{ON}, the high-side power switch is turned off, the low-side synchronous rectifier is turned on and the inductor current ramps down linearly.

This action also initiates the minimum t_{OFF} timer to ensure sufficient time for stabilizing any transient conditions and settling the feedback comparator before the next cycle is initiated. This minimum t_{OFF} is relatively short so that during fast load transient t_{ON} can be retriggered with minimal delay, allowing the inductor current to ramp up quickly to provide sufficient energy to the load.

To avoid shoot-through current, a dead time (t_{DEAD}) is generated internally to ensure that only one switch is on at any time.

Switching Frequency

SQ76030A/A1 supports four selectable operating frequencies which can be programmed through the PMBus command of D2h[2:1]: 400kHz, 600kHz, 800kHz and 1000kHz.

Soft Start

The internal soft-start circuit smoothly ramps the output to the desired voltage whenever the device is enabled. Internally, the soft-start circuit clamps the output at a low voltage and then allows it to rise to the desired voltage over one soft-start time (t_{SS}), which avoids high current flow and transients during startup.

Differential Remote Sense (RSP, RSN)

RSP and RSN may be used as a differential feedback connection directly to the output capacitor or main load connection. This helps to compensate for DC losses in the PCB at high output currents. The pair of the remote sense trace should be kept in low impedance to achieve the best performance.

Output Discharge Function

The SQ76030A/A1 discharges the output voltage if the shutdown logic is triggered from V_{IN} UVLO, EN OFF, or thermal shutdown so that output voltage can be discharged in minimal time, even if load current is zero. The discharge MOSFET in parallel with the low side synchronous rectifier, turns on after the low side synchronous rectifier turns off when shut down logic is triggered. The output discharge MOSFET $R_{DS(ON)}$ is typically 50Ω at room temperature. Note that discharge MOSFET is not active beyond these shutdown conditions.

Power Good Indicator (PG)

PG is an open drain output controlled by a window comparator connected to the feedback signal. PG allows system monitoring of the device. Connect PG with a resistor in the range 10kΩ~100kΩ to VCC or another voltage source less than 4V. During startup, PG is pulled low, if the internal V_{FB} reaches the threshold $V_{PG\_H\_RISING}$ and less than $V_{PG\_L\_RISING}$, PG will become high impedance after a delay time, indicating that the output is good. If V_{FB} drops below $V_{PG\_L\_FALLING}$, or rises above $V_{PG\_L\_RISING}$, PG is pulled low. PG is also pulled low if the device encounters any other fault condition (e.g. OTP, OCP, UVLO, etc.). PG functionality is active even in the absence of V_{IN} or VCC, as long as the pull-up power source is available.

Input Capacitor C_{IN}

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply and to reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X7R or X7T series ceramic capacitors are most often selected due to their small size, low cost, surge current capability and high RMS current ratings over a wide temperature and voltage range.

In situations where the input rail is supplied through long wires it is recommended adding some bulk capacitance like electrolytic, tantalum or polymer type capacitors to reduce the overshoot and ringing caused by the added parasitic inductance.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications, four 22uF X7R capacitors are sufficient.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting the component. For the best performance, it is recommended using X7R or X7T series ceramic capacitors with 2.5V rating and a capacitance that is greater than 138uF.

For applications where the design must meet strict ripple requirements, the following considerations must be followed:

The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitors ESR (ESR ripple) as well as the stored charge (capacitive ripple). When considering total ripple, both should be considered.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Consider a typical application with ΔI_L = (25A I_{OUT} x 40%) = 10 A and using two 22μF and two 47μF ceramic capacitors with an ESR of ~3mΩ.

$$V_{RIPPLE,ESR} = 10A \times 3m\Omega / 4 = 7.5\,mV$$
$$V_{RIPPLE,CAP} = 10A / [8 \times (22+47)\mu F \times 2 \times 1MHz] = 9\,mV$$

The capacitive ripple might be higher because for ceramic capacitors the effective capacitance decreases with the voltage across the terminals. The voltage derating is usually included in the capacitor datasheet as a chart and the ripple can be re-calculated taking the target output voltage into account.

Application recommendations

In applications with different output voltage, the output current and output capacitance should be limited to achieve the optimal stability. Please refer to Table 1 for the recommended settings based on -40°C to +85°C ambient temperature, and all peripheral ceramic capacitors. If the output current is beyond the range, it may cause unstable operation and the output ripple may increase.

Table 1. Application Settings Recommendation

V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)	$C_{OUT,MIN}$ (μF)	$C_{OUT,MAX}$ (μF)
2.9-5.5	0.35 ≤V_{OUT}≤0.75	0-25	138	800
2.9-5.5	0.75<V_{OUT}≤0.94	0-20	138	800
2.9-5.5	0.94<V_{OUT}≤1.25	0-15	138	800

For the best performance, it is recommended to use X7R or better grade ceramic capacitor. Place this ceramic capacitor really close to the VOUT and GND pins to minimize the loop area formed by COUT, and the VOUT/GND pins.

Table 2. External Capacitor Recommendation

	Description	Vendor	PN
C_{IN} C_{OUT}	22μF/6.3V/ X7T,0603	Murata	GRM188D70J226ME01#
C_{OUT}	47μF/2.5V/ X7T,0603	Murata	GRM188D70E476ME01#

Over Current Protection (OCP)

Three cycle-by-cycle over-current protections(Valley Current Limit, Peak Current limit, Negative Current Limit) are integrated in this device to prevent excessive current flow.

Valley Current Limit

Inductor current is measured in the low-side synchronous rectifier when it turns on and as the inductor current ramps down. If the current exceeds I_{VALLEY_LIMIT} (30A typical), the synchronous rectifier is turned off and t_{ON} is inhibited until the current is less than I_{VALLEY_LIMIT}.

Peak Current Limit

During t_{ON}, and after t_{ON_MIN}, if the high-side power switch current exceeds I_{PEAK_LIMIT} (50A typical), the switch is turned off, the lowside synchronous rectifier is turned on and t_{ON} is inhibited until the low-side synchronous rectifier current is below I_{VALLEY_LIMIT}.

Negative Current Limit

If the low-side synchronous rectifier current exceeds $I_{NEGATIVE\_LIMIT}$(-20A typical) after t_{OFF_MIN}, the low-side synchronous rectifier is turned off and the high-side power switch is turned on.

Output Under Voltage Protection (UVP)

After startup, if the internal V_{FB} drops below UVP threshold, UVP will be triggered, device will react as hiccup mode and shut down for 2×t_{SS}, after which the device will restart with a complete soft start cycle. This 'hiccup' cycle of startup and shutdown will continue unless the fault condition removed or the junction temperature exceeds T_{OT_FAULT}.

Output Over Voltage Protection (OVP)

The device auto-recovery protection response will be performed if V_{FB} exceeds $V_{OVP\_DEFAULT}$, the high-side power switch will be turned off and the low-side synchronous rectifier is turned on in an attempt to bring the V_{FB} below $V_{OVP\_DEFAULT}$ until IL reaches the $I_{NEGATIVE\_LIMIT}$. Then, the low-side synchronous rectifier is turned off and the high-side power switch is turned on again for the on-time determined by V_{IN}, V_{OUT}, and f_{SW} to limit the negative inductor current. The IC repeats this operation until V_{FB} is again in regulation or until the junction temperature exceeds T_{OT_FAULT}.

Over Temperature Protection (OTP)

The over temperature protection (OTP) circuitry prevents overheating due to excessive power dissipation. This will shut down the device when the monitored junction temperature exceeds T_{OT_FAULT}. The device can resume normal operation after a complete soft-start cycle once the junction temperature cools down by T_{OT_HYS}. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the T_{OT_FAULT}.

PMBus 1.3 Compatible Interface

SQ76030A/A1 integrates a PMBus 1.3 compatible interface. To ensure compatibility with a wide range of system processors, the PMBus interface supports bus speeds of up to 400kHz and uses standard PMBus 1.3 commands. SQ76030A/A1 always operates as a peripheral device, and is addressed using a 7-bit peripheral address followed by an 8th bit, which indicates whether the transaction is a read-operation or a write-operation.

PMBus Interface Timing Diagram

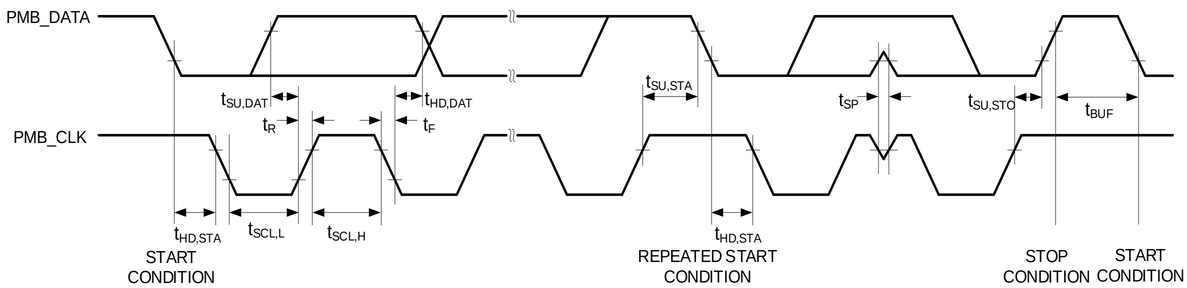


Figure 4. PMBus Interface Timing Diagram

PMBus Device Address

When communicating with multiple devices using the PMBus interface, each device must have its own unique address so the host can distinguish between the devices. The 7-bit device address of SQ76030A/A1 is selected by ADDR pin, as shown below:

Table 3. PMBus address configuration by ADDR resistor R_{ADDR}

PMBus Address	R_{ADDR}/kΩ
30h	1, 4.99
31h	15
32h	24.9
33h	34.8
34h	45.3
35h	54.9
36h	61.9
37h	75
38h	115
39h	150

START and STOP Conditions

The START condition is a HIGH to LOW transition of the PMB_DATA line while PMB_CLK is HIGH. The STOP condition is a LOW to HIGH transition on the PMB_DATA line while PMB_CLK is HIGH. A STOP condition must be sent before each START condition. The I2C controller always generates the START and STOP conditions.

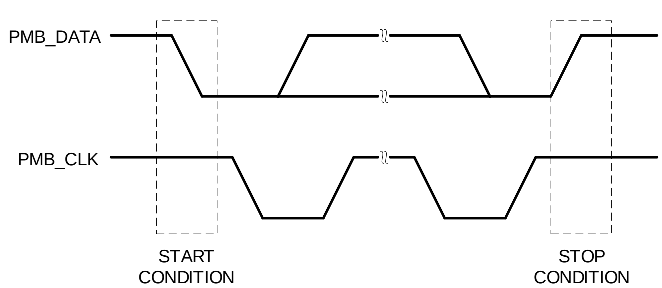


Figure 5. START and STOP Conditions Diagram

Data Validity

The data on the PMB_DATA line must be stable during the HIGH period of the PMB_CLK, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the PMB_CLK line is LOW.

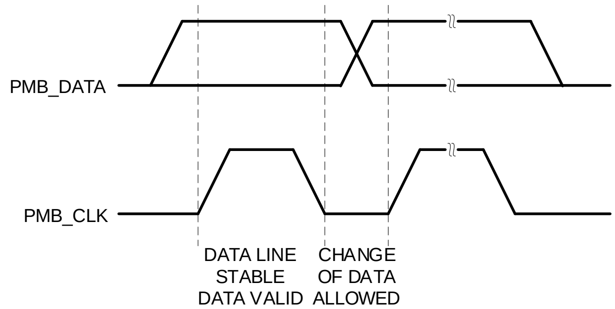


Figure 6. Data Validity Diagram

Acknowledge

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the controller sends 7-periphera address bits and an R/$\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the controller and the peripheral to acknowledge receipt of register addresses and data.

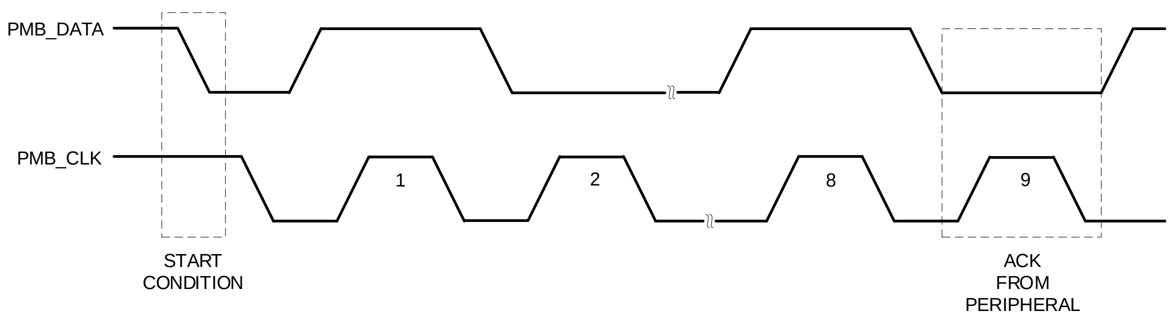


Figure 7. Acknowledge Diagram

Data Transactions

All transactions start with a control byte sent from the PMBus controller. The control byte begins with a START condition, followed by 7-bits of peripheral address and one R/W bit. The R/W bit is 0 for a write or 1 for a read. If the peripheral on the PMBus recognize its address, it will acknowledge by pulling the PMB_DATA line low for the last clock cycle in the control byte. If no peripheral exist at that address or is not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition. Once the control byte is sent, and the SQ76030A/A1 acknowledges it, the 2nd byte sent by the controller must be a command code. Once the SQ76030A/A1 receives a command code byte it responds with an Acknowledge. If a STOP condition is detected, the SQ76030A/A1 processes the execution commands immediately.

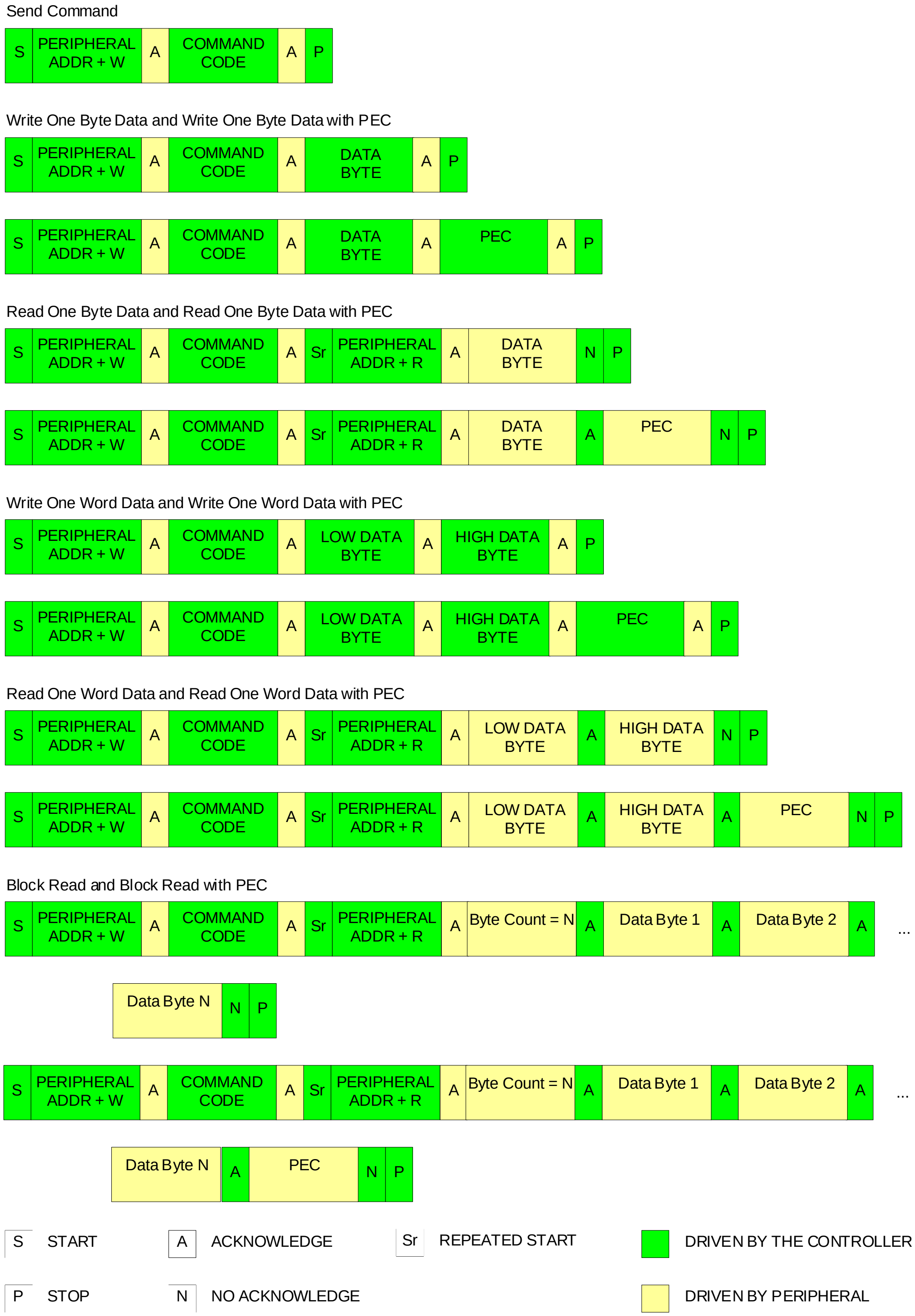


Figure 8. Data Transmission Diagram

Supported PMBus Command Code and Default Value

Command Code	Command Name	Type	Bytes	Default Value	MTP
01h	OPERATION	R/W	1	0x00 (SQ76030A) 0x80 (SQ76030A1)	√
15h	STORE_USER_ALL	Send	0	/	/
21h	VOUT_COMMAND	R/W	2	0x00E6 (SQ76030A) 0x01D8 (SQ76030A1)	√
24h	VOUT_MAX	R/W	2	0x0280	√
2Bh	VOUT_MIN	R/W	2	0x00B3	√
99h	MFR_ID	Block Read	1(byte)+ 7(data)	0x53 0x49 0x4C 0x45 0x52 0x47 0x59, ASCII “SILERGY”	/
D2h	MFR_VOUT_CTRL2	R/W	1	0x37	√

Register Description

OPERATION (01h)

Format: Unsigned binary

The OPERATION command turns the device output on or off in conjunction with input from the EN signal. This OPERATION command is also used to re-enable the module after a fault-triggered shutdown. Writing an off command followed by an on command clears all faults. Writing only an on command after a fault-triggered shutdown will not clear the fault registers.

Bits	R/W	Name	Default	Description
7	R/W	SOFTWARE EN BIT	0 (SQ76030A) 1 (SQ76030A1)	0: disable 1: enable
6:0	R/W	RESERVED	000 0000	Always read/write as 000 0000, don’t write other value.

The I²C communication is enabled as soon as the appropriate V_{IN} is applied. Both hardware EN pin and SOFTWARE EN BIT determine the module output. Please see the logic table below.

Table 4. I²C and Module output enable logic

V_{IN} OK	EN pin	SOFTWARE EN BIT	I²C	Module output
0	X	X	Disabled	Disabled
1	0	X	Enabled	Disabled
1	X	0	Enabled	Disabled
1	1	1	Enabled	Enabled

STORE_USER_ALL(15h)

The STORE_USER_ALL command stores all of the current storable register settings in the EEPROM memory as the new defaults on power up.

This command has no data bytes. This command can only be written.

VOUT_COMMAND (21h)

Format: Linear, Unsigned binary

The VOUT_COMMAND command sets output voltage to the commanded value.

Bits	R/W	Name	Default	Description
15:12	R	RESERVED	0000	Always read as 0000.
11:0	R/W	VOUT_COMMAND	0000 1110 0110 (SQ76030A) 0001 1101 1000 (SQ76030A1)	LSB = 1.95mV. V_{OUT}(mV)= 1.95*VOUT_COMMAND(Decimal). VOUT_COMMAND(Decimal) range is 179~845. Thus V_{OUT} range is 0.35~1.65V. The default value is 0.45V(SQ76030A) / 0.92V(SQ76030A1)

VOUT_MAX(24h)
Format: Linear, Unsigned binary
The VOUT_ MAX command sets an upper limit on the output voltage. If an attempt is made to program the output voltage higher than the limit set by this command, the device shall respond as follows:
• The commanded output voltage shall be set to VOUT_MAX;
The data bytes are two bytes formatted.

Bits	R/W	Name	Default	Description
15:12	R	RESERVED	0000	Always read as 0000.
11:0	R/W	VOUT_MAX	0010 1000 0000	LSB = 1.95mV. VOUT_MAX Voltage range is 0.55~1.65V. The default value is 1.25V.

VOUT_MIN(2Bh)
Format: Linear, Unsigned binary
The VOUT_ MIN command sets a lower limit on the output voltage. If an attempt is made to program the output voltage lower than the limit set by this command, the device shall respond as follows:
• The commanded output voltage shall be set to VOUT_MIN;
The data bytes are two bytes formatted.

Bits	R/W	Name	Default	Description
15:12	R	RESERVED	0000	Always read as 0000.
11:0	R/W	VOUT_MIN	0000 1011 0011	LSB = 1.95mV. VOUT_MIN Voltage range is 0.35~1.5V. The default value is 0.35V.

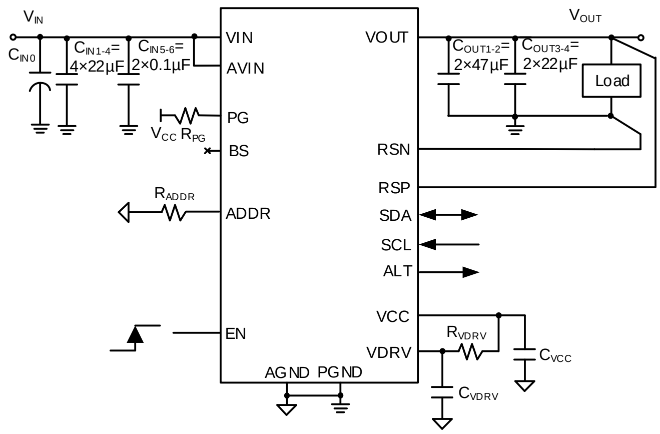
MFR_ID(99h)
The MFR_ID command returns the company identification.

Byte	Name	Description
0	Byte Count	Always read as 0x07.The number of date bytes that the block read command expects to read.
1	Character 1	Always read as 0x53, ASCII of “S”.
2	Character 2	Always read as 0x49, ASCII of “I”.
3	Character 3	Always read as 0x4C, ASCII of “L”.
4	Character 4	Always read as 0x45, ASCII of “E”.
5	Character 5	Always read as 0x52, ASCII of “R”.
6	Character 6	Always read as 0x47, ASCII of “G”.
7	Character 7	Always read as 0x59, ASCII of “Y”.

MFR_VOUT_CTRL2(D2h)
Format: Unsigned binary
MFR_VOUT_CTRL2 command sets the output voltage behaviors of the device.

Bits	R/W	Name	Default	Description
7:6	R	RESERVED	00	Always read as 00.
5:3	R/W	RESERVED	110	Always read/write as 110, don’t write other value.
2:1	R/W	SWITCHING FREQUENCY	11	Sets the switching frequency: 00:400kHz 01:600kHz 10:800kHz 11:1MHz
0	R/W	RESERVED	1	Always read/write as 1, don’t write other value.

Application Schematic



BOM List

Designator	Description	Part Number	Manufacturer
C_{IN0}	100µF/25V Electrolytic Cap		
C_{IN1-4}	22µF, 6.3V, X7T, 0603	GRM188D70J226ME01#	Murata
C_{IN5-6}	0.1µF, 50V, X7R, 0402	GRM155R71H104KE14D	Murata
C_{OUT1-2}	22µF, 6.3V, X7T, 0603	GRM188D70J226ME01#	Murata
C_{OUT3-4}	47µF, 2.5V, X7T,0603	GRM188D70E476ME01#	Murata
C_{VCC}	1µF, 16V, 0603	GCM188R71C105MA64#	Murata
C_{VDRV}	1µF, 16V, 0603	GCM188R71C105MA64#	Murata
R_{PG}	100kΩ, 1%, 0603		
R_{ADDR}	4.99kΩ, 1%, 0603		
R_{VDRV}	1Ω, 1%, 0603		

Layout Design

Follow these PCB layout guidelines to achieve a higher efficiency and better noise immunity.

- Major MLCC capacitors (C_{IN}, C_{OUT}, C_{VCC}, C_{VDRV}) should be placed close to the module.
- C_{IN} must be close to each VIN pins and PGND. The loop area formed by C_{IN} and PGND must be minimized. 0.1μF capacitors with small package (such as 0402) are recommended strongly to be placed as close as possible to VIN pin5 and VIN pin27 separately, and all C_{IN} PGND terminals are connected by a dedicated PGND plane.
- Connect VIN pin and AVIN pin together directly.
- C_{OUT} must be close to the VOUT pins and PGND. The loop area formed by C_{OUT} and PGND must be minimized.
- It is desirable to maximize the PCB copper area connecting to the PGND pin to achieve the best thermal and noise performance. A ground plane is highly desirable.
- The RSP/RSN trace should be kept as short as possible and away from noise sources on the PCB.
- C_{VCC} must be close to the VCC pin and AGND pin. The loop area formed by C_{VCC} and VCC/AGND pin must be minimized. AGND should be connected to the dedicated PGND plane by via close to C_{VCC}.
- The NC pin48 should be left floating.

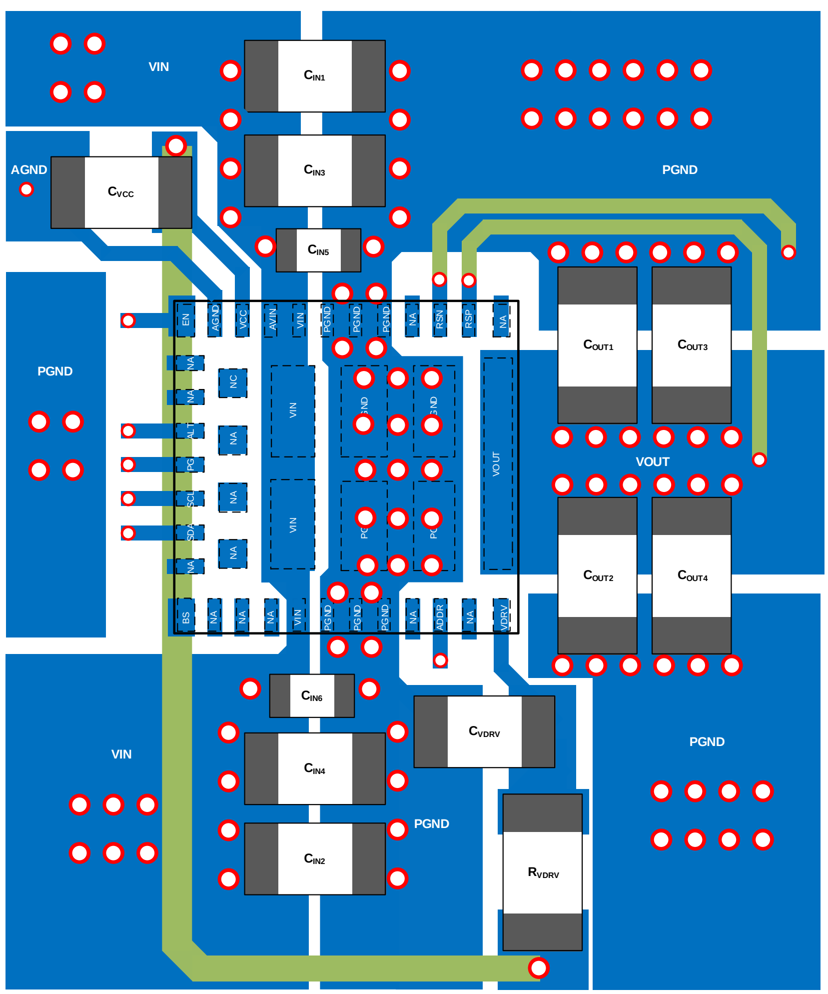
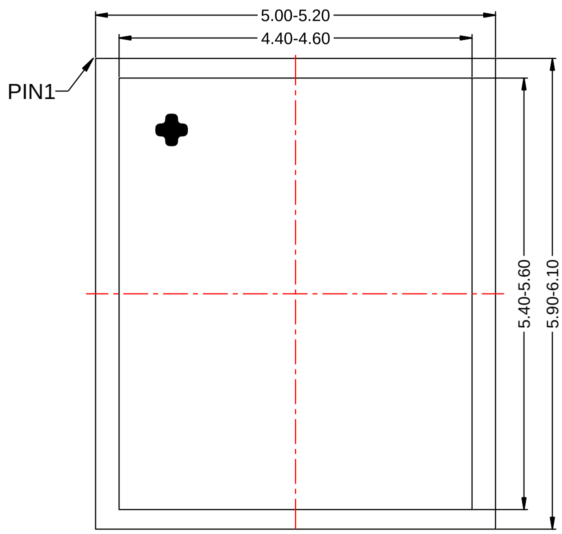
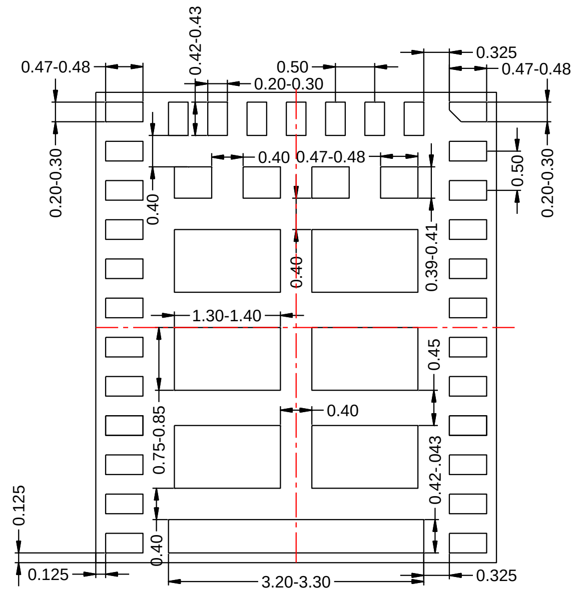


Figure 9. Suggested PCB Layout

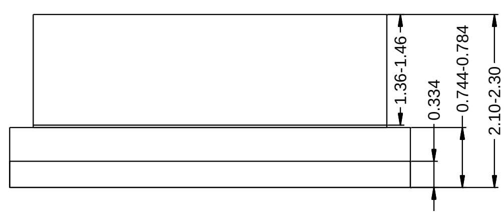
MLGA5.1X6-48 Package Outline Drawing



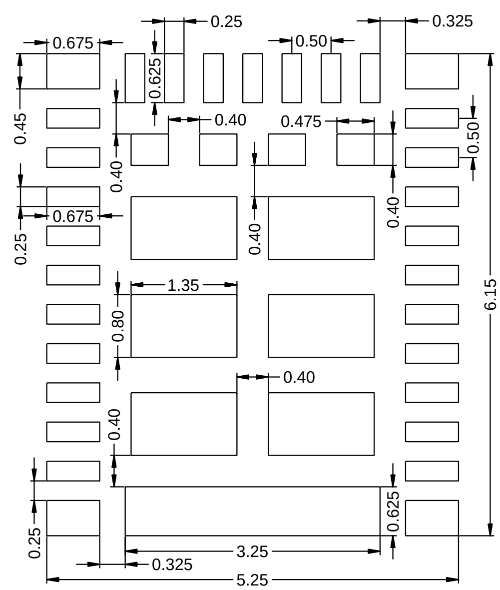
Top View



Bottom View



Side View



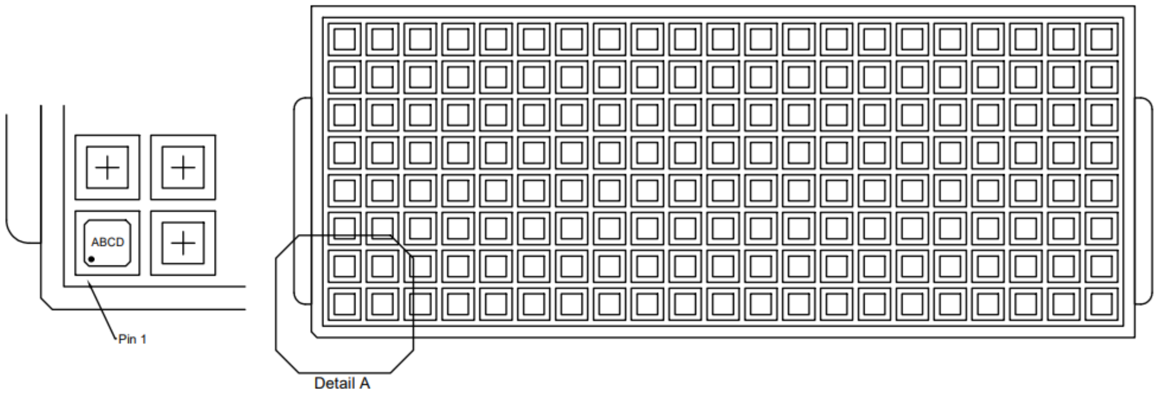
Recommended PCB layout
(Reference only)

Notes: 1.All dimension in millimeter and exclude mold flash & metal burr.

2.Center line on drawing refers to the chip body center.

Taping orientation

MLGA5.1*6-48 Tray information



Part number	Package types	Qty Per Tray (pcs)	Trays per box	Qty per box (pcs)
SQ76030AALG	MLGA5.1*6-48	360	10	3600
SQ76030A1ALG	MLGA5.1*6-48	360	10	3600

Packaging Information

Device Code: **LRJ** (SQ76030AALG)

Device Code: **MEB** (SQ76030A1ALG)

Label Information

W/O: XXXXXXXXXX

P/N: SQ76030AALG

QTY: XXXX

D/C Lot: XXXXXXXXXX

MSL3

Pb-Free

RoHS Compliant
Halogen Free

(The barcode is for demonstration only.)

W/O: XXXXXXXXXX

P/N: SQ76030A1ALG

QTY: XXXX

D/C Lot: XXXXXXXXXX

MSL3

Pb-Free

RoHS Compliant
Halogen Free

(The barcode is for demonstration only.)

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