SA33756

LED Matrix Manager with Internal Clock and MTP

General Description

The SA33756 is a matrix LED controller capable of controlling 16 LEDs, enabling features such as sequential flow lighting effects and Adaptive Driving Beams (ADB). These 16 LEDs can be connected to one to four constant current sources, catering to multiple sets of applications.

The SA33756 integrates a 20 MHz internal oscillator, enabling clock calibration over the communication interface and supporting inter-chip clock synchronization. An integrated 8-bit ADC allows monitoring of both the IC die temperature and an external NTC resistor for thermal management.

The communication interface is compatible with external CAN transceivers and utilizes Multiple-Time Programmable (MTP) memory to store factory-customized configurations. To reduce communication overhead, the chip includes a dedicated flow lighting mode: after an initial one-time setup, each subsequent lighting sequence requires only a single communication command.

For functional safety, the device implements a limp-home mode that ensures basic headlight illumination remains active even in the event of a communication failure.

Features

- AEC-Q100 qualified for automotive applications
- Functional Safety Quality-Managed
- 16 integrated bypass switches
- Embedded MTP memory
- UART communication is compatible with the CAN physical layer
- Integrated ADC with 2 ADC pin Inputs and IC die temperature measurement
- Programmable 10bit PWM dimming with phase shift
- LED open protection and short detection
- Integrated flow light mode and dual flashing light mode to minimize communication transactions
- Internal trimmed oscillator
- Communication system clock calibration and inter-chip system clock calibration and synchronization

Applications

- Automotive Headlight Systems
- ADB or Glare-free High Beam
- Sequential Turn/animated Daytime Running Lights

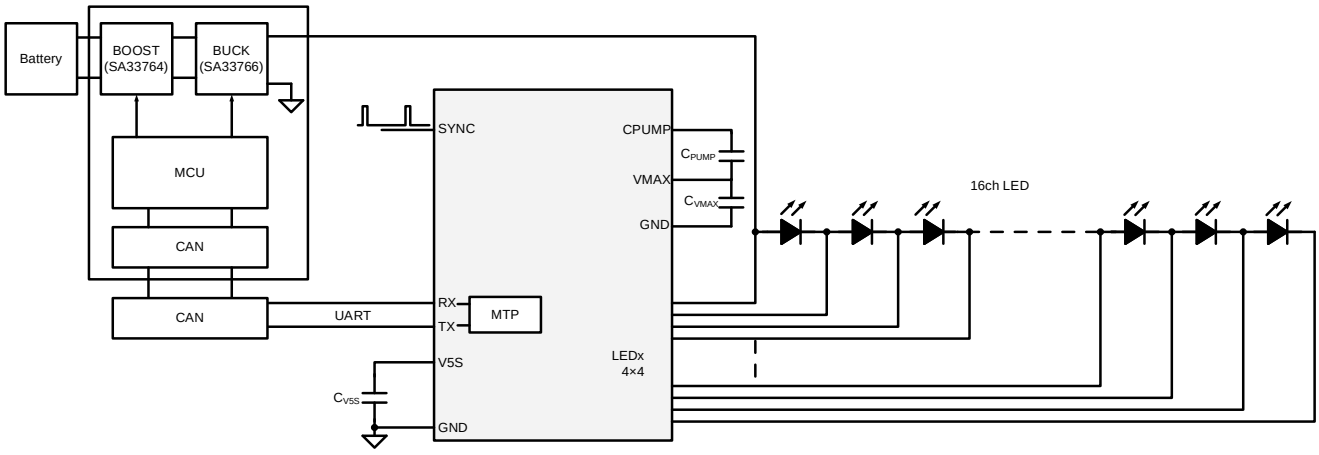


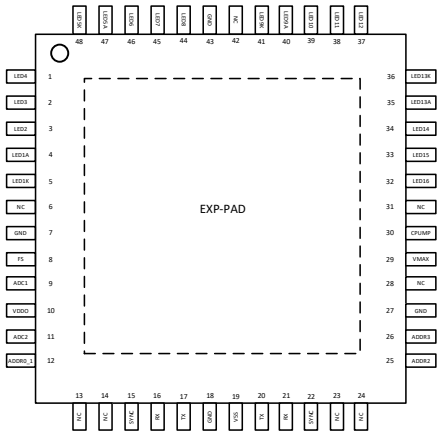
Fig. 1. Typical Application Circuit

Ordering Information

Ordering Part Number	Package type	Top Mark
SA33756GCF	LQFP7x7-48E RoHS-Compliant and Halogen-Free	**HQG*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description (A: Analog Pin, G: Ground Pin, P: Power Pin)

PIN		Type	DESCRIPTION
NAME	NO.		
LED4	1	I/O	Connect to anode of LED4.
LED3	2	I/O	Connect to anode of LED3 and cathode of LED4.
LED2	3	I/O	Connect to anode of LED2 and cathode of LED3.
LED1A	4	I/O	Connect to anode of LED1 and cathode of LED2.
LED1K	5	I/O	Connect to cathode of LED1.
FS	8	I	Failsafe state configuration pin.
ADC1	9	I	Customer Use ADC Input.
VDDO	10	O	VDD pass through to be used in pin configuration only.
ADC2	11	I	Customer Use ADC Input.
ADDR0_1	12	I	Address Pin. 2 MSB of ADC conversion become 2 LSBs of IC Address.
V5S	19	I	Connect 5V supply here to the device.
ADRR2	25	I	(MSb - 1) of IC Address.
ADRR3	26	I	MSb of Address.
VMAX	29	O	Select the max voltage of 4 part of led and V5S.
CPUMP	30	O	Output of charge pump.
LED16	32	I/O	Connect to anode of LED16
LED15	33	I/O	Connect to anode of LED15 and cathode of LED16.
LED14	34	I/O	Connect to anode of LED13 and cathode of LED14.
LED13A	35	I/O	Connect to anode of LED13 and cathode of LED14.
LED13K	36	I/O	Connect to anode of LED13 and cathode of LED14.
LED12	37	I/O	Connect to anode of LED12.
LED11	38	I/O	Connect to anode of LED11 and cathode of LED12.
LED10	39	I/O	Connect to anode of LED10 and cathode of LED11.
LED9A	40	I/O	Connect to anode of LED9 and cathode of LED10.
LED9K	41	I/O	Connect to cathode of LED9.
LED8	44	I/O	Connect to anode of LED8.
LED7	45	I/O	Connect to anode of LED7 and cathode of LED8.
LED6	46	I/O	Connect to anode of LED6 and cathode of LED7.

LED5A	47	I/O	Connect to anode of LED5 and cathode of LED6.
LED5K	48	I/O	Connect to cathode of LED5h.
SYNC	15,22	I/O	Synchronization pins, connect all the SYNC pin together for hardware synchronization function.
RX	16,21	I	UART communication RX pin.
TX	17,20	O	UART communication TX pin.
NC	6,13,14,23,24,28,31,42	NC	Do not connect.
GND	7,18,27,43	G	Ground.

Block Diagram

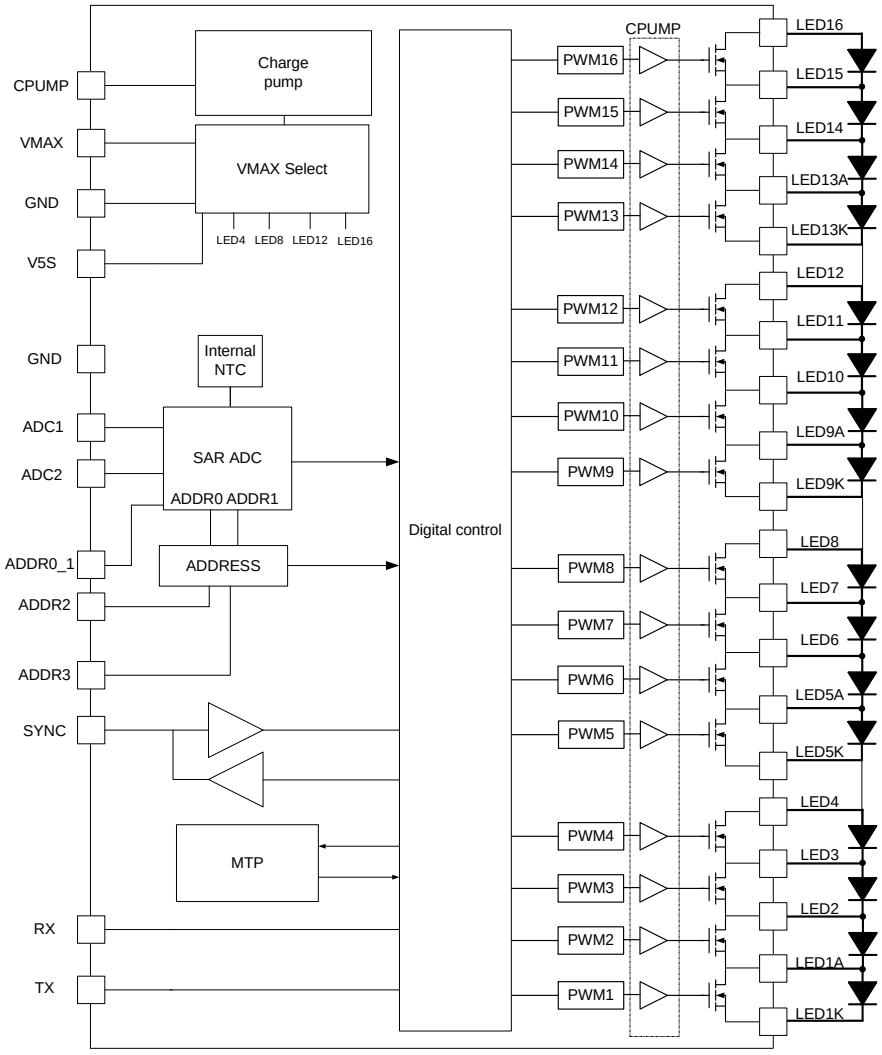


Fig. 2. Block Diagram

Absolute Maximum Ratings

Parameter		Min	Max	Unit
Voltage	V5S	-0.3	5.5	V
	CPUMP to VMAX	-0.3	5.5	
	LED1K-LED4/LED5K-LED8/LED9K-LED12/LED13K-LED16, LED4/LED8/LED12/LED16, or VMAX to GND	-0.3	61	
	LEDx to LED(x-1)	-0.3	20	
	RX,TX,ADC1,ADC2,ADDR0_1,ADDR2/3,SYNC,FS	-0.3	5.5	
Operating Junction Temperature, T_j		-40	150	°C
Lead Temperature, Soldering, 10s			260	
Storage Temperature, T_{stg}		-40	150	

Thermal Information

Parameter		48 PINS	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	23	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.7	

ESD Ratings

Parameter	Test Condition	Min	Typ	Max	Unit
V(ESD) Electrostatic discharge	HBM		±2000		V
	CDM		±750		

Recommended Operating Conditions

Parameter	Min	Max	Unit
Switch Continuous Current		1.5	A
Switch Pulse Current at 20us and FREQ=400Hz		5	A
One Series LED Operate Voltage	4.5	60	V
Maximum Rise Time of RX		150	ns
Maximum Fall Time of RX		150	ns
Input Low Voltage(RX/SYNC/ADDR2/ADDR3/FS)	0	0.7	V
Input High Voltage(RX/SYNC/ADDR2/ADDR3/FS)	2	5	V
20MHz Internal OSC Accuracy	97.5	102.5	%
Operating Ambient Temperature	-40	125	℃
Operating Junction Temperature	-40	150	℃

Electrical Characteristics

(T_J = -40°C to +150°C (unless otherwise noted) (1) (2) V5S = 5V)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
V5S	Quiescent Current	I_{V5S}	V_{LEDx} = 0 V(Charge pump being sourced from V5S)		8.3		mA
	V5S Current in Sleep Mode	I_{SLEEP_V5S}	V_{V5S}=5V		60	120	μA
	UVLO Rising Threshold	$V5S_{UVLO\_ON}$	V_{V5S} rising		4.1	4.4	V
	UVLO Falling Threshold	$V5S_{UVLO\_OFF}$	V_{V5S} falling	3.7	3.95		V
Charge Pump	Charge Pump Operating Voltage	$V_{CPUMP-VMAX}$	0 < V_{LEDx}≤60V		4.8		V
	Charge Pump Switching Frequency	F_{CPP}	Charge pump spread spectrum disabled		8.5		MHz
	Charge Pump Operating Current	I_{CPP_OPE}	LED- and GND are connected		4.5	6	mA
	VMAX Saturation Current	I_{VMAX_SAT}	VMAX short to GND		10		mA
LED MATRIX SWITCHES	LED Switch on Resistance(with Bonding Wire)	$R_{DS(ON)}$	Include bonding wire		175		mΩ
	LED Switch on Resistance	$R_{DS(ON)-4LEDS}$	Include bonding wire		450		mΩ
	OFF State FET Bias and Leakage Current	$I_{DS(off)}$	V_{DS}=20V, V_{LEDx}=0V		100		μA
	LED Short Threshold Voltage	$V_{TH-S(rise)}$		1		1.7	V
	LED OPEN Threshold Voltage	$V_{TH-O(rise)}$		7.5	10.5	13.5	V
	LEDx drain voltage rise rate	$dvdt_{rise3\_SWx}$	I_{LEDx}=0.1A, V_{LEDx}=3.1V, Voltage range from 1V to 2V.Register setting: 11.	0.53	1.06	1.59	V/μs
	LEDx drain voltage fall rate	$dvdt_{fall3\_SWx}$	I_{LEDx}=0.1A, V_{LEDx}=3.1V, Voltage range from 1V to 2V.Register setting: 11.	0.53	1.06	1.59	V/μs
	LEDx drain voltage rise rate	$dvdt_{rise2\_SWx}$	I_{LEDx}=0.1A, V_{LEDx}=3.1V, Voltage range from 1V to 2V.Register setting: 10.	0.27	0.54	0.81	V/μs
	LEDx drain voltage rise rate	$dvdt_{fall2\_SWx}$	I_{LEDx}=0.1A, V_{LEDx}=3.1V, Voltage range from 1V to 2V.Register setting: 10.	0.27	0.54	0.81	V/μs
OSCILLATOR	Internal OSC, Trimmed	F_{OSC}	V_{V5S}=5V,Spec within 2.5%	19.5	20	20.5	MHz
IO Leakage	Input Leakage Current (ADDR1_0, ADDR2, ADDR3, ADC1, ADC2, RX, FS)	I_{leak_5V5}	V_{PIN}=5.5V,V_{V5S}=5.5V	-1		1	μA

	Input Leakage Current, Pin Grounded (ADDR1_0, ADDR2, ADDR3, ADC1, ADC2, RX, FS)	I_{leak_GND}	V_{PIN}=0V,V_{V5S}=5.5V	-1		1	μA
Resistance for IO	Resistance from SYNC1 to SYNC2	$R_{PASS-SYNC}$			7.5		Ω
	Resistance from TX1 to TX2	$R_{PASS-TX}$			4		Ω
	Resistance from RX1 to RX2	$R_{PASS-RX}$			9		Ω
	Resistance from V5S to VDDO	$R_{V5S-VDDO}$			0.5		Ω
DIGITAL IO	High-Level Output Voltage(TX,SYNC)	V_{OH}	I_{SOURCE}=2mA, V_{V5S}=5V	4.79			V
	Low-level Output Voltage(TX,SYNC)	V_{OL}	I_{SINK}=2mA, V_{V5S}=5V			0.19	V
	Output Short Circuit Current, Source or Sink (TX, SYNC)	I_{OS}	V_{V5S}=5.5V, V_{PIN}=5.5V/0V short to source or GND		50		mA

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C according to JESD51-2 and PCB is built as Silergy test board. θ_{JC_TOP} is measured according to JESD51-14.

Note 3: The device is not guaranteed to function outside its operating condition.

Application information

Controlling the Internal LED Bypass Switches

The SA33756 device connects the 4 switches within the same group to reduce the number of bond wires between switches.

The $R_{DS(ON)}$ of a single switch is 175mΩ (typical) when using 2 bond wires.

When grouping switches, the total $R_{DS(ON)}$ of the group is 450 mΩ (typical) due to the shared use of 2 bond wires instead of 2 bond wires per switch.

Power Loss

When PWM dimming is applied to the LEDs with a duty cycle of D, the effective switch resistance for power dissipation calculation is:

$$P_{LOSS} = I^2 \times (1 - D) \times R_{DS(ON)series}$$

PWM Dimming

The SA33756 device provides 12-bit phase-shifted PWM dimming for each individual LED. The phase-shift and pulse width for each LED are separately programmed via the LEDxPS and TONx registers, respectively (where x = 1 to 16). The PWM period is determined by the DIV1 and DIV2 settings, which are configured in the corresponding registers.

$$F_{OSC} = 20\ Mhz$$

$$F_{PWM} = \frac{Fosc}{DIV1 \times DIV2 \times 1024}$$

DIV1[1:0]	DIVISION FACTOR DIV1
0(default)	÷1
1	÷50
2	÷125
3	÷200

DIV2 [5:0]	DIVISION FACTOR DIV2	DIV2 [5:0]	DIVISION FACTOR DIV2	DIV2 [5:0]	DIVISION FACTOR DI2	DIV2 [5:0]	DIVISION FACTOR DIV2
0	÷4	16(default)	÷20	32	÷36	48	÷52
1	÷5	17	÷21	33	÷37	49	÷53
2	÷6	18	÷22	34	÷38	50	÷54
3	÷7	19	÷23	35	÷39	51	÷55
4	÷8	20	÷24	36	÷40	52	÷56
5	÷9	21	÷25	37	÷41	53	÷57
6	÷10	22	÷26	38	÷42	54	÷58
7	÷11	23	÷27	39	÷43	55	÷59
8	÷12	24	÷28	40	÷44	56	÷60
9	÷13	25	÷29	41	÷45	57	÷61
10	÷14	26	÷30	42	÷46	58	÷62
11	÷15	27	÷31	43	÷47	59	÷63
12	÷16	28	÷32	44	÷48	60	÷64
13	÷17	29	÷33	45	÷49	61	÷65
14	÷18	30	÷34	46	÷50	62	÷66
15	÷19	31	÷35	47	÷51	63	÷67

Phase Shift

The LED turn-on phase can be independently programmed for each LED via the LEDxPS registers (where x = 1 to 16). It is recommended that the phase shift applied to each LED be configured such that the turn-on phases of all LEDs are evenly distributed within a single PWM period.

In Limp-Home Mode, the phase shift is set to the average of the 16 channels. (Phase shift is configurable via registers in Normal Mode; the default setting in Limp-Home Mode is the channel-average phase shift.) The PWM period is divided into 1024 sub-periods, and by default, the phase shifts for the 16 LEDs are evenly distributed according to the principle of equal distribution.

$$\begin{gathered} \mathrm{LED1PS} = 0 \\ \mathrm{LED2PS} = 1024/16 = 64 \\ \mathrm{LED3PS} = 2 * 1024/16 = 128 \\ \ldots\ldots \\ \mathrm{LED16PS} = 15 * 1024/16 = 960 \end{gathered}$$

PWM ON Time

The PWM on-time is configured via a 10-bit TONx register (0~1023). When TONx[9:0] = 0, the duty cycle is 0%; when TONx[9:0] = 1023, the duty cycle is 100%.

The PWM starts when charge pump is ready or when triggered via the register (configured by the register selection bits).

The PS_ON bit determines the reference edge of the PWM signal:

When PS_ON = 1, the rising edge of the PWM signal is the start point.

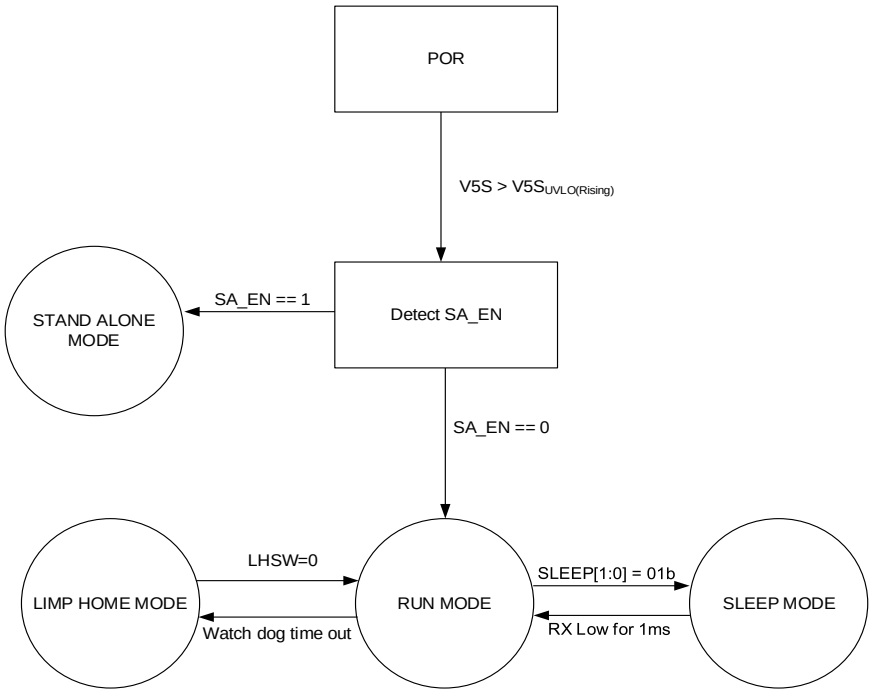
When PS_ON = 0, the falling edge of the PWM signal is the start point.

LED Parallel

The 16-ch is divided into 4-string S1(LED1-LED4), S2(LED5-LED8), S3(LED9-LED12),S4(LED13-LED16). 4-string can be paralleled by setting register PARLED[1:0].

PARLED[1:0]	Parallel type
00	All LED independent
01	S1||S2,other independent
10	S1||S2, S3||S4
11	S1||S2||S3||S4

State Machine



POR (Power of reset)

When V5S > 4.1V (rising edge of V5S UVLO threshold), the device starts and enters RUN MODE.

When V5S < 3.95V, V5S UVLO is triggered, and the device is shut down.

STAND ALONE MODE

The SA33756 defines Stand-Alone Mode (SA Mode) as a communication-free operation mode. In this mode, the LED brightness and flow lighting effect can be controlled via the FS pin. Additionally, Pin 2 is redefined as follows:

PIN	Normal Mode	Standalone Mode	Description
TX	Communication	Fault	Open-drain, active-low; OR's all channel Fault SHORT and OPEN status bits. Not latched. Faults are cleared each cycle.
FS	NA	FLOW_SEL[1:0](Register Setting)	FLOW_SEL=B00: No Flow. FLOW_SEL=B01: Input PWM Signal from FS pin control 16ch LED directly. FLOW_SEL=B10: FLOW begin when FS is high and stop when FS is low. FLOW_SEL=B11: Flow once is set when receive rising edge of FS pin.

RUN MODE

In RUN mode, the device operates normally, and its configuration is determined by the normal register (TONx/LEDxPS).

LIMP HOME MODE

In Limp-Home Mode, the configuration is stored in the Limp-Home Register. The MCU can program this configuration into the Multiple-Time Programmable (MTP) memory for persistent storage.

SLEEP MODE

The device enters Sleep Mode by writing b'01' (binary 01) to the SLEEP[1:0] register.

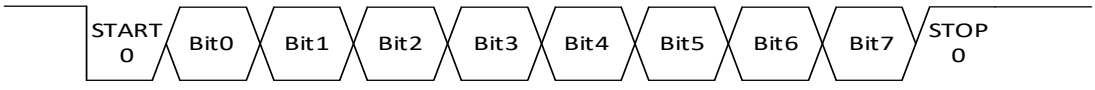
In Sleep Mode, only the analog circuit for detecting the RESET signal on RX remains active. The device exits Sleep Mode and returns to Run Mode when the MCU pulls the RX pin low for at least 1ms.

UART Interface

The MCU communicates with the SA33756 device via a Universal Asynchronous Receiver/Transmitter (UART) interface. The UART communication follows a command-response protocol, initiated by the MCU, to read and write registers and MTP memory on each device.

UART DATA Format

The UART interface uses the standard 8N1 configuration (8 data bits, no parity, 1 stop bit). The baud rate is 1 Mbps (1 million bits per second).



UART Communications Reset

Asserting the TX line low for at least 12 bit times (20 × 12 clock cycles) signifies a communication break, causing all SA33756 devices on the network to reset to a known good state. This enables them to receive the next command frame, and immediately aborts all ongoing response frames.

UART Communications time-out

The UART controller interprets a sequence of bytes as a single data frame. If the inter-byte stop time exceeds 51us (i.e., the idle period between consecutive bytes within a frame), a timeout error is triggered. Upon timeout:

- All previously received bytes in the current frame are discarded.

- The next incoming byte is treated as the start of a new frame to initiate frame recognition.

UART Communications Protocol

Write Command Frame

Write Command							
DEVID	BYTE_NUM	REG_ADDR	DATA1	……	DATAn	CRCL	CRCH

Read Command Frame

Read Command				
DEVID	BYTE_NUM	REG_ADDR	CRCL	CRCH

DEVID Frame

DEVID	Device ID & MTP							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	P[1]	P[0]	VOL	Broadcast	ADDR3	ADDR2	ADDR0_1	

- VOL Bit Functionality:
  - VOL = 1: Enables read/write operations on registers.
  - VOL = 0: Restricts access to reading MTP memory (Multiple-Time Programmable memory).
- Broadcast and Device Addressing:
  - Broadcast = 1:
  - If DEVID = 0xBF (device ID), write commands are broadcast to all devices on the bus.
  - Broadcast = 0, The device address is determined by:
    - ADDR0_1 (ADC-derived 2-bit address: ADDR0 and ADDR1).
    - ADDR2 and ADDR3 (direct pin inputs).
- ADDR0–ADDR3 Address Mapping:
  - ADDR0_1 is an analog input whose voltage is measured by the ADC (reference voltage = 1.2 V).
  - The ADC value is split into two bits (ADDR0 and ADDR1) based on predefined thresholds.
  - ADDR2 and ADDR3 are digital pins set via external resistors or logic levels.
- Parity Bit Calculation:
  - p[1] = ~(b1 ^ b3 ^ b4 ^ b5)
  - p[0] = b0 ^ b1 ^ b2 ^ b4
  - ~ = bitwise NOT
  - ^ = bitwise XOR

  These parity bits are used for error detection in command/data frames.

BYTE_NUM Frame

BYTE_NUM	Byte Number							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	P[1]	P[0]	WR	Num4	Num3	Num2	Num1	Num0

- Data Length Encoding
  - The number of bytes to be read or written is determined by the 5-bit field Num[4:0] in the command frame. The actual byte count is calculated as:
    - Byte Count = Num[4:0] + 1 (range: 1 to 32 bytes).
  - This applies to both register access and MTP memory operations.
- Read/Write Direction Control
  - The WR bit in the command frame defines the data transfer direction:
  - WR = 1: Write operation (data sent from MCU to the device).
  - WR = 0: Read operation (data sent from the device to MCU).
- Parity Bit Calculation
  - Parity bits p[1] and p[0] are used for error detection in command/data frames. Their values are computed as follows:

- p[1] = ~(b1 ^ b3 ^ b4 ^ b5)
- p[0] = b0 ^ b1 ^ b2 ^ b4
- ~ = bitwise NOT
- ^ = bitwise XOR

- These parity bits ensure data integrity during UART communication.

REG_ADDR

REG_ADDR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Register Address							

- Set the starting register address for read/write operations

ADDR0_1

- The ADDR0 and ADDR1 pins are configured based on ADC measurements of the ADDR0_1 voltage input.
  - The ADC uses a 1.2 V reference voltage (VREF). When the voltage at ADDR0_1 (VADDR0_1) is ≥ 1.2 V, the ADC reading reaches its maximum value of 1023 (assuming a 10-bit ADC resolution).

ADDR0_1 ADC READ(10bit)	ADDR1	ADDR0	Recommended Voltage
ADC<C0h	0	0	0V
C0h<ADC<180h	0	1	0.35V
180h<ADC<240h	1	0	0.58V
>240h	1	1	5V

Module	ADDR0_1 address	Min	Recommended Voltage	Max	unit
ADDR0_1	ADC Reference Voltage		1.2		V
	ADDR0_1=00b	0	0	0.222	V
	ADDR0_1=01b	0.242	0.35	0.454	V
	ADDR0_1=10b	0.474	0.58	0.685	V
	ADDR0_1=11b	0.71	5	5.5	V

Read Response Frame

Response of read command with correct CRC

Read Response					
DATA1	DATA2	……	DATAn	CRCL	CRCH

Response of read command with CRC error

- ERR_RSP_EN = 1: The device generates a fixed response of 0x55 (binary: 01010101) to the MCU after a command frame. This response does not include CRC validation (no parity/CRC check is performed).
- ERR_RSP_EN = 0: The device does not respond to any command frames (including error conditions).

(ERR_RSP_EN is a software-configurable bit in the system control register)

CRC Error Read Response(0x55)							
0	1	0	1	0	1	0	1

Write Response Frame

- ACKEN = 1: The device responds with a fixed value of 0x7F (hexadecimal, equivalent to ASCII DEL or binary 01111111) after a command frame.
- ACKEN = 0: The device suppresses all responses (no acknowledgment sent).

(ACKEN is a software-configurable bit in the control register)

Write Response(if ACKEN==1, Response is 0x7F)

0	1	1	1	1	1	1	1

Communication Clock Calibration

Communication calibration step

- Enable COMCAL_EN (write 1) before starting the communication clock calibration sequence.
- Transmit the calibration command to finalize the communication calibration operation

Communication calibration frame

Calibration Command									
CBYTE1	CBYTE2	0x55	0x55	0x55	0x55	0x55	0x55	0x55	0x55
Calibration Command		Calibration Time(8 byte 0x55)							

CBYTE1 frame

CBYTE1	Calibration Byte1							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
	~P[1]	~P[0]	1	Broadcast	ADDR3	ADDR2	ADDR1	ADDR0

- Broadcast and Device Addressing:
  - Broadcast = 1:
    - If CBYTE1==0x7F, calibration command will broadcast to all device.
  - Broadcast = 0, The device address is determined by:
    - ADDR0_1 (ADC-derived 2-bit address: ADDR0 and ADDR1).
    - ADDR2 and ADDR3 (direct pin inputs).
- ADDR0–ADDR3 Address Mapping:
  - ADDR0_1 is an analog input whose voltage is measured by the ADC (reference voltage = 1.2 V).
  - The ADC value is split into two bits (ADDR0 and ADDR1) based on predefined thresholds.
  - ADDR2 and ADDR3 are digital pins set via external resistors or logic levels.
- Parity Bit Calculation:
  - ~p[1] = b1 ^ b3 ^ b4 ^ b5
  - ~p[0] = ~(b0 ^ b1 ^ b2 ^ b4)
  - ~ = bitwise NOT
  - ^ = bitwise XOR

CBYTE2 frame

CBYTE2	Calibration Byte2								
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex
	0	1	1	1	1	0	1	0	0x7A

- This byte format is fixed at 0x7A.

Calibration Time

- Send 8 bytes of 0x55 for calibration.

Calibration Success

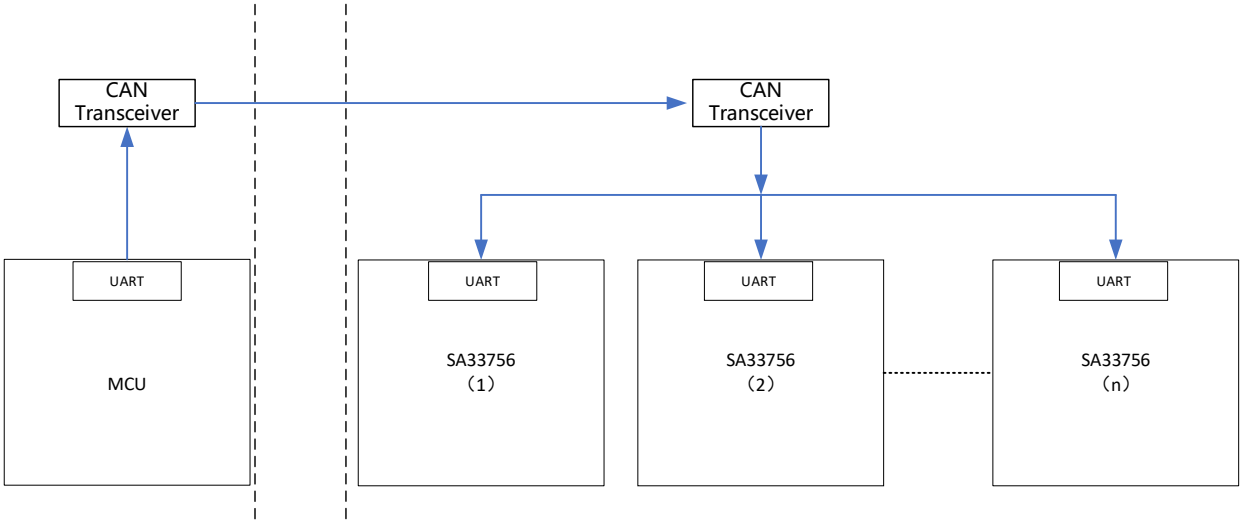
- If the calibration is successful and COMCAL_RSP_EN = 1, the slave device will return 0xA5 as an acknowledgment of successful communication calibration.
- Purpose of 0xA5: Indicates that communication timing has been calibrated and data exchange is ready.

Calibration Failure:

- If the calibration fails (e.g., the communication baud rate error between the slave and master exceeds ±6%), the slave clock parameters will remain unchanged.

Application

- MCU can send a 10-byte command via CAN/UART communication to calibrate the clock of SA33756.



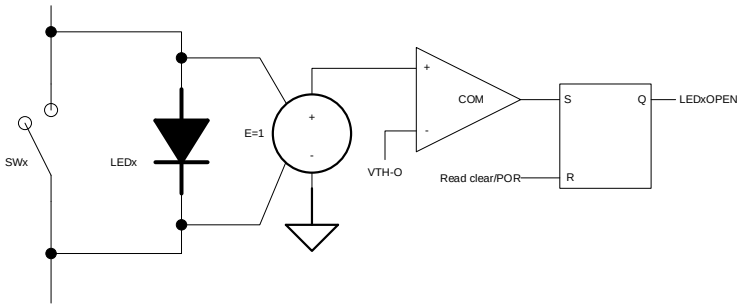
Protection

LED Open

When the PWM enable counter is activated, the switching circuit initiates operation. This delay prevents false triggering of the open-circuit LED protection mechanism during normal startup sequences.

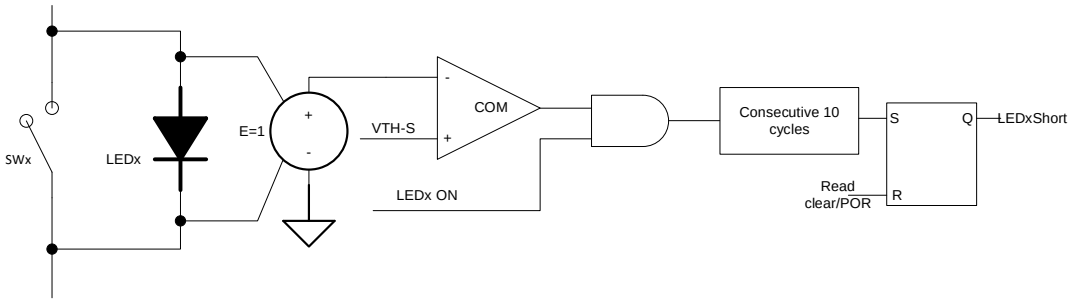
In the event of an open LED failure, an internal compactor monitors the drain-to-source voltage of the internal switch. If the voltage exceeds the threshold voltage (VTH-O), the device will turns on the switch. This action maintains current flow in the rest of the LED string in the presence of a faulty or damaged LED and protects the internal switch from electrical over stress (EOS).

- After trigger OLP, IC will short the MOS during the PWM cycle and reset at the beginning of next PWM cycle.
- LED open fault will Report in LEDxOPEN Register, when LEDxOPEN=1, that means the LEDx is open. LEDxOPEN=0, means the corresponding LED is not open. LEDxOPEN will be reset by reading corresponding LEDxOPEN register or POR.



LED Short

During the LED ON period of each PWM cycle, SA33756 monitors whether the LED voltage falls below the short-circuit threshold voltage (VTH-S). If the LED voltage remains below VTH-S for 10 consecutive cycles, a fault flag will be reported to the corresponding bit in the LEDxSHORT register. The fault flag bit can be cleared by reading the LEDxSHORT register or through a Power-On Reset (POR).



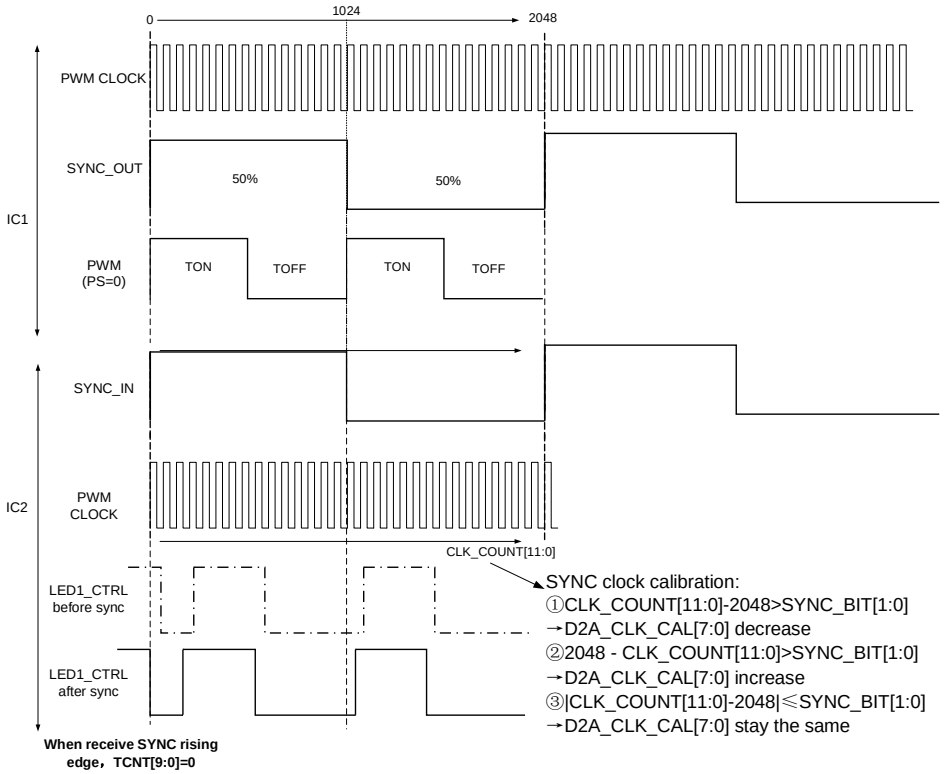
SYNC function during operation

Application

- PCB Layout:
  - Connect the SYNC pins of multiple chips on the PCB.
- Master Device Configuration:
  - Select one chip as the master to generate the SYNC signal.
  - Configuration: Set SYNC_EN=1 and SYNC_OUTPUT=1.
- Slave Device Configuration:
  - Other chips act as slaves to receive the SYNC signal.
  - Configuration: Set SYNC_EN=1 and SYNC_OUTPUT=0.
  - Function Selection:
    - Enable SYNC Calibration Clock Function: Set SYNC_CAL_EN=1.
    - Enable SYNC Synchronization Function: Set SYNC_SY_EN=1.

SYNC_EN	SYNC_OUTPUT	Function
0	0	Disable
0	1	Disable
1	0	SYNC input device
1	1	SYNC output host

- As shown in the diagram, IC1 operates as the master, while IC2 is set as the slave. The slave device enables both the SYNC calibration clock function (SYNC_CAL_EN=1) and the SYNC synchronization function (SYNC_SY_EN=1).



Software Synchronization

The TCNT counter and the PWM clock can both be reset to 0 at any time by issuing a broadcast write synchronization command, which involves writing a 1 to the SSYNC bit of the SOFTSYNC register. Due to UART bit sampling variability, synchronization is achieved within 4 OSC cycles between SA33756 devices.

ADC

The SA33756 device integrates an 8-bit analog-to-digital converter (ADC) with two multiplexed general-purpose input pins. Additionally, one of the device's address pins (ADDR1_0) is connected to the ADC input, extending the address width from 3 bits to 4 bits. This allows up to 16 SA33756 devices to be connected on a single UART bus. In this configuration, the two least significant bits (LSBs) of the device's UART address are determined by the most significant bit (MSB) of the ADC conversion result—effectively encoding part of the address through analog voltage levels. For the specific voltage ranges corresponding to each address code, please refer to the SA33756 register map documentation. Furthermore, the temperature-sensing ADC channel can be used to read the die temperature, enabling real-time monitoring of the chip's thermal status.

The two ADC channels (ADC1 and ADC2) are alternately converted during each sampling cycle, with their respective 8-bit digital results stored in the ADC1 and ADC2 registers. The ADC uses an internal 1.2 V reference voltage. The following is the calculation table for the ADC section.

ADC type	Scale	Calculation formula
ADC1	4.7mV/step	V_{ADC1}=ADC1/255*1.2
ADC2	4.7mV/step	V_{ADC2}=ADC2/255*1.2
Die Temp	1.98℃/step	Temperature=(ADC_{temp}-77.4)/0.506

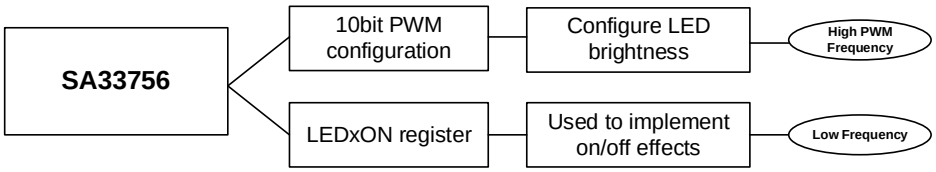
Charge Pump

To ensure that each channel's MOSFET can be controlled and to accommodate four sets of LEDs, the SA33756 device selects the highest voltage among the four LED voltages and the V5S voltage as VMAX. It then uses a charge pump circuit to boost the voltage to V_{VMAX} + 4.8V, which serves as the driving voltage to control all LEDs.

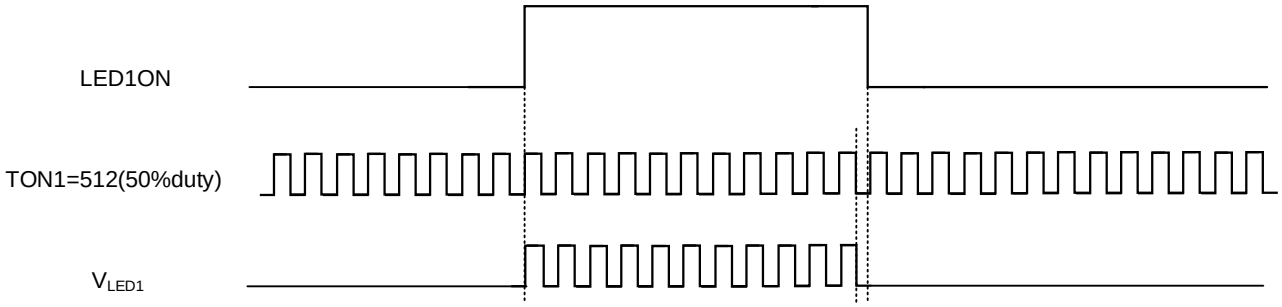
Application Description

ON OFF Mode

- Use Case: Individual LED on/off control in ADB/moving-light LED applications.
- Benefit: Simplified control and reduced communication overhead.
- Description
  - LED Brightness (PWM Duty): Controlled by the TON register (register addresses 0x1C–0x2F).
  - LED On/Off Control: Managed by the LEDON register.
- Implementation Steps
  - Enable LEDON Control:
    - Set ONOFF_EN = 1 (bit 1 of register address 0x0D).
  - Control LED On/Off:
    - Write to the 2-byte LEDON register (register addresses 0x0E–0x0F) to toggle all LEDs:
    - Write 1: Turn on LED.
    - Write 0: Turn off LED.
- Note
  - Control Logic: The LEDON and TON registers operate in a logical AND relationship:
  - If LEDON = 1, the LED follows the PWM duty cycle configured in TON.
  - If LEDON = 0, the LED remains off, regardless of the TON setting.
- Refer to the simplified block diagram below.



- The following figure shows the relationship between the actual LED control signal, LEDxON, and TONx.



FLOW Mode

- Use Case: LED flowing light.
- Benefits: A single byte can trigger a flowing sequence across 16 LEDs at once.
- Description: After power-up, configure the FLOW settings first. Once configured, writing 1 to FLOW_ONCE triggers a single flowing-light sequence.
- Configuration Steps
  - Enable Flow Mode
    - Set FLOW_EN = 1 and select the desired pattern via FLOW_SEL.
  - Set FLOW frequency
    - Configure FLOW_DIV1 and FLOW_DIV2 to define how long each LED stays lit during the flow.
    - In the context of a FLOW cycle, each LED occupies one $FLOW\_CLK_{ONOFF}$ segment. For instance, a system with 16 LEDs would require 16 consecutive $FLOW\_CLK_{ONOFF}$ segments to complete a full FLOW cycle.

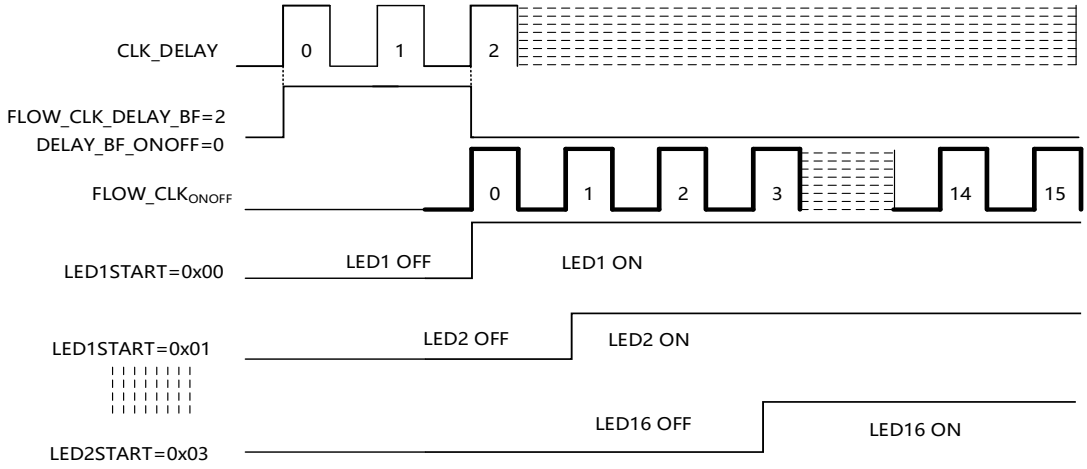
DIV_ONOFF1[1:0]	DIVISION FACTOR DIV1
0(default)	÷500k
1	÷1M
2	÷2M
3	÷NA

$$\mathrm{FLOW\_CLK_{ONOFF}} = 20\mathrm{MHz}/\mathrm{DIV\_ONOFF1}/\mathrm{DIV\_ONOFF2}$$

$$\mathrm{DIV\_ONOFF2} = \mathrm{DIV\_ONOFF2}[7:0] + 1$$

  - Multi-Chip Cascading (if needed)
    - For cascaded chips (e.g., second chip should wait until the first completes its 16-LED flow), configure the following delay
    - parameters: DELAY_BF_ONOFF, FLOW_CLK_DELAY_BF, DELAY_AF_ONOFF, FLOW_CLK_DELAY_AF
  - Customize LED Order or Usage
    - If fewer than 16 LEDs are used or a different lighting sequence is required, adjust the starting position using LEDSTART registers.
  - Trigger
    - After completing the above setup, write 1 to FLOW_ONCE to activate one complete flowing sequence.
    - For multi-chip systems, broadcast a write of 1 to FLOW_ONCE across all chips simultaneously to synchronize the entire chain's flow effect.
- Note on CON_FLOW_EN
  - When CON_FLOW_EN is enabled, the chip runs the flow continuously.
  - This mode is suitable for single-chip applications only.
  - Recommendation: Use FLOW_ONCE instead. Each write to FLOW_ONCE acts as a global synchronization pulse for all chips, ensuring perfectly aligned flowing effects across the entire chain.

- The operational specifications and configuration registers for the FLOW function are as follows:



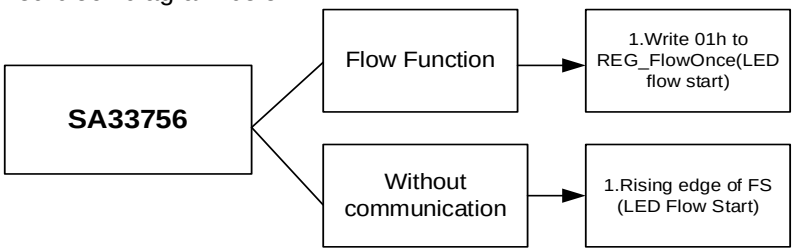
Configuration	Register Address	Description	Use for
FLOW_ONCE	0x0C[1]	If FLOW_EN =1: Write 1 to FLOW_ONCE will execute FLOW once.	Trigger flow.
CON_FLOW_EN	0x0C[0]	If FLOW_EN =1: Constant FLOW enable. 0=Disable constant FLOW. 1=Enable constant FLOW.	Constant flow.
FLOW_EN	0x0D[1]	Enable Flow function	Function Enable
FLOW_SEL	0x0D[3:2]	FLOW Function type selection. 0x0/0x3=No FLOW. 0x1=Flow light mode. 0x2= dual flashing light mode.	Select flow or dual flashing light mode
LED_NUM_SET[3:0]	0x0D[7:4]	Set the LED number in FLOW Mode LED number = LEDNUM_SET +1	Set the number of LED in use
FLOW_DIV1	0x10[7:6]	Set the frequency of FLOW clock. f_div2=FLOWDIV2+5	Set the frequency of FLOW clock.
FLOW_DIV2	0x10[7:6]	Set the frequency of FLOW clock. f_div1=20 f_div1=100 f_div1=500 f_div1=PWM period*1024	
FLOW_CLK_DELAY_BF	0x11[7]	FLOW mode delay n flow clock before flow. n=FLOW_CLK_DELAY_BF	When multiple chips are cascaded to achieve a flowing (pipeline) effect, configure the waiting time before and after the flow for each individual chip.
DELAY_BF_ONOFF	0x11[6:0]	All LED on or off before flow during delay. 0=Off. 1=On.	
FLOW_CLK_DELAY_AF	0x12[7]	FLOW mode delay n flow clock after flow. n=FLOW_CLK_DELAY_AF	
DELAY_AF_ONOFF	0x12[6:0]	All LED on or off after flow during delay. 0=Off. 1=On.	
LED<x>START	0x14-0x1B	LEDx start flow on i clock. i=LEDxSTART+1(1-16)	When LEDs are not used sequentially one by one, the flow sequence can be configured.

SA Mode

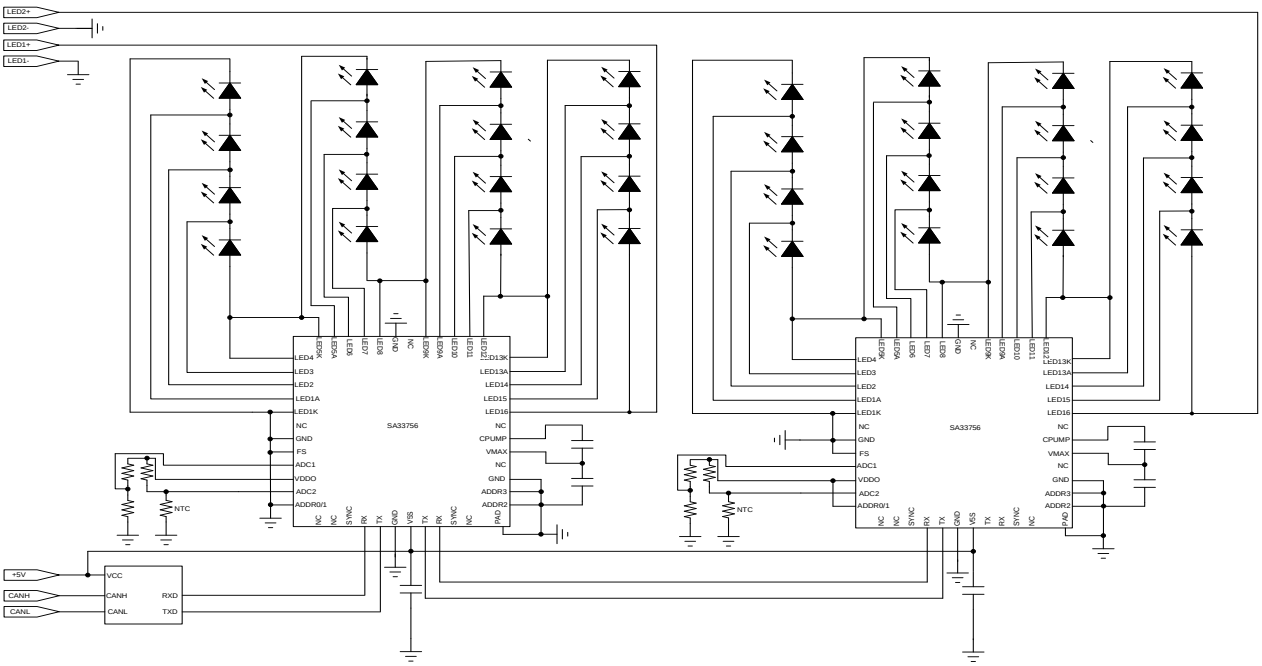
- Use Case: Controlling LED chasing (flow) or brightness without any communication interface—using only a single signal line connected to the FS pin.
- Benefits:
  - No communication protocol required.
  - Simply apply a PWM signal to the FS pin to either:
    - Trigger a flowing-light effect, or
    - Control the brightness of all LEDs simultaneously
- Description: Before shipment, configure the required parameters and store them in MTP (Memory Trim Parameter). During board-level testing or operation, control the LEDs by applying a PWM signal to the FS pin.
- Control Options via FS Signal
  - Brightness Control Mode:
    - The PWM duty cycle applied to FS directly sets the PWM duty (brightness) for all LEDs.
  - On/Off Flow Mode

- When FS = HIGH, the FLOW effect is enabled.
- When FS = LOW, the FLOW effect is disabled.

- Edge-Triggered Flow Mode:
  - Each rising edge on the FS signal triggers one complete FLOW sequence (functionally equivalent to writing 1 to FLOW_ONCE).
- Configuration Steps
  - Enter Standalone (SA) Mode.
    - Set SA_EN = 1 (bit 2 of register 0x01) and write this setting to MTP.
    - When this bit is 1, the device automatically enters SA mode after power-up.
  - Select FS Control Behavior
    - Configure the SA_FLOW register to choose how the FS signal controls the LEDs (e.g., brightness, toggle flow, or edge-triggered flow).
  - Operate via FS Pin
    - Apply the desired PWM or digital signal to FS to control LED behavior as configured.
- Note: Once SA mode is enabled, the TX pin is repurposed as a Fault output pin for error reporting (e.g., over-temperature, open/short detection).
- Refer to the simplified block diagram below.

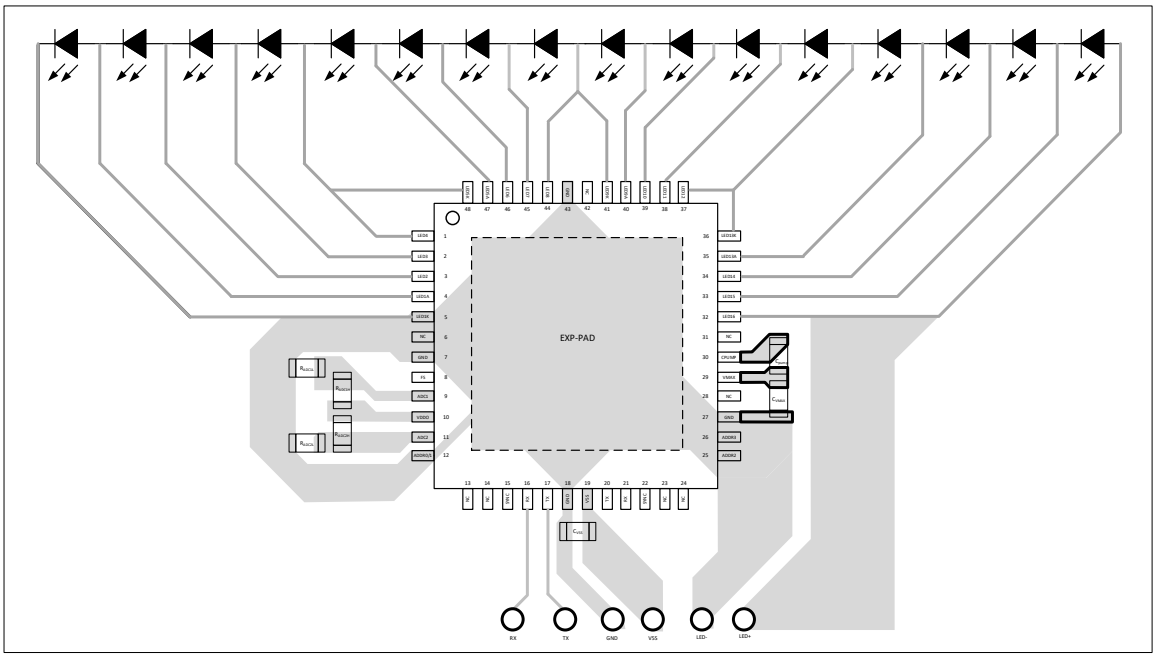


Typical Application



- The above is the application of two SA33756 devices using the same communication module, which communicate through differentiation via different device addresses (0x00 and 0x03).

Layout Application



Key Components	Parameters
C_{V5S}	100nf(or 100nf+10nf)
C_{PUMP}	10nf
C_{VMAX}	470pf-1nf
R_{ADC1H}	Use a voltage divider to ensure the ADC sampling voltage range is between 0 and 1.2V
R_{ADC2H}	
R_{ADC1L}	NTC resistor or ordinary resistor
R_{ADC2L}	

- The above are recommendations for PCB layout and parameters.

Register map

Register											
Address	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
System Configuration											
0x00	SYSCFG0	SLEEP_SEL	ACKEN	MULTI_EN	LHSW	CMWTAP[2:0]			CMWEN	R/W	0x09
0x01	SYSCFG1	SA_FLOW		RESERVE	ERR_RSP_EN	LH_SA_SAME	SA_EN	PARLED[1:0]		R/W	0x00
0x02	SYSCFG2	CAL_STOP_BIT		COMCAL_RSP_EN	COMCAL_EN	TONINVERT	PS_ON	PWM_START	START_SEL	R/W	0x07
0x03	SYSCFG3	fun_res1[2:0]			OTP_SET[1:0]		OTPEN	OPEN_EN	SHORTEN	R/W	0x03
0x04	PWMDIV	PWM_DIV1[2:0]		PWM_DIV2[5:0]						R/W	0x10
0x05	SLEW	SLEW16_13		SLEW12_9		SLEW8_5		SLEW4_1		R/W	0xFF
0x06	SYNC_CTRL	RESERVE	SYNC_BIT[2:0]			SYNC_SY_EN	SYNC_CAL_EN	SYNC_OUTPUT	SYNC_EN	R/W	0x00
0x07	RESERVE	RESERVE		fun_res2[5:0]						R/W	0x00
0x08	TWSET	TW_LIMIT[7:0]								R/W	0x90
0x09	BAUD	BAUD_PW[3:0]				RESERVE		BAUD_DIV[1:0]		R/W	0x00
0x0A	SSYNC	RESERVE						SOFTRST[1:0]		Write Only	0x00
0x0B	SLEEP	RESERVE						SLEEP[1:0]		Write Only	0x00
LED FLOW											
0x0C	FLOW_CTRL	RESERVE						FLOW_ONCE	CON_FLOW	R/W	0x00
0x0D	FLOW_SET	LED_NUM_SET[3:0]				FLOW_SEL[1:0]		ONOFF_EN	FLOW_EN	R/W	0xF0
0x0E	LEDONOFF	LED8ON	LED7ON	LED6ON	LED5ON	LED4ON	LED3ON	LED2ON	LED1OLEN	R/W	0xFF
0x0F	LEDONOFF	LED16ON	LED15ON	LED14ON	LED13ON	LED12ON	LED11ON	LED10ON	LED9ON	R/W	0xFF
0x10	FLOWDIV	FLOW_DIV1[1:0]		FLOW_DIV2[5:0]						R/W	0x00
0x11	DELAY	DELAY_BF_ONOFF	FLOW_CLK_BF[6:0]							R/W	0x01
0x12	DELAY	DELAY_AF_ONOFF	FLOW_CLK_DELAY_AF[6:0]							R/W	0x00
0x13	RESERVE	RESERVE								R/W	0x00
0x14	LEDSTART	LED2START[3:0]				LED1START[3:0]				R/W	0x10
0x15	LEDSTART	LED4START[3:0]				LED3START[3:0]				R/W	0x32
0x16	LEDSTART	LED6START[3:0]				LED5START[3:0]				R/W	0x54
0x17	LEDSTART	LED8START[3:0]				LED7START[3:0]				R/W	0x76
0x18	LEDSTART	LED10START[3:0]				LED9START[3:0]				R/W	0x98
0x19	LEDSTART	LED12START[3:0]				LED11START[3:0]				R/W	0xBA
0x1A	LEDSTART	LED14START[3:0]				LED13START[3:0]				R/W	0xDC
0x1B	LEDSTART	LED16START[3:0]				LED15START[3:0]				R/W	0xFE
LED Control											
0x1C	TON1	TON1[9:2]								R/W	0x00
0x1D	TON2	TON2[9:2]								R/W	0x00
0x1E	TON3	TON3[9:2]								R/W	0x00
0x1F	TON4	TON4[9:2]								R/W	0x00
0x20	TON1_4	TON4[1:0]		TON3[1:0]		TON2[1:0]		TON1[1:0]		R/W	0x00
0x21	TON5	TON5[9:2]								R/W	0x00
0x22	TON6	TON6[9:2]								R/W	0x00
0x23	TON7	TON7[9:2]								R/W	0x00
0x24	TON8	TON8[9:2]								R/W	0x00
0x25	TON5_8	TON8[1:0]		TON7[1:0]		TON6[1:0]		TON5[1:0]		R/W	0x00
0x26	TON9	TON9[9:2]								R/W	0x00

0x27	TON10	TON10[9:2]						R/W	0x00
0x28	TON11	TON11[9:2]						R/W	0x00
0x29	TON12	TON12[9:2]						R/W	0x00
0x2A	TON9_12	TON12[1:0]		TON11[1:0]		TON10[1:0]	TON9[1:0]	R/W	0x00
0x2B	TON13	TON13[9:2]						R/W	0x00
0x2C	TON14	TON14[9:2]						R/W	0x00
0x2D	TON15	TON15[9:2]						R/W	0x00
0x2E	TON16	TON16[9:2]						R/W	0x00
0x2F	TON13_16	TON16[1:0]		TON15[1:0]		TON14[1:0]	TON13[1:0]	R/W	0x00
0x30	PS1	LED1PS						R/W	0x00
0x31	PS2	LED2PS						R/W	0x10
0x32	PS3	LED3PS						R/W	0x20
0x33	PS4	LED4PS						R/W	0x30
0x34	PS1_4	LED4PS		LED3PS		LED2PS	LED1PS	R/W	0x00
0x35	PS5	LED5PS						R/W	0x40
0x36	PS6	LED6PS						R/W	0x50
0x37	PS7	LED7PS						R/W	0x60
0x38	PS8	LED8PS						R/W	0x70
0x39	PS5_8	LED8PS		LED7PS		LED6PS	LED5PS	R/W	0x00
0x3A	PS9	LED9PS						R/W	0x80
0x3B	PS10	LED10PS						R/W	0x90
0x3C	PS11	LED11PS						R/W	0xA0
0x3D	PS12	LED12PS						R/W	0xB0
0x3E	PS9_12	LED12PS		LED11PS		LED10PS	LED9PS	R/W	0x00
0x3F	PS13	LED13PS						R/W	0xC0
0x40	PS14	LED14PS						R/W	0xD0
0x41	PS15	LED15PS						R/W	0xE0
0x42	PS16	LED16PS						R/W	0xF0
0x43	PS13_16	LED16PS		LED15PS		LED14PS	LED13PS	R/W	0x00
LIMP HOME CONFIG									
0x44	LH_CONFIG	RESERVE	LH_TONSEL	RESERVE	LHFLOW_EN	LH_PS_SEL	LH_FLOW_SEL[1:0]	R/W	0x00
0x45	LHTON	LHTON1[9:2]						R/W	0x00
0x46	LHTON	LHTON2[9:2]						R/W	0x00
0x47	LHTON	LHTON3[9:2]						R/W	0x00
0x48	LHTON	LHTON4[9:2]						R/W	0x00
0x49	LHTON	LHTON4[1:0]		LHTON3[1:0]		LHTON2[1:0]	LHTON1[1:0]	R/W	0x00
0x4A	LHTON	LHTON5[9:2]						R/W	0x00
0x4B	LHTON	LHTON6[9:2]						R/W	0x00
0x4C	LHTON	LHTON7[9:2]						R/W	0x00
0x4D	LHTON	LHTON8[9:2]						R/W	0x00
0x4E	LHTON	LHTON8[1:0]		LHTON7[1:0]		LHTON6[1:0]	LHTON5[1:0]	R/W	0x00
0x4F	LHTON	LHTON9[9:2]						R/W	0x00
0x50	LHTON	LHTON10[9:2]						R/W	0x00
0x51	LHTON	LHTON11[9:2]						R/W	0x00
0x52	LHTON	LHTON12[9:2]						R/W	0x00
0x53	LHTON	LHTON12[1:0]		LHTON11[1:0]		LHTON10[1:0]	LHTON9[1:0]	R/W	0x00
0x54	LHTON	LHTON13[9:2]						R/W	0x00
0x55	LHTON	LHTON14[9:2]						R/W	0x00
0x56	LHTON	LHTON15[9:2]						R/W	0x00
0x57	LHTON	LHTON16[9:2]						R/W	0x00

0x58	LHTON	LHTON16[1:0]		LHTON15[1:0]		LHTON14[1:0]		LHTON13[1:0]		R/W	0x00
Read and Report											
0x59	STATUS1	CSERR	TW	CECOUNT[2:0]			RESERVE	OTP	LED_FAULT	ReadClear	n/a
0x5A	STATUS2							ECC_WARNING	ECC_ERR	ReadClear	n/a
0x5B	ADC1	ADC1[9:2]								ReadOnly	n/a
0x5C	ADC2	ADC2[9:2]								ReadOnly	n/a
0x5D	TEMP	TEMP[9:2]								ReadOnly	n/a
0x5E	ADC	ADDR1	ADDR0	TEMP[1:0]		ADC2[1:0]		ADC1[1:0]		ReadOnly	n/a
0x5F	LEDOPEN	LED8OPEN	LED7OPEN	LED6OPEN	LED5OPEN	LED4OPEN	LED3OPEN	LED2OPEN	LED1OPEN	ReadClear	n/a
0x60	LEDOPEN	LED16OPEN	LED15OPEN	LED14OPEN	LED13OPEN	LED12OPEN	LED11OPEN	LED10OPEN	LED9OPEN	ReadClear	n/a
0x61	LEDSHORT	LED8SHORT	LED7SHORT	LED6SHORT	LED5SHORT	LED4SHORT	LED3SHORT	LED2SHORT	LED1SHORT	ReadClear	n/a
0x62	LEDSHORT	LED16SHORT	LED15SHORT	LED14SHORT	LED13SHORT	LED12SHORT	LED11SHORT	LED10SHORT	LED9SHORT	ReadClear	n/a
0xFE	ICID	Checksum[7:0]								R	n/a
0xFF	MTP	MTP RELOAD:Password = 69h，MTP Write ALL=96h								Write Only	0x00

MTP Map

MTP Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
System Configuration											
0x00	SYSCFG0	SLEEP_SEL	ACKEN	MULTI_EN	LHSW	CMWTAP[2:0]			CMWEN	R/W	0x09
0x01	SYSCFG1	SA_FLOW		RESERVE	ERR_RSP_EN	LH_SA_SAME	SA_EN	PARLED[1:0]		R/W	0x00
0x02	SYSCFG2	CAL_STOP_BIT		COMCAL_RSP_EN	COMCAL_EN	TONINVERT	PS_ON	PWM_START	START_SEL	R/W	0x07
0x03	SYSCFG3	fun_res1[2:0]			OTP_SET[1:0]		OTPEN	OPEN_EN	SHORTEN	R/W	0x03
0x04	PWMDIV	PWM_DIV1[2:0]		PWM_DIV2[5:0]						R/W	0x10
0x05	SLEW	SLEW16_13		SLEW12_9		SLEW8_5		SLEW4_1		R/W	0xFF
0x06	SYNC_CTRL	RESERVE	SYNC_BIT[2:0]			SYNC_SY_EN	SYNC_CAL_EN	SYNC_OUTPUT	SYNC_EN	R/W	0x00
0x07	RESERVE	RESERVE		fun_res2[5:0]						R/W	0x00
0x08	TWSET	TW_LIMIT[7:0]								R/W	0x90
0x09	BAUD	BAUD_PW[3:0]				RESERVE		BAUD_DIV[1:0]		R/W	0x00
LED FLOW											
0x0C	FLOW_CTRL	RESERVE						FLOW_ONCE	CON_FLOW	R/W	0x00
0x0D	FLOW_SET	LED_NUM_SET[3:0]				FLOW_SEL[1:0]		ONOFF_EN	FLOW_EN	R/W	0xF0
0x0E	LEDONOFF	LED8ON	LED7ON	LED6ON	LED5ON	LED4ON	LED3ON	LED2ON	LED1ON	R/W	0xFF
0x0F	LEDONOFF	LED16ON	LED15ON	LED14ON	LED13ON	LED12ON	LED11ON	LED10ON	LED9ON	R/W	0xFF
0x10	FLOWDIV	FLOW_DIV1[1:0]		FLOW_DIV2[5:0]						R/W	0x00
0x11	DELAY	DELAY_BF_ONOFF	FLOW_CLK_DELAY_BF[6:0]							R/W	0x01
0x12	DELAYFLOW	DELAY_AF_ONOFF	FLOW_CLK_DELAY_AF[6:0]							R/W	0x00
0x13	DELAYFLOW	RESERVE								R/W	0x00
0x14	LEDSTART	LED2START[3:0]				LED1START[3:0]				R/W	0x10
0x15	LEDSTART	LED4START[3:0]				LED3START[3:0]				R/W	0x32
0x16	LEDSTART	LED6START[3:0]				LED5START[3:0]				R/W	0x54
0x17	LEDSTART	LED8START[3:0]				LED7START[3:0]				R/W	0x76
0x18	LEDSTART	LED10START[3:0]				LED9START[3:0]				R/W	0x98
0x19	LEDSTART	LED12START[3:0]				LED11START[3:0]				R/W	0xBA
0x1A	LEDSTART	LED14START[3:0]				LED13START[3:0]				R/W	0xDC
0x1B	LEDSTART	LED16START[3:0]				LED15START[3:0]				R/W	0xFE
LED Control											
0x1C	TON1	TON1[9:2]								R/W	0x00

0x1D	TON2	TON2[9:2]				R/W	0x00
0x1E	TON3	TON3[9:2]				R/W	0x00
0x1F	TON4	TON4[9:2]				R/W	0x00
0x20	TON1_4	TON4[1:0]	TON3[1:0]	TON2[1:0]	TON1[1:0]	R/W	0x00
0x21	TON5	TON5[9:2]				R/W	0x00
0x22	TON6	TON6[9:2]				R/W	0x00
0x23	TON7	TON7[9:2]				R/W	0x00
0x24	TON8	TON8[9:2]				R/W	0x00
0x25	TON5_8	TON8[1:0]	TON7[1:0]	TON6[1:0]	TON5[1:0]	R/W	0x00
0x26	TON9	TON9[9:2]				R/W	0x00
0x27	TON10	TON10[9:2]				R/W	0x00
0x28	TON11	TON11[9:2]				R/W	0x00
0x29	TON12	TON12[9:2]				R/W	0x00
0x2A	TON9_12	TON12[1:0]	TON11[1:0]	TON10[1:0]	TON9[1:0]	R/W	0x00
0x2B	TON13	TON13[9:2]				R/W	0x00
0x2C	TON14	TON14[9:2]				R/W	0x00
0x2D	TON15	TON15[9:2]				R/W	0x00
0x2E	TON16	TON16[9:2]				R/W	0x00
0x2F	TON13_16	TON16[1:0]	TON15[1:0]	TON14[1:0]	TON13[1:0]	R/W	0x00
0x30	PS1	LED1PS				R/W	0x00
0x31	PS2	LED2PS				R/W	0x10
0x32	PS3	LED3PS				R/W	0x20
0x33	PS4	LED4PS				R/W	0x30
0x34	PS1_4	LED4PS	LED3PS	LED2PS	LED1PS	R/W	0x00
0x35	PS5	LED5PS				R/W	0x40
0x36	PS6	LED6PS				R/W	0x50
0x37	PS7	LED7PS				R/W	0x60
0x38	PS8	LED8PS				R/W	0x70
0x39	PS5_8	LED8PS	LED7PS	LED6PS	LED5PS	R/W	0x00
0x3A	PS9	LED9PS				R/W	0x80
0x3B	PS10	LED10PS				R/W	0x90
0x3C	PS11	LED11PS				R/W	0xA0
0x3D	PS12	LED12PS				R/W	0xB0
0x3E	PS9_12	LED12PS	LED11PS	LED10PS	LED9PS	R/W	0x00
0x3F	PS13	LED13PS				R/W	0xC0
0x40	PS14	LED14PS				R/W	0xD0
0x41	PS15	LED15PS				R/W	0xE0
0x42	PS16	LED16PS				R/W	0xF0
0x43	PS13_16	LED16PS	LED15PS	LED14PS	LED13PS	R/W	0x00
LIMP HOME CONFIG							
0x44	LH_CONFIG	RESERVE	LH_TONSEL	RESERVE	LH_FLOW_SEL[1:0]	R/W	0x00
0x45	LHTON	LHTON1[9:2]				R/W	0x00
0x46	LHTON	LHTON2[9:2]				R/W	0x00
0x47	LHTON	LHTON3[9:2]				R/W	0x00
0x48	LHTON	LHTON4[9:2]				R/W	0x00
0x49	LHTON	LHTON4[1:0]	LHTON3[1:0]	LHTON2[1:0]	LHTON1[1:0]	R/W	0x00
0x4A	LHTON	LHTON5[9:2]				R/W	0x00

0x4B	LHTON	LHTON6[9:2]				R/W	0x00
0x4C	LHTON	LHTON7[9:2]				R/W	0x00
0x4D	LHTON	LHTON8[9:2]				R/W	0x00
0x4E	LHTON	LHTON8[1:0]	LHTON7[1:0]	LHTON6[1:0]	LHTON5[1:0]	R/W	0x00
0x4F	LHTON	LHTON9[9:2]				R/W	0x00
0x50	LHTON	LHTON10[9:2]				R/W	0x00
0x51	LHTON	LHTON11[9:2]				R/W	0x00
0x52	LHTON	LHTON12[9:2]				R/W	0x00
0x53	LHTON	LHTON12[1:0]	LHTON11[1:0]	LHTON10[1:0]	LHTON9[1:0]	R/W	0x00
0x54	LHTON	LHTON13[9:2]				R/W	0x00
0x55	LHTON	LHTON14[9:2]				R/W	0x00
0x56	LHTON	LHTON15[9:2]				R/W	0x00
0x57	LHTON	LHTON16[9:2]				R/W	0x00
0x58	LHTON	LHTON16[1:0]	LHTON15[1:0]	LHTON14[1:0]	LHTON13[1:0]	R/W	0x00

Register Description

Register Address: 0x00				
Bit	Field	Type	Reset	Description
0	CMWEN	R/W	0x1	Communication watch dog enable. 0=Disable 1=Enable
3-1	CMWTAP	R/W	0x4	Watchdog timeout time: 0=65ms 1=131ms 2=262ms 3=524ms 4=1048ms 5=2097ms 6=4194ms 7=8388ms
4	LHSW	R/W	0x0	Limp home switch. 0=not in Limp Home Mode 1=in Limp Home Mode
5	MULTI_EN	R/W	0x0	0=Single chip application 1=Application for multiple chips.
6	ACKEN	R/W	0x0	Write command acknowledge enable. 0=Disable 1=Enable
7	SLEEP_SEL	R/W	0x0	0=Internal clock will close in SLEEP Mode 1=Internal clock will not close in SLEEP Mode

Register Address: 0x01				
Bit	Field	Type	Reset	Description

1-0	PARLED	R/W	0x0	Communication watch dog enable. 0=Disable 1=Enable
2	SA_EN	R/W	0x0	MTP Value:1=Enter Stand Alone Mode MTP Value:0=Normal Mode
3	LH_SA_SAME	R/W	0x0	0=TX pin will not change in Limp Home Mode. 1=TX pin will be set as Fault pin in Limp Home Mode.
4	ERR_RSP_EN	R/W	0x0	0=No response when receive error CRC or Parity check. 1=Device will send 0x55 when receive error CRC or Parity check.
7-6	SA_FLOW	R/W	0x0	FLOW Set in Stand Alone Mode. FS Pin is set as input to control LED. 0x0=No flow. 0x1=Input of FS pin control the ton and toff directly for all LED. 0x2=Input of FS pin control the FLOW on and off(High level-Constant Flow). ①Input of FS pin is high: FLOW on. ②Input of FS pin is high: FLOW off. 0x3=Input of FS pin control the FLOW on and off.(Rising Edge trigger-Flow Once) FLOW Once is triggered when receive rising edge.

Register Address: 0x02				
Bit	Field	Type	Reset	Description
0	START_SEL	R/W	0x1	0=LED Control is begin when Charge Pump is ready.(Controlled automatically) 1=LED Control is begin when PWM_START==1.(Controlled by register)
1	PWM_START	R/W	0x1	If START_SEL=1: 0=LED PWM Control stop. 1=LED PWM Control start. If START_SEL=0: This bit does not work.
2	PS_ON	R/W	0x1	Phase shift LED ON 0=LED phase shifts apply to LED turn-off times. 1=LED phase shifts apply to LED turn-on times.
3	TONINVERT	R/W	0x0	0=LEDxOn register set the ton duty of LEDx. 1=LEDxOn register set the toff duty of LEDx.
4	COMCAL_EN	R/W	0x0	Communication clock calibration enable. 0=Disable communication calibration. 1=Enable communication calibration.

5	COMCAL_RSP_EN	R/W	0x0	Communication clock calibration response enable. 0=There is no response when receive a correct communication clock calibration command. 1=0xA5 will be response when receive a correct communication clock calibration command.
7--6	CAL_STOP_BIT	R/W	0x0	Communication clock calibration stop bit number. （Only for communication clock calibration） 0= 1 bit stop bit. 1= 1.5 bit stop bit. 2= 2 bits top bit. 3= 1 bit stop bit.

Register Address: 0x03				
Bit	Field	Type	Reset	Description
0	SHORTEN	R/W	0x1	LED Short report enable. 0=Disable. 1=Enable.
1	OPEN_EN	R/W	0x1	LED open protection enable. 0=Disable. 1=Enable.
2	OTPEN	R/W	0x0	LED Short protection enable.(Error report is enable all the way) 0=Disable protection. But OTP flag will be reported. 1=All LED ON as duty 100% when OTP is triggered.
4-3	OTP_SET[1:0]	R/W	0x1	Set the temperature for OTP protection. 0=160℃ 1=165℃ 2=170℃ 3=175℃

Register Address: 0x04				
Bit	Field	Type	Reset	Description
5-0	PWM_DIV2	R/W	0x10	LED PWM frequency = 20Mhz/(div1×div2×1024) div2=PWM_DIV2+4 PWM_DIV1: 0=div1 is 1(default) 1=div1 is 50 2=div1 is 125 3=div1 is 200
7-6	PWM_DIV1	R/W	0x0	

Register Address: 0x05				
Bit	Field	Type	Reset	Description
1-0	SLEW4_1	R/W	0x3	Set slew rate of switch. For example: SLEW4_1 set slew rate of switch(LED) 1,2,3,4. 0=0.075V/us 1=0.25V/us
3-2	SLEW8_5	R/W	0x3	
5-4	SLEW12_9	R/W	0x3	
7-6	SLEW16_13	R/W	0x3	

				2=0.5V/us 3=1V/us

Register Address: 0x06				
Bit	Field	Type	Reset	Description
0	SYNC_EN	R/W	0x0	SYNC function enable. 0=Disable. 1=Enable.
1	SYNC_OUTPUT	R/W	0x0	SYNC pin as output enable. If SYNC_EN=1: 0=SYNC input enable. 1=SYNC output enable.
2	SYNC_CAL_EN	R/W	0x0	SYNC clock calibration function enable. 0=Disable. 1=Enable.
3	SYNC_SY_EN	R/W	0x0	SYNC synchronization function enable. 0=Disable. 1=Enable.
6-4	SYNC_BIT[2:0]	R/W	0x0	SYNC clock calibration pause bit set. sy_bit=SYNC_BIT+1 When calibrate result - original result <= sy_bit, sync calibrate pause. It will start when opposite

Register Address: 0x08				
Bit	Field	Type	Reset	Description
7-0	TW_LMT	R/W	0x0	Thermal warning limit set. When TEMP[9:2]>TW_LMT[7:0], TW is reported high.

Register Address: 0x09				
Bit	Field	Type	Reset	Description
1-0	BAUD_DIV	R/W	0x0	Baud rate divide set. 0=Baud rate is 1M bps. 1=Baud rate is 500k bps. 2=Baud rate is 250k bps. 3=Baud rate is 125k bps.
7-4	BAUD_PW	R/W	0x0	Baud setting password. BAUD_DIV is active when BAUD_PW=0x5. Otherwise, baud rate is 1M bps.

Register Address: 0x0A				
Bit	Field	Type	Reset	Description

1-0	SOFTRST	Write Only	0x0	LED PWM reset when is written 0x01 to the register. Only 0x01 is active for soft reset. This bit is write only bit.

Register Address: 0x0B				
Bit	Field	Type	Reset	Description
1-0	SLEEP	Write Only	0x0	Device enter SLEEP MODE when 0x01 is written to the register. Device exit SLEEP MODE by pull down RX Pin for 600us. This bit is write only bit.

Register Address: 0x0C				
Bit	Field	Type	Reset	Description
0	CON_FLOW	R/W	0x0	If FLOW_EN =1: Constant FLOW enable. 0=Disable constant FLOW. 1=Enable constant FLOW.
1	FLOW_ONCE	Write Only	0x0	If FLOW_EN =1: Write 1 to FLOW_ONCE will execute FLOW once.

Register Address: 0x0D				
Bit	Field	Type	Reset	Description
0	FLOW_EN	R/W	0x0	FLOW function enable. 0=Disable. 1=Enable.
1	ONOFF_EN	R/W	0x0	Enable modification for register 0x0E&0x0F. 0=Disable 1=Enable
2	FLOW_SEL	R/W	0x0	FLOW Function type selection. 0/3= No use. 1= Flow light mode. 2= Dual flashing light mode.
3	LEDNUM_SET	R/W	0xF	Set the LED number in FLOW Mode LED number = LEDNUM_SET +1

Register Address: 0x0E&0x0F				
Bit	Field	Type	Reset	Description
-	LEDxON	R/W	0x1	LEDx on and off control. LEDxON can be modify only when ONOFF_EN=1. 0=LEDx off all the time. 1=LEDx on and off control by TONx.

Register Address: 0x10

Bit	Field	Type	Reset	Description
Frequency of FLOW CLK=20MHz/(f_div1×f_div2)				
5-0	FLOW_DIV2	R/W	0x0	Set the frequency of FLOW clock. f_div2=FLOWDIV2+5
7-6	FLOW_DIV1	R/W	0x0	Set the frequency of FLOW clock. 0=f_div1 is 20 1=f_div1 is 100 2=f_div1 is 500 3=f_div1 is PWM period*1024

Register Address: 0x0C				
Bit	Field	Type	Reset	Description
0	FLOW_CLK_DELAY_BF	R/W	0x0	FLOW mode delay n flow clock before flow. n=FLOW_CLK_DELAY_BF
1	DELAY_BF_ONOFF	R/W	0x0	All LED on or off before flow during delay. 0=Off. 1=On.

Register Address: 0x0D				
Bit	Field	Type	Reset	Description
0	FLOW_CLK_DELAY_AF	R/W	0x0	FLOW mode delay n flow clock after flow. n=FLOW_CLK_DELAY_AF
1	DELAY_AF_ONOFF	R/W	0x0	All LED on or off after flow during delay. 0=Off. 1=On.

Register Address: 0x13-0x1B				
Bit	Field	Type	Reset	Description
[3:0]	LEDxSTART	R/W	-	LEDx start flow on i clock. i=LEDxSTART+1(1-16)

Register Address: 0x1C-0x2F				
Bit	Field	Type	Reset	Description
[9:0]	TONx	R/W	0x00	Set LEDx PWM duty. LEDx_duty = TONx/1024 if TONx=1023,LEDx_duty will be set to 100%

Register Address: 0x30-0x43				
Bit	Field	Type	Reset	Description
[9:0]	PSx	R/W	0x00	Set LEDx PWM phase shift.

Register Address: 0x44				
Bit	Field	Type	Reset	Description
0	LH_FLOW_SEL	R/W	0x0	FLOW function enable. 0=Disable. 1=Enable.
1	LH_PS_SEL	R/W	0x0	Phase shift set. 0=Phase shift is set as LED1-0x00,LED2-0x10,LED3-0x20,etc. 1=Phase shift is same to NORMAL MODE.
2	LHFLOW_EN	R/W	0x0	FLOW function enable in LIMP HOME MODE. 0=Disable. 1=Enable.

Register Address: 0x45-0x58				
Bit	Field	Type	Reset	Description
[9:0]	LHTONx	R/W	0x00	Set LEDx PWM duty in LIMP HOME MODE. LEDx_duty = LHTONx/1024 if LHTONx=1023,LEDx_duty will be set to 100%

Register Address: 0x59				
Bit	Field	Type	Reset	Description
0	LED_FAULT	Read Clear	-	LED_FAULT=OR(LEDxOPEN,LEDxSHORT)
1	OTP	Read Clear	-	Over temperature protection report.
5-3	CECOUNT	Read Clear	-	CRC error count.
6	TW	Read Clear	-	Thermal warning. When TEMP[9:2]>TW_LMT[7:0], TW is reported high.
7	CSERR	Read Clear	-	Check sum error report.

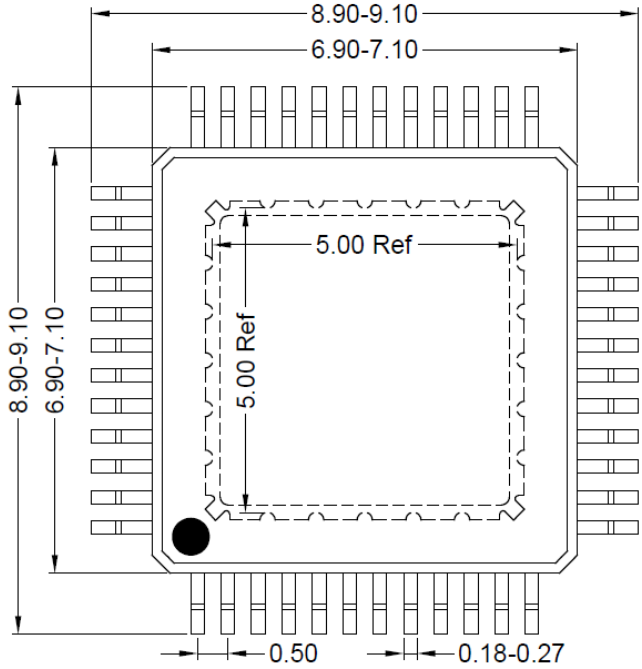
Register Address: 0x5B-0x5E				
Bit	Field	Type	Reset	Description
[7:0]	ADC1	Read Only	-	V_{ADC1}=ADC1/255*1.2
[7:0]	ADC2	Read Only	-	V_{ADC2}=ADC2/255*1.2
[7:0]	TEMP	Read Only	-	Temperature=(ADC_{temp}-77.4)/0.506
-	ADDR0	Read Only	-	ADDR0 address number(0/1) from input of ADDR0_1
-	ADDR1	Read Only	-	ADDR1 address number(0/1) from input of ADDR0_1

Register Address: 0x5F-0x62				
Bit	Field	Type	Reset	Description
-	LEDxOPEN	Read Only	-	LEDx open protection report.
-	LEDxSHORT	Read Only	-	LEDx short protection report.

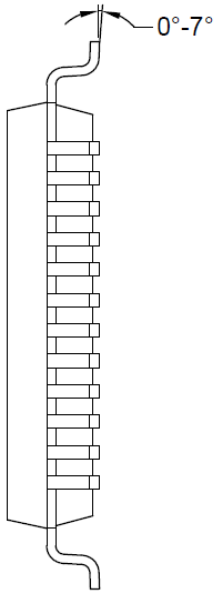
Register Address: 0xFE				
Bit	Field	Type	Reset	Description
7-0	CHECKSUM	Read Only	-	Check device MTP load code.

Register Address: 0xFF				
Bit	Field	Type	Reset	Description
7-0	MTP_CTRL	Write Only	-	0x96= Write register value to MTP. 0x69=Load register value from MTP.

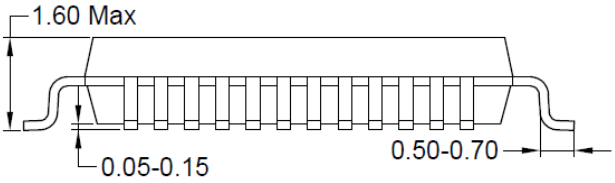
LQFP7x7-48E Package Outline Drawing



Top View



Side View

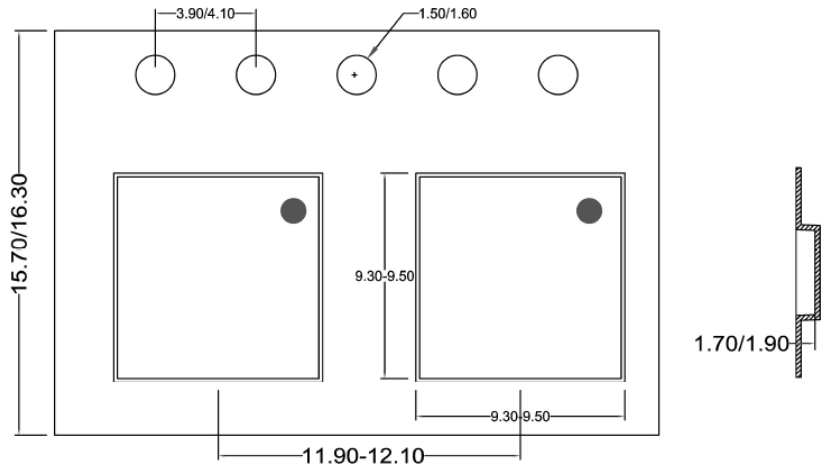


Front View

Notes: All dimension in millimeter and exclude mold flash & metal burr.

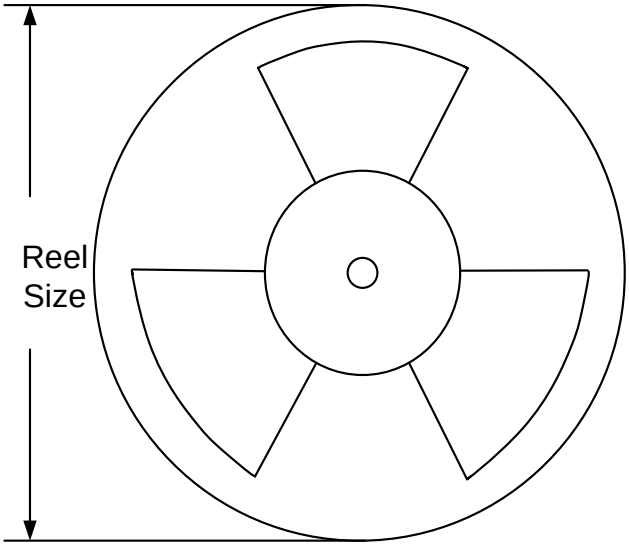
Taping & Reel Specification

1. Taping Orientation



Feeding Direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
TQFP7X7-48E	16	12	13	400	400	2000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
December 29,2025	Revision 1.0	Initial Release

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