SA33766

Dual Channel Buck Controller for Automotive Lamp

General Description

The SA33766 is a dual-channel buck controller designed for automotive LED front lighting systems, including high beams, low beams, daytime running lights, turn signals, fog lights, and static cornering illumination.

The SA33766 implements boundary control to generate two separately adjustable constant current outputs simultaneously, ensuring a rapid LED current response and high precision. This design is particularly well-suited for advanced lighting technologies, such as Adaptive Driving Beam (ADB) and flexible lighting effects.

The SA33766 supports a wide input voltage range of 4.5V to 60V, accommodating LED voltages up to 53V and LED currents up to 1.6A.

The SA33766 incorporates several fault protection features, including thermal warning, thermal shutdown, SPI error detection, short-circuit protection, and open-circuit LED protection.

In the event of a communication failure, the chip will automatically switch to limp-home mode to ensure normal system operation.

Features

- Input Voltage Range from 4.5V to 60V.
- Independent Dual Channel Constant Current Buck Converter.
- ILED up to 1.6A
- Support 10 Bits Analog Dimming and Internal or External PWM Dimming
- Support LED Voltage from 0V-57V
- AEC-Q100 Grade 1 Qualified
- SPI Communication Interface
- Stand-alone Mode, Limp-home Mode, Run Mode, Sleep Mode are Available.
- ±3% Current Accuracy at 1.6A
- Short LED, Open LED, Thermal Shut down Protection
- Fast LED Current Response
- Operating Ambient Temperature Range of −40 °C to +125 °C
- Package TSSOP32E-UP

Applications

- High Beam
- Low Beam
- DRL
- Position or Park Light
- Turn Indicator
- Fog Lights
- Static Cornering

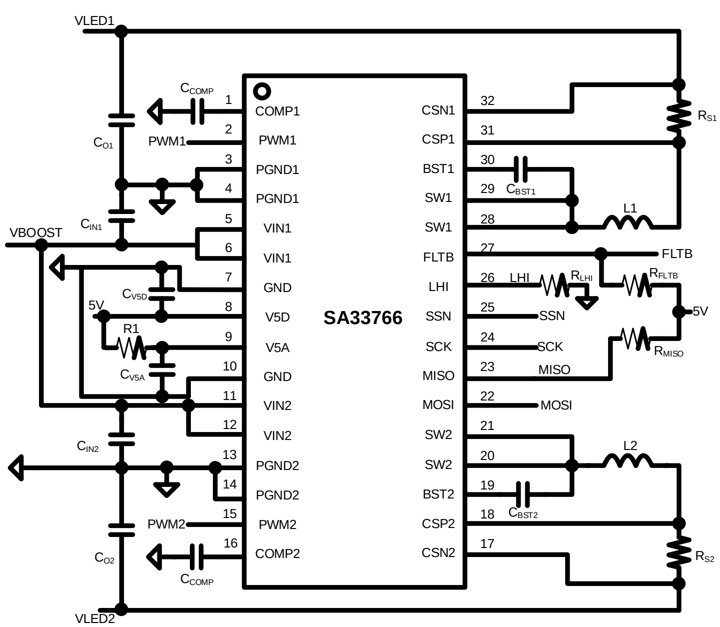
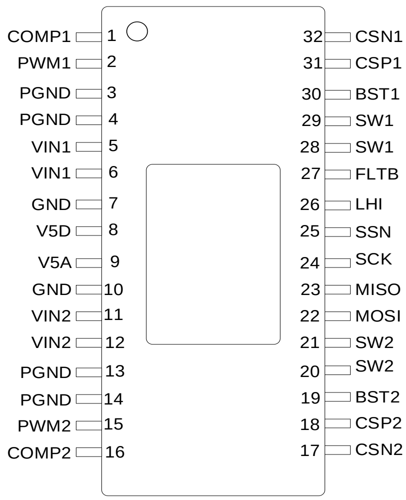


Fig. 1. Typical Application Circuit

Ordering Information

Ordering Part Number	Package type	Top Mark
SA33766IDP	TSSOP32E-UP RoHS-Compliant and Halogen-Free	**AAKDxyz**

Pinout (Top View)



Pin Description (A: Analog Pin, G: Ground Pin, P: Power Pin)

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
1	COMP1	A	Channel 1 loop compensation PIN, connect a ceramic capacitor to GND.
2	PWM1	A	Channel 1 PWM dimming signal input PIN.
3,4,13,14	PGND	G	Low side MOSFET GND PIN.
5,6	VIN1	P	Power input PIN for channel 1 high side MOSFET.
7,10	GND	G	Signal ground PIN.
8	V5D	P	IC power supply PIN, connect to external 5V supply, a MLCC is suggested from V5D to GND, for MOS driver supply
9	V5A	P	IC power supply PIN, connect to external 5V supply, a MLCC is suggested from V5A to GND, for IC analog and digital supply.
11,12	VIN2	P	Power input PIN for channel 2 high side MOSFET.
15	PWM2	A	Channel 2 PWM dimming signal input PIN.
16	COMP2	A	Channel 2 loop compensation PIN, connect a ceramic capacitor to GND.
17	CSN2	A	Channel 2 LED current sense negative PIN.
18	CSP2	A	Channel 2 LED current sense positive PIN.
19	BST2	P	Power supply for channel 2 high side MOS driver, connect a ceramic capacitor to SW2.
20,21	SW2	P	Channel 2 midpoint of high MOSFE, connect to external inductor.
22	MOSI	A	SPI slave data input.
23	MISO	A	Open-drain SPI slave data output. Connect a 4.7-kΩ resistor to V5D digital supply voltage.

24	SCK	A	SPI clock input.
25	SSN	A	SPI chip select input.
26	LHI	A	Limp-home and standalone mode LED current reference set point.
27	FLTB	A	Open-drain fault indicator. Connect to V5D with a resistor to create an active low fault signal output.
28,29	SW1	P	Channel 1 midpoint of high MOSFE, connect to external inductor.
30	BST1	P	Power supply for channel 1 high side MOS driver, connect a ceramic capacitor to SW1.
31	CSP1	A	Channel 1 LED current sense positive PIN.
32	CSN1	A	Channel 1 LED current sense negative PIN.
PAD	Thermal PAD	G	Thermal Pad is on the top of package.

Block Diagram

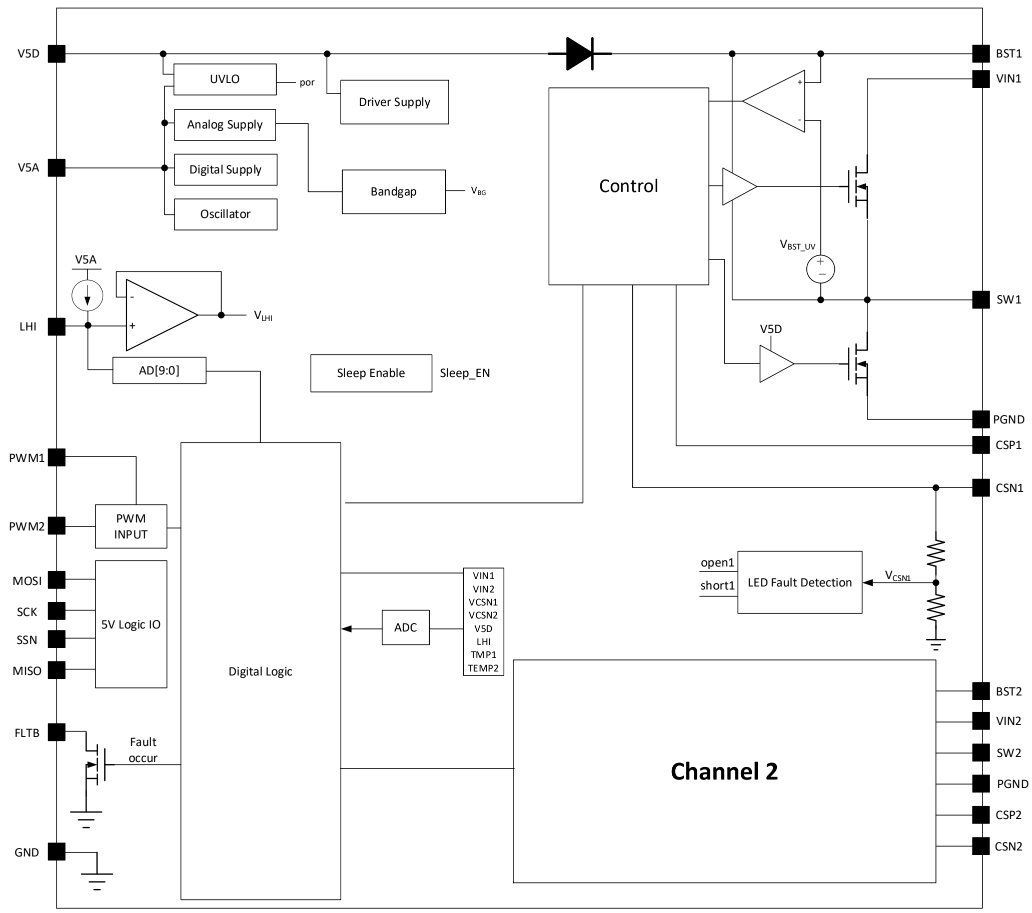


Fig.2 Block Diagram

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)

Parameter	Min	Max	Unit
BST1, BST2	-0.3	70	V
SW1,SW2,VIN1,VIN2,CSP1,CSP2,CSN1,CSN2,PWM1,PWM2	-0.3	65	V
V5A,V5D,BST1-SWN1,BST2-SWN2,LHI,SCK,SSN,MISO,FLTB,MOSI, COMP1,COMP2	-0.3	6	V
Continuous power dissipation(3)	Internally Limited		
Ambient temperature, T_A(4)	-40	125	°C
Junction temperature, T_J(4)	-40	150	°C
Maximum Lead Temperature (Soldering)		260	°C
Storage Temperature Range, T_{stg}	-65	150	°C

Stresses beyond those listed under Absolute Maximum Rating may cause permanent damage to the device. These are stress ratings only and do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to the potential at the GND pins.

Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 165°C (typical) and disengages at T_J = 150°C (typical).

In applications where high power dissipation and/or poor package thermal resistance are present, the maximum ambient temperature may need to be derated. The maximum ambient temperature (T A-MAX) is dependent on the maximum operating junction temperature (T J-MAX = 150°C), the power dissipation of the device in the application (P), the junction-to-board thermal resistance, and the temperature difference between the system board and the ambient (Δt BA). This relationship is expressed by the following equation: T A-MAX = T J-MAX – (Θ JB × P) - Δt BA.

Thermal Information

Parameter		Min	Max	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance		115.5	°C/W
$R_{\theta JC}$	Junction-to-case (top) thermal resistance		2.4	°C/W
$R_{\theta JB}$	Junction-to-Bottom thermal resistance		115.5	°C/W

(1) For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics.

Junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications with high maximum power dissipation, special attention must be given to thermal dissipation issues during board design.

ESD Ratings

Parameter		Min	Max	Unit
HBM (Human Body Mode), per AEC Q100-002(1)			±2000	V
CDM (Electrostatic Discharge Mode), per AEC Q100-011			±500	V
	Corner PIN		±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted) (1)

Parameter(Note 1)	Min	Max	Unit
VIN	4.5	60	V
V5A,V5D	4.5	5.3	V
ILED		1.6	A
T_A(Ambient Temperature)	-40	125	°C
T_J(Junction Temperature)	5	150	°C

(1) All voltages are with respect to the potential at the GND pins

Electrical Characteristics

T_J = -40°C to +125°C (unless otherwise noted) V_{INx} =12V, V5A = V5D=5V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Pin VIN	Analog Supply Stand-by Current	$I_{V5A(STBY)}$	CH1VIN[7:0]<VIN_UVLO_SET[7:0], CH2VIN[7:0]<VIN_UVLO_SET[7:0]		5	8.5	mA
	Gate Drive Supply Stand-by Current	$I_{V5D(STBY)}$	CH1VIN[7:0]<VIN_UVLO_SET[7:0], CH2VIN[7:0]<VIN_UVLO_SET[7:0]		0.3	0.7	mA
	Analog Supply Sleep State Current	$I_{V5A(SLEEP)}$			34	100	µA
	Gate Drive Supply Sleep State Current	$I_{V5D(SLEEP)}$				5	µA
	VIN Pin Sleep State Current	$I_{VINx(SLEEP)}$	VINx= 15V			5	µA
	Gate Drive Supply Switching Current	$I_{V5D(SW)}$	V5D = 5V,fsw=1MHz. CH1 and CH2 switching		3.5		mA
Supply Pin V5D AND V5A	V5A and V5D UVLO Threshold	V5A,V5D UVLO	Rising		4.2	4.38	V
			Falling	3.78	4.0		V
			Hysteresis		200		mV
High Side FET/BST and Low Side FET	High side power MOS on resistance, with R of wire	R_{dson_HS}	VINx=6V,VBSTx=11V,IHSx=100mA		300		mΩ
	BST UVLO Threshold	V_{BSTxUV}	Falling, VINx=6V,VSWx=0V		2.5		V
			Hysteresis, VINx=6V, VSWx=0V		200		mV
	BST Quiescent Current	I_{Q_BSTx}	VINx=6V, ILSx=100mA		0.4		mA
	Low Side Power MOS on Resistance, with R of Wire	R_{dson_LS}	VINx=6V, ILSx=100mA		300		mΩ
High Side Current Limit	High Side Current Limit Threshold	$I_{HSx(LIM)}$	VINx=10V		2		A
	High Side MOS Maximum ton Setting	T_{on_max}	0x09 [3:2]/[7:6]= 00		5		µS
			0x09 [3:2]/[7:6]= 01		7.4		µS
			0x09 [3:2]/[7:6]= 10		10		µS
			0x09 [3:2]/[7:6]= 11		12.8		µS
	From High Side GATE Start to Turn on to High Side GATE off	T_{on_min}			220		nS
Low Side Current Limit	Low Side Current Limit	$I_{LSx(LIM)}$	VINx=6V		0.5		A
	Low Side MOS Maximum ton Setting	T_{off_MAX}	VINx=6V		16		uS
	From Low Side GATE Start to Turn on to High Side GATE off	T_{off_min}	Vout>2.5V & 0x09 [3:2]/[7:6]= 00		208		nS
			Vout>2.5V & 0x09 [3:2]/[7:6]= 01		283		nS
			Vout>2.5V & 0x09 [3:2]/[7:6]= 10		360		nS
			Vout>2.5V & 0x09 [3:2]/[7:6]= 11		460		nS
PWM Dimming and Programmable UVLO INPUT (PWMx)	PWMx Input Threshold	V_{PWMx}	Rising		1.22		V
			Falling		1.11		V
Oscillator	V5A=V5D=5V	F_OSC			10		MHz
Current accuracy and LHI PIN	CS_REF when CHxIADJ[9:0]=1023	CS_REF		163	168	173	mV
	CS_REF when CHxIADJ[9:0]=512			79	84	89	mV
	CS_REF when CHxIADJ[9:0]=256			37	42	47	mV

	CS_REF when CHxIADJ[9:0]=128			16.5	21	25.5	mV
	Ripple when CHxRipple=255	Ripple			80		mV
	Ripple when CHxRipple=128				40		mV
	Ripple when CHxRipple=64				20		mV
	LHI Pin Output Current	I_{LHI}		9	10	11	uA
	LHI PIN Full Code Voltage	V_{LHI_Full}		1.1	1.2	1.3	V
SPI inputs: pins MOSI,SCK and SSN	High-level Input Voltage	LOG_HI				2	V
	Low-level Input Voltage	LOG_LO		0.7			V
SPI output: pins MISO	Pull down resistance	R_{pull_down}			16		Ω
Temperature Protection	Thermal Shutdown	TSD			160		℃
	TEMP_HYST	TEMP_HYST			20		℃

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied.

Note 2: θ_{JA} is measured under natural convection at T_A = 25°C, mounted on a four-layer Silergy evaluation board with referenced thermal vias.

Note 3: The device is not guaranteed to function outside its operating conditions. Internal

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions with $T_A \approx T_J$ = 25°C. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage ranges are guaranteed by design, testing, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested under equipped.

Note 6: AEC Q100-002 specifies that HBM stressing shall be conducted in accordance with the ANSI/ESDA/JEDEC JS-001 specification, including range testing.

Note 7: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown activates at T_J = 165°C (typical) and deactivates at T_J = 150°C (typical).

Note 8: All voltages are with respect to the potential at the GND pins.

Serial Peripheral Interface Timing

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Serial Peripheral Interface Timing; Pins SSN, SCK, MOSI, and MISO	Transfer Frequency					4	MHz
	Clock Cycle Time	$t_{cy(clk)}$		250		-	ns
	SPI Enable Lead Time	$t_{SPILEAD}$		300	-		
	SPI Enable Lag time	t_{SPILAG}		50	-		
	Clock HIGH Time	$t_{clk(H)}$		125	-	-	ns
	Clock LOW Time	$t_{clk(L)}$		125	-	-	ns
	Data Input Set-up Time	$t_{su(D)}$		50	-	-	ns
	Data Input Hold Time	$t_{h(D)}$		50	-	-	ns
	Data Output Valid Time	$t_{v(Q)}$	pin MISO; CL = 20pF	-	-	130	ns
	Chip Select Pulse Width HIGH	$t_{WH(S)}$		300	-	-	ns

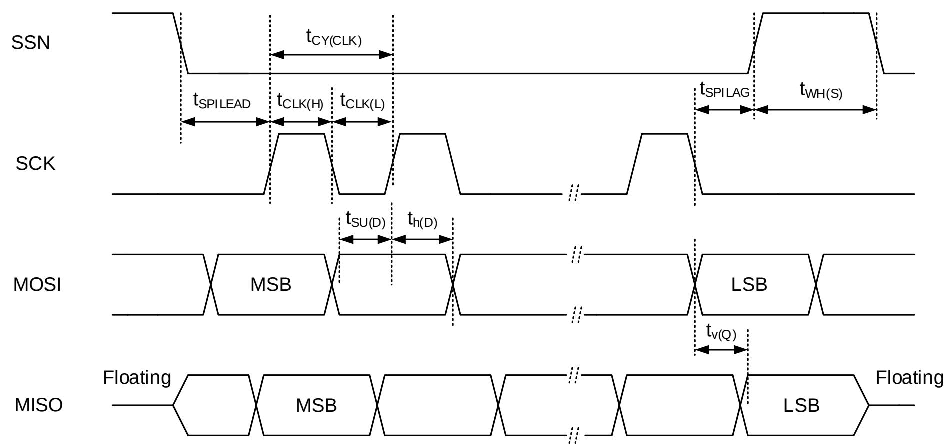


Figure 3: SPI Timing

Detailed Description

1. Over view

The SA33766 is a dual synchronous buck LED driver with an input voltage range of 4.5 V to 60 V. It can deliver up to 1.6 A of continuous current per channel to power two independent strings of one to 16 series-connected LEDs.

The device features hysteresis control, making it suitable for fast LED voltage transients. Inductor current sensing and closed-loop feedback ensure a full load current accuracy of better than ±3% across a wide range of input voltage, output voltage, and ambient temperature.

The LED current reference is set by the 10-bit IADJ DAC and is programmed through the CHxIADJ register to achieve linear analog dimming. Pulse width modulation (PWM) dimming of the LED current is accomplished by either programming the internal PWM generator or modulating the duty cycle of an external voltage signal at the PWMx pin. When enabled, the internal PWM generator determines the LED current duty cycle based on the 10-bit CHxPWM command. The external PWMx input functions as an enable signal and directly controls the LED current. This device optimizes the inductor current response and achieves a PWM dimming ratio exceeding 1000:1.

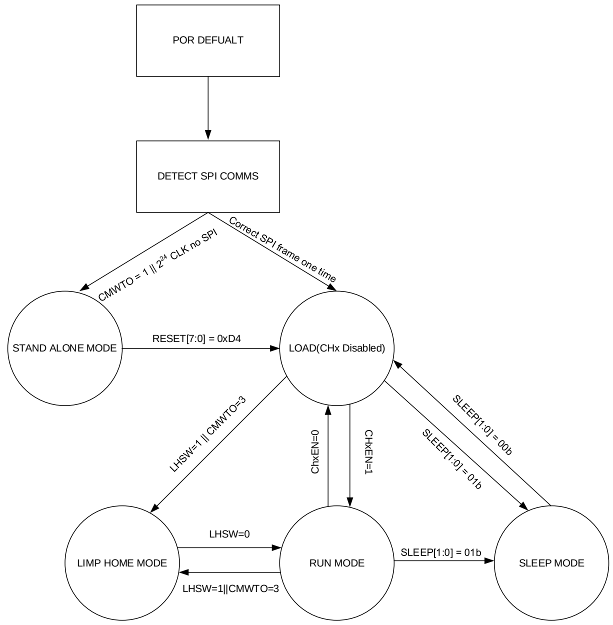
The device incorporates an enhanced programmable fault feature including the following:

- Cycle-by-cycle switch overcurrent limit
- Input undervoltage protection
- BST undervoltage protection
- Thermal warning
- LED short circuit indication

In addition, thermal shutdown (TSD) protection is implemented to limit the junction temperature to a typical value of 170°C. For each fault, there is a corresponding status register that can be easily accessed via SPI read commands.

The SA33766 includes a communication watchdog timer that enables both standalone and limp-home (LH) functionality. The watchdog timer is configured via register CMWTAP [3:0]. When enabled, the watchdog timer monitors the SPI communication during startup and normal operation. A communication failure during startup forces the device into standalone mode. In this mode, the operation of each channel is controlled by the PWMx and LHI inputs, while SPI communication is disabled. Limp-home (LH) mode is activated upon detection of a communication failure during normal operation. In LH mode, device operation is governed by the limp-home registers, which are initialized and loaded during the device startup sequence.

2. Operation mode:



2.1 Power on Reset (POR)

The device is in the Power-On Reset (POR) state when the V5A or V5D input is below the undervoltage threshold. In the POR state, all register settings are reset to their default values, and both channels are disabled. The device exits the POR state and enters functional modes when the V5A supply exceeds 4.2 V.

2.2 Detect SPI Communication

After the existing Power-On Reset (POR) state, the device waits for the correct SPI interface. If a valid SPI frame is not received within 2^{24} system clock cycles, the communication watchdog timer times out, and the device enters stand-alone mode. If a valid SPI frame is received, the IC enters load mode.

2.3 Standalone Mode

The SA33766 is designed to operate in stand-alone mode without the need for external communication. In this mode, the watchdog timer circuit is disabled, and each channel is controlled by the voltage on the LHI pin and the PWM pin. The LHI pin sets the operating current, while the PWM pin determines the operating phase. The default value for the channel current ripple is fixed at 4D. The device also defaults to auto-restart mode for all faults, with the fault timer set to a typical value of 3.3 ms. Connecting the LHI pin to GND (below the 80 mV threshold) disables both channels and turns off both outputs. If the logic is in stand-alone mode, writing 0x32:D4 returns the LOAD state.

2.4 Load Mode

The load mode is an intermediate state; it is not necessary to configure this mode specifically, as the SPI can be directly set to the desired mode after power-up. The device operates in run mode and limp-home mode by loading information into the configuration and control registers via SPI. The CHxEN bit is set to low to prevent the converters from turning on and operating with default system parameters. Writing "01" bits to the SLEEP register bypasses run mode, causing the device to enter a low-power sleep state directly.

2.5 Run Mode

SA33766 can enter run mode from load mode when one of the channels, CHxEN, is set to 1. It can also enter run mode from limp home mode by programming LHSW to 0 (0x00[5]). In run mode, the average current is set by CHxIADJ, while the ripple setting is determined by CHxRIPPLE.

In the event of an SPI communication failure, the device transitions to limp-home mode. For this to occur, the watchdog timer must be enabled (the CMWEN bit must be set to 1 in the SYSCFG1 register). The device enters limp-home mode after counting three consecutive watchdog timeout events. Alternatively, the device can be forced into limp-home mode by setting the LHSW bit to high in the SYSCFG1 register.

The transition to sleep mode is initiated by writing "01" bits to the SLEEP register via SPI, which causes the device to enter a low-power state.

2.6 Sleep Mode

The SA33766 features a digital access sleep mode function. When in run mode or load mode, write to the sleep control bit 0x07[1:0]. In sleep mode, the following actions occur:

1. The internal regulators are disconnected from the V5A pin.
2. The oscillator is disabled.
3. The CHxEN bit is set low.
4. The channels are disabled.
5. ADC and DAC operation are disabled.
6. The MOSFETs are turned off.

In addition, the resistor divider networks for VINx measurements and the V5D measurement are disconnected to conserve power. Only the SPI communication logic, powered by the V5A supply, remains active, and the SPI bus is monitored to check for command writes to the SLEEP register. Upon receiving the wake command (writing "00" to the SLEEP[1:0] bits in the SLEEP register), the device transitions from sleep mode to load mode. In sleep mode, the output voltage rises above 3 V as all internal loads are switched off, and the leakage current associated with the high-side gate drive is forced through the switch node.

2.7 Limp-Home Mode

The SA33766 enters limp-home mode after detecting three consecutive watchdog timeout events or when the LHSW bit (0x00[5]) is set high. In limp-home mode, the device's operation is determined by the LHxIADJ and LHCHxRIPPLE settings. The limp-home registers must be programmed during the device's initialization in load mode.

The LED current reference can be programmed through the LHxIADJ registers when LHEXTIADJ is set to 0, or it can be configured using an external voltage measured at the LHI pin by the ADC when LHEXTIADJ is set to 1. This enables LED control through the LHI pin.

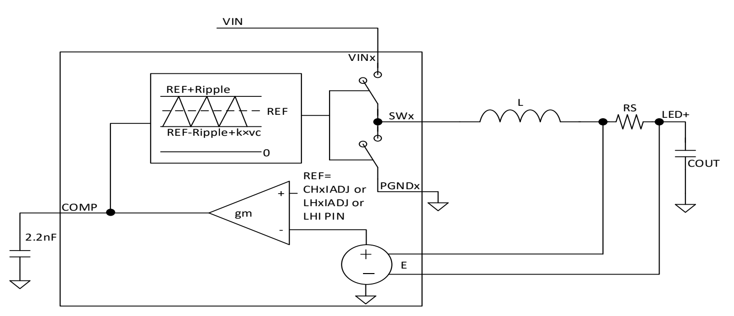
The LHI voltage measured by the ADC is converted to a 10-bit value and stored in the LHI registers. An internal digital low-pass filter attenuates any switching noise coupled to the LHI pin. The output of the filter is stored in the LHIFILT registers.

When the external LHI pin is selected as the LED current reference, an LHI pin voltage below 80mV disables both channels and turns off the LEDs. In this condition, the device ensures that no light output is generated for the associated channels. The LHI pin voltage must exceed 120 mV to enable both channels. The hysteresis rejects external noise on the LHI pin and prevents light flickering.

To exit limp-home mode, write 0x00[5]=0.

3. Buck Converter Switching Operation

The operating description of the SA33766 outlines the hysteresis control logic. The Comp signal is generated by the average control loop, and a 2.2 nF capacitor is recommended between Comp and GND. Vcomp compensates only for the current, while the average current sets the LED average current, and the ripple setting determines the inductor ripple during operation.



3.1 Inductor current ripple setting:

3.1.1 Run mode or standalone mode ripple:

Channel 1 ripple is set by CH1_RIPPLE[7:0] (address: 0x0C), and Channel 2 ripple is set by CH2_RIPPLE[7:0] (address: 0x0F). The formula for calculating the inductor current ripple of Channel x is as follows:

$$I_{ripplex} = \frac{CHxRIPPLE[7:0] \times 0.08}{R_{Sx} \times 255}$$

3.1.2 Limp home mode ripple:

Channel 1 ripple is set by LHCH1RIPPLE[7:0] (address: 0x28), and channel 2 ripple is set by LHCH2RIPPLE[7:0] (address: 0x2B). The formula for calculating the inductor current ripple of Channel x is as follows:

$$I_{ripplex} = \frac{LHCHxRIPPLE[7:0] \times 0.08}{R_{Sx} \times 255}$$

The ripple value from code [00] to code [FF] is linear corresponding to 0 to 80mV ripple.

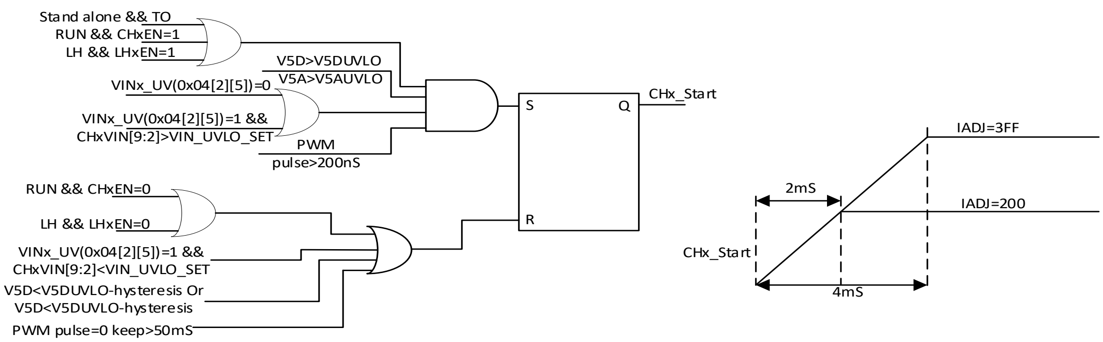
When the voltage CSP-CSN is less than or equal to Vref + Ripple + (Vcomp - Voffset) and Toff is greater than Toff_min, the low-side MOSFET is turned off. The inductor current is directly sensed by an external resistor RS. This design leads to a fast response and high current accuracy.

The ripple setting will affect the switching frequency directly, the switching frequency is as follow:

$$F_S = \frac{(V_{IN} - V_O) \times V_O}{V_{IN} \times L \times \Delta I_L}$$

$$\Delta I_L = 2 \times I_{ripple}$$

3.2 Start up



As shown channel can start to operate when four conditions are met simultaneously:

1, V5D>V5DUVLO and V5A>V5AUVLO;

2, PWMx>VPWMx_rising and keep 200nS at least;

3. Standalone mode: When CMWTO=1 or a Power-On Reset (POR) occurs, the system counts to 2^{24} without a correct frame interface. In run mode, one channel is enabled via the register, and in limp home mode, one channel is also enabled via the register.

4, Disable VIN under voltage lock out detect function (VINx_UV 0x04[2]=0 and 0x04[5]=0) or ADC result CHxVIN[9:2]>VIN_UVLO_SET(0x15[7:0])

Channel is disable when one of condition below is met:

Chanel can be disabled via the register. In RUN mode, both channels are disabled by the CHxEN register, while in LHI mode, both channels are disabled by setting LHxEN to 0.

2, PWM=0 and keep longer than 50mS;

3, V5D<V5D_UVLO_Falling.

The current reference increases from 0 to the target with a fixed slope of CHxIADJ from 0 to 3FF over a duration of 4 ms. This soft start feature is enabled at the beginning of each channel.

3.3 External PWM Dimming and Input Undervoltage Lockout (UVLO)

The PWM pin is a dual-function input that features an accurate 1.22V threshold with programmable hysteresis. This pin serves as both the external PWM dimming input for the LEDs and as a VIN_UVLO. When V5A exceeds the UVLO, 1 μA (typical) is sourced from the PWM pin. When the rising pin voltage surpasses the 1.22V threshold, 10 μA (typical) of current is sourced from the PWM pin into the resistor divider, providing programmable hysteresis.

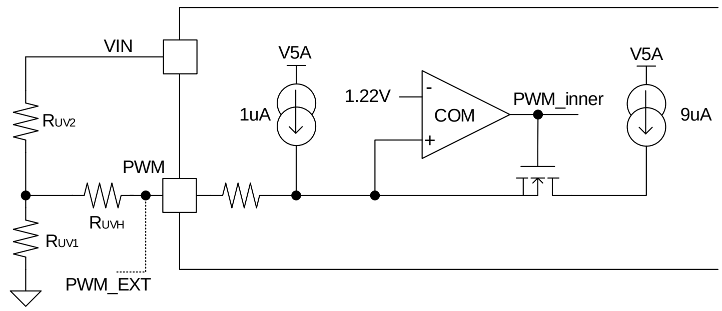


Figure 4: PWM control logic

The brightness of LEDs can be varied by modulating the duty cycle of the signal connected directly to the PWM input.

When using the PWM pin for both UVLO and PWM dimming concurrently, the UVLO circuit can include an additional resistor to set the hysteresis. This configuration allows the standard resistor divider to utilize smaller values, thereby minimizing PWM delays. It is recommended to have at least 1 V of hysteresis when operating near the UVLO threshold. Use the following equation to define the rising threshold:

$$V_{IN\ (rise)}=V_{PWM\ (rise)}\times\frac{R_{UV1}+R_{UV2}}{R_{UV1}}$$

Use Equation 2 to define the hysteresis.

UVLO only:

$$V_{HYS}=R_{UV2}\times I_{PWMx2}$$

PWM and UVLO:

$$V_{HYS}=I_{PWMx2}\times(R_{UV2}+\frac{R_{UVH}\times(R_{UV1}+R_{UV2})}{R_{UV1}})$$

3.4 Internal PWM Dimming

The SA33766 incorporates an internal 10-bit counter to independently configure PWM dimming for each channel. To utilize the internal PWM, set the CHxINTPWM bit in the SYSCFG1 register. The duty cycle of the internal PWM can be configured using a 10-bit value in the CHxPWML and CHxPWMH registers. Since CHxPWM is a 10-bit value, updating the PWM duty cycle may require two SPI writes: one to the CHxPWMH register and the other to the CHxPWML register. To prevent the transfer of unintended values, the contents of the two registers are only transferred to the CHxPWM counter upon writing to the CHxPWML register. Therefore, to update the PWM duty cycle, it is necessary to write a value to the CHxPWMH first, followed by a consecutive command to write a value to the CHxPWML register. Additionally, to avoid corrupting the progress of the current PWM duty cycle, the update from the CHxPWM register to the CHxPWM counter occurs two PWMCLK counts before the end of each PWM period.

The PWM cycle 10bit PWM counter is set by a 3bit value in the PWMDIV register.

The device can be controlled through the PWM input independently of the internal PWM setting. The signal at the PWM input is ANDed with the internal PWM to generate a combined output that controls the switching operation. Therefore, each channel can be independently disabled based on the external PWM signal, even when the device is configured to operate with internal PWM settings.

3.5 Bias Supply

The device is powered by an external 5-V supply connected to the V5D and V5A pins. Operation is enabled when V5D and V5A exceed the 4.2-V (typ) rising threshold and is disabled when either V5D or V5A drops below the 4-V (typ) falling threshold. The comparator provides 200 mV of hysteresis to avoid chatter during transitions. The V5D supply powers the high-side and low-side gate driver circuits, while the V5A supply powers the internal analog and digital components of the SA33766. The two bias pins can be connected together on the PCB or through a series 10-Ω resistor between V5D and V5A, with the 5-V external supply connected directly to the V5D pin. Silergy recommends a capacitor from each pin to ground. The recommended range for the bypass capacitor from the V5D pin to ground is between 1 µF and 4.7 µF. The recommended range from the V5A pin to ground is between 100 nF and 1 µF.

The bypass capacitor from V5D to GND must be ten times larger than the bootstrap capacitor, C_{BST}, to ensure proper operation during PWM dimming. The voltage on V5D and V5A must not exceed 5.5 V.

As the V5D voltage drops below the 4-V threshold, the V5DUV bit in the STATUS2 register is set to indicate a bias undervoltage condition. The fault clears when the V5D voltage exceeds the 4.2-V (typ) rising threshold and STATUS2 is read once.

3.6 Bootstrap Supply

The SA33766 contains both high-side and low-side MOSFETs. The high-side gate driver operates in conjunction with an internal bootstrap diode and an external bootstrap capacitor, C_{BST}. During the on-time of the low-side MOSFET, the SW pin voltage is approximately 0 V, and CBST is charged from the V5D supply through the internal diode. Silergy recommends using a capacitor of approximately 220 nF, connected with short traces between the BST and SW pins. A larger capacitor is necessary to prevent a bootstrap undervoltage fault when operating at low PWM dimming frequencies.

4. Serial Interface

The programming of the SA33766 registers can be performed via a serial communication interface. The 4-wire control interface of the SA33766 is compatible with the Serial Peripheral Interface (SPI) bus. A microcontroller unit (MCU) can write to and read from the device registers to configure channel operation and enable or disable specific channels.

The SPI bus uses four signals:

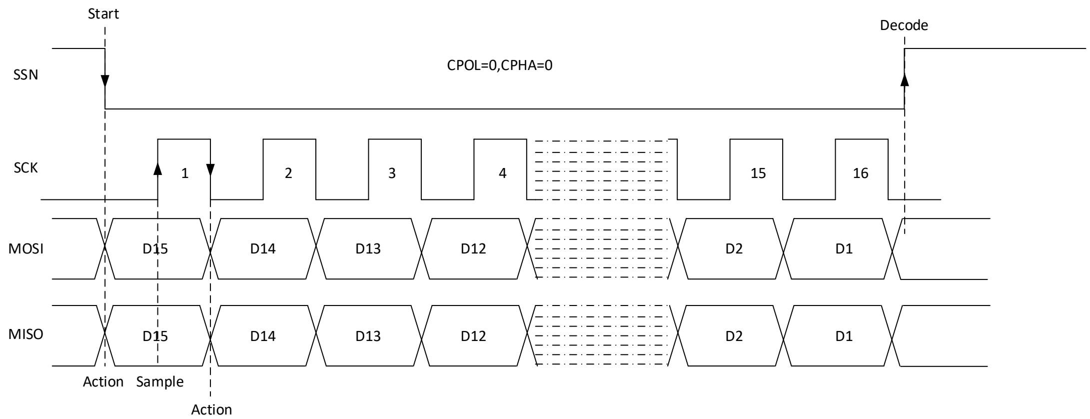
- SSN (Target Select)
- SCK (Clock)
- MOSI (Controller Out Target In)
- MISO (Controller In Target Out)

SSN, SCK, and MOSI are TTL-compatible inputs, while MISO is an open-drain output. The SPI bus supports both star and daisy-chain configurations.

A transaction begins when the MCU pulls the SSN line low. While the SSN line is low, input data on the MOSI line is recorded on the rising edge of SCK, starting with the most significant bit (MSB). Output data is transmitted on the MISO line at the falling edge of SCK. Each transaction must utilize 16, 32, 48, or other multiples of 16 SCK cycles.

When the SSN signal remains inactive (low) for 16 clock cycles, information propagates sequentially through the device. Upon SSN activation (high), the SA33766 interprets the final 16-bit sequence received. The MISO line enters a high-impedance state when SSN is asserted high. During SSN deactivation (low), the MISO line transmits data corresponding to the most recent instruction.

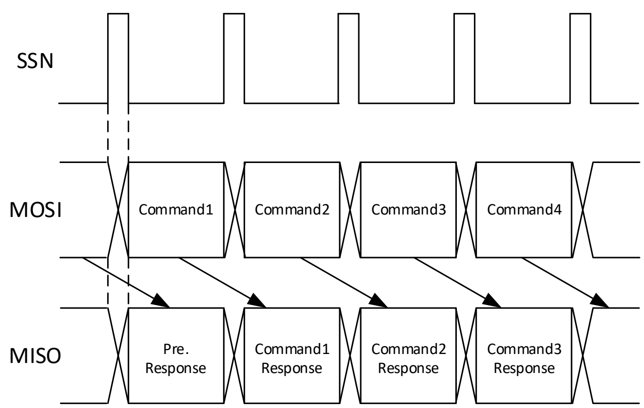
Data synchronization occurs through bidirectional shift operations: incoming bits on MOSI populate a 16-bit internal register (MSB-first), while outgoing bits stream through MISO. During bus idle states (SSN high), MISO remains tri-stated via open-drain control. Active communication (SSN low) enables MISO to output data aligned with the stored command pattern. Transaction initiation coincides with the falling edge of SSN, at which point MISO immediately presents the MSB of the output data, with subsequent updates synchronized to the falling edges of SCK.



SPI Data Format

A valid transfer requires a non-zero integer multiple of 16 SCK cycles (i.e., 16, 32, 48, etc.). If SSN is pulsed low and no SCK pulses are issued before SSN rises, a SPI error is reported. Similarly, if SSN is raised before the 16th rising edge of SCK, the transfer is aborted, and a SPI error is reported. If SSN is held low after the 16th falling edge of SCK and additional SCK edges occur, data continues to flow through the SA33766 shift register and out of the MISO pin. When SSN transitions from low to high, the internal digital block decodes the most recent 16 bits received prior to the rising edge of SSN.

SSN must transition to high only after a multiple of 16 SCK cycles for a transaction to be valid; otherwise, a SPI error is reported. In the case of a write transaction, the SA33766 logic performs the requested operation when SSN transitions high, provided that no SPI error has occurred. For a read transaction, the read data is transferred during the next frame, regardless of whether a SPI error has occurred.



SPI Command and Response

The data bit on the MOSI line is shifted into an internal 16-bit shift register (MS-bit first) while data is simultaneously shifted out of the MISO pin. When SSN is high (bus idle), MISO is tri-stated by the open-drain driver. When SSN is low, MISO is driven according to the 16-bit data pattern being shifted out based on the previously received command. To initiate a transaction at the falling edge of SSN, MISO is driven to the MS-bit of the outbound data and is updated on each subsequent falling edge of SCK.

4.1 Command Frame

The command frames are the only defined frame format sent from the master to the slave on MOSI. A command frame can be either a read command or a write command and consists of a CMD bit, six bits of ADDRESS, a PARITY bit (odd parity), and eight bits of DATA. The following illustrates the format of the command frame. The bit sequence is as follows:

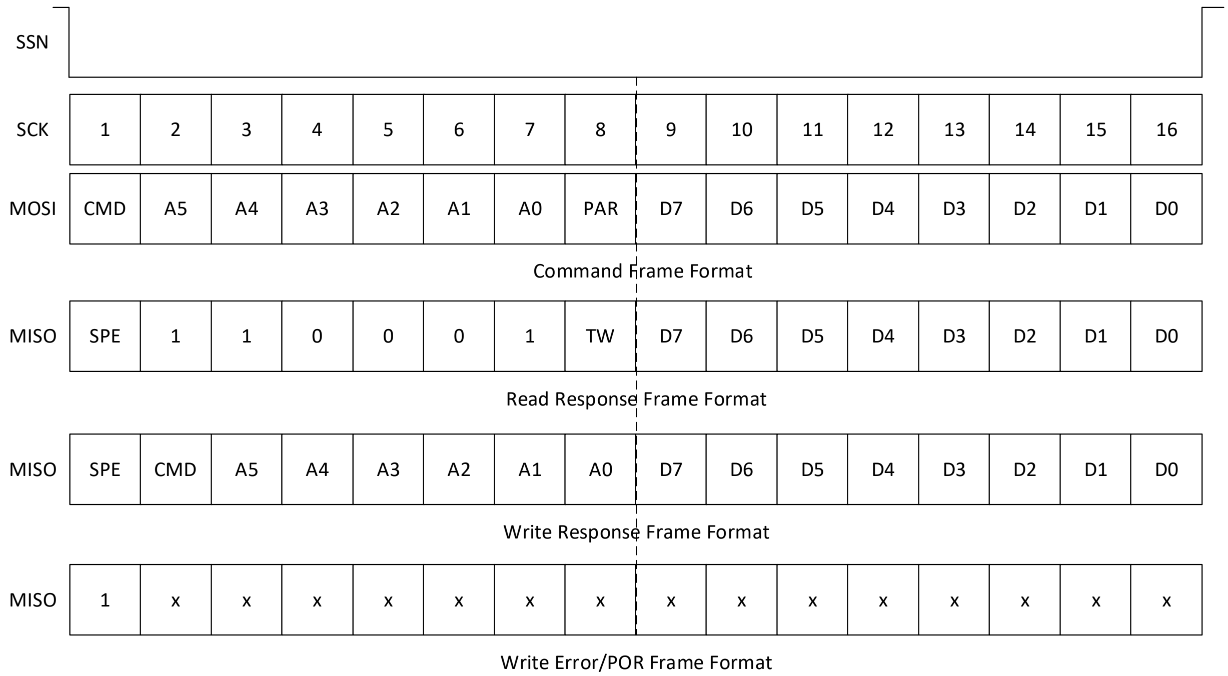
The COMMAND bit (CMD) indicates the type of transfer. CMD = 1 signifies that the transfer is a write command, while CMD = 0 indicates a read command.

2. Six bits of ADDRESS (A5:A0).

3. The PARITY bit (PAR). This bit is set by the following equation: PARITY = XNOR(CMD, A5..A0, D7..D0).

4. Eight bits of DATA (D7..D0). For read commands, set the DATA bits to zero.

Both the read and the write command follow the command frame format.



Write/Response Frame Format

4.2 Response Frame

There are three possible response frame formats: read response, write response, and write error/POR.

4.3 Read Response Frame Format

The read response has the following format:

1. The SPI Error bit (SPE)
2. Five reserved bits (always '110001')
3. The Thermal Warning bit (TW)
4. Eight bits of DATA (D7..D0) (only valid if SPE = 0)

4.4 Write Response Frame Format

The write response frame has the following format:

1. The SPI Error bit (SPE)
2. The COMMAND bit (CMD)
3. Six bits of ADDRESS (A5..A0)
4. Eight bits of DATA read from the destination register (D7..D0)

The picture illustrates the write response format. This frame is transmitted following a write command if the previously received frame was a write command and no SPI error occurred during that frame. The data bits in the write response are read back from the destination register that was just written. There is no need to issue a read command or evaluate the read response to verify that the destination register has been written correctly.

4.5 Write Error/POR Frame Format

The write error/POR frame consists of a '1' in the most significant bit (MSB) followed by the SA33766 internal digital block during the first SPI transfer after a power-on reset or following a write command that encounters an SPI error.

4.6 SPI Error

The SA33766 device records a SPI Error if any of the following conditions occur:

1. The SPI command has a non-integer multiple of 16 SCK pulses or no SCK pulses at all.

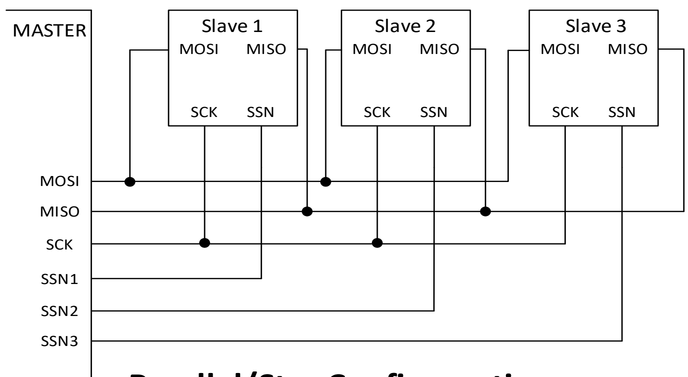
2. Any of the DATA bits during a read command are non-zero.

3. There is a parity error in the previously received command.

If any of these conditions are true, the SA33766 sets the SPE bit high in the next response frame. A write command with a SPI error does not write to the addressed register. Similarly, a read command does not clear any active fault bits if the command contains a SPI error. Additionally, if a read response has SPE = 1, the read data bits are invalid and must be disregarded.

4.7 SPI for Multiple Slave Devices in Parallel Configuration

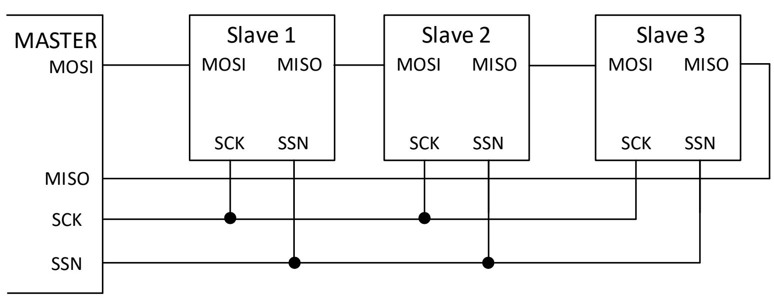
The SA33766 device can be connected in a star configuration, where the SSN of each device is independently controlled by the microcontroller. The diagram below illustrates the topology when three devices are connected.



Parallel/Star Configuaration

4.8 SPI for Multiple Slave Devices in Daisy Chain Configuration

The SA33766 device can be connected in a daisy-chain configuration to ensure the availability of GPIO when multiple devices communicate with the same microcontroller. The following diagram illustrates the topology when three devices are connected.



Daisy chain configuration

The data is shifted through each slave device, from the MOSI input to the MISO output, via each device's internal 16-bit shift register. After 16 clock cycles, the data is transferred from one device to another. The sequence continues until all data is passed from the first device, with MOSI connected to the microcontroller, to the last device, with MISO connected to the microcontroller. On the rising edge of SSN, each device decodes the last 16 bits that were received and held in the internal shift register.

4.9 ADC

The SA33766 incorporates a 10-bit successive approximation register (SAR) ADC. The single ADC is multiplexed to sample the following signals:

• VINx

- CSNx
- V5D
- LHI
- Internal temperature sensor nodes

The SAR ADC requires a typical sampling and conversion time of 12 µs. Priority is given to the CSNx inputs to ensure accurate output voltage measurements when operating at low PWM duty cycles. The ADC scheduler samples the CSN1 and CSN2 inputs four times consecutively, followed by other input parameters. The complete round-robin sampling sequence is illustrated below.

Counter 0-9	0	1	2	3	4	5	6	7	8	9	0	1	2
Select	CSN1	CSN2	LHI	VIN1	VIN2	CSN1	CSN2	V5D	TEMP1	TEMP2	CSN1	CSN2	LHI

The CSN1 and CSN2 inputs are sampled at intervals of 36 µs, with an additional delay occurring every ninth sample. All other parameters are sampled at a rate of 360 µs. For example, the VIN1 input is sampled after 30 ADC conversion cycles. The round-robin sampling scheme ensures adequate sampling to allow for rapid failure detection without data link loss, even during PWM dimming.

4.9.1 Input Voltage Measurement: VINx

The CHxVIN ADC input measures the voltage at the VINx pin. This voltage is internally attenuated with a 10-bit conversion ratio of 65/1023 (V/dec). The contents of the register provide diagnostics for the input power supply or, in many applications, the output voltage of the boost stage converter.

4.9.2 LED Voltage Measurement: CSNx

The ADC updates the CHxVLED register every time it samples the CSNx input. The CSNx pin voltage is converted using a 10-bit conversion ratio of 65/1023 (V/dec). Since the sampling interval is asynchronous to the PWM operation, the logic incorporates two additional registers, CHxVLEDON and CHxVLEDOFF, to store output voltage information based on the PWM operation. The contents of the CHxVLED register are copied to CHxVLEDON on the falling edge of the PWM signal to record the CSNx voltage when the PWM input is high. Similarly, the CHxVLED register is copied to CHxVLEDOFF on the rising edge of the PWM signal to record the CSNx voltage when the PWM input is low. This ensures consistent LED voltage readings during PWM operation.

4.9.3 Bias Supply Measurement: V5D

The V5D pin measurement indicates the status of the external bias converter. The voltage at the V5D pin is internally attenuated by a factor of 6/1023 (V/dec).

4.9.4 External Limp-Home Input Measurement: LHI

The ADC monitors the LHI pin and sets the internal current reference in limp-home mode. The LHI input voltage is digitized to provide a 10-bit reference with a resolution of 1.2 V/1023. The LHIL and LHIH registers are updated based on the ADC output.

4.9.5 Junction Temperature Measurement: TEMP

The combined TEMPL and TEMPH register values represent a 10-bit junction temperature measurement with a resolution of 0.463°C/LSB. The registers are updated only when TEMPL is read; therefore, TEMPL must be read first, followed by TEMPH, to obtain the junction temperature. Use the following equation to calculate the junction temperature.

$$T=0.493\times(TEMP[9:0]-296.897)$$

The over-temperature warning (TW) threshold is set by register TWLMT[7:0], and calculate equation as follow：

$$T_{TWLMT}=1.972\times(TWLMT[7:0]-74.224)$$

Protection

Fault Description

Fault	Detection	Action	Description
Thermal warning (TW)	TJ 8 bit MSB(0x20 or 0x21)>TJ(LMT)(0x06[7:0])	TW report in 0x04[6]	Sense the TJ from CH1 power MOS and CH2 power MOS, when one of TJ>TJLMT[7:0], TW(0x04[6]) bit is set high.
Thermal protection (TSD)	TJ>170℃	1:Report in CH1TP(0x04[1]) or CH2TP(0x04[4]) 2: Channel shut down	Each channel is protected by an individual thermal sensor located close to the switching MOSFETs, when channel is TSD, the corresponding channel is shut down(high side and low side MOS are off, report to the corresponding bit) and fault is read clear; IC recovery after TJ<TSD-THYS.
SPI Error	1. The SPI command has a non-integer multiple of 16 SCK pulses. 2. Any of the DATA bits during a read command are non-zero. 3. There is a parity error in the previously received command.	1: When SPE during first start up, IC enter stand alone mode, when SPE during operating, IC enter Limp-home. 2: SPE is set high in frame, and disable write to slaver.	After POR, IC will detect SPI communication, when no transaction in 2^24 clock, IC will enter stand alone mode, otherwise, IC will enter load mode. If SPE in the response frame is high, the write data into slaver is invalid. If the data frame written to slave is right, pull low SPE again.
V5D under voltage lockout	V5D<4.2V in first POR, or V5D<4V after POR	1:Stop switching 2:Report to 0x04[7]	The switching operation is disable and report to 0x04[7]
V5A undervoltage lockout	V5A<4.2V in first POR, or V5A<4V after POR	Stop switching	The device enter undervoltage lockout, the switching operation is disable, and the digital logic is reset to default values.
VINx undervoltage lockout	When VIN AD value CHxVIN[7:0]<VIN_UVLO_SET[7:0] and VINUV_EN=1(0x02[0]=1)	VINUV_EN=0,NA; VINUV_EN=1, IC will stop high side and low side MOS, and reset CHIADJ for soft start	VINUV_EN=0,NA; VINUV_EN=1, IC will stop high side and low side MOS, and reset CHIADJ for soft start
BSTx Undervoltage Lockout	VBSTx<2.5V in first POR, or VBSTx<2.3V after POR	1: High side MOS off and low side MOS on	Turn off high side MOS and turn on low side MOS to charge CBST
Short CHx output	VLED<SCHSET(0x02[3:2])	CHxSHORT bit is set	VLED is sense from CSN and save in CHxVLED, IC will detect after CHxIADJ rise to target value, and the action is based on 0x02[3:2] , Blanking time of SLP is 100uS.
Open CHx	Detect 16 times CHxVLED>VINx-2.5V	1: High side and low side MOS are off 2:Report to 0x03[4] or 0x03[0]	Detect 16 times Ton_max, IC stop the HGATE of corresponding channel and report to 0x03[4] or 0x03[0], once VLED drop below Open threshold, IC rework again.
High side Switch Current Limit	HIS>IHSx(LIM)	1:High side MOS off, low side MOS on 2:CHxHSILIM bit is set(0x03[2] or 0x03[6])	IC turn off the high side MOS and turn on low side MOS after min on time, low side MOS off after current zero. The recovery action is base on CHxHSILIMFL(0x01[1] and 0x01[4]), if CHxHSILIMFL=1, IC will enter latch off and pull low ChxEN, channel recovery until ChxEN is set high again, if CHxHSLIMFL=0, ic will auto restart after IFT in 0x01[7:6]

Low side Switch Current Limit	ILS<-0.5A	1: Both high/low side MOS are off 2:CHxLSILIM bit is set high	When ILS<-0.5A turn off high side and low side MOS, the recovery action is base on CHxLSILIMFL(0x01[0] and 0x01[3]), if CHxLSILIMFL=1, IC will enter latch off and pull low ChxEN, channel recovery until ChxEN is set high again, if CHxLSLIMFL=0, ic will auto restart after IFT in 0x01[7:6]

All fault and diagnostic features have an associated Fault-Read bit in the STATUS1, STATUS2, and STATUS3 registers. The corresponding Fault-Read bit is set in the register map. Reading these registers clears the bits if the condition no longer exists. The clearing of the Fault-Read bits occurs at the end of the SPI transfer read response, not at the end of the read command.

The SA33766 can be configured to auto-restart or latch-off upon detection of high-side or low-side current limit faults. The device enters the latched-off state when the bit associated with the fault and channel is set high in the SYSCFG2 register. This action disables the channel and ensures it remains off after the fault condition is detected. The channel can be reactivated by clearing the fault bit in STATUS1 and resetting the ChxEN bit in the SYSCFG1 register.

The SA33766 logic features a communication watchdog timer based on the system clock (CLK). This watchdog timer is enabled by default upon power-up, as the CMWEN bit is set to 1 in the SYSCFG1 register. The tap point for the communications watchdog timer is configured by writing the desired value to the CMWTAP register.

The communication watchdog timer has a default duration of 1.67 seconds. This timer monitors the status of the SPI bus and determines the device's operation in the event of an SPI communication error, specifically when the SPE bit is set to 1. For more details, refer to the device functional modes.

The high-side current limit, low-side current limit, and thermal protection faults pull the FLTB pin low when biased through an external resistor and connected to a 5V supply. The FLTB output can be utilized in conjunction with other signals. Setting the FPINRST bit to one in the SYSCFG1 register resets the FLTB pin when no active faults are detected by the device.

Faults and Diagnostics Summary

LIST	DESCRIPTION	FAULT OR DIAGNOSTIC	FAULT READ BIT	ENABLE FAULT TIMER(3.6mS)
TW	Thermal Warning	Diagnostics	Yes	No
CHxTP	Thermal Protection	Fault	Yes	No
VINx(UVLO)	VIN Supply Undervoltage Lockout	Fault	Yes	No
CHxBSTUV	BST Supply Undervoltage Lockout	Fault	Yes	No
CHxSHORT	Short Circuit Detected	Diagnostics	Yes	No
CHxOPEN	Open Circuit Detected	Fault	Yes	No
CHxHSILIM	High-side Current Limit	Fault	Yes	Yes
CHxLSILIM	Low-side Current Limit	Fault	Yes	Yes
V5DUV	V5D Undervoltage	Fault	Yes	No
SPE	SPI Communication Error	Diagnostics	Yes	No
LHSW	Limp-Home Mode(Communication Error)	Fault	Yes	No
VOUTx_OVP	Detect VLED, when VLED higher than VIN-2.5V	Fault	Yes	No

5. Register Map

The SPI-accessible registers are each eight bits wide and are located in a six-bit addressable register array (0x00 through 0x32). The registers in the SA33766 device contain programmed information and operational status.

Upon power-up, the registers are reset to their default values. Writes to unlisted addresses are not permitted and may result in undesired operation. Reads from unlisted addresses return a zero value. Reserved bits ("RESERVED") must be written with '0' values. Registers can be read or written unless indicated otherwise in the register description. This is the SA33766 register map.

Register Map

Reg.	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
0x00	SYSCFG1	FPINRST	RESERVED	LHSW	CMWEN	CH2INTPWM	CH2EN	CH1INTPWM	CH1EN	R/W	0001,0000
0x01	SYSCFG2	IFT[1:0]		CH2TSFL	CH2HSILIMFL	CH2LSILIMFL	CH1TSFL	CH1HSILIMFL	CH1LSILIMFL	R/W	0000,0000
0x02	SYSCFG3	CMWTAP[3:0]				SCHSET		RESERVED	VINUV_EN	R/W	1000,0000
0x03	STATUS1	CH2LSILIM	CH2HSILIM	CH2SHORT	CH2_OV	CH1LSILIM	CH1HSILIM	CH1SHORT	CH1_OV	RC	n/a
0x04	STATUS2	V5DUV	TW	VIN2_UV	CH2TP	CH2BSTUV	VIN1_UV	CH1TP	CH1BSTUV	RC	n/a
0x05	STATUS3	CMWTO		STANDALONE	LHI	LOAD	RUN	CH2STATUS	CH1STATUS	RC	n/a
0x06	TWLMT	TWLMT[7:0](Thermal Warning Limit, compare to the high one of TEMPx[9:2])								R/W	1001,0000
0x07	SLEEP	CHxCOMPSG		JITTER_SET		RESERVED		SLEEP[1:0]		R/W	0000,0000
0x08	RESERVED	RESERVED								R/W	0000,0000
0x09	TONMAXSET	CH2_Tonmax/Toffmin		RESERVED		CH2_Tonmax/Toffmin		RESERVED		R/W	0000,0000
0x0A	CH1IADJL	RESERVED						CH1IADJ[1:0]		R/W	0000,0000
0x0B	CH1IADJH	CH1IADJ[9:2]								R/W	0000,0000
0x0C	CH1RIPPLE	CH1RIPPLE [7:0]								R/W	0100,1101
0x0D	CH2IADJL	RESERVED						CH2IADJ[1:0]		R/W	0000,0000
0x0E	CH2IADJH	CH2IADJ[9:2]								R/W	0000,0000
0x0F	CH2RIPPLE	CH2RIPPLE[7:0]								R/W	0100,1101
0x10	PWMDIV	RESERVED					PWMDIV[2:0]			R/W	0000,0100
0x11	CHIP WML	RESERVED						CH1PWM[1:0]		R/W	0000,0000
0x12	CH1PWMH	CH1PWM[9:2]								R/W	0000,0000
0x13	CH2PWML	RESERVED						CH2PWM[1:0]		R/W	0000,0000
0x14	CH2PWMH	CH2PWM[9:2]								R/W	0000,0000
0x15	VINUVLO	VIN_UVLO_SET[7:0]								R/W	0000,0000
0x16	CH1VIN	CH1VIN[9:2]								R	-
0x17	CH1VLED	CH1VLED[[9:2]								R	-
0x18	CH1VLEDON	CH1VLEDON[[9:2]								R	-
0x19	CH1VLEDOFF	CH1VLEDOFF[[9:2]								R	-
0x1A	MIX	CH1VLEDOFF[1:0]		CH1VLEDON[[1:0]		CH1VLED[1:0]		CH1VIN[1:0]		R	-
0x1B	CH2VIN	CH2VIN[[9:2]								R	-
0x1C	CH2VLED	CH2VLED[[9:2]								R	-
0x1D	CH2VLEDON	CH2VLEDON[[9:2]								R	-
0x1E	CH2VLEDOFF	CH2VLEDOFF[[9:2]								R	-
0x1F	MIX	CH2VLEDOFF[1:0]		CH2VLEDON[1:0]		CH2VLED[1:0]		CH2VIN[1:0]		R	-
0x20	TEMP1H	TEMP1[9:2]								R	-
0x21	TEMP2H	TEMP2[9:2]								R	-
0x22	V5D	V5D[9:2]								R	-
0x23	LHI	LHI[9:2](Limp home current set)								R	-
0x24	MIX	LHI[1:0]		V5D[1:0]		TEMP2[1:0]		TEMP1[1:0]		R	-
0x25	LHCFG1	RESERVED	LHEXTIADJ	LH2100DC	LH2INTPWM	LH2EN	LH1100DC	LH11NTPWM	LH1EN	R/W	0000,0000
0x26	LHCFG2	LHIFT[1:0]		LH2TSFL	LH2HSILIMFL	LH2LSILIMFL	LH1TSFL	LH1HSILIMFL	LH1LSILIMFL	R/W	0000,0000
0x27	LHOVSET	RESERVED								R/W	0000,0000
0x28	LHCH1RIPPLE	LHCH1RIPPLE[7:0]								R/W	0100,1101
0x29	LH1IADJL	RESERVED						LH1IADJ[1:0]		R/W	0000,0000
0x2A	LH1IADJH	LH1IADJ(9:2]								R/W	0000,0000
0x2B	LHCH2RIPPLE	LHCH2RIPPLE[7:0]								R/W	0100,1101
0x2C	LH2IADJL	RESERVED						LH2IADJ[1:0]		R/W	0000,0000
0x2D	LH2IADJH	LH2IADJ(9:2]								R/W	0000,0000
0x2E	LHCH1PWML	RESERVED						LH1PWM[1:0]		R/W	0000,0000
0x2F	LHCH1PWMH	LH1PWM[9:2]								R/W	0000,0000

0x30	LHCH2PWML	RESERVED	LH2PWM[1:0]	R/W	0000,0000
0x31	LHCH2PWMH	LH2PWM[9:2]		R/W	0000,0000
0x32	EXTI	=0xD4 Exit SA mode and enter load mode		W	0000,0000

Complex bit access types are encoded to fit into small table cells. The table displays the codes used for access types in this section.

Access Type Codes

Access Type	Code	Description
W	W	Write
R	R	Read
R/W	R/W	Read and Write
RC	RC	Read to clear

5.1 Configuration Registers

The configuration registers control device operation and program the fault response. These registers support both reading and writing functions.

5.1.1 SYSCFG1 Register (address = 0x00) [reset = 0x10]

The SYSCFG1 register is the first system configuration register and contains bits that enable various channels and functions. Table 1 provides a description of the SYSCFG1 register.

System Configuration Register 1 Field Description

System Configuration Register 1(0x00)				
bit	field	type	Reset	Description
7	FPINRST	W	0	Reset open drain fault output if there are no active faults in the system. Note that this bit is write only. Any reads of this register return 0 in the FPINRST bit location. 0 = Do not care 1 = Reset open drain fault output
6	Reserve	NA		
5	LHSW	R/W	0	Software to enter limp home mode. Write 0 to this bit to enter run mode from limp home mode. 0 = Normal Operation 1 = Operation in limp home state
4	CMWEN	R/W	1	Communication watch dog timer 0 = Disable communication watch dog timer 1 = Enable communication watch dog timer
3	CH2INTPWM	R/W	0	This bit is used to enable internal PWM generator function for channel 2. 0 = LED current duty cycle of channel 2 controlled by the external signal connected to PWM2 1 = LED current duty cycle of channel 2 controlled by the internal PWM generator, external PWM2 must be pull high.
2	CH2EN	R/W	0	This bit is used to enable channel channel 2 in run mode. 0 = Disable LED channel 2 1 = Enable LED channel 2
1	CH1INTPWM	R/W	0	This bit is used to enable internal PWM generator function for channel 1. 0 = LED current duty cycle of channel 1 controlled by the external signal connected to PWM2 1 = LED current duty cycle of channel 1 controlled by the internal PWM generator, external PWM1 must be pull high.
0	CH1EN	R/W	0	This bit is used to enable channel channel 1 in run mode. 0 = Disable LED channel 1 1 = Enable LED channel 1

5.1.2 SYSCFG2 Register (address = 0x01) [reset = 0x00]

The SYSCFG2 register is the second system configuration register. This register contains bits related to enabling fault handling for both channels and configuring the fault timer.

System Configuration Register 2 Field Description

System Configuration Register 2 (0x01=00000000)

bit	field	type	Reset	Description
[7:6]	IFT	R/W	0	IFT sets the counter limit for the fault timer as shown below.(For HSLIM and LSLIM fault) 00 = 3.0 ms fault timer 01 = 7.0 ms fault timer 10 = 14.0 ms fault timer 11 = 25.0 ms fault timer
5	CH2TSFL	R/W	0	IC thermal shut down fault response. 0 = Auto restart after channel 2 thermal shut down 1 = Latch channel 2 after channel 2 thermal shut down
4	CH2HSILIMFL	R/W	0	Channel 2 high side FET current limit fault response 0 = Channel 2 auto restarts after the fault timer has expired (Fault timer is set by IFT). 1 = Channel 2 Latch after high side FET current limit is happen
3	CH2LSILIMFL	R/W	0	Channel 2 low side FET current limit fault response 0 = Channel 2 auto restarts after the fault timer has expired (Fault timer is set by IFT). 1 = Channel 2 Latch after low side FET current limit happen
2	CH1TSFL	R/W	0	IC thermal shut down fault response. 0 = Auto restart after channel 1 thermal shut down 1 = Latch channel 1 after channel 1 thermal shut down
1	CH1HSILIMFL	R/W	0	Channel 1 high side FET current limit fault response 0 = Channel 1 auto restarts after the fault timer has expired (Fault timer is set by IFT). 1 = Channel 1 Latch after high side FET current limit is happen
0	CH2LSILIMFL	R/W	0	Channel 1 low side FET current limit fault response 0 = Channel 1 auto restarts after the fault timer has expired (Fault timer is set by IFT). 1 = Channel 1 Latch after low side FET current limit happen

5.1.3 SYSCFG3 Register (address = 0x02) [reset = 0x80]

The SYSCFG3 register is the second system configuration register. This register contains bits related to short protection threshold set handling for both channels and the watchdog timer.

System Configuration Register 2 Field Description

System Configuration Register 3 (0x02=10000000)				
bit	field	type	Reset	Description
[7:4]	CMWTAP	R/W	1000	CMWTAP bits to set the watch dog time out period 0000 = 6.1ms watch dog period 0001 = 12.1ms watch dog period 0010 =24.3ms watch dog period 0011 = 48.5ms watch dog period 0100 =97.1ms watch dog period 0101 = 194.2ms watch dog period 0110 = 388.3mswatch dog period 0111 =776.7ms watch dog period 1000 through 1111 =1.52s watchdog period
[3:2]	SCHSET	R/W	0	CHx Short protection threshold set. 00: Disable short LED protection 01: Short LED protection threshold is 2.5V 11/10: Short LED protection threshold is 5V
1	Reserved	R/W	0	
0	VINUV_EN	RW	0	VIN under voltage lock out function setting 0: Disable VINUV protection 1: Enable VINUV protection, channel will disable after VINUV, and re-start after VIN exit under voltage.

5.2 STATUS Register

The status registers report warning and fault conditions. These registers are read-only. Reading the register clears the bits that are set if the condition that caused them no longer exists.

5.2.1 STATUS1 Register (address = 0x03)

STATUS1 Register Field Description

Status 1 Register (Read-Only) (0x03=NA)				
bit	field	type	Reset	Description
7	CH2LSILIM	RC	0	Indicates low side switch current limit fault on channel 2. Low side switch current is greater than 0.5A.
6	CH2HSILIM	RC	0	Indicates high side switch current limit fault on channel 2. High side switch current is greater than 2A.
5	CH2SHORT	RC	0	Indicates output short circuit fault on channel 2. CSP pin voltage is below short LED protection threshold.

4	CH2_OV	RC	0	Channel 2 VLED>VIN-2.5V(Typical), this bit may false triggering during BUCK input voltage rising and falling, can read clear this bit after input rising or input falling.
3	CH1LSILIM	RC	0	Indicates low side switch current limit fault on channel 1. Low side switch current is greater than 0.5A.
2	CH1HSILIM	RC	0	Indicates high-side switch current limit fault on channel 1. High-side switch current is greater than 2.A (typical).
1	CH1SHORT	RC	0	Indicates output short circuit fault on channel 1. CSP 1 pin voltage is below SLP threshold.
0	CH1_OV	RC	0	Channel 1 VLED>VIN-2.5V(Typical), this bit may false triggering during BUCK input voltage rising and falling, can read clear this bit after input rising or input falling.

5.2.2 STATUS2 Register (address = 0x04)

STATUS2 Register Field Description

Status 2 Register (Read-Only) (0x04=NA)				
bit	field	type	Reset	Description
7	V5DUV	RC	0	Indicates V5D under voltage fault condition
6	TW	RC	0	Thermal warning protection
5	VIN2_UV	R	0	Internal VIN2 UVLO 0: Disable VIN2 under voltage protection 1: Enable VIN2 under voltage protection
4	CH2TP	RC	0	Indicates over temperature thermal protection for channel 2. The channel automatically restarts when the bit is cleared to 0.
3	CH2BSTUV	RC	0	Indicates bootstrap under voltage fault condition on channel 2. BST2 pin voltage is less than 2.95 V.
2	VIN1_UV	R	0	Internal VIN1 UVLO 0: VIN1 under voltage normal 1: VIN1 under voltage protection
1	CH1TP	RC	0	Indicates over temperature thermal protection for channel 1. The channel automatically restarts when the bit is cleared to 0.
0	CH1BSTUV	RC	0	Indicates bootstrap under voltage fault condition on channel 1. BST1 pin voltage is less than 2.5 V.

5.2.3 STATUS3 Register (address = 0x05)

STATUS3 Register Field Description

Status 3 Register (Read-Only) (0x05=NA)				
bit	field	type	Reset	Description
[7:6]	CMWTO	RC	00	Indicates the number of times the communication watchdog timer has expired. 00 = Default (normal operation) 01 = Watchdog has expired 1 time. 10 = Watchdog has expired 2 times. 11 = Watchdog has expired 3 times. Device transitions into limp-home mode.
5	STANDALONE	R	0	Indicates standalone mode. This bit can be cleared by issuing the RESET or DETECT command (see RESET register).
4	LHI	R	0	Indicates LHI mode
3	LOAD	RC	0	Indicates Load mode
2	RUN	R	0	Indicates RUN mode
1	CH2STATUS	RC	0	Logic OR of the fault bits for channel 2 excluding over temperature thermal warning.
0	CH1STATUS	RC	0	Logic OR of the fault bits for channel 1 excluding over temperature thermal warning.

5.3 Device Control Registers

The control registers are used to enable sleep mode and to program the temperature warning threshold, as well as the CHx Ton_max and Toff_min set points. These registers support both read and write operations.

Device Control Registers Summary

Address	Acronym	Register Name
0x06	TWLMT	Thermal Warning Limit
0x07	SLEEP	COMP short and Sleep Command Register
0x08	RESERVED	Reserved
0x09	TONMAXSET	CHx Tonmax setting register
0x0A	CH1IADJL	Channel 1 run mode Analog Current Control Register (LSB)
0x0B	CH1IADJH	Channel 1 run mode Analog Current Control Register (MSB)
0x0C	CH1RIPPLE	Channel 1 run mode and stand alone mode Ripple Current Set Register

0x0D	CH2IADJL	Channel 2 run mode Analog Current Control Register (LSB)
0x0E	CH2IADJH	Channel 2 run mode Analog Current Control Register (MSB)
0x0F	CH2RIPPLE	Channel 2 run mode and stand alone mode Ripple Current Set Register
0x10	PWMDIV	Internal PWM frequency setting
0x11	CHIPWML	Channel 1 PWM Width Register(LSB)
0x12	CH1PWMH	Channel 1 run mode PWM Width Register(MSB)
0x13	CH2PWML	Channel 2 run mode PWM Width Register(LSB)
0x14	CH2PWMH	Channel 2 run mode PWM Width Register(MSB)
0x15	VINUVLO	Input Under Voltage threshold setting Register

5.3.1 Thermal Warning Limit (address = 0x06) [reset = 0x90]

TWLMT Register Field Description

Thermal Warning Limit Register(0x06=10001010)				
bit	field	type	Reset	Description
[7:0]	TWLMT[7:0]	R/W	10010000	TWLMT [7:0] sets the Thermal Warning (TW) bit when the 8 bits MSB of the ADC reading of the TEMP value exceed the programmed value. The default value is 144 decimal, or 0x90h (corresponding to a temperature of 124°C)

5.3.2 SLEEP Command (address = 0x07) [reset = 0x00]

Sleep Register Field Description

Sleep Command Register(0x07=00000000)				
bit	field	type	Reset	Description
[7:6]	CHxCOMPSG	R	00	Indicates COMP exception register 00: Normal 01:Channel 1 COMP short to GND 10:Channel 2 COMP short to GND 11:Channel 1 and Channel 2 COMP short to GND
[5:4]	JITTER_SET	R/W	00	Buck Jitter Range 00: ±6% 01: ±3% 10: ±12% 11: Disable jitter
[3:2]	RESERVED	R	000000	Reserved
[1:0]	SLEEP	R/W	00	Device sleep mode. The low-power sleep mode can be activated by writing to the register. 00 = Exit sleep mode and return to normal operation (SLEEP OFF). 01 = Enter sleep mode (SLEEP ON). 10 = No effect 11 = No effect

5.3.3 RESERVED (address = 0x08) [reset = 0x00]

Reserved Register Field Description

Reserved Control Register (address = 0x08=00000000)				
bit	field	type	Reset	Description
[7:0]	RESERVED	R	00000000	Reserved

5.3.4 TONMAXSET (address = 0x09) [reset = 0x00]

TONMAX SET Register Field Description

TONMAXSET Control Register (address = 0x09=00000000)				
bit	field	type	Reset	Description
[7:6]	CH2_Tonmax/Toffmin	R/W	00	00:CH2 tonmax=5us,toffmin=208ns; 01:CH2 tonmax=7.4us,toffmin=283ns; 10:CH2 tonmax=10us,toffmin=360ns; 11:CH2 tonmax=12.8us,toffmin=460ns;
[5:4]	RESERVED	R	000000	Reserved
[3:2]	CH1_Tonmax/Toffmin	R/W	00	00:CH1 tonmax=5us,toffmin=208ns; 01:CH1 tonmax=7.4us,toffmin=283ns; 10:CH1 tonmax=10us,toffmin=360ns; 11:CH1 tonmax=12.8us,toffmin=460ns;
1:0]	RESERVED	R	000000	Reserved

5.3.5 CH1IADJL Control Register (address = 0x0A) [reset = 0x00]

Channel 1 Analog Current Register (LSB)

CH1IADJL Control Register (address = 0x0A=00000000)				
bit	field	type	Reset	Description
[7:2]	RESERVED	R	000000	Reserved
[1:0]	CH1IADJ[1:0]	R/W	00	Channel 1 analog current control.

5.3.6 CH1IADJH Control Register (address = 0x0B) [reset = 0x00]

Channel 1 Analog Current Register

CH1IADJL Control Register (address = 0x0B=00000000)				
bit	field	type	Reset	Description
[7:0]	CH1IADJ[9:2]	R/W	00	Channel 1 analog current control.

5.3.7 CH1RIPPLE Control Register (address = 0x0C) [reset = 0x4D]

Channel 1 RIPPLE Control Register

CHIRIPPLE Control Register (address = 0x0C=01001101)				
bit	field	type	Reset	Description
[7:0]	CH1RIPPLE	R/W	01001101	Run mode Channel 1 Ripple control

5.3.8 CH2IADJL Control Register (address = 0x0D) [reset = 0x00]

Channel 2 Analog Current Register (LSB)

CH2IADJL Control Register (address = 0x0D=00000000)				
bit	field	type	Reset	Description
[7:2]	RESERVED	R	000000	Reserved
[1:0]	CH2IADJ[1:0]	R/W	00	Channel 2 analog current control.

5.3.9 CH2IADJH Control Register (address = 0x0E) [reset = 0x00]

Channel 2 Analog Current Register

CH2IADJL Control Register (address = 0x0E=00000000)				
bit	field	type	Reset	Description
[7:0]	CH2IADJ[9:2]	R/W	00	Channel 2 analog current control.

5.3.10 CH1RIPPLE Control Register (address = 0x0F) [reset = 0x4D]

Channel 2 RIPPLE Control Register

CHIRIPPLE Control Register (address = 0x0F=01001101)				
bit	field	type	Reset	Description
[7:0]	CH2RIPPLE	R/W	01001101	Run mode Channel 2 Ripple control

5.3.11 PWMDIV Register (address = 0x10) [reset = 0x04]

Internal PWM Clock Divider Register Field Description

PWMDIV Register (address = 0x10=00000100)				
bit	field	type	Reset	Description
[7:3]	RESERVED	R	00000	Reserved
[2:0]	PWMDIV[2:0]	R/W	100	This 3-bit value selects the clock divider for the internal PWM generator. The PWM clock is derived based on typical oscillator frequency of 20 MHz. 000 = Divide oscillator clock (fPWM = 1507 Hz). 001 = Divide oscillator clock (fPWM = 1318 Hz). 010 = Divide oscillator clock (fPWM = 1055 Hz). 011 = Divide oscillator clock (fPWM = 879 Hz). 100 = Divide oscillator clock (fPWM = 659 Hz). 101 = Divide oscillator clock (fPWM = 439 Hz). 110 = Divide oscillator clock (fPWM = 215 Hz). 111 = Divide oscillator clock (fPWM = 108 Hz).

5.3.12 CH1PWML Register (address = 0x11) [reset = 0x00]

Channel 1 PWM Width Register (LSB)

CH1PWML Register (address = 0x11=00000000)				
bit	field	type	Reset	Description
[7:2]	RESERVED	R	000000	Reserved
[1:0]	CH1PWM[1:0]	R/W	00	Channel 1 PWM width control. The 2 LSBs of the 10-bit PWM WIDTH for channel 1 can be programmed by writing to the register.

5.3.13 CH1PWMH Register (address = 0x12) [reset = 0x00]

Channel 1 PWM Width Register

CH1PWML Register (address = 0x12=00000000)				
bit	field	type	Reset	Description
[7:0]	CH1PWM[9:2]	R/W	00000000	Channel 1 PWM width control. The 8 MSBs of the 10-bit PWM WIDTH for channel 1 can be programmed by writing to the register.

5.3.14 CH2PWML Register (address = 0x13) [reset = 0x00]

Channel 2 PWM Width Register (LSB)

CH2PWML Register (address = 0x13=00000000)				
bit	field	type	Reset	Description
[7:2]	RESERVED	R	000000	Reserved
[1:0]	CH2PWM[1:0]	R/W	00	Channel 2 PWM width control. The 2 LSBs of the 10-bit PWM WIDTH for channel 2can be programmed by writing to the register.

5.3.15 CH2PWMH Register (address = 0x14) [reset = 0x00]

Channel 2 PWM Width Register

CH1PWML Register (address = 0x14=00000000)				
bit	field	type	Reset	Description
[7:0]	CH2PWM[9:2]	R/w	00000000	Channel 2 PWM width control. The 8 MSBs of the 10-bit PWM WIDTH for channel 2 can be programmed by writing to the register.

5.3.16 VINUVLO Register (address = 0x15) [reset = 0x00]

VINUVLO SET Register

VINUVLO Register (address = 0x15=00000000)				
bit	field	type	Reset	Description
[7:0]	VIN_UVLO_SET[7:0]	R/W	00000000	8LSB of buck control ref voltage. max Vin=67V when 0x15=FF

5.4 ADC Measurements

The output of the ADC conversion is stored in the read-only ADC measurement registers. Only the 8 most significant bits (MSBs) from the 10-bit ADC are utilized, while the remaining 2 least significant bits (LSBs) are ignored.

Address	Acronym	Register Name
0x16	CH1VIN	CH1 VIN Register
0x17	CH1VLED	CH1VLED Register
0x18	CH1VLEDON	CH1VLEDON Reserved
0x19	CH1VLEDOFF	CH1VLEDOFF Register
0x1A	MIX	CH2VIN/CH1VLED/CH1VLEDON /CH1VLEDOFF Register
0x1B	CH2VIN	CH2 VIN Register
0x1C	CH2VLED	CH2VLED Register
0x1D	CH2VLEDON	CH2VLEDON Reserved
0x1E	CH2VLEDOFF	CH2VLEDOFF Register
0x1F	MIX	CH2VIN/CH2VLED/CH2VLEDON /CH2VLEDOFF Register
0x20	TEMP1H	CH1 TEMP1H Register
0x21	TEMP2H	CH2 TEMP2H Register
0x22	V5D	V5DH Register
0x23	LHI	LHIH Register

0x24	MIX	TEMP1L/TEMP2L/V5DL/LHIL Register(MSB)

5.4.1 CH1VIN Register (address = 0x16)

CH1VIN Measurement Register

CH1VIN Measurement (address = 0x16)				
bit	field	type	Reset	Description
[7:0]	CH1VIN[9:2]	R	00000000	ADC the input voltage of channel 1, the full ADC value 0x16[9:2]+0X1A[1:0] =3FF corresponding to VIN=67V

5.4.2 CH1VLED Register (address = 0x17)

CH1VLED Measurement Register

CH1VLED Measurement (address = 0x17)				
bit	field	type	Reset	Description
[7:0]	CH1VLED[[9:2]	R	00000000	ADC the output voltage of channel 1, the full ADC value 0x17[9:2]+0X1A[3:2] =3FF corresponding to VLED=67V

5.4.3 CH1VLEDON Register (address = 0x18)

CH1VLEDON Measurement Register

CH1VLEDON Measurement (address = 0x17)				
bit	field	type	Reset	Description
[7:0]	CH1VLEDON[[9:2]	R	00000000	ADC measurement of the channel 1 output voltage before falling edge of PWM signal.The full ADC code: 0x18[9:2]+0x1A[5:4]=3FF ,corresponding to VLED=67V

5.4.4 CH1VLEDOFF Register (address = 0x19)

CH1VLEDOFF Measurement Register

CH1VLEDOFF Measurement (address = 0x18)				
bit	field	type	Reset	Description
[7:0]	CH1VLEDOFF[[9:2]	R	00000000	ADC measurement of the CSN1 node for channel 1 before rising edge of PWM signal. The full ADC code: 0x19[9:2]+0x1A[7:6]=3FF ,corresponding to VLED=67V

5.4.5 MIX Register (address = 0x1A)

MIX Register

MIX Measurement (address = 0x1A)				
bit	field	type	Reset	Description
[7:6]	CH1VLEDOFF[1:0]	R	00	2 LSB for channel 1 PWM off LED voltage
[5:4]	CH1VLEDON[[1:0]	R	00	2 LSB for channel 1 PWM on LED voltage
[3:2]	CH1VLED[1:0]	R	00	2 LSB for channel 1 LED voltage at the reading moment
[1:0]	CH1VIN[1:0]	R	00	2 LSB channel 1 input voltage

5.4.6 CH2VIN Register (address = 0x1B)

CH2VIN Register

CH2VIN Measurement (address = 0x1B)				
bit	field	type	Reset	Description
[7:0]	CH2VIN[9:2]	R	00000000	ADC the input voltage of channel 1, the full ADC value 0x1B[9:2]+0X1F[1:0] =3FF corresponding to VIN=67V

5.4.7 CH2VLED Register (address = 0x1C)

CH2VLED Measurement Register

CH2VLED Measurement (address = 0x1c)				
bit	field	type	Reset	Description
[7:0]	CH2VLED[[9:2]	R	00000000	ADC the output voltage of channel 1, the full ADC value 0x1C[9:2]+0X1F[3:2] =3FF corresponding to VLED=67V

5.4.8 CH2VLEDON Register (address = 0x1D)

CH1VLEDON Measurement Register

CH2VLEDON Measurement (address = 0x1d)				
bit	field	type	Reset	Description
[7:0]	CH2VLEDON[[9:2]	R	00000000	ADC measurement of the channel 1 output voltage before falling edge of PWM signal.The full ADC code: 0x1D[9:2]+0x1F[5:4]=3FF ,corresponding to VLED=67V

5.4.9 CH2VLEDOFF Register (address = 0x1E)

Tabel 3-35 CH2VLEDOFF Measurement Register

CH2VLEDOFF Measurement (address = 0x1E)				
bit	field	type	Reset	Description
[7:0]	CH2VLEDOFF[[9:2]	R	00000000	ADC measurement of the CSN1 node for channel 1 before rising edge of PWM signal. The full ADC code: 0x1E[9:2]+0x1F[7:6]=3FF, corresponding to VLED=67V

5.4.10 MIX Register (address = 0x1F)

Tabel 3-36 MIX Register

MIX Measurement (address = 0x1F)				
bit	field	type	Reset	Description
[7:6]	CH2VLEDOFF[1:0]	R	00	2 LSB for channel 2 PWM off LED voltage
[5:4]	CH2VLEDON[1:0]	R	00	2 LSB for channel 2 PWM on LED voltage
[3:2]	CH2VLED[1:0]	R	00	2 LSB for channel 2 LED voltage at the reading moment
[1:0]	CH2VIN[1:0]	R	00	2 LSB channel 2 input voltage

5.4.11 TEMP1H Measurement Register (address = 0x20)

TEMP1H Measurement Register

TEMP1H Measurement (address = 0x20)				
bit	field	type	Reset	Description
[7:0]	TEMP1[9:2]	R	00000000	ADC measurement of the channel 1 junction temperature. The register reports the 8 MSBs of the junction/exposed pad temperature.

5.4.12 TEMP2H Measurement Register (address = 0x21)

TEMP2H Measurement Register

TEMP2H Measurement (address = 0x21)				
bit	field	type	Reset	Description
[7:0]	TEMP2[9:2]	R	00000000	ADC measurement of the channel 2 junction temperature. The register reports the 8 MSBs of the junction/exposed pad temperature.

5.4.13 V5D Measurement Register (address = 0x22)

Tabel 3-38 V5DH Measurement Register

V5DH Measurement (address = 0x21)				
bit	field	type	Reset	Description
[7:0]	V5D	R	00000000	ADC the V5D voltage, the full ADC: 0x22[7:0]+0x24[5:4] corresponding to V5D=6.1V

5.4.14 LHI Measurement Register (address = 0x23)

LHI Measurement Register

LHIH Measurement (address = 0x23)				
bit	field	type	Reset	Description
[7:0]	LHI	R	00000000	ADC measurement of the Limp home current ref, 8 bits MSB

5.4.15 MIX Measurement Register (address = 0x24)

MIX Register

MIX Measurement (address = 0x24)				
bit	field	type	Reset	Description
[7:6]	LHI[1:0]	R	0000	ADC measurement of the Limp home current ref, 2 bits LSB
[5:4]	V5D[1:0]	R	0000	ADC measurement of the 5-V bias supply. 2bits LSB
[3:2]	TEMP2[1:0]	R	00	ADC measurement of the channel 2 junction temperature. 2 bits LSB

[1:0]	TEMP1[1:0]	R	00	ADC measurement of the channel 1 junction temperature. 2 bits LSB

5.5 Limp-Home Configuration and Command Registers

The limp-home registers control the device during operation in limp-home mode. These registers support both reading and writing functions.

Limp-Home Configuration and Command Registers

Address	Acronym	Register Name
0x25	LHCFG1	Limp-Home Configuration Register 1
0x26	LHCFG2	Limp-Home Configuration Register 2
0x27	RESERVED	Reserved
0x28	LHCH1RIPPLE	Limp-Home Mode Channel 1 Ripple Current Set Register
0x29	LH1IADJL	Limp-Home Mode Channel 1 Analog Current Control Register (LSB)
0x2A	LH1IADJH	Limp-Home Mode Channel 1 Analog Current Control Register (MSB)
0x2B	LHCH2RIPPLE	Limp-Home Mode Channel 2 Ripple Current Set Register
0x2C	LH2IADJL	Limp-Home Mode Channel 2Analog Current Control Register (LSB)
0x2D	LH2IADJH	Limp-Home Mode Channel 2 Analog Current Control Register (MSB)
0x2E	LHCH1PWML	Limp-Home Mode Channel 1 PWM Width Register(LSB)
0x2F	LHCH1PWMH	Limp-Home Mode Channel 1 PWM Width Register(MSB)
0x30	LHCH2PWML	Limp-Home Mode Channel 1 PWM Width Register(LSB)
0x31	LHCH2PWMH	Limp-Home Mode Channel 1 PWM Width Register(MSB)

5.5.1 LHCFG1 Register (address = 0x25) [reset =0x00]

LHCFG1 Register

LHCFG1 Registers (address = 0x25)				
bit	field	type	Reset	Description
7	RESERVED	R	NA	NA
6	LHEXTIADJ	R/W	0	This bit is used to select between internal or external current reference set point. The external reference is set by voltage on LHI pin and is converted to a 10-bit value by internal ADC. 0 = Use internal LHxIADJ register as the CHxIADJ setting in limp-home mode. 1 = Use external LHI reference as the current reference setting in limp-home mode.
5	LH2100DC	R/W	0	Set channel 2 PWM duty cycle to 100% in limp-home mode. 0 = LED current duty cycle based on internal or external command 1 = LED current duty cycle set to 100%
4	LH2INTPWM	R/W	0	This bit is used to enable internal PWM generator function for channel 2 in limp home mode. 0 = LED current duty cycle of channel 2 controlled by an external signal connected to PWM2 input 1 = LED current duty cycle of channel 2 controlled by an internal PWM generator (registers PWMDIV and LH2PWM).
3	LH2EN	R/W	0	CH2 enable. This bit controls the operation of channel 2 in limp-home mode. 0 = Disable LED channel 2. 1 = Enable LED channel 2.
2	LH1100DC	R/W	0	Set channel 1 PWM duty cycle to 100% in limp-home mode. 0 = LED current duty cycle based on internal or external command 1 = LED current duty cycle set to 100%
1	LH1INTPWM	R/W	0	This bit is used to enable internal PWM generator function for channel 1 in limp home mode. 0 = LED current duty cycle of channel 1controlled by external signal connected to PWM1 input 1 = LED current duty cycle of channel 1 controlled by internal PWM generator (registers PWMDIV and LH1PWM).
0	LH1EN	R/W	0	CH1 enable. This bit controls the operation of channel 1 in limp-home mode. 0 = Disable LED channel 1. 1 = Enable LED channel 1.

5.5.2 LHCFG2 Register (address = 0x26) [reset =0x00]

LHCFG2 Register

LHCFG2 Register (address = 0x26)				
bit	field	type	Reset	Description

[7:6]	LHIFT	R/W	00	LHIFT sets the counter limit for the ILIM fault timer in limp-home mode. 00 = 3.3 ms fault timer 01 = 6.6 ms fault timer 10 = 13.1 ms fault timer 11 = 26.2 ms fault timer
5	LH2TSFH	R/W	0	Channel 2 thermal shutdown fault response in limp-home mode 0 = Channel 2 auto-restarts based on internal temperature hysteresis. 1 = Channel 2 is latched off;
4	LH2HSILIMFL	R/W	0	Channel 2 high-side FET current limit fault response in limp-home mode 0 = Channel 2 auto-restarts after the ILIM fault timer has expired. 1 = Channel 2 is latched off;
3	LH2LSILIMFL	R/W	0	Channel 2 low-side FET current limit fault response in limp-home mode 0 = Channel 2 auto-restarts after the ILIM fault timer has expired. 1 = Channel 2 is latched off;
2	LH1TSFL	R/W	0	Channel 1 thermal shutdown fault response in limp-home mode 0 = Channel 1 auto-restarts based on internal temperature hysteresis. 1 = Channel 1 is latched off;
1	LH1HSILIMFL	R/W	0	Channel 1 high-side FET current limit fault response in limp-home mode 0 = Channel 1 auto-restarts after the ILIM fault timer has expired. 1 = Channel 1 is latched off;
0	LH1LSILIMFL	R/W	0	Channel 1 low-side FET current limit fault response in limp-home mode 0 = Channel 1 auto-restarts after the ILIM fault timer has expired. 1 = Channel 1 is latched off;

5.5.3 RESERVED Register (address = 0x27) [reset =0xFF]

RESERVED Register

RESERVED (address = 0x27)				
bit	field	type	Reset	Description
[7:0]	RESERVED	R/W	00000000	NA

5.5.4 LHCH1RIPPLE Register (address = 0x28) [reset =0x4D]

LHCH1RIPPLE Register

LHICH1_RIPPLE (address = 0x28)				
bit	field	type	Reset	Description
[7:0]	LHCH1RIPPLE[7:0]	R/W	01001101	LHI Home mode channel 1 ripple control

5.5.5 LH1IADJL Control Register (address = 0x29) [reset = 0x00]

LIMP HOME Mode Channel 1Analog Current Register (LSB)

LH1IADJL Control Register (address = 0x0D)				
bit	field	type	Reset	Description
[7:2]	RESERVED	R	000000	Reserved
[1:0]	LH1IADJ[1:0]	R/W	00	Channel 1 analog current control in limp-home mode. The 2 LSBs of the 10-bit IADJ DAC for channel 1 can be programmed by writing to the register.

5.5.6 CH1IADJH Control Register (address = 0x2A) [reset = 0x00]

LIMP HOME Mode Channel 2 Analog Current Register

CH2IADJL Control Register (address = 0x2A)				
bit	field	type	Reset	Description
[7:0]	LH1IADJ[9:2]	R/W	00000000	Channel 1 analog current control in limp-home mode. The 8 MSBs of the 10-bit IADJ DAC for channel 1 can be programmed by writing to the register.

5.5.7 LHCH2RIPPLE Control Register (address = 0x2B) [reset = 0x4D]

LIMP HOME Mode Channel 2 CH1RIPPLE Control Register

CHIRIPPLE Control Register (address = 0x2B)				
bit	field	type	Reset	Description
[7:0]	LHCH2RIPPLE2[7:0]	R/W	01001101	LHI Home mode channel 2 ripple control

5.5.8 LH2IADJL Control Register (address = 0x2C) [reset = 0x00]

LIMP HOME Mode Channel 2 Analog Current Register (LSB)

LH2IADJL Control Register (address = 0x2C)				
bit	field	type	Reset	Description
[7:2]	RESERVED	R	000000	Reserved
[1:0]	LH2IADJ[1:0]	R/W	00	Channel 2 analog current control in limp-home mode. The 2 LSBs of the 10-bit IADJ DAC for channel 2 can be programmed by writing to the register.

5.5.9 LH2IADJH Control Register (address = 0x2D) [reset = 0x00]

LIMP HOME Mode Channel 2 Analog Current Register

CH2IADJL Control Register (address = 0x2D)				
bit	field	type	Reset	Description
[7:0]	LH2IADJ[9:2]	R/W	00000000	Channel 2 analog current control in limp-home mode. The 8 MSBs of the 10-bit IADJ DAC for channel 1 can be programmed by writing to the register.

5.5.10 LHCH1PWML Register (address = 0x2E) [reset = 0x00]

LIMP HOME Mode Channel 1 PWM Width Register (LSB)

CH1PWML Register (address = 0x2E)				
bit	field	type	Reset	Description
[7:2]	RESERVED	R	00000	Reserved
[1:0]	LH1PWM[1:0]	R/W	00	Channel 1 PWM width control in limp-home mode. The 2 LSBs of the 10-bit PWM WIDTH for channel 1 can be programmed by writing to the register.

5.5.11 LHCH1PWMH Register (address = 0x2F) [reset = 0x00]

LIMP HOME Mode Channel 1 PWM Width Register

LHCH1PWMH Register (address = 0x2F)				
bit	field	type	Reset	Description
[7:0]	LH1PWM[9:2]	R/W	00000000	Channel 1 PWM width control in limp-home mode. The 8 MSBs of the 10-bit PWM WIDTH for channel 1 can be programmed by writing to the register.

5.5.12 LHCH2PWML Register (address = 0x30) [reset = 0x00]

LIMP HOME Mode Channel 2 PWM Width Register (LSB)

CH2PWML Register (address = 0x30)				
bit	field	type	Reset	Description
[7:2]	RESERVED	R	00000	Reserved
[1:0]	LH2PWM[1:0]	R/W	00	Channel 2 PWM width control in limp-home mode. The 2 LSBs of the 10-bit PWM WIDTH for channel 2 can be programmed by writing to the register.

5.5.13 LHCH2PWMH Register (address = 0x31) [reset = 0x00]

LIMP HOME Mode Channel 2 PWM Width Register

CH1PWMH Register (address = 0x31)				
bit	field	type	Reset	Description
[7:0]	LH2PWM[9:2]	R/W	00000000	Channel 2 PWM width control in limp-home mode. The 8 MSBs of the 10-bit PWM WIDTH for channel 1 can be programmed by writing to the register.

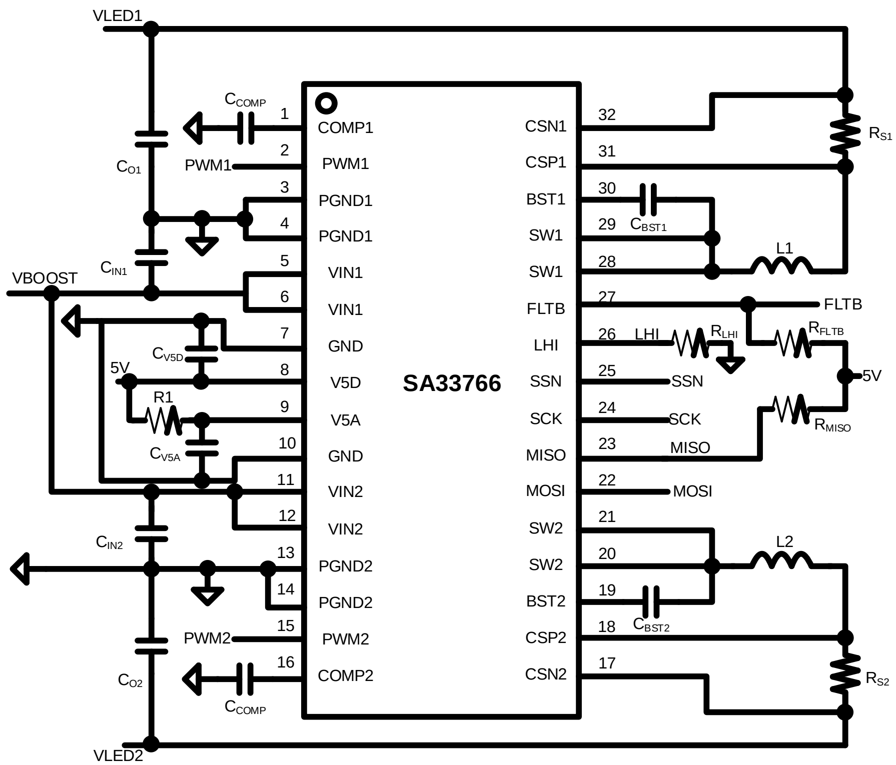
5.6 RESET Register (address = 0x32) (Write-Only)

Reset Register

Reset Register (address = 0x32)				
bit	field	type	Reset	Description
[7:0]	RESET	W	00000000	Write 0xD4 to the RESET register to reset all writable registers to their default values. If the logic is in stand-alone mode, reading the STATUS3 register to clear the CMWTO bits and then writing 0xD4 to the RESET register returns the channel enable state machines to the DETECT state. Watchdog timer is enabled.

6. Application Design

The schematic of a typical application for the SA33766 is as follow:



6.1 Duty Cycle

The switch duty cycle, D, defines the operation of the converter and is a function of the input and output voltages. In steady state, the duty cycle is defined using the following equation:

$$D=\frac{V_O}{V_{IN}}$$

There is no limitation for small duty cycles. The maximum attainable duty cycle is limited by the minimum off-time duration and is a function of the switching frequency.

6.2 Swiching Frequency

Since the SA33766 employs hysteresis control, the switching frequency is determined by the power inductor, inductor current ripple, and input/output voltage.

$$F_S=\frac{(V_{IN}-V_O)\times V_O}{2\times V_{IN}\times L\times I_{ripple}}$$

The inductor current ripple setting can refer to *Section 3.2.*

6.3 LED Current REF Setting

6.3.1 Run mode LED current setting

The average current for Channel 1 is determined by the combination of 0x0B[7:0] (8-bit MSB) and 0x0A[1:0] (2-bit LSB). The 10-bit CH1IADJ setting will take effect only when 0x0B[7:0] is written. The average current for Channel 2 is determined by the combination of 0x0E[7:0] (8-bit MSB) and 0x0D[1:0] (2-bit LSB). Similarly, this 10-bit setting will take effect only when 0x0E[7:0] is written. The 10-bit CHxIADJ setting will directly determine the CS_REF.

The formula for calculating the Channelx LED average current in Run mode is as follow:

$$I_{LEDx}=\frac{CHxIADJ[9:0]\times 0.168}{R_{Sx}\times 1023}$$

6.3.2 Limp home mode LED current setting

0x25[6] decide LHI PIN voltage or internal register setting:

When 0x25[6] = 0, select the internal register to set the average current. The average current for channel 1 is determined by 0x2A[7:0] (8-bit MSB) combined with 0x29[1:0] (2-bit LSB). The average current for channel 2 is determined by 0x2D[7:0] (8-bit MSB) combined with 0x2C[1:0] (2-bit LSB). The average current setting, a 10-bit data value LHxIADJ, is effective only when the MSB is written.

The formula for calculating the Channelx LED average current in limphome mode is as follow:

$$I_{LEDx}=\frac{LHxIADJ[9:0]\times 0.168}{R_{Sx}\times 1023}$$

When 0x25[6] = 1, select the external LHI PIN voltage to set the average current. The SA33766 will output a current ILHI from the LHI PIN. A resistor is connected in parallel from the LHI PIN to GND to obtain different values of VLHI. The IC ADC will read VHI as 0x23[7:0] (8-bit MSB) + 0x24[7:6] (2-bit LSB). This 10-bit data will determine the current for both channels 1 and 2.

The formula for calculating the Channelx LED average current in limphome mode is as follow:

$$I_{LEDx}=\frac{V_{LHI}\times 0.168}{R_{Sx}\times 1.2}$$

6.3.3 Stand-alone mode LED current setting

The channel current is decided by LHI PIN voltage from register 0x23[7:0](8 bit MSB) + 0x24[7:6](2 bit LSB).

The formula for calculating the Channelx LED average current in limphome mode is as follow:

$$I_{LEDx}=\frac{V_{LHI}\times 0.168}{R_{Sx}\times 1.2}$$

V_{LHI} is as follow:

$$V_{LHI}=R_{LHI}\times 10\times 10^{-6}$$

6.4 Inductor Selection

In the hysteresis control method, the selection of the inductance value influences the switching frequency, F_S. Therefore, under the system's steady-state operating conditions, once the required switching frequency is determined, the inductance value is selected according to the following formula:

$$L=\frac{(V_{IN}-V_O)\times V_O}{2\times V_{IN}\times F_S\times I_{ripple}}$$

Use the following equation to calculate the RMS and peak currents through the inductor. It is essential that the inductor is rated to handle these currents.

$$i_{L(RMS)}=\sqrt{I_{LED}^2+\frac{\Delta I_L^2}{12}}$$

$$i_{LPeak}=I_{LED}+\frac{\Delta I_L}{2}=I_{LED}+I_{ripple}$$

6.5 Bootstrap Capacitor Selection

The bootstrap capacitor biases the high-side gate driver during the on-time of the high-side MOSFET. The required capacitance depends on the PWM dimming frequency (PWMFREQ) and is sized to prevent boot undervoltage and faults during PWM dimming operation. The bootstrap capacitance (C_{BST}) is calculated using the following equation.

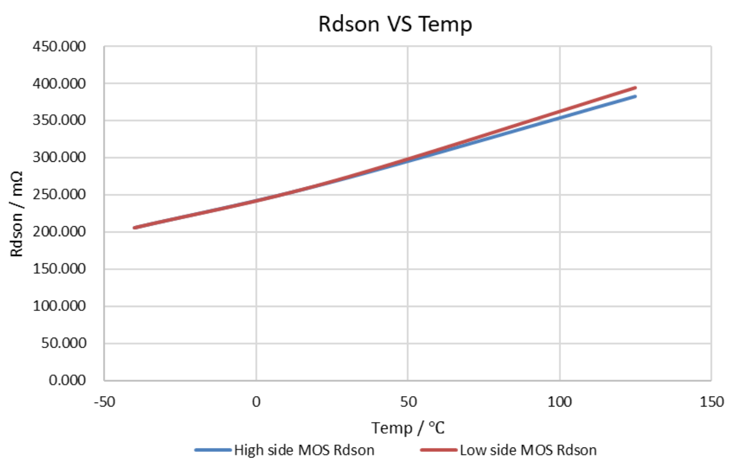
$$C_{BST} = \frac{I_{Q\_BSTx}}{(V_{V5D} + V_{BST(HYS)} - V_{BSTxUV}) \times PWM_{FREQ}}$$

6.6 CSN Protection Diode

An external Schottky diode is selected to protect the CSP/CSN node by clamping the negative voltage during short circuit transients. The Schottky diode should be chosen based on the length of the cable harness and the selection of the output capacitor. A Schottky diode with a low forward voltage drop at room temperature and a nonrepetitive peak surge current rating of 10 A for a duration of 5 µs is recommended. The diode should be positioned close to the CSN pin.

6.7 Rdson of Internal MOS

The characteristic curve of the Rdson of the internally integrated MOS in SA33766 varying with temperature is as follows:

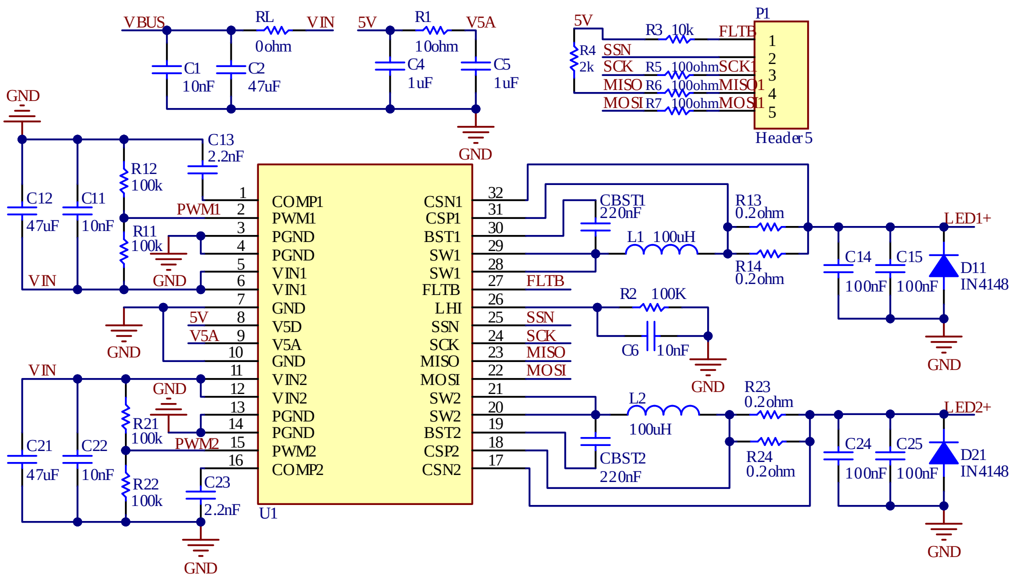


7. Application Example

7.1 Design Specification

Input Voltage (V)	LED Current (A)	VLED (V)	Switching Freqency(kHz)
55	1	40	400

7.2 Schematic



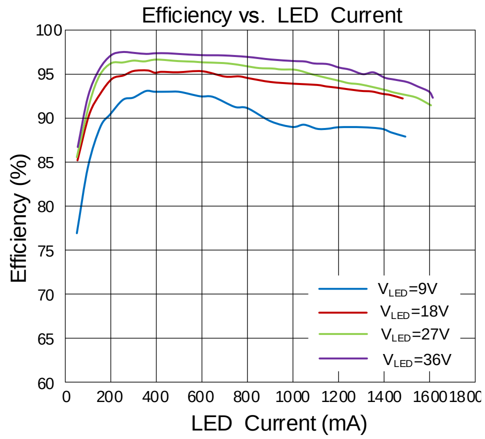
7.3 BOM List

Designator	Comment	Description	LibRef	Quantity
U1	SA33766	2 Channle Buck CC LED Driver	SA33766	1
C2, C12, C21	47uF, 100V	Ceramic Capacitor	1206C	3
C1, C11, C22	10nF, 100V	Ceramic Capacitor	0805C	3
C4, C5	1uF, 50V	Ceramic Capacitor	0805C	2
R1	10ohm	SMD Resistor	0805R	1
R2	100k	SMD Resistor	0805R	1
R3	10k	SMD Resistor	0805C	1
R4	2k	SMD Resistor	0805C	1
R5, R6, R7	100ohm	SMD Resistor	0805C	3
RL	0ohm	SMD Resistor	1206R	1
R11, R12, R21, R22	100k	SMD Resistor	0805R	4
C13, C23	2.2nF, 25V	SMD Resistor	0805C	2
C14, C15, C24, C25	100nF, 100V	Ceramic Capacitor	0805C	2
R13, R14, R23,R24	0.1ohm	SMD Resistor	0805R	2
L1, L2	100uH	Inductor	0608H	2
CBST1, CBST2	220nF, 25V	Ceramic Capacitor	0805C	2
C6	10nF, 25V	Ceramic Capacitor	0805C	1
D11, D21	IN4148	Diode	Diode	2

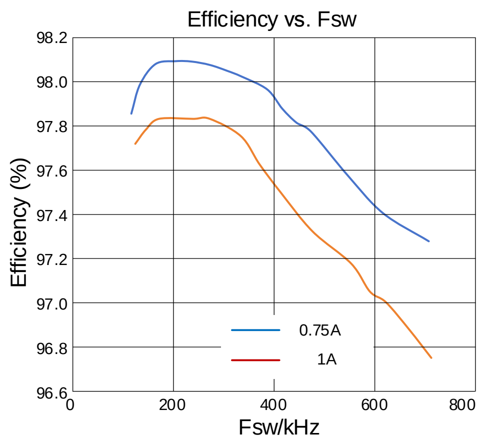
7.4 Operation Performance

7.4.1 Efficiency

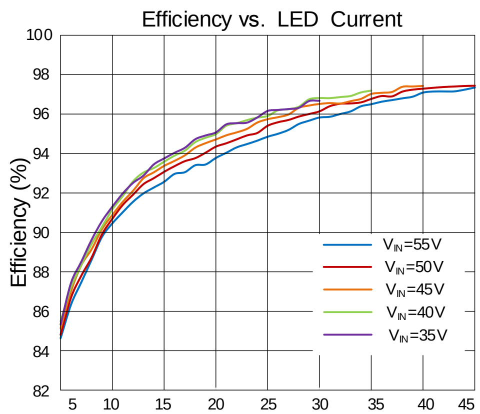
Test condition: V_{IN}=60V, Fsw=400kHz



Test condition: V_{IN}=60V, V_{LED}=45V

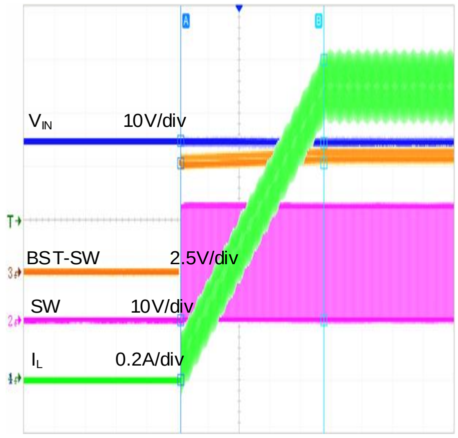


Test condition: I_{LED}=1A

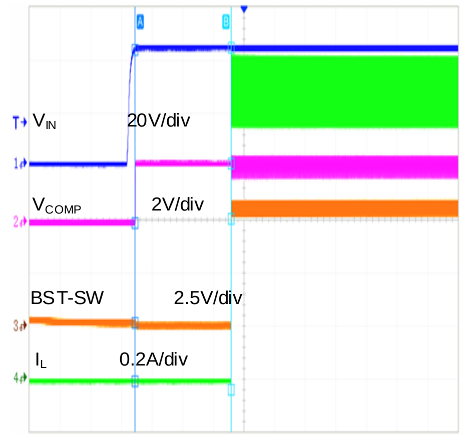


7.4.2 Start Up

Test condition: V_{IN}=45V, V_{LED}=18V, I_{LED}=1A



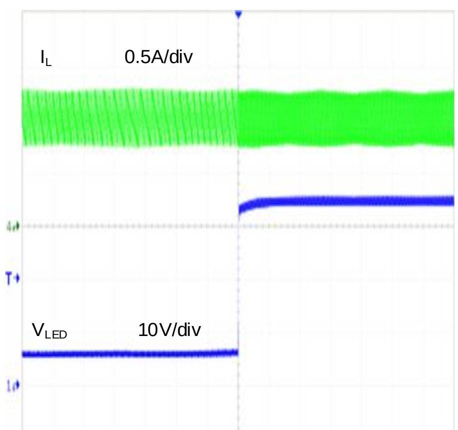
Time (1ms/div)



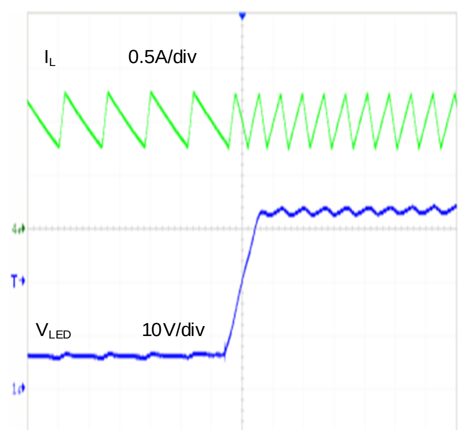
Time (500ms/div)

7.4.3 Load Transient

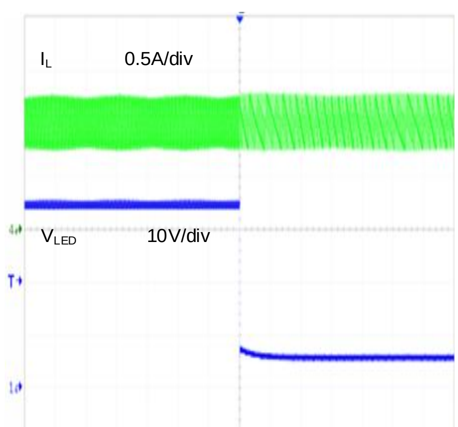
Test condition: V_{IN}=55V, V_{LED}=6V-36V, I_{LED}=1A



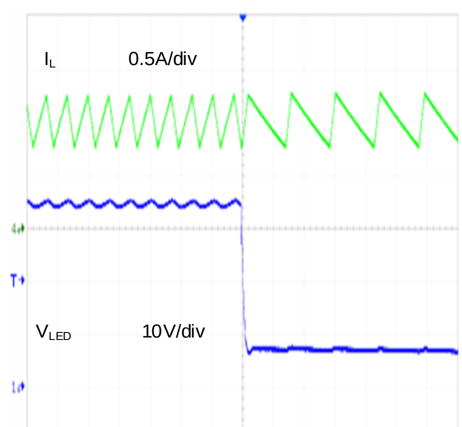
Time (200µs/div)



Time (5µs/div)



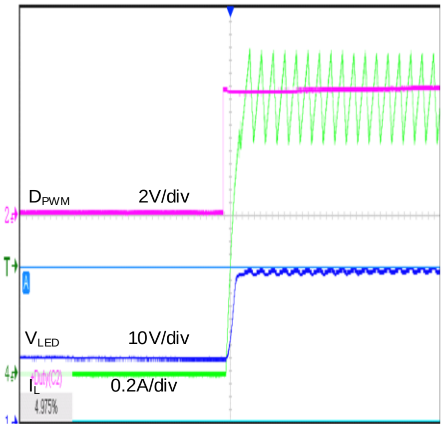
Time (200µs/div)



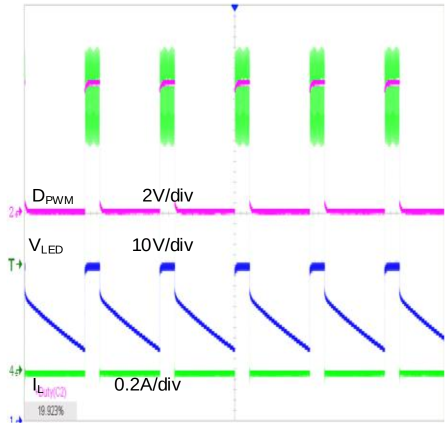
Time (5µs/div)

7.4.4 PWM Dimming

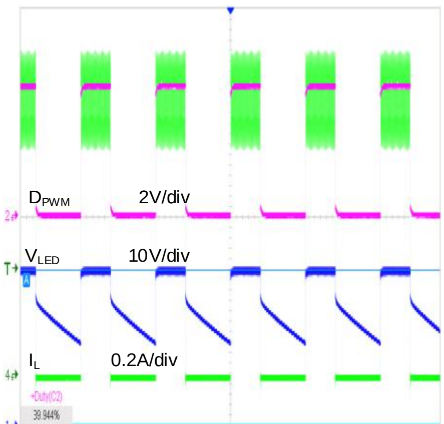
Test condition: V_{IN}=45V, V_{LED}=28V, I_{LED}=1A, F_{PWM}=200Hz



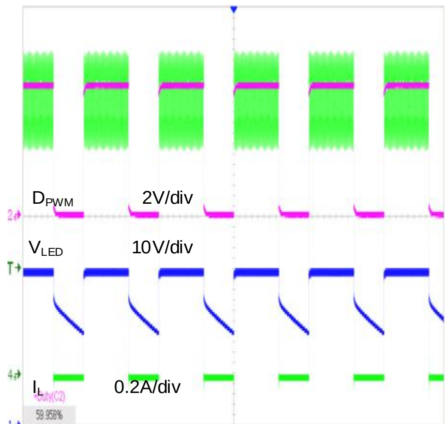
Time (2ms/div)



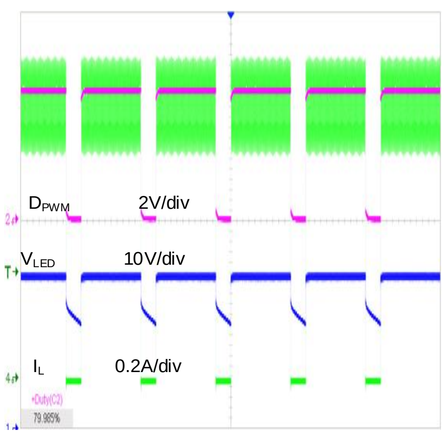
Time (2ms/div)



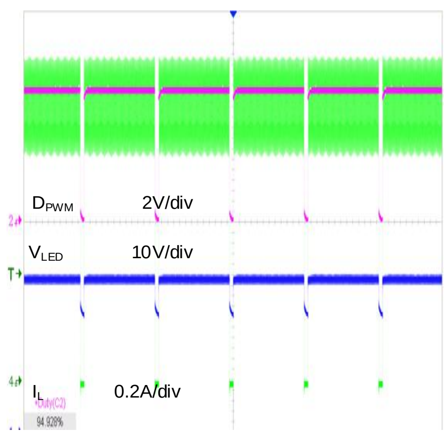
Time (2ms/div)



Time (2ms/div)



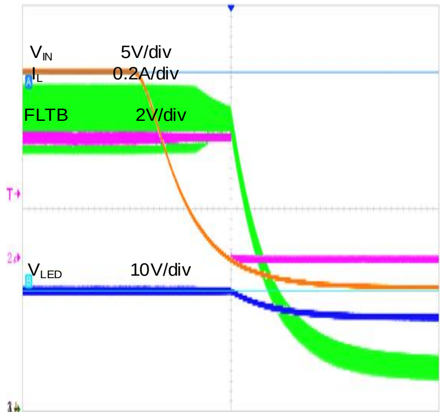
Time (2ms/div)



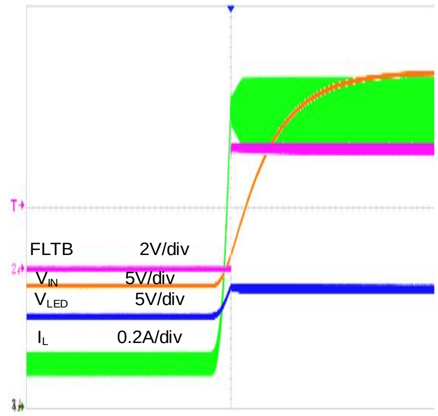
Time (2ms/div)

7.4.5 Over LED Voltage Protection

Test condition: V_{IN}=45V, V_{LED}=23V, I_{LED}=1A



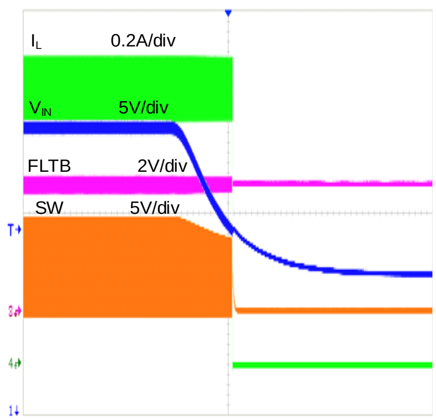
Time (20ms/div)



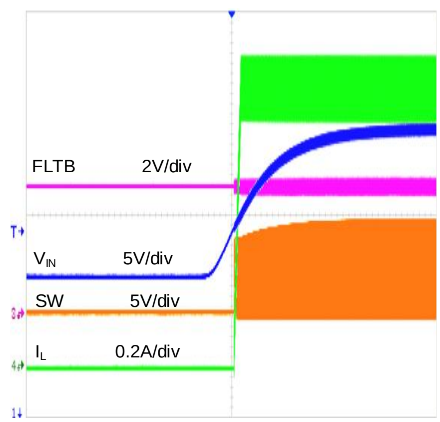
Time (20ms/div)

7.4.6 VIN Under Voltage Protection

Test condition: V_{IN}=45V, V_{LED}=23V, I_{LED}=1A



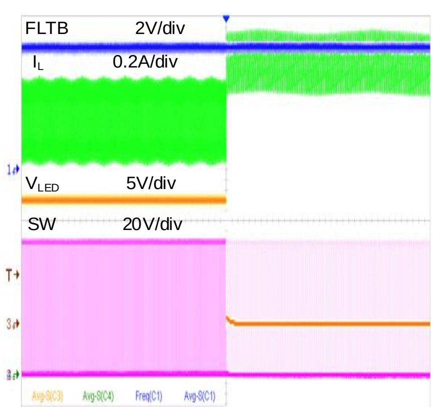
Time (20ms/div)



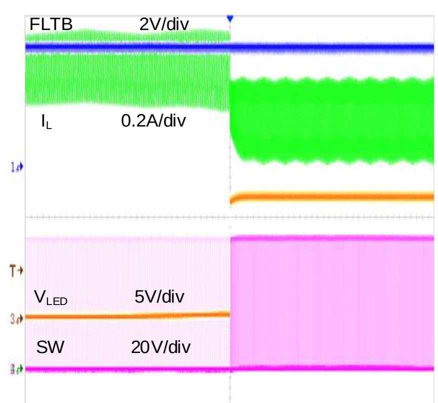
Time (20ms/div)

7.4.7 LED Short Protection

Test condition: V_{IN}=45V, V_{LED}=18V, I_{LED}=1A



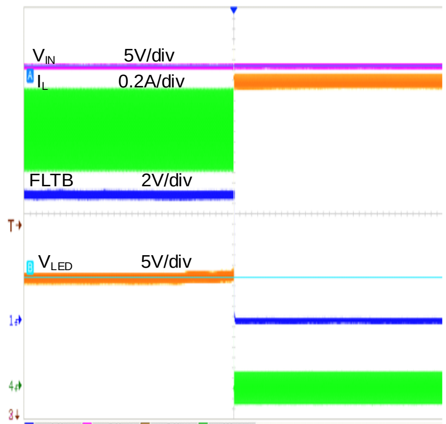
Time (500µs/div)



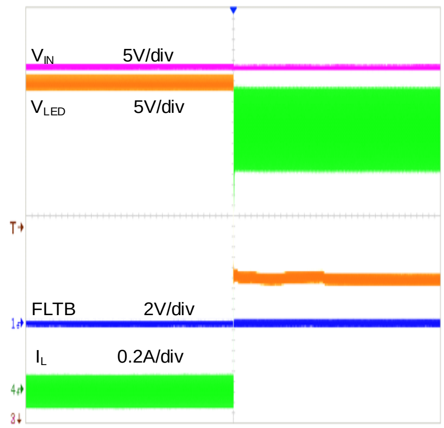
Time (500µs/div)

7.4.8 LED Open Protection

Test condition: V_{IN}=45V, V_{LED}=18V, I_{LED}=1A



Time (10ms/div)

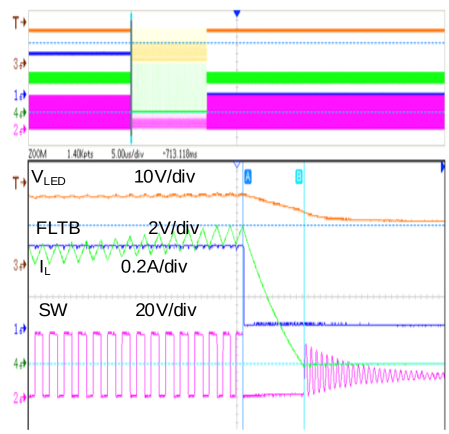


Time (10ms/div)

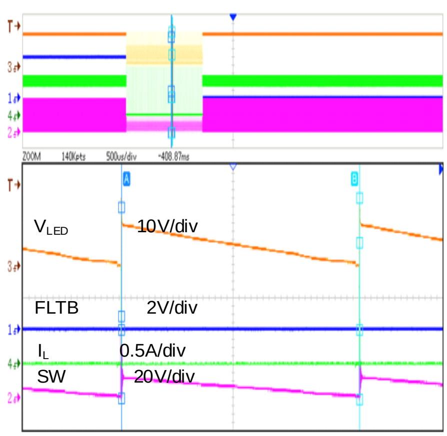
7.4.9 High Side Switch Current Limit

Test condition: V_{IN}=45V, V_{LED}=18V, I_{LED}=1A, IFT[1:0]=00

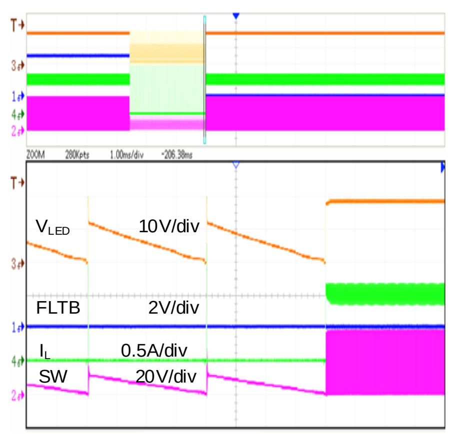
Time (200ms/div)



Time (200ms/div)



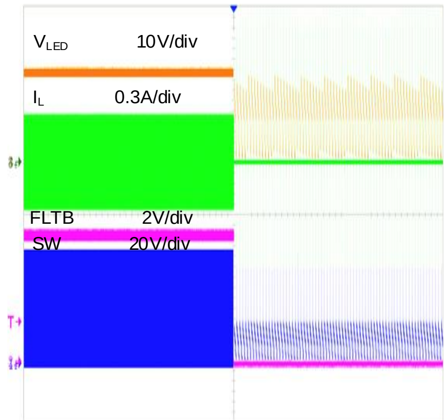
Time (200ms/div)



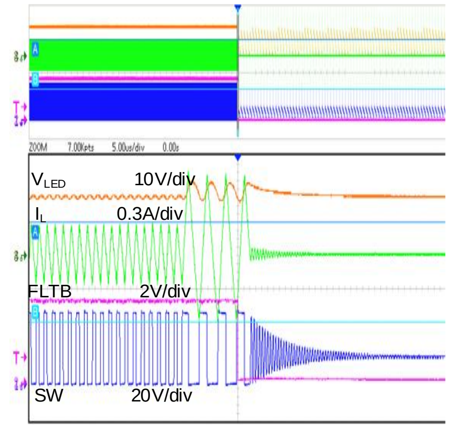
Time (200ms/div)

7.4.10 Low Side Switch Current Limit

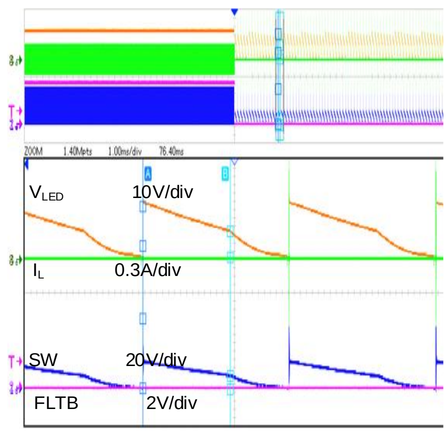
Test condition: V_{IN}=45V, V_{LED}=24V, I_{LED}=1A, IFT[1:0]=00



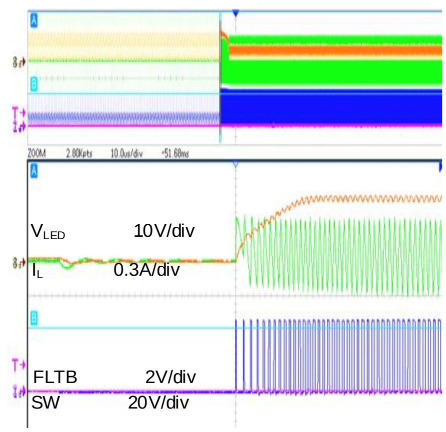
Time (50ms/div)



Time (50ms/div)



Time (50ms/div)



Time (50ms/div)

8 Layout Design

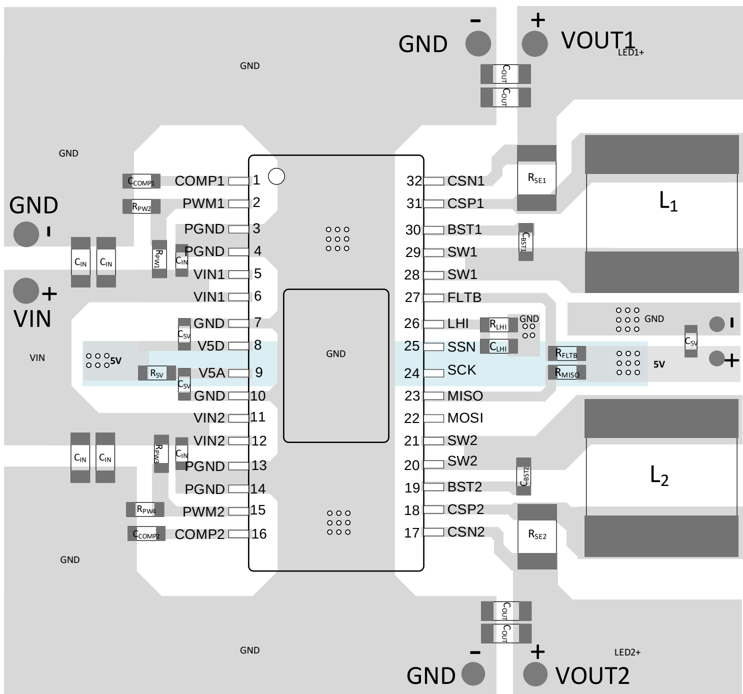
Follow these layout guidelines for optimal performance:

Power Stage:

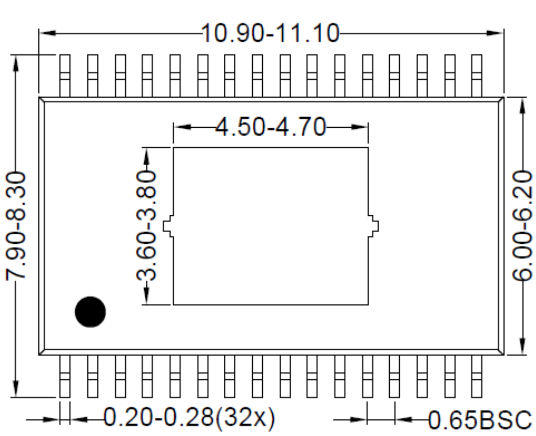
- Place the BUCK components as close together as possible to minimize the current loop. Minimize the loop area for high-frequency return currents.
- The grounding of the input and output capacitors should be placed in close proximity to enhance EMC performance.
- Use ground plane in one of the middle layers for noise shielding.

Chip Level:

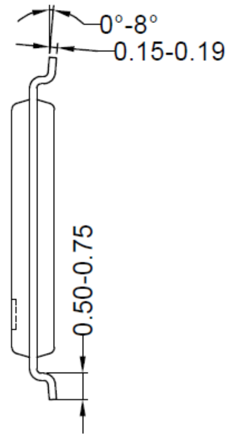
- Place the V5A, V5D capacitor as close as possible to the chip's V5A, V5D pin
- Differentially route the CSP and CSN pins to sense resistor. Route the traces away from noisy nodes, preferably through a layer on the other side of a shielding/ground layer.
- Place a ceramic high-frequency bypass capacitor as close as possible to the VIN pin and PGND pin.



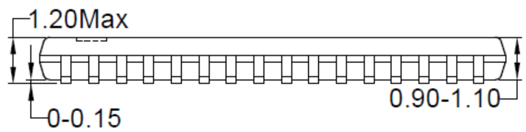
TSSOP32E-UP Package Outline Drawing



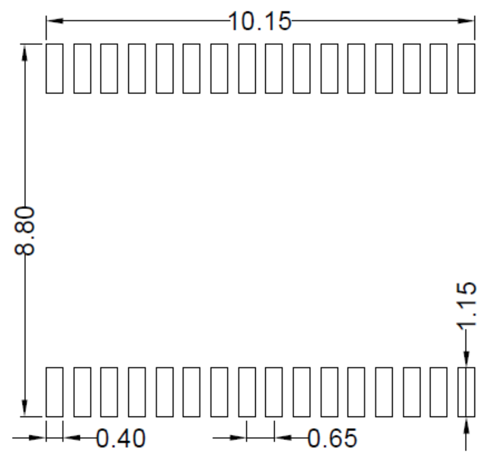
Top View



Side View



Front View



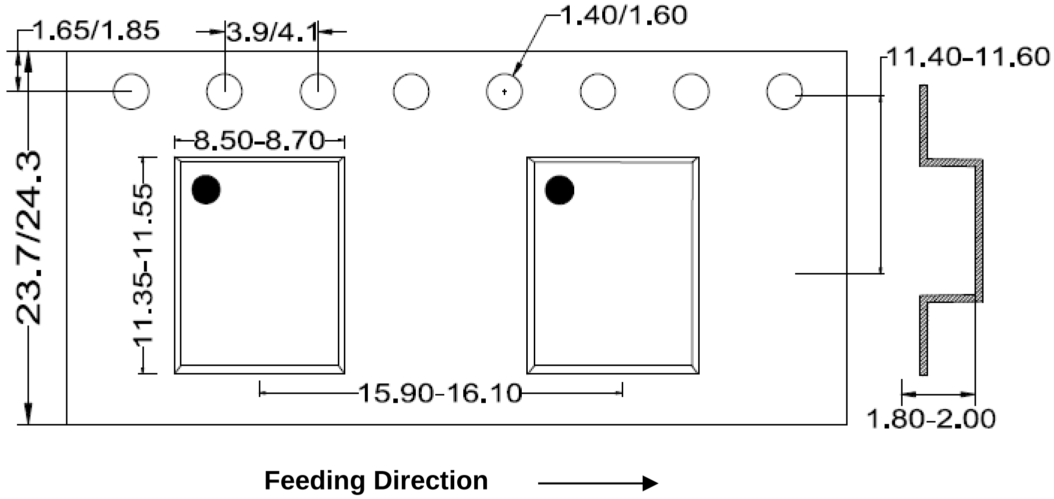
Recommended PCB Layout (Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

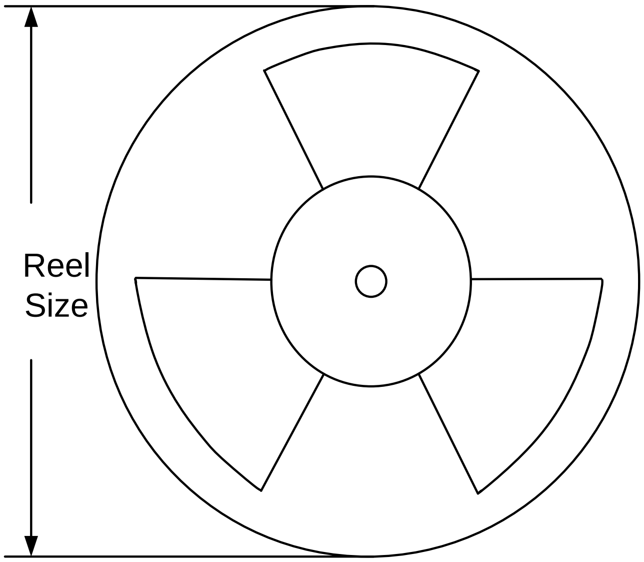
Taping & Reel Specification

1. Taping Orientation

TSSOP32E



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
TSSOP32E	24	16	13"	800	800	2000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
December 29,2025	Revision 1.0	Initial Release

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