SA21803A

Single Channel, Smart High-Side Power Switch

General Description

The SA21803A is a 50mΩ smart high-side power switch with single channel, mainly providing overload protection and signal diagnostics. The power switch is an N-channel vertical power MOSFET with charge pump.

The package type of SA21803A is TSOP14E with exposed pads. The main purpose of SA21803A is to drive lamps up to P21W 24V and LEDs in the tough automotive environment.

Applications

- Suitable for Resistive, Inductive and Capacitive Loads
- Replaces Electromechanical Relays, Fuses and Discrete Circuits
- Most Suitable for Loads with High Inrush Current, Such as Lamps
- Suitable for 12V and 24V Truck and Transportation System

Features

- AEC-Q100/ Q104 Qualified for Automotive Applications
- One Channel Device
- Very Low Shutdown Current
- 3.3V and 5V Compatible Logic Inputs
- Logic Ground Independent from Load Ground
- Very Low Power DMOS Leakage Current in OFF State
- Diagnostic Functions
  - ✧ Proportional Load Current Sense
  - ✧ Open Load in OFF State
  - ✧ Short Circuit to Battery and Ground
  - ✧ Over Temperature
  - ✧ Stable Diagnostic Signal During Short Circuit
  - ✧ Enhanced k_{ILIS} Dependency with Temperature and Load Current
- Protection Functions
  - ✧ Stable Behavior during Under Voltage
  - ✧ Reverse Polarity Protection with External Components
  - ✧ Secure Load Turn-off during Logic Ground Disconnect with External Components
  - ✧ Over Temperature Protection with Latch
  - ✧ Overvoltage Protection with External Components
  - ✧ Voltage Dependent Current Limitation
  - ✧ Enhanced Short Circuit Operation

Typical Applications

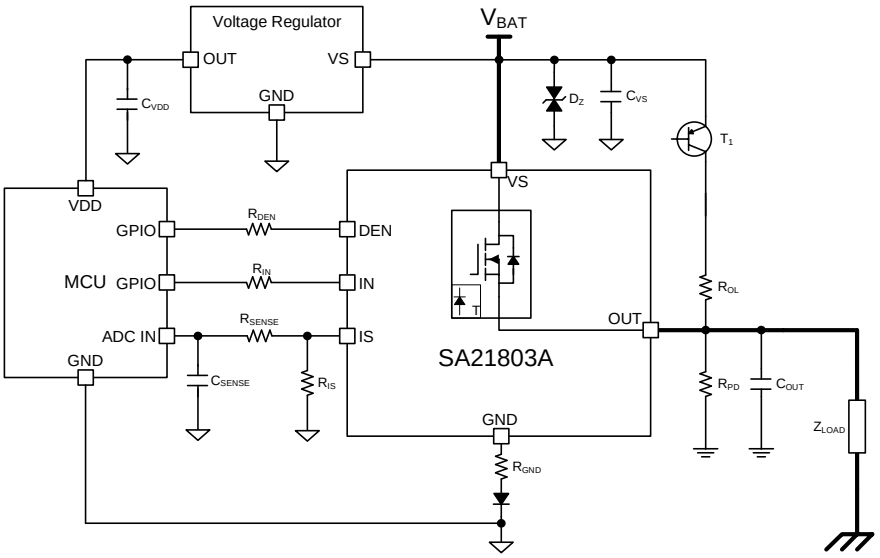


Figure.1 Schematic Diagram

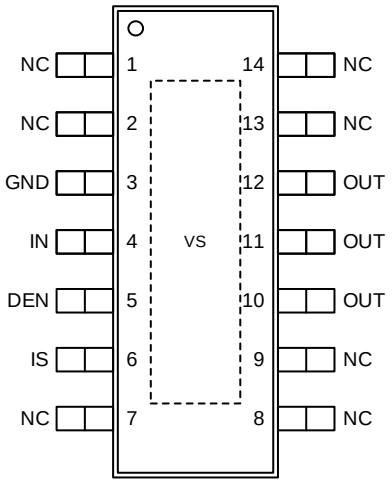
Ordering Information

Ordering Part Number	Package Type	Top Mark
SA21803AHTP	TSOP14E RoHS Compliant and Halogen Free	**FDH*xyz***

Device code: FDH

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Number	Symbol	Pin Description
Cooling Tab	VS	**Voltage Supply;** Battery voltage.
1, 2, 7, 8, 9, 13, 14	NC	**Not Connected;** No internal connection to the chip.
3	GND	**Ground;** Ground connection.
4	IN	**Input Channel;** Input signal for channel activation. If not used, connected with a 15kΩ resistor either to the GND pin or to the module ground.
5	DEN	**Diagnostic Enable;** Digital signal to enable/disable the diagnosis of the device. If not used, connected with a 15kΩ resistor either to the GND pin or to the module ground.
6	IS	**Sense;** Current sense. If not used, connected with a 15kΩ resistor either to the GND pin or to the module ground.
10, 11, 12	OUT	**Output;** Protected high side power output channel. All output pins must be connected together on the PCB. All pins of the output are internally connected together. PCB traces have to be designed to withstand the maximum current which can flow.

Block Diagram

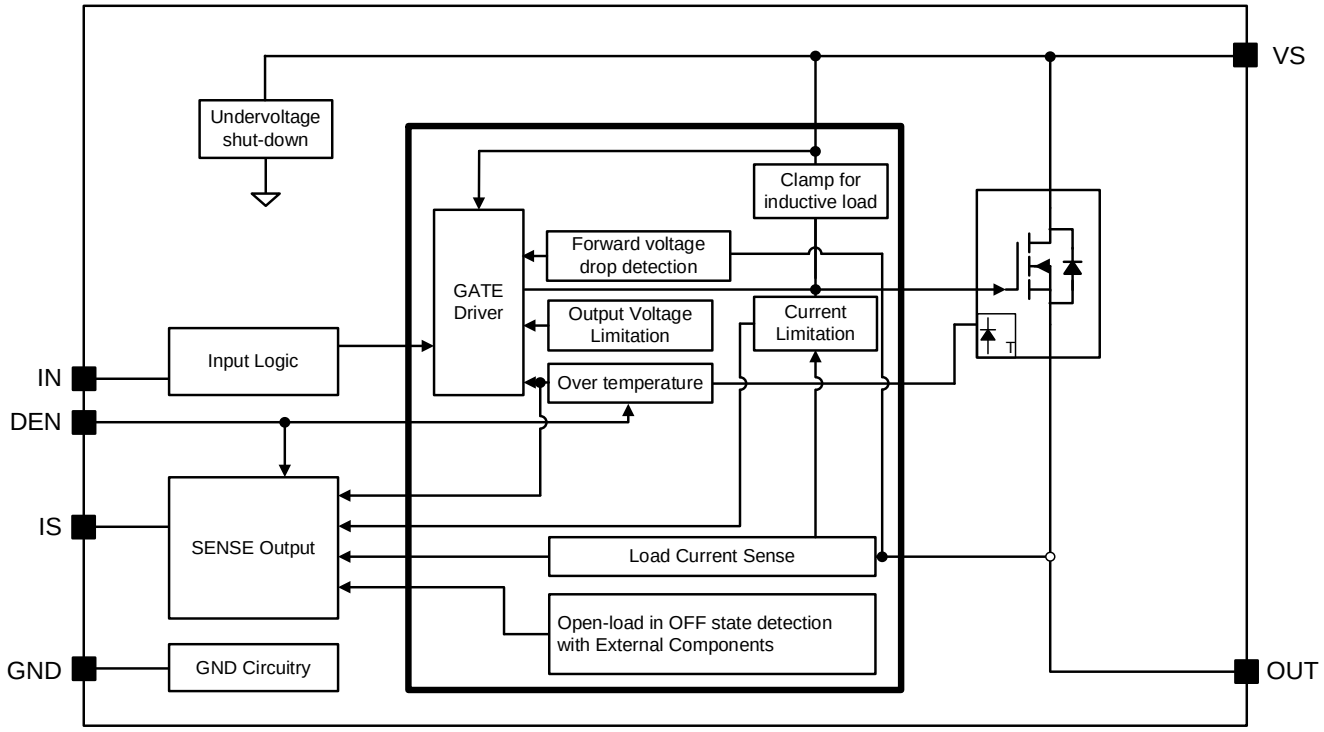


Figure2. Block Diagram

Current and Voltage Conventions

Figure3 shows all terms used in this data sheet, with associated convention for positive values.

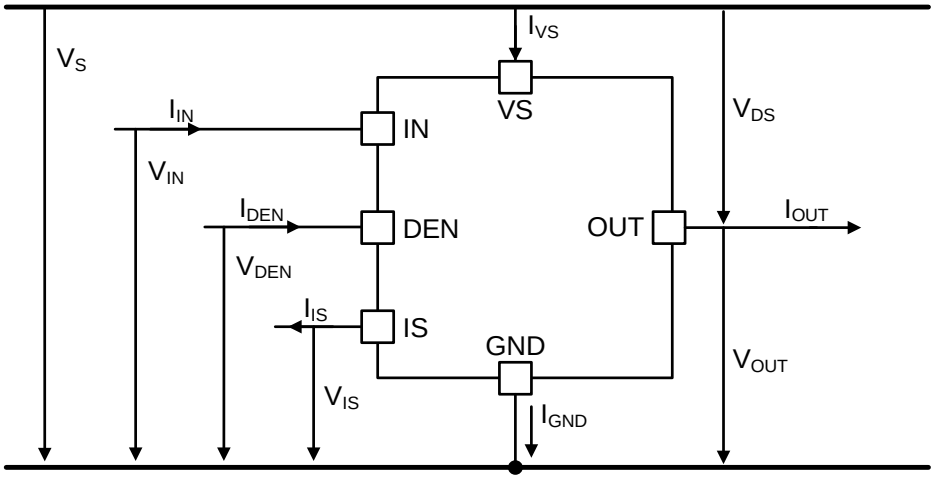


Figure3. Voltage and Current Definition

Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
VS	-0.3	48	V
VS Supply Voltage for Load Dump Protection ($V_{S(LD)}$ is Setup without the DUT Connected to the Generator per ISO 7637-1.)		65	
VS Supply Voltage for Short Circuit Protection		36	
VS Reverse Polarity Voltage(t< 2min, T_A=25°C, R_L≥12Ω, R_{GND}=150Ω)		-28	
IN, DEN, IS	-0.3	Vs	
Voltage at Power Transistor (V_{DS})		65	
Permanent Short Circuit IN Pin toggles (V_S=28V)		100k	cycles
IN, DEN Input Current	-2	2	mA
IS Input Current	-25	50	
Load Current		$I_{L(LIM)}$	
GND Pin Current	-20	20	mA
GND Pin Current (t<2min)	-200	20	
Maximum Energy Dissipation Single Pulse (V_S=28V, I_L=4.5A, T_J=125°C)		38	mJ
Lead Temperature (Soldering, 10 sec.)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	19	°C/W
$\theta_{JC\_(BOTTOM)}$ Junction-to-case Thermal Resistance (Bottom)	2	
P_D Power Dissipation T_A=85°C	2.11	W

ESD Susceptibility

Parameter	Min	Max	Unit
HBM (Human Body Mode)			
HBM (all pins)	-2	+2	kV
HBM (OUT pin vs. GND and V_S connected)	-4	+4	
CDM (Charged Device Mode)			
CDM (all pins)	-500	+500	V
CDM (corner pins)	-750	+750	

Recommended Operating Conditions

Parameter	Min	Max	Unit
VS	8	36	V
IN, DEN	0	Vs	
IS	-0.3	V_S–(V_S-$V_{IS(RANGE)}$)	
Operating Junction Temperature	-40	125	°C

Electrical Characteristics

(V_S=8V to 36V, T_J=-40°C to +125°C, unless otherwise specified. The values are guaranteed by test, design or statistical correlation. Typical values are given at V_S=28V, T_J=25°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Functional Range						
Nominal Operating Voltage	V_{NOM}		8	28	36	V
Extended Operating Voltage	$V_{S(OP)}$	V_{IN}=4.5V, R_L=12Ω, V_{DS}<0.5V (Note 3)	5		48	V
Minimum Functional Supply Voltage	$V_{S(OP)\_MIN}$	V_{IN}=4.5V, R_L=12Ω, From I_{OUT}=0A to V_{DS}<0.5V	3.8	4.3	5	V
Under Voltage Shutdown	$V_{S(UV)}$	VIN=4.5V, V_{DEN}=0V, R_L=12Ω, From V_{DS}<1V to I_{OUT}=0A	3	3.5	4.1	V
Under Voltage Shutdown Hysteresis	$V_{S(UV)\_HYS}$			850		mV
Operating Current Channel Active	I_{GND_1}	V_{IN}=5.5V, V_{DEN}=5.5V, Device in $R_{DS(ON)}$, V_S=36V		2.5	4	mA
Shutdown Current for Whole Device with Load (Ambient)	$I_{S(OFF)}$	V_S=36V, V_{OUT}=0V, V_{IN} floating, V_{DEN} floating, T_J≤85°C			5	μA
Maximum Shutdown Current for Whole Device with Load	$I_{S(OFF)\_125}$	V_S=36V, V_{OUT}=0V, V_{IN} floating, V_{DEN} floating, T_J=125°C		2	15	μA
Shutdown Current for Whole Device with Load, Diagnostic Active	$I_{S(OFF\_DEN)}$	V_S=36V, V_{OUT}=0V, V_{IN} floating, V_{DEN}=5.5V	0.3	0.9	1.5	mA
Power Stage						
ON-state Resistance	$R_{DS(ON)\_125}$	I_L=I_{L4}=1A, V_{IN}=4.5V, T_J=125°C	50	60	70	mΩ
ON-state Resistance	$R_{DS(ON)\_25}$	T_J=25°C		38		mΩ
Nominal Load Current	$I_{L(NOM)}$	T_A=85°C, T_J<125°C (Note 3)		4.5		A
Output Voltage Drop Limitation at Small Load Currents	$V_{DS(NL)}$	I_L=I_{L0}=50mA		10	22	mV
Drain to Source Clamping Voltage $V_{DS(AZ)}$=[V_S-V_{OUT}]	$V_{DS(AZ)}$	I_{DS}=20mA	65	72	81	V
Output Leakage Current, T_J≤85°C	$I_{L(OFF)}$	V_{IN} floating, V_{OUT}=0V, T_J≤85°C		0.05	0.5	μA
Output Leakage Current, T_J=125°C	$I_{L(OFF)\_125}$	V_{IN} floating, V_{OUT}=0V, T_J=125°C		2	10	μA
Slew Rate 30% to 70% V_S	dV/dt_{ON}	R_L=12Ω, V_S=28V	0.3	0.8	1.4	V/μs
Slew Rate 70% to 30% V_S	$-dV/dt_{OFF}$	R_L=12Ω, V_S=28V	0.3	0.8	1.4	V/μs
Slew Rate Matching dV/dt_{ON}-dV/dt_{OFF}	ΔdV/dt	R_L=12Ω, V_S=28V	-0.15	0	0.15	V/μs
Turn-On Time to V_{OUT}=90% V_S	t_{ON}	R_L=12Ω, V_S=28V	20	100	150	μs
Turn-Off Time to V_{OUT}=10% V_S	t_{OFF}	R_L=12Ω, V_S=28V	20	100	150	μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Turn-On/Off Matching t_{OFF}-t_{ON}	Δt_{SW}	R_L=12Ω, V_S=28V	-50	0	50	μs
Turn-On Time to V_{OUT}=10% V_S	t_{ON_delay}	R_L=12Ω, V_S=28V		30	70	μs
Turn-Off Time to V_{OUT}=90% V_S	t_{OFF_delay}	R_L=12Ω, V_S=28V		30	70	μs
Switch ON Energy	E_{ON}	R_L=12Ω, V_{OUT}=90% V_S, V_S=36V (Note 3)		0.6		mJ
Switch OFF Energy	E_{OFF}	R_L=12Ω, V_{OUT}=10% V_S, V_S=36V (Note 3)		0.7		mJ
Loss of Ground						
Output Leakage Current While GND Disconnected	$I_{OUT(GND)}$	All pins are disconnected except VS and OUT, V_S=48V (Note 3)		0.1		mA
Reverse Polarity						
Drain Source Diode Voltage During Reverse Polarity	$V_{DS(REV)}$	I_L=-2A, T_J=125°C	200	610	700	mV
Overvoltage						
Overvoltage Protection	$V_{S(AZ)}$	I_{SOV}=5mA	65	72	81	V
Overload Condition						
Load Current Limitation	$I_{L5(SC)}$	V_{DS}=5V (Note 3)	38	47	56	A
Load Current Limitation	$I_{L28(SC)}$	V_{DS}=42V (Note 3)		22		A
Dynamic Temperature Increase While Switching	$\Delta T_{J(SW)}$			60		K
Thermal Shutdown Temperature	$T_{J(SC)}$		150	170	190	°C
Thermal Shutdown Hysteresis	$\Delta T_{J(SC)}$	(Note 3)		20		K
Load Condition Threshold for Diagnostic						
Open Load Detection Threshold in OFF State	V_S-$V_{OL(OFF)}$	V_{IN}=0V, V_{DEN}=4.5V	4		6	V
Open Load Detection Threshold in ON State	$I_{L(OL)}$	V_{IN}=V_{DEN}=4.5V, $I_{IS(OL)}$=25μA	10		65	mA
Sense Pin						
IS Pin Leakage Current When Sense Is Disabled	$I_{IS\_(DIS)}$	V_{IN}=4.5V, V_{DEN}=0V, I_L=I_{L4}=4A			1	μA
Sense Signal Saturation Voltage	V_S-$V_{IS\ (RANGE)}$	V_{IN}=0V, V_{OUT}=V_S>10V, V_{DEN}=4.5V, I_{IS}=6mA	1		3.5	V
Sense Signal Maximum Current in Fault Condition	$I_{IS(FAULT)}$	V_{IS}=V_{IN}=0V, V_{OUT}=V_S>10V, V_{DEN}=4.5V	6	15	40	mA
Sense Pin Maximum Voltage	$V_{IS(AZ)}$	I_{IS}=5mA, V_{IN}=V_{DEN}=0V, Measure V_S-V_{IS}	65	72	81	V
Current Sense Ratio Signal in the Nominal Area, Stable Load Current Condition						
Current Sense Ratio I_{L0}=50mA	k_{ILIS0}	V_{IN}=4.5V, V_{DEN}=4.5V, T_J=-40°C, T_J=125°C	-50%	1600	70%	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Sense Ratio I_{L1}=0.5A	k_{ILIS1}	V_{IN}=4.5V, V_{DEN}=4.5V, T_J=-40°C, T_J=125°C	-25%	1500	25%	
Current Sense Ratio I_{L2}=1A	k_{ILIS2}	V_{IN}=4.5V, V_{DEN}=4.5V, T_J=-40°C, T_J=125°C	-12%	1500	12%	
Current Sense Ratio I_{L3}=2A	k_{ILIS3}	V_{IN}=4.5V, V_{DEN}=4.5V, T_J=-40°C, T_J=125°C	-9%	1500	9%	
Current Sense Ratio I_{L4}=4A	k_{ILIS4}	V_{IN}=4.5V, V_{DEN}=4.5V, T_J=-40°C, T_J=125°C	-8%	1500	8%	
k_{ILIS} Derating with Current and Temperature	Δk_{ILIS}	k_{ILIS3} versus k_{ILIS2}	-5	0	5	%
Diagnostic Timing in Normal Condition						
Current Sense Settling Time to k_{ILIS} Function Stable After Positive Input Slope on Both IN and DEN	$t_{sIS(ON)}$	V_{IN}= V_{DEN}=0V to 4.5V, V_S=28V, R_{IS}=1.2kΩ, C_{SENSE}<100pF, I_L=I_{L3}=1A			150	µs
Current Sense Settling Time with Load Current Stable and Transition of the DEN	$t_{sIS(ON\_DEN)}$	V_{IN}=4.5V, V_{DEN}=0V to 4.5V, R_{IS}=1.2kΩ, C_{SENSE}<100pF, I_L=I_{L3}=1A			10	µs
Current Sense Settling Time to I_{IS} Stable After Positive Input Slope on Current Load	$t_{sIS(LC)}$	V_{IN}=4.5V, V_{DEN}=4.5V, R_{IS}=1.2kΩ, C_{SENSE}<100pF, I_L=I_{L2}=1A to I_{L3}=2A			20	µs
Diagnostic Timing in Open Load Condition						
Current Sense Settling Time to I_{IS} stable for Open Load Detection in OFF state	$t_{sIS(FAULT\_OL\_OFF)}$	V_{IN}=0V, V_{DEN}=0V to 4.5V, R_{IS}=1.2kΩ, C_{SENSE}<100pF, V_{OUT}=V_S=28V			100	µs
Current Sense Settling Time for Open Load Detection in ON-OFF Transition	$t_{sIS(FAULT\_OL\_ON\_OFF)}$	V_{IN}=4.5V to 0V, V_{DEN}=4.5V, R_{IS}=1.2kΩ, C_{SENSE}<100pF, V_{OUT}=V_S=28V; (Note 3)		200		µs
Diagnostic Timing in Overload Condition						
Current Sense Settling Time to I_{IS} Stable for Overload Detection	$t_{sIS(FAULT)}$	V_{IN}=V_{DEN}=0V to 4.5V, R_{IS}=1.2kΩ, C_{SENSE}<100pF, V_{DS}=24V; (Note 3)	0		150	µs
Current Sense Over Current Blanking Time	$t_{sIS(OC\_blank)}$	V_{IN}=V_{DEN}=4.5V, R_{IS}=1.2kΩ, C_{SENSE}<100pF, V_{DS}=5V to 0V (Note 3)		350		µs
Diagnostic Disable Time DEN Transition to I_{IS}<50% I_L/k_{ILIS}	$t_{sIS(OFF)}$	V_{IN}=4.5V, V_{DEN}=4.5V to 0V, R_{IS}=1.2kΩ, C_{SENSE}<100pF, I_L=I_{L3}=2A	0		20	µs
IN Pins Characteristics						
Low Level Input Voltage Range	$V_{IN(L)}$		-0.3		0.8	V
High Level Input Voltage Range	$V_{IN(H)}$		2		6	V
Input Voltage Hysteresis	$V_{IN(HYS)}$			250		mV
Low Level Input Current	$I_{IN(L)}$	V_{IN}=0.8V	1	10	25	µA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High Level Input Current	$I_{IN(H)}$	V_{IN}=5.5V	2	10	25	μA
DEN Pin						
Low Level Input Voltage Range	$V_{DEN(L)}$		-0.3		0.8	V
High Level Input Voltage Range	$V_{DEN(H)}$		2		6	V
Input Voltage Hysteresis	$V_{IDEN(HYS)}$			250		mV
Low Level Input Current	$I_{DEN(L)}$	V_{DEN}=0.8V	1	10	25	μA
High Level Input Current	$I_{DEN(H)}$	V_{DEN}=5.5V	2	10	25	μA

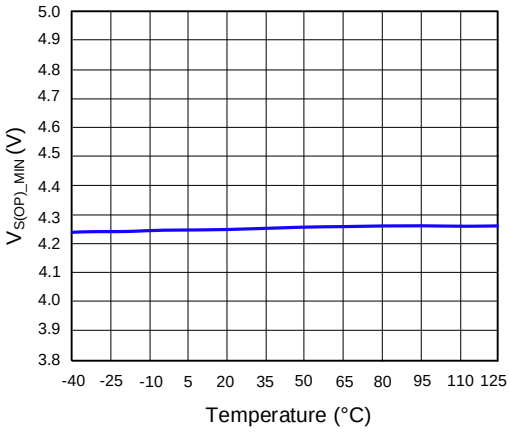
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured under the natural convection on a FR4 2s2p(with 600mm^2 cooper) board with thermal via of JEDEC51-3 thermal measurement standard. Please refer to Figure 4.

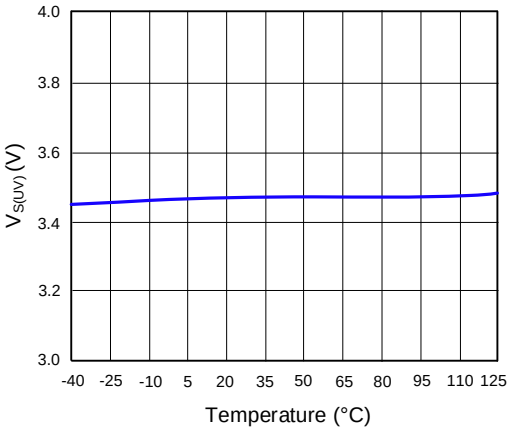
Note 3: This specification is guaranteed by design.

Typical Performance Characteristics

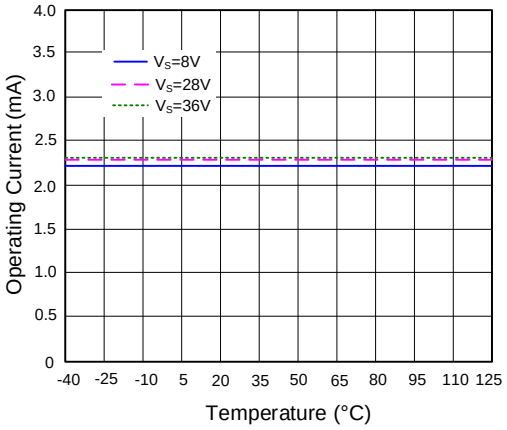
Minimum Functional Supply Voltage vs. Temperature
(V_{IN}=V_{DEN}=4.5V)



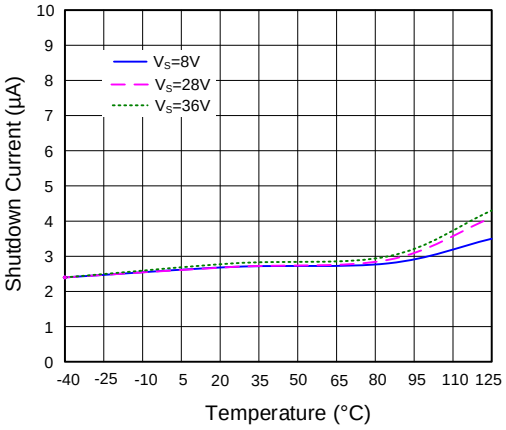
Under Voltage Shutdown vs. Temperature
(V_{IN}=V_{DEN}=4.5V)



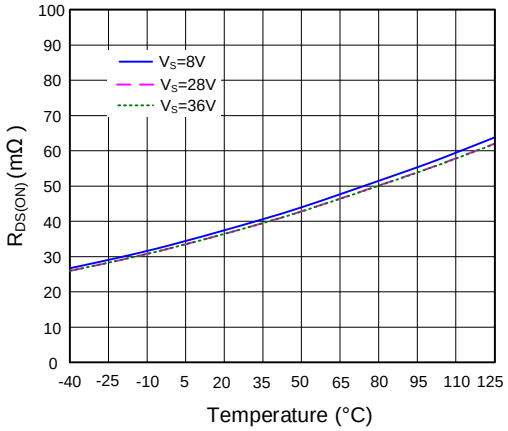
Operating Current vs. Temperature
(V_{IN}=V_{DEN}=5.5V, Null Load)



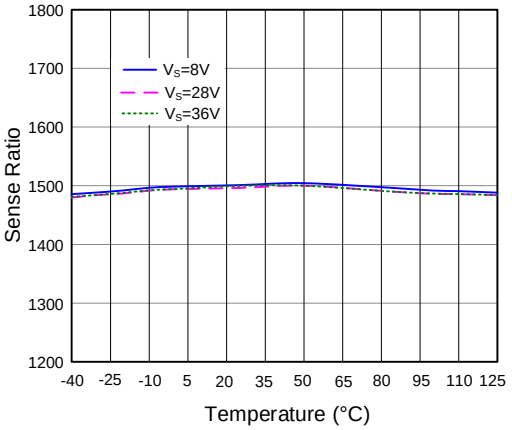
Shutdown Current vs. Temperature
(V_{IN}=V_{DEN}=0V, Null Load)



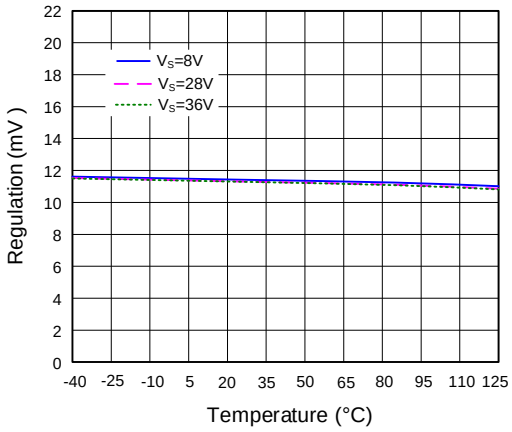
$R_{DS(ON)}$ vs. Temperature
(V_{IN}=5.5V, CC Load=1A)



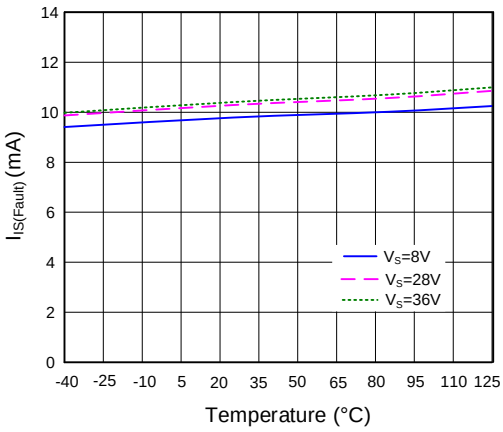
Sense Ratio vs. Temperature
(V_{IN}=5.5V, CC Load=4A)



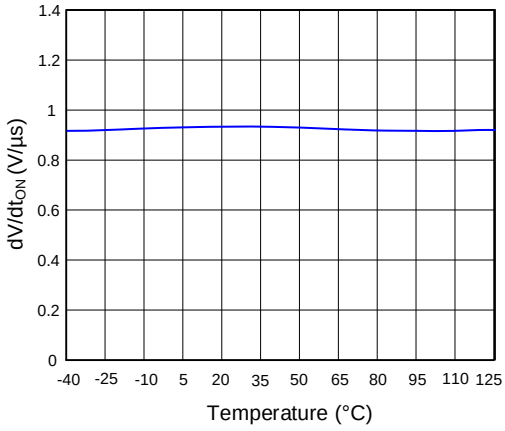
Regulation vs. Temperature
(V_{IN}=5.5V, CC Load=50mA)



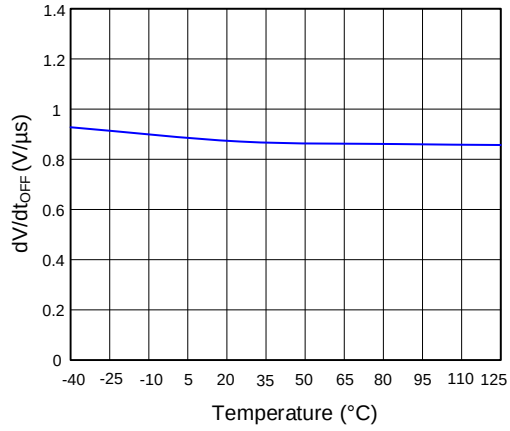
$I_{IS(Fault)}$ vs. Temperature
(V_S=V_{OUT}, V_{IN}=0V, V_{DEN}=5.5V)



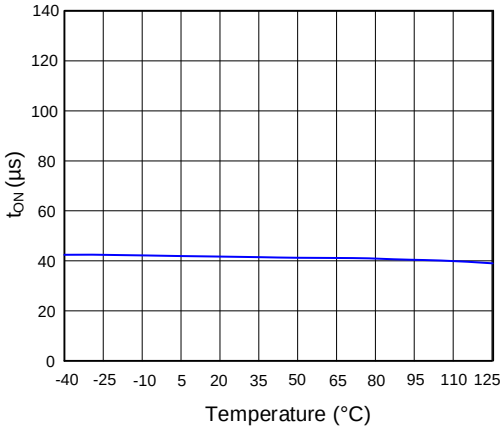
dV/dt_{ON} vs. Temperature
(V_S= 28V, V_{IN}=V_{DEN}=5.5V, R_{LOAD}=12Ω)



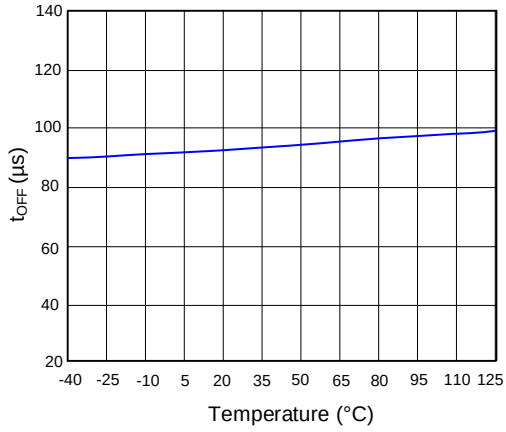
dV/dt_{OFF} vs. Temperature
(V_S= 28V, V_{IN}=V_{DEN}=5.5V, R_{LOAD}=12Ω)



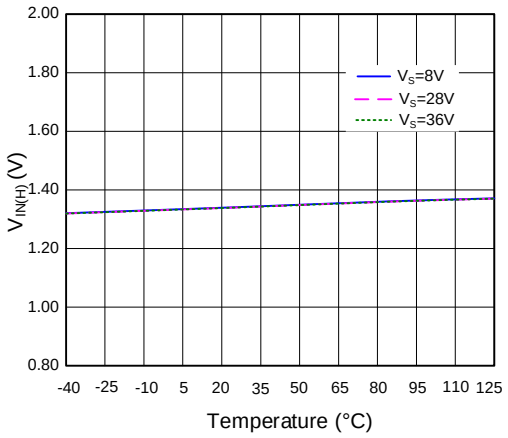
t_{ON} vs. Temperature
(V_S= 28V, V_{IN}=V_{DEN}=5.5V, R_{LOAD}=12Ω)



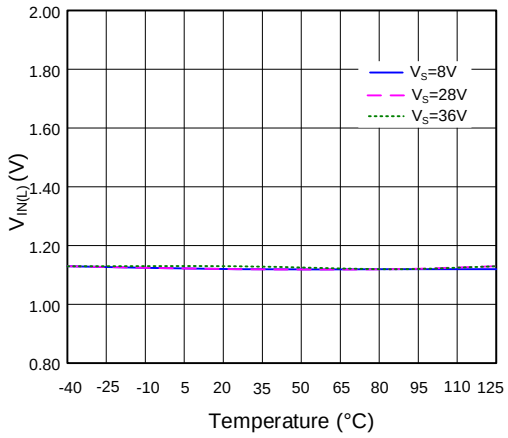
t_{OFF} vs. Temperature
(V_S= 28V, V_{IN}=V_{DEN}=5.5V, R_{LOAD}=12Ω)



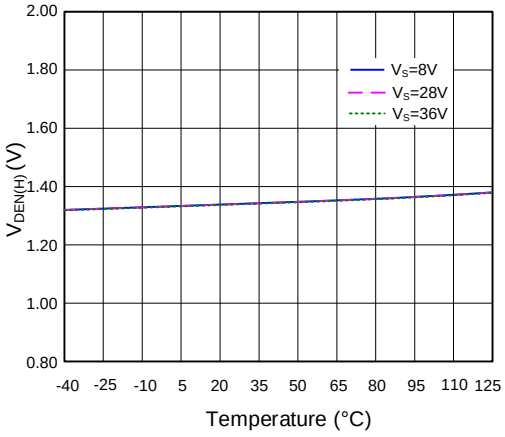
$V_{IN(H)}$ vs. Temperature



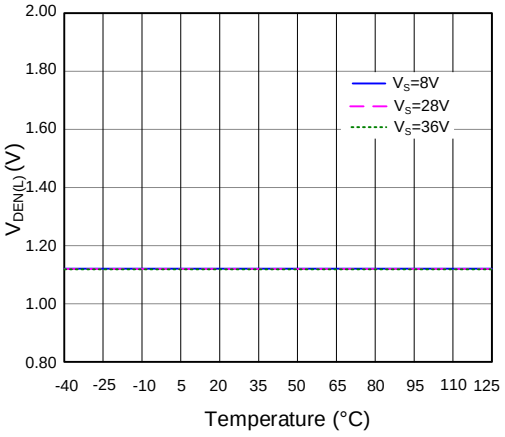
$V_{IN(L)}$ vs. Temperature



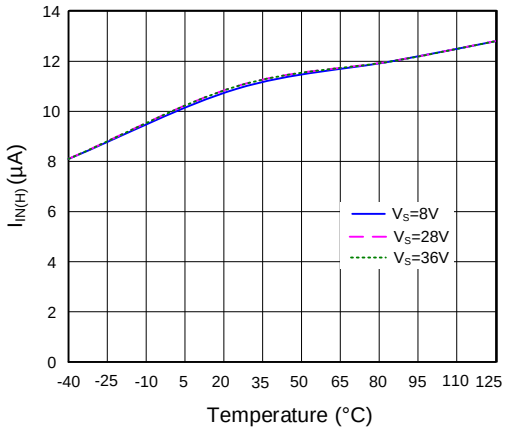
$V_{DEN(H)}$ vs. Temperature



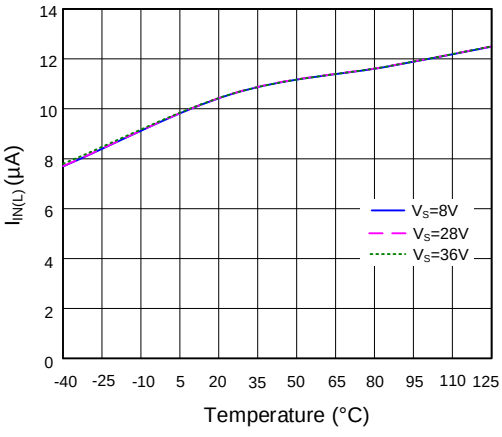
$V_{DEN(L)}$ vs. Temperature



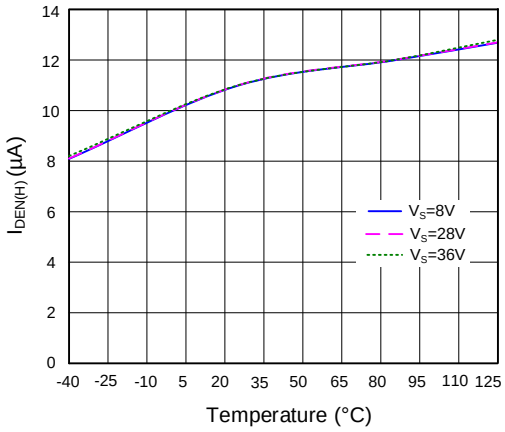
$I_{IN(H)}$ vs. Temperature
(V_{IN}=5.5V, Null Load)



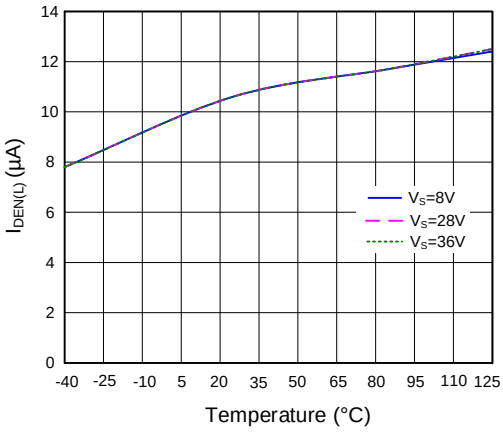
$I_{IN(L)}$ vs. Temperature
(V_{IN}=0.8V, Null Load)



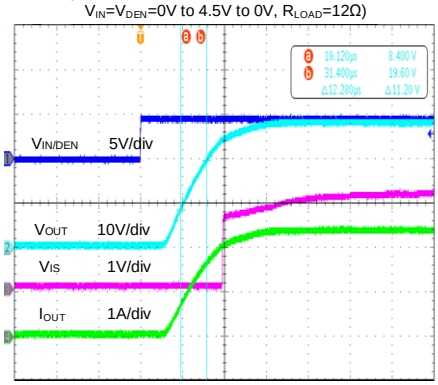
$I_{DEN(H)}$ vs. Temperature
(V_{DEN}=5.5V, Null Load)



$I_{DEN(L)}$ vs. Temperature
(V_{DEN}=0.8V, Null Load)

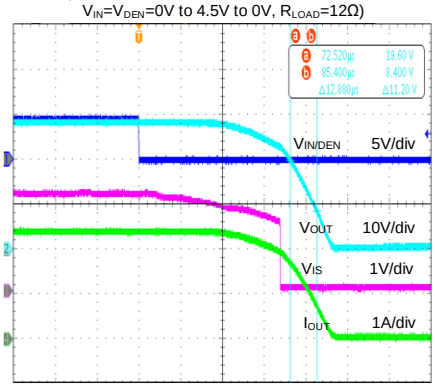


IN/DEN ON with Resistive Load
(V_S=28V, C_{VS}=100nF, C_{OUT}=Null ,R_{IS}=1.2kΩ,
V_{IN}=V_{DEN}=0V to 4.5V to 0V, R_{LOAD}=12Ω)



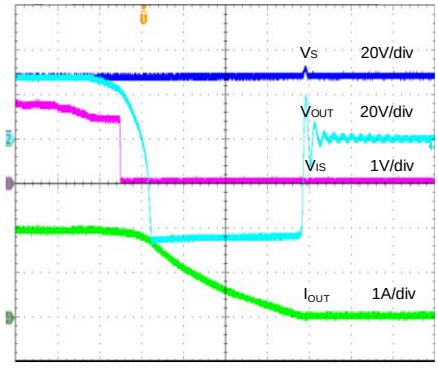
Time (20μs/div)

IN/DEN OFF with Resistive Load
(V_S=28V, C_{VS}=100nF, C_{OUT}=Null ,R_{IS}=1.2kΩ,
V_{IN}=V_{DEN}=0V to 4.5V to 0V, R_{LOAD}=12Ω)



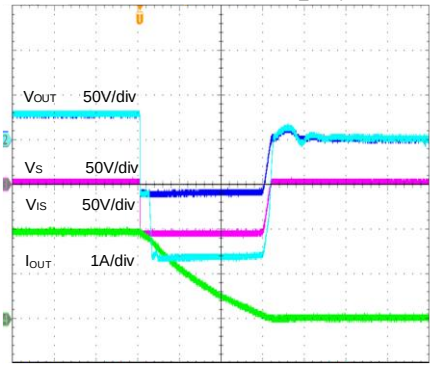
Time (20μs/div)

IN OFF with Inductive Load
(V_S=28V, V_{IN}=5V to 0V, V_{DEN}=5V. C_{VS}=C_{OUT}=Null,
R_{IS} =1.2kΩ, Z_{LOAD}=14Ω+6mH ,R_{DEN}=R_{IN}=10kΩ)



Time (40μs/div)

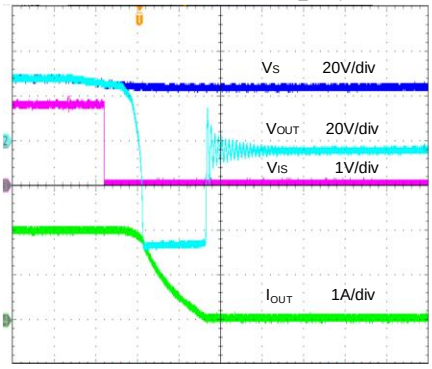
Loss of Battery with Inductive Load
(V_S=28V, C_{VS}=C_{OUT}=Null, Z_{LOAD}=14Ω+6mH,
R_{DEN}=R_{IN}=10kΩ，REF: GND_SYS)



Time (20μs/div)

Loss of IC GND with Inductive Load

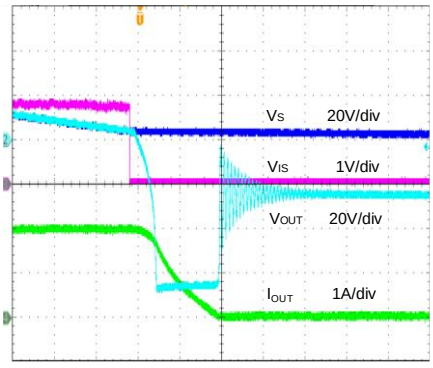
(V_S=28V, C_{VS}=C_{OUT}=Null, Z_{LOAD}=14Ω+6mH, R_{DEN}=R_{IN}=10kΩ，REF: GND_SYS)



Time (100μs/div)

Loss of SYS GND with Inductive Load

(V_S=28V, C_{VS}=C_{OUT}=Null, Z_{LOAD}=14Ω+6mH, R_{DEN}=R_{IN}=10kΩ，REF: GND_SYS)



Time (100μs/div)

Application Information

1. Thermal Resistance

1.1 PCB Set-Up

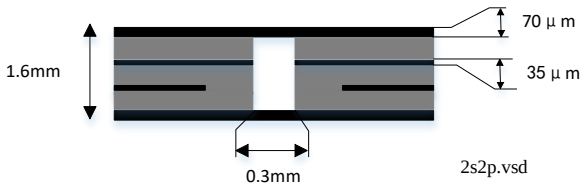


Figure 4 2s2p PCB Cross Section

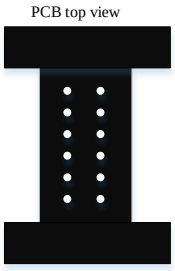


Figure 5 PCB Board Top View of 1s0p with 600 mm² Cooling Area

1.2 Thermal Impedance

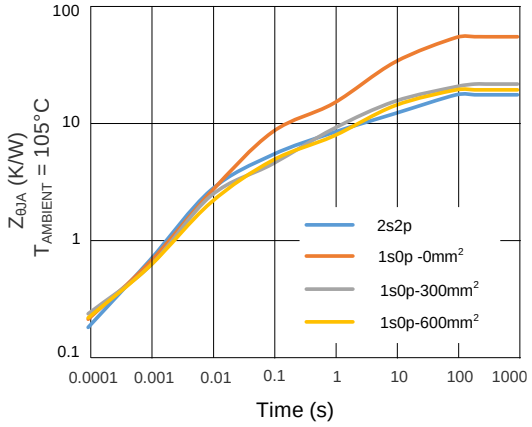


Figure 6 Typical Thermal Impedance. 2s2p set-up according to Figure 4

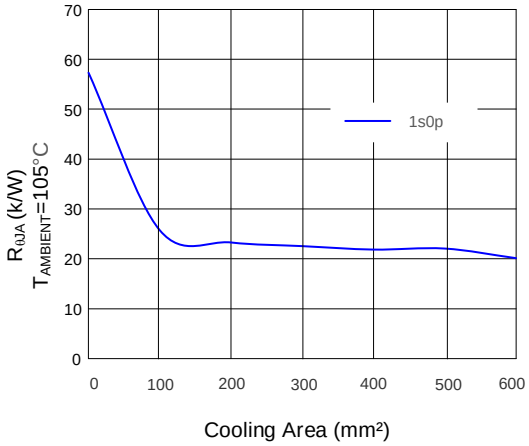


Figure 7 Typical Thermal Resistance. PCB set-up 1s0p

2. Switch ON/OFF Characteristics

2.1 Switch ON/OFF Characteristics with Resistive Load

Applying a voltage higher than 2V to IN pin enables the power DMOS to switch ON with a dedicated slope, which is optimized in terms of EMC emission. Figure 8 shows the typical timing when switching a resistive load.

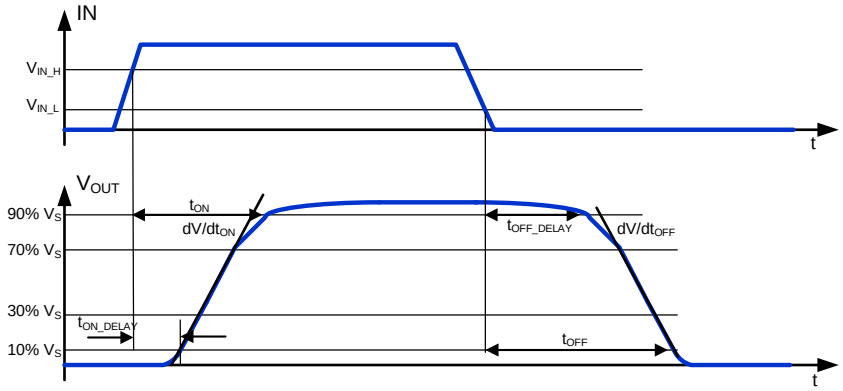


Figure8. Switching a Resistive Load Timing

2.2 Switch ON/OFF Characteristics with Inductive Load

Inductive loads consist of inductance L and resistance R. When switching ON, the inductive load causes a slow current ramp up. And when switching OFF due to the inductance, the current attempts to continue to flow in the same direction which causes V_{OUT} to invert. In order to prevent chip damage due to excessive V_{DS}, a voltage clamp function is designed to clamp the negative output voltage at a certain value(V_S-$V_{DS(AZ)}$). For detailed information, please refer to Figure 9 and Figure 10.

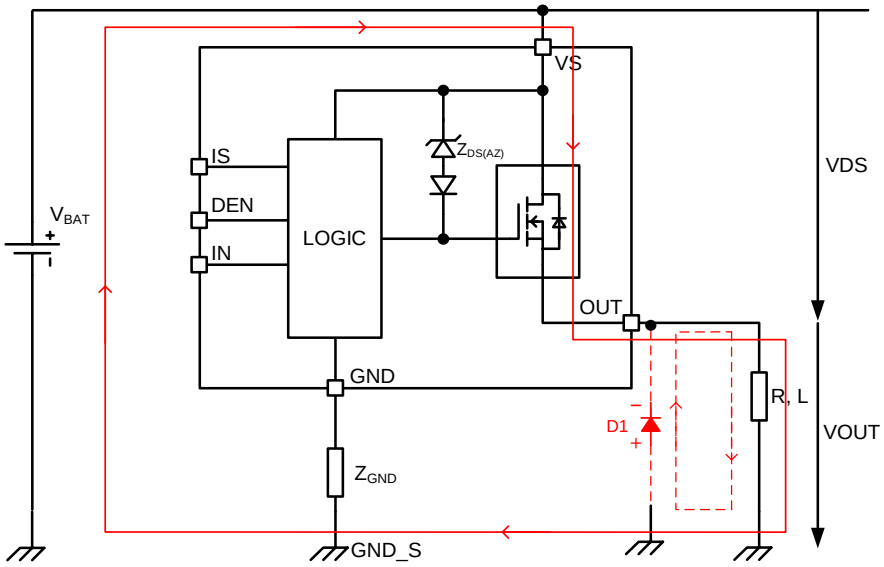


Figure.9 Current Path during Switch OFF with Inductive Load

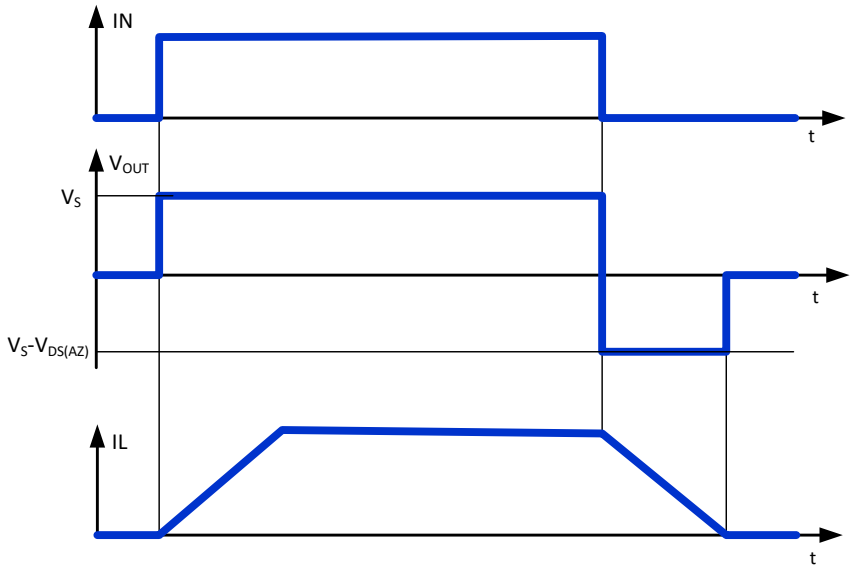


Figure.10 Waveforms during Switch OFF with Inductive Load (without D1)

However, the maximum value of inductive load is limited. Figure 11 shows the maximum allowable energy dissipation at different load current.

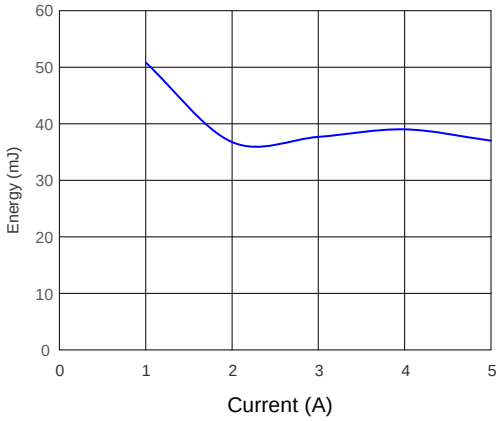


Figure 11.Maximum Energy Dissipation Single Pulse

During V_{DS} clamp, the power dissipation is large, to make system robust. A diode connect from GND_S to VOUT is recommended.

3. Inverse Current Capability

In the case of VS drops with capacitive load and out short to VS, output voltage will be higher than supply voltage, generating inverse current. If IN pin is on, the inverse current will flow through DMOS. If IN pin is off, the inverse current will flow through the body diode of DMOS. During inverse current, no protection functions are provided.

4. Reverse Polarity Protection with External Components

The following Figure 12 shows the current path when a reverse polarity event occurs. Where R_{SENSE}, R_{IS}, R_{DEN} and R_{IN} are used to limit the current flowing to the logical Pin, the recommended value for R_{DEN}=R_{IN}=R_{SENSE}=10kΩ. The current flowing through the parasitic diode is limited by the load. The path from GND to VS is blocked by the Z_{GND} network, it is recommended to be a resistor in series to a diode.

During reverse polarity, no protection functions are available.

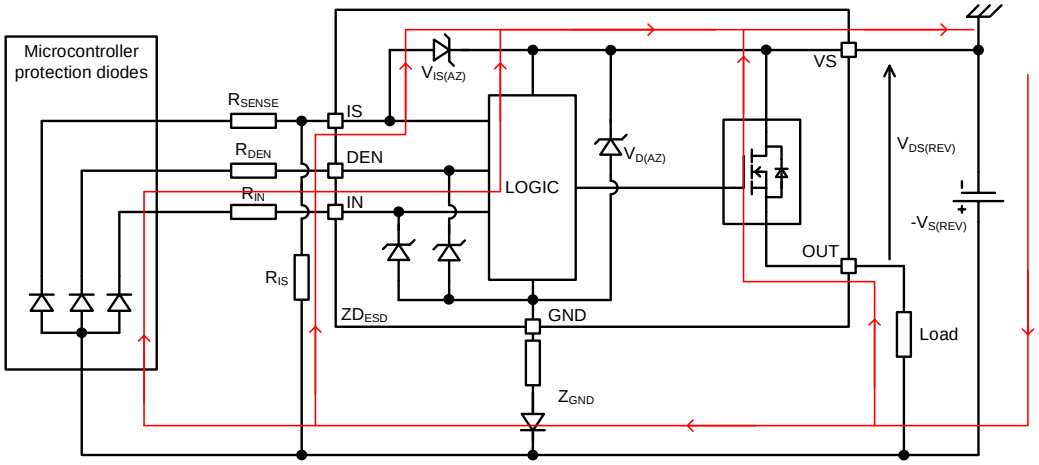


Figure 12. Reverse Polarity Protection with External Components

5. Loss of GND Characteristics with Inductive Load

In the case of output with load and loss of system or chip ground, if the IN pin is on, the chip will turn off. When loss of GND, the current will flow through of the DMOS, as shown in Figure 13. The path from GND to VS is blocked by the Z_{GND} network, it is recommended to be a resistor in series to a diode.

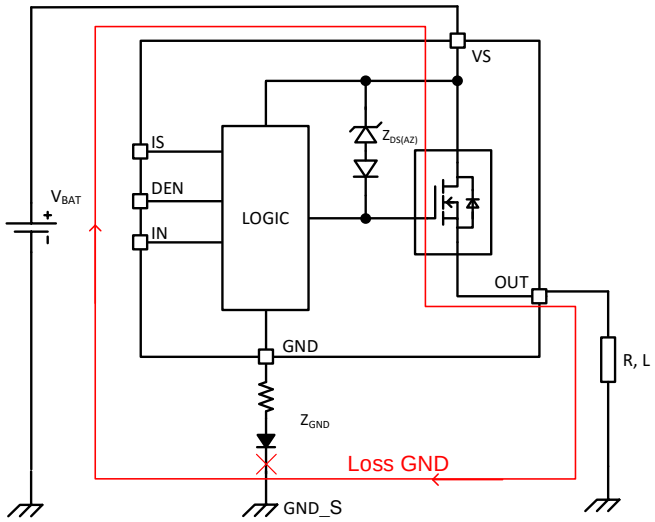


Figure 13 Loss of Ground Protection with External Components

6. Loss of Battery Characteristics with Inductive Load

When a loss battery event occurs, the VS pin voltage follows the OUT pin voltage when VS is above UVLO. In the case of VS is below UVLO, the V_{DS} can rise up to the $V_{DSCLAMP}$ as indicated on the Figure 14.
An external TVS diode (between VS and GND_S) is required to handle the energy and to provide a well-defined path to the load current. The path from GND to VS is blocked by the Z_{GND} network, it is recommended to be a resistor in series to a diode.

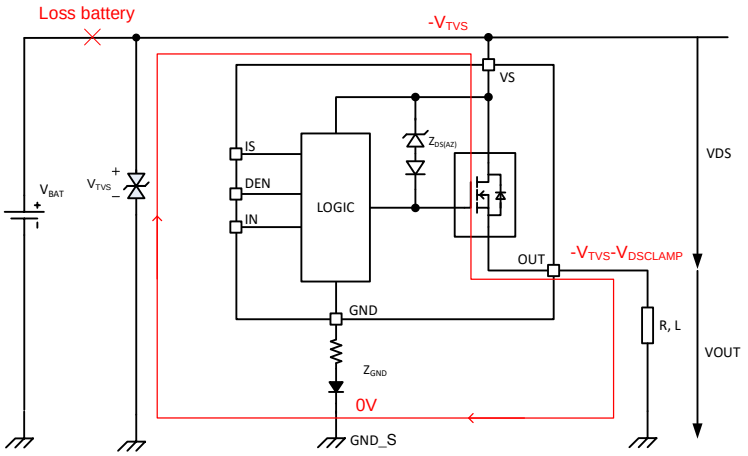


Figure14. Current Path during Loss Of Battery With Inductive Load

7. Under voltage Protection

The following Figure 15 shows the under voltage mechanism. $V_{S\ (UV)}$ means the minimum voltage that the chip can remain on, while $V_{S\ (OP)}$ means the minimum voltage that the chip can switch normally. When V_S is below $V_{S\ (UV)}$, the chip turns off. When V_S is above $V_{S\ (OP)}$, the chip turns on. However, the mechanism is not ensured when V_S is in normal operating voltage range.

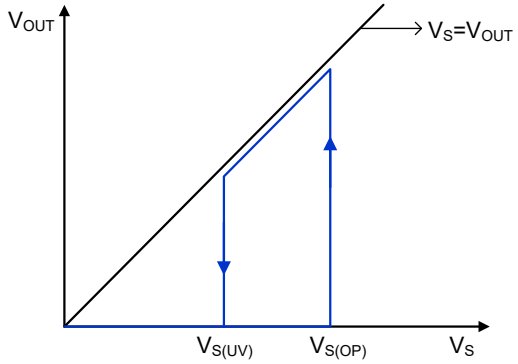


Figure 15. Under voltage Behavior

8. Over Load Protection

Under overload conditions, such as driving large capacitive loads, or short circuits to ground, the chip provides current limit and over temperature protection mechanisms.

8.1 Current limit Protection

When an overload event occurs, the chip will limit the current flowing through the power FET to $I_{L(SC)}$ to ensure that the instantaneous power of the power FET remains at a safe value.

During overload, the chip can work in the normal operating voltage range, and exceeding the normal operating range may cause the chip to fail.

8.2 Over temperature Protection

The chip integrates absolute ($T_{J\ (SC)}$) and dynamic ($T_{J\ (SW)}$) over temperature protection. Either over temperature protection trigger will cause the chip to turn off to prevent over temperature damage. Figure 16 shows a sketch of the situation. (Latching behavior) When the temperature of the DMOS becomes low enough, enable IN pin to restart the chip.

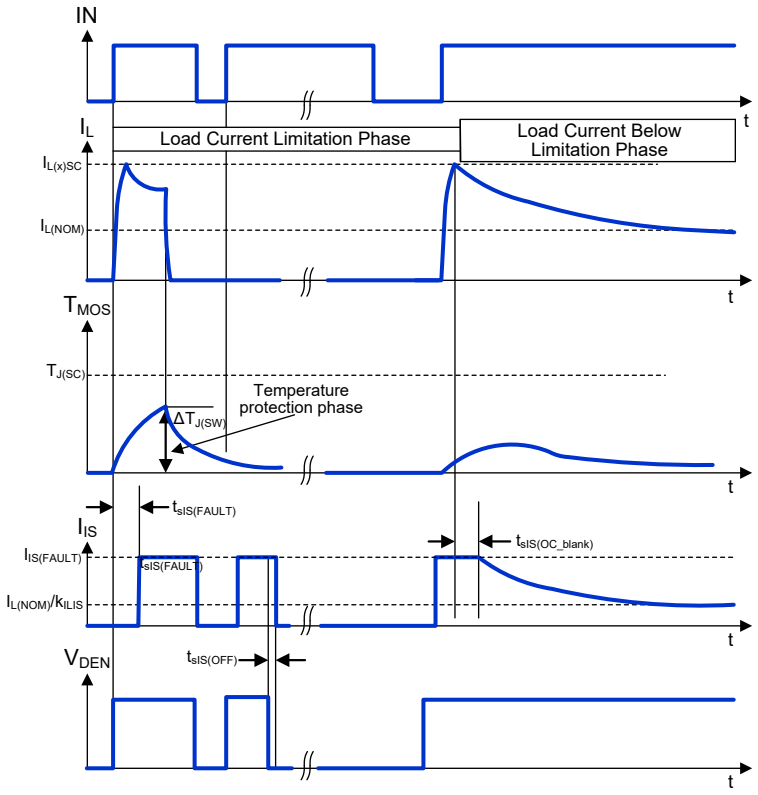


Figure 16. Over Temperature Protection

9. Diagnostic Functions

The chip provides signal diagnostics via the IS pin. If DEN pin is disabled, IS pin becomes high impedance. If DEN pin is enabled, current sense is achieved through the IS pin.

The function of the IS pin is to flow a current proportional to the load current under normal operating conditions. In the case of overload, or over temperature and open load in OFF state, IS pin will flow out a fault current ($I_{IS(FAULT)}$)around 15mA.

9.1 SENSE Signal in Different operation modes

Table 1 shows the status of the IS pin in different operation modes.

Table 1. Truth table

Sense Signal, Function of Operation Mode				
Operation Mode	**Input level Channel X**	**DEN**	**Output Level**	**Diagnostic Output**
Normal Operation	OFF	H	Z	Z
Short Circuit to GND			~GND	Z
Over Temperature			Z	Z
Short Circuit to V_S			V_S	$I_{IS(FAULT)}$
Open Load			< $V_{OL(OFF)}$ > $V_{OL(OFF)}$[1)]	Z $I_{IS(FAULT)}$
Inverse Current			> V_S	$I_{IS(FAULT)}$
Normal Operation	ON		~ V_S	$I_{IS}=I_L/k_{ILIS}$
Current Limitation			< V_S	$I_{IS(FAULT)}$
Short Circuit to GND			~ GND	$I_{IS(FAULT)}$
Over Temperature $T_{J(SW)}$ Event			~ GND	$I_{IS(FAULT)}$
Short Circuit to V_S			V_S	$I_{IS}<I_L/k_{ILIS}$
Open Load			~ V_S[2)]	$I_{IS}<I_{IS(OL)}$
Inverse Current			> V_S	$I_{IS}<I_{IS(OL)}$
Underload			~ V_S[3)]	$I_{IS(OL)}<I_{IS}<I_L/k_{ILIS}$
Don't Care	Don't care	L	Don't care	Z

1) With additional pull-up resistor.
2) The output current has to be smaller than $I_{L(OL)}$.
3) The output current has to be higher than $I_{L(OL)}$.

9.2 SENSE Signal in the Nominal Current Range

IS pin needs to connect a pull-down resistor R_{IS} to the GND_S to limit the current flowing through the pin, recommended value for R_{IS} =1.2kΩ. Figure 17 shows timing during enabling and disabling of the sense.

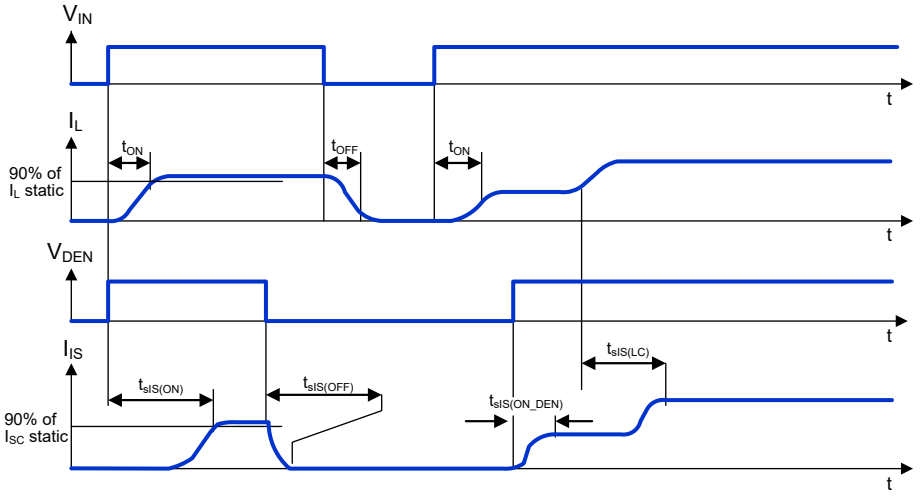


Figure 17. Current Sense Settling / Disabling Timing

9.3 SENSE Signal in open load

If the chip is turned on, a small leakage current flows through the open load due to certain factors, such as humidity. If the leakage current is less than $I_{L(OL)}$ and DEN pin is enabled, IS pin cannot provide sense current signal.
If the chip is turned off, an additional pull-up resistor (R_{OL}) is recommended, and its resistance value needs to consider the leakage current and open load threshold voltage $V_{OL(OFF)}$. To reduce the operation current of the system, it is recommended to use open load resistor transistor. When open load in off diagnostic, the output voltage value becomes V_S- $V_{OL(OFF)}$,IS pin will flow out $I_{IS(FAULT)}$. Figure 18 shows the timing during either open load in ON and OFF condition when the DEN pin is high.

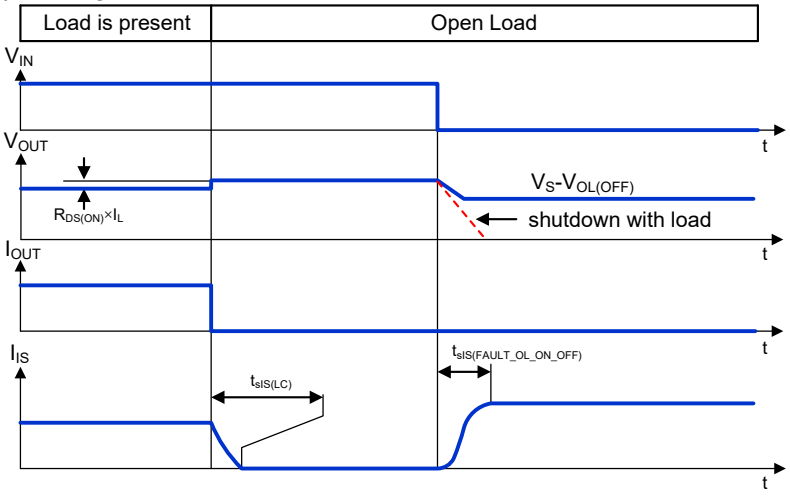


Figure 18. SENSE Signal in Open Load Timing

10. PCB Layout Guide

Good board layout practices must be used or instability can be induced because of ground loops and voltage drops, and large PCB copper area can improve the thermal performance. The input and output capacitors MUST be directly connected to the input, output and ground pins of the device using traces which have no other currents flowing through them.
Below is the recommended PCB Layout diagram:

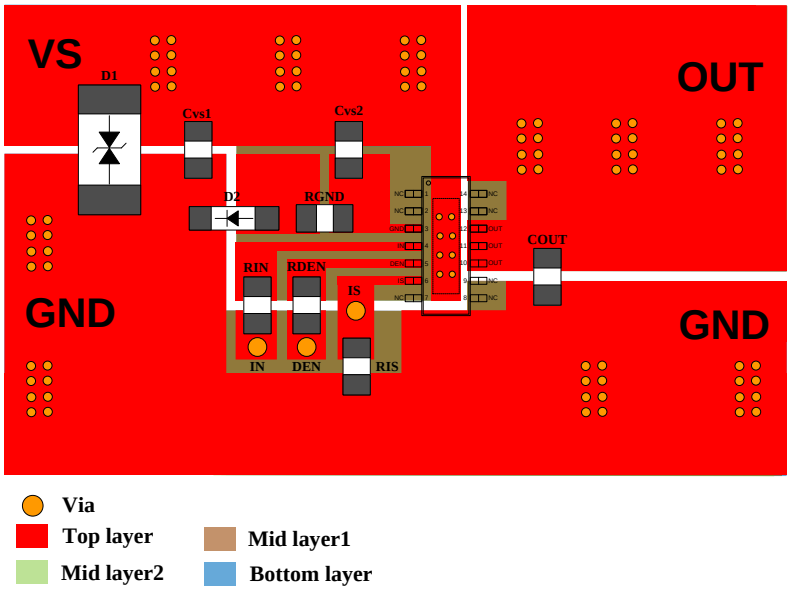


Figure 19. PCB Layout Suggestion

11. Typical Application Recommendation

Figure 20 shows the typical application circuit.

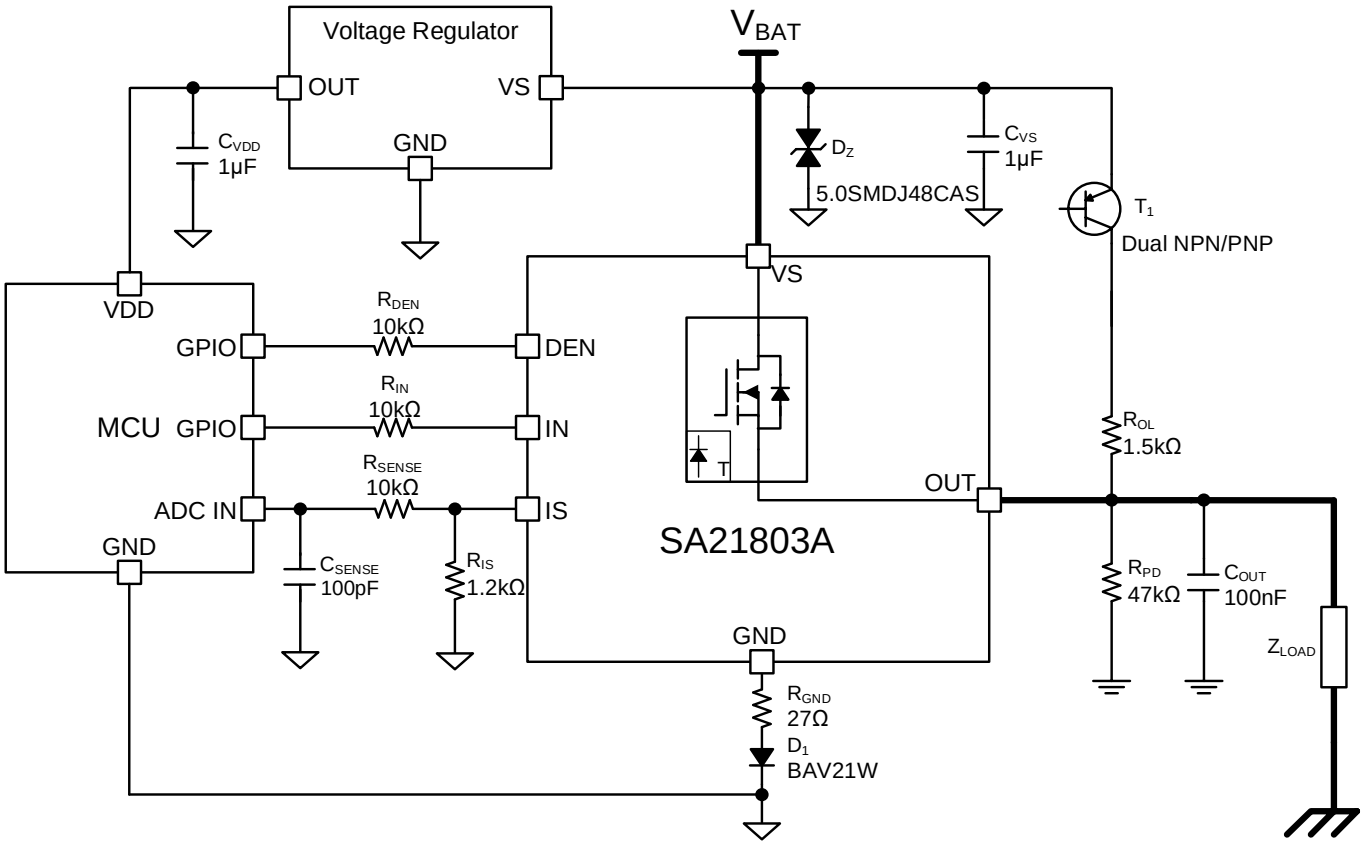
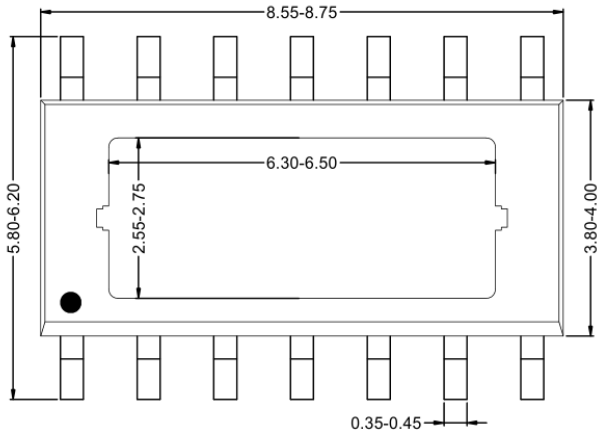


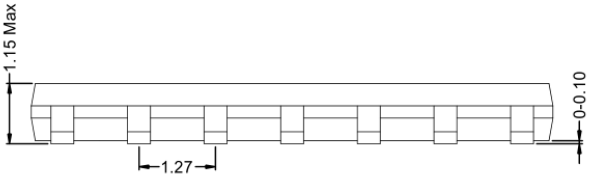
Figure 20. Application Diagram with SA21803AHTP

TSOP14E Package Outline Drawing

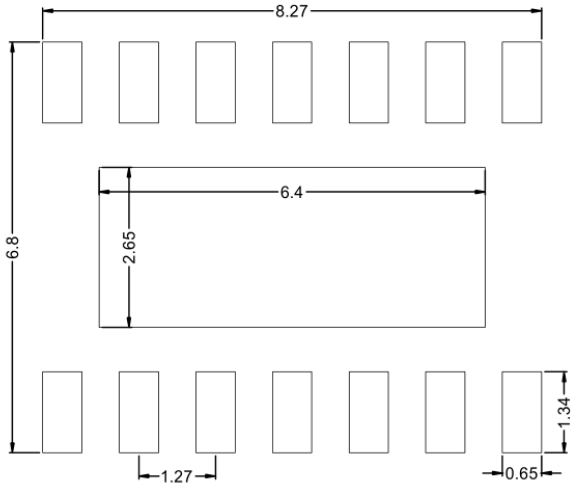


Top view

Side view



Front view

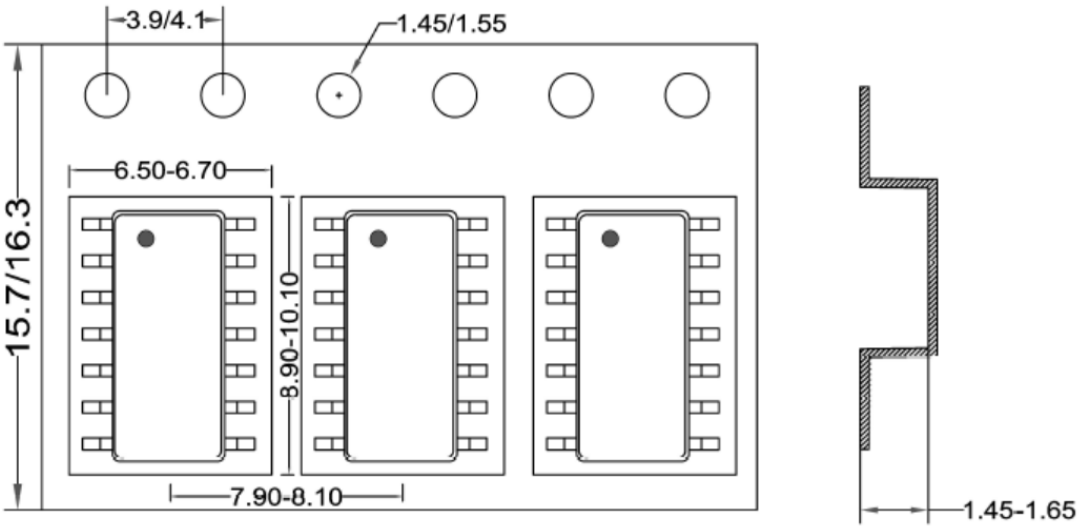


Recommended PCB Layout
Only for reference

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

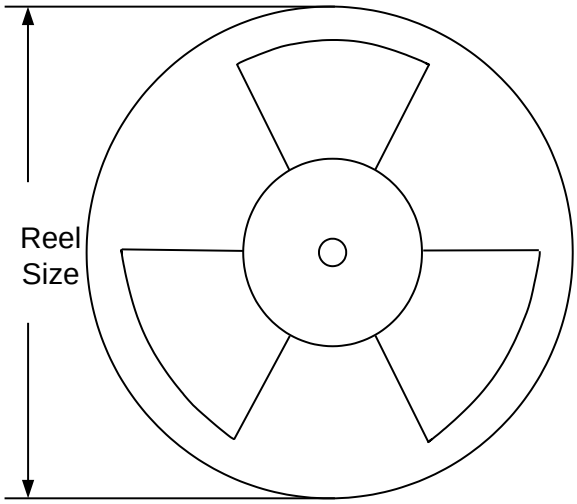
Taping & Reel Specification

1. Taping orientation



Feeding direction

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
TSOP14E	16	8	13"	400	400	2500

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Dec.15, 2023	Revision 1.0	Initial Release

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