SY7T6xx/SY7T6xxE

Energy Measurement Processor with Integrated Oscillator

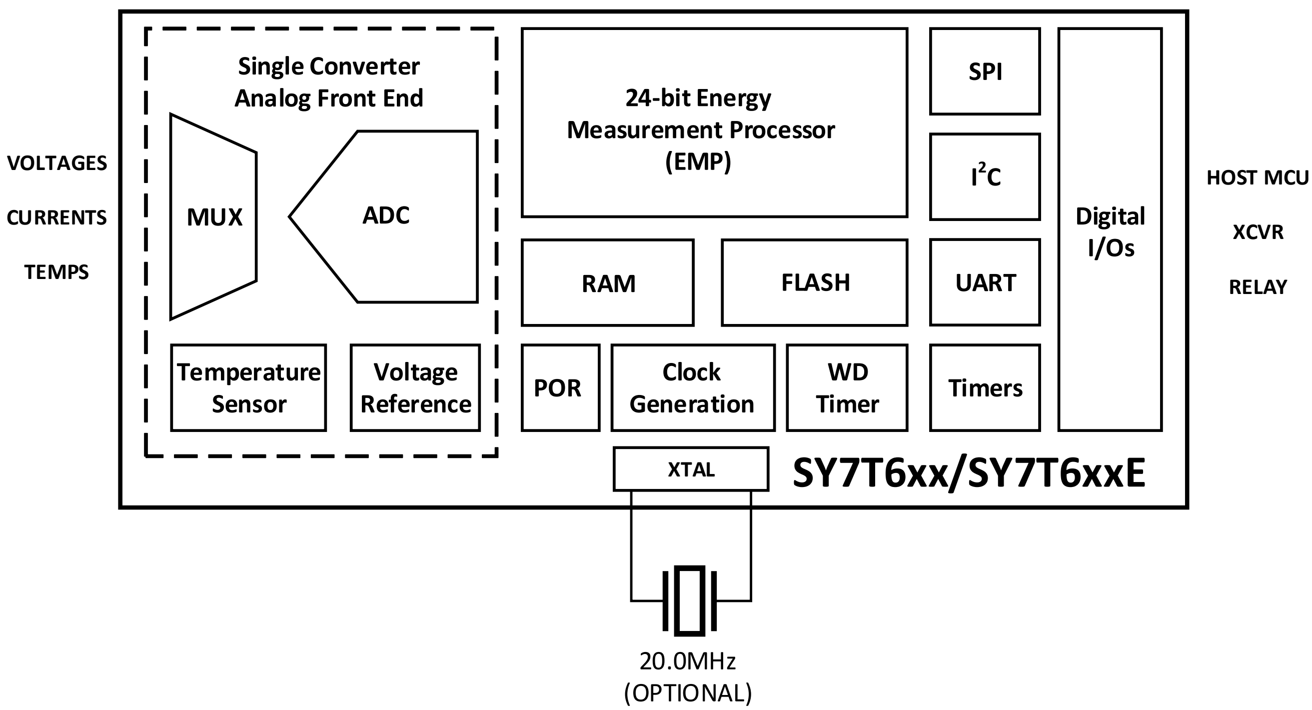
DESCRIPTION

The SY7T6xx/SY7T6xxE are energy measurement processors (EMPs) with up to six analog (sense) inputs. They are ideally suited for embedded poly-phase or power distribution applications.

The analog front end (AFE) provides analog (sense) inputs for interfacing with up to six current or voltage sensors. Scaled voltages from the sensors are fed to a high-resolution delta-sigma converter. A low power 24-bit energy measurement processor (EMP) with embedded firmware performs all the necessary computation, compensation, and data formatting. With integrated flash memory for storing nonvolatile data such as calibration coefficients and device configuration settings, the SY7T6xx/SY7T6xxE provide an autonomous solution that simplifies system integration.

FEATURES

- High resolution delta-sigma ADC with up to six time-multiplexed analog inputs
- Precision voltage and timing references
- 24-bit energy measurement processor with nonvolatile storage of calibration and configuration data
- Flexible SPI, UART, I²C interface options with configurable DIO for alarm signaling, address pins, or user control
- SY7T6xxE offers an extended temperature range (-40°C to +105°C)
- Various compact package options (14-32pin)



1 Ordering Information

Ordering Number [1)]	Carrier	Firmware	Temperature Range	Package	Top Marking
SY7T609B	Bulk	None	-40°C to +85°C	TSSOP-14	BNExyz
SY7T609T	Tape & Reel				
SY7T609E+B	Bulk		-40°C to +105°C		SY7T609E YYWW RRRR ###@@
SY7T609E+T	Tape & Reel				
SY7T610B	Bulk	None	-40°C to +85°C	TSSOP-16	YYWW RRRR ###@@
SY7T610T	Tape & Reel				
SY7T610E+T	Tape & Reel		-40°C to +105°C		SY7T610E YYWW RRRR ###@@
SY7T611B	Bulk	None	-40°C to +85°C	TQFN-24	EMP YYWW RRRR ###@@
SY7T611T	Tape & Reel				
SY7T612B	Bulk	None	-40°C to +85°C	TQFN-32 5x5mm	EMP YYWW RRRR ###@@
SY7T612T	Tape & Reel				
SY7T612E+T	Tape & Reel		-40°C to +105°C		SY7T612E YYWW RRRR ###@@

Example:

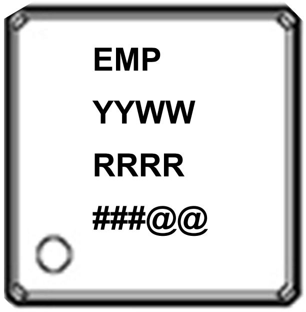
S Y 7 T 6 1 2 □+ □□

- Firmware version code
- Pre-programming adder
- Carrier Type (B for bulk, T for tape & reel)

S Y 7 T 6 1 2 E + □□□

- Carrier Type (B for bulk, T for tape & reel)
- Firmware version code
- Pre-programming adder
- Extended temperature range

x year code
y week code
z lot code



YY	The last two digits of year of assembly
WW	Week of assembly
RRRR	Die Rev Code
###	The last 3 numeric characters from the lot number
@@	The first two alpha characters after the numeric characters from the lot number

Note:

1) Ordering Numbers for pre-programmed devices with firmware include a '+' character followed by one or more alphanumeric characters (Example: SY7T612B+ABC123 for ABC123 firmware shipped in bulk). To support re-programmability, the top marking is the same for both all programmed and unprogrammed ordering options. Material traceability is digitally maintained within the device.

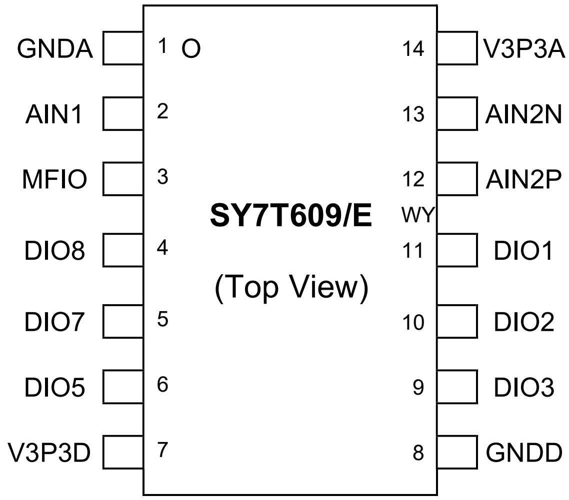
2 Functional Description

This datasheet only contains a description of the various on-chip hardware resources, electrical specifications, mechanical specifications, and ordering numbers. Reference firmware documentation for information on:

- Signal processing, compensation, and measurement outputs
- Fault detection and alarms
- Calibration, configuration, and commands
- Serial communication protocols

3 Pinout

3.1 SY7T609/SY7T609E

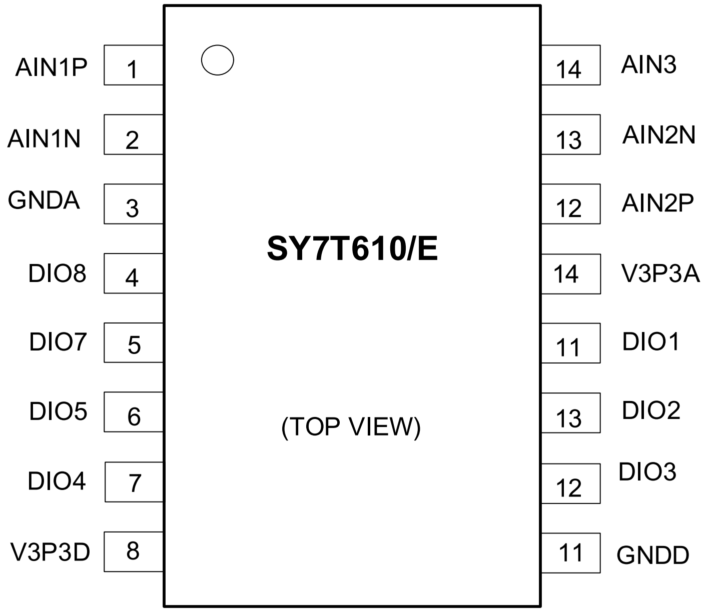


Pin	Name	Description
1	GNDA	Ground pin (Analog)
2	AIN1	Analog Sense Input
3	MFIO	Multi-function I/O: (Analog Sense Input or Digital I/O)
4	DIO8	Interface Select (1), Digital I/O
5	DIO7	Digital I/O
6	DIO5	SPI SSB or Digital I/O
7	V3P3D	3.3VDC Supply (Digital)
8	GNDD	GROUND (Digital)
9	DIO3	SPI MISO, UART TX (Data Out)
10	DIO2	SPI MOSI, UART RX (Data In)
11	DIO1	SPI SCK or Digital I/O
12	AIN2P	Analog Sense Input
13	AIN2N	Analog Sense Input
14	V3P3A	3.3VDC Supply (Analog)

Notes:

1) DIO8 is sampled at power-on or reset to determine the selection of SPI (DIO8 = low) or UART/I^{2}C (DIO8 = high). The selection of I^{2}C or UART is determined by the firmware.

3.2 SY7T610/SY7T610E

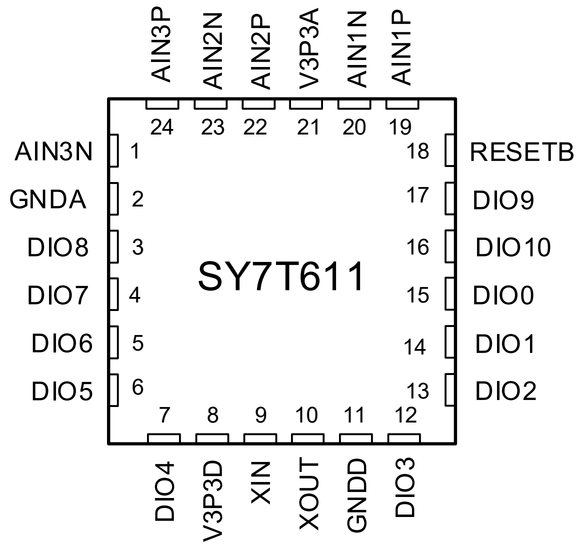


Pin	Name	Description
1	AIN1P	Analog Input 1 (Positive)
2	AIN1N	Analog Input 1 (Negative)
3	GNDA	Ground pin (Analog)
4	DIO8	Interface Select, and Digital I/O. Pin is sampled upon reset to select the serial interface.
5	DIO7	Digital I/O
6	DIO5	SPI SSB, I^2C SCL, or Digital I/O
7	DIO4	Digital I/O
8	V3P3D	3.3VDC Supply (Digital)
9	GNDD	GROUND (Digital)
10	DIO3	SPI MISO, UART TX, or I^2C SDAo (Data Out)
11	DIO2	SPI MOSI, UART RX, or I^2C SDAi (Data In)
12	DIO1	SPI SCK or Digital I/O
13	V3P3A	3.3VDC Supply (Analog)
14	AIN2P	Analog Input 2 (Positive)
15	AIN2N	Analog Input 2 (Negative)
16	AIN3	Analog Input 3 (Single-End)

Notes:

1) DIO8 is sampled at power-on or reset to determine the selection of SPI (DIO8 = low) or UART/I^2C (DIO8 = high). The selection of I^2C or UART is determined by the firmware.

3.3 SY7T611/SY7T611E

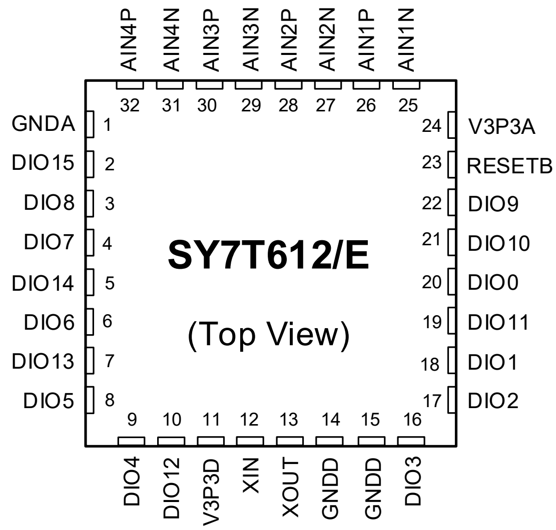


Pin	Signal	Function	Pin	Signal	Function
1	AIN3N	Analog Input 3 (negative)	13	DIO2	SPI MOSI / UART RX/ I²C SDAi (Data In)
2	GNDA	Ground (Analog)	14	DIO1	SPI SCK, Digital I/O
3	DIO8	Interface Select (1), Digital I/O	15	DIO0	Digital I/O
4	DIO7	Digital I/O	16	DIO10	Digital I/O
5	DIO6	Digital I/O	17	DIO9	Digital I/O
6	DIO5	SPI SSB, I²C SCL, Digital I/O	18	RESETB	Reset Input (Active Low)
7	DIO4	Digital I/O	19	AIN1P	Analog Input 1 (positive)
8	V3P3D	3.3VDC Supply (Digital)	20	AIN1N	Analog Input 1 (negative)
9	XIN	Crystal Oscillator Input	21	V3P3A	3.3VDC Supply (Analog)
10	XOUT	Crystal Oscillator Output	22	AIN2P	Analog Input 2 (positive)
11	GNDD	Ground (Digital)	23	AIN2N	Analog Input 2 (negative)
12	DIO3	SPI MISO, UART TX, I²C SDAo (Data Out)	24	AIN3P	Analog Input 3 (positive)

Notes:

1) DIO8 is sampled at power-on or reset to determine the selection of SPI (DIO8 = low) or UART/I²C (DIO8 = high). The selection of I²C or UART is determined by the firmware.

3.4 SY7T612/SY7T612E



Pin	Signal	Function	Pin	Signal	Function
1	GNDA	Analog GND	17	DIO2	Digital I/O, SPI MOSI, UART RX, SDAi(1)
2	DIO15	Digital I/O	18	DIO1	Digital I/O, SPI SCK(1)
3	DIO8	Interface Select (1), Digital I/O	19	DIO11	Digital I/O
4	DIO7	Digital I/O	20	DIO0	Digital I/O
5	DIO14	Digital I/O	21	DIO10	Digital I/O
6	DIO6	Digital I/O	22	DIO9	Digital I/O
7	DIO13	Digital I/O	23	RESETB	Reset Input (Active Low)
8	DIO5	Digital I/O, SPI SSB, UART TXEN, SCL(1)	24	V3P3A	3.3VDC Supply (Analog)
9	DIO4	Digital I/O	25	AIN1N	Analog Input 1 (negative)
10	DIO12	Digital I/O	26	AIN1P	Analog Input 1 (positive)
11	V3P3D	3.3VDC Supply (Digital)	27	AIN2N	Analog Input 2 (negative)
12	XIN	Crystal Oscillator Input	28	AIN2P	Analog Input 2 (positive)
13	XOUT	Crystal Oscillator Output	29	AIN3N	Analog Input 3 (negative)
14	GNDD	Ground (Digital)	30	AIN3P	Analog Input 3 (positive)
15	GNDD	Ground (Digital)	31	AIN4N	Analog Input 4 (negative)
16	DIO3	Digital I/O, SPI MISO, UART TX, SDAo(1)	32	AIN4P	Analog Input 4 (positive)
33	EP	Thermal Pad - Tie to GND (Optional) (2)			

Notes:

1) DIO8 is sampled at power-on or reset to determine the selection of SPI (DIO8 = low) or UART/I²C (DIO8 = high). The selection of I²C or UART is determined by the firmware.
2) The exposed thermal pad is connected to the device substrate. It can be connected to GND; however it cannot be used to replace the GND connection. The GND must be connected through GNDD (digital) and GNDA (analog) ground pins.

4 Hardware Resources Overview

The SY7T6xx/SY7T6xxE integrates all the functional hardware blocks required for solid-state power and energy measurement. Only a few external resistors and capacitors are required. Included on the device are:

- Temperature compensated oscillator and clock management logic
- Integrated power-on reset and watchdog timer
- High-accuracy analog front-end (AFE) with trimmed voltage reference and temperature sensor
- 24-bit energy measurement processor with RAM and flash memory
- Peripheral interfaces (UART, I2C or SPI) with Digital I/O and PWM outputs

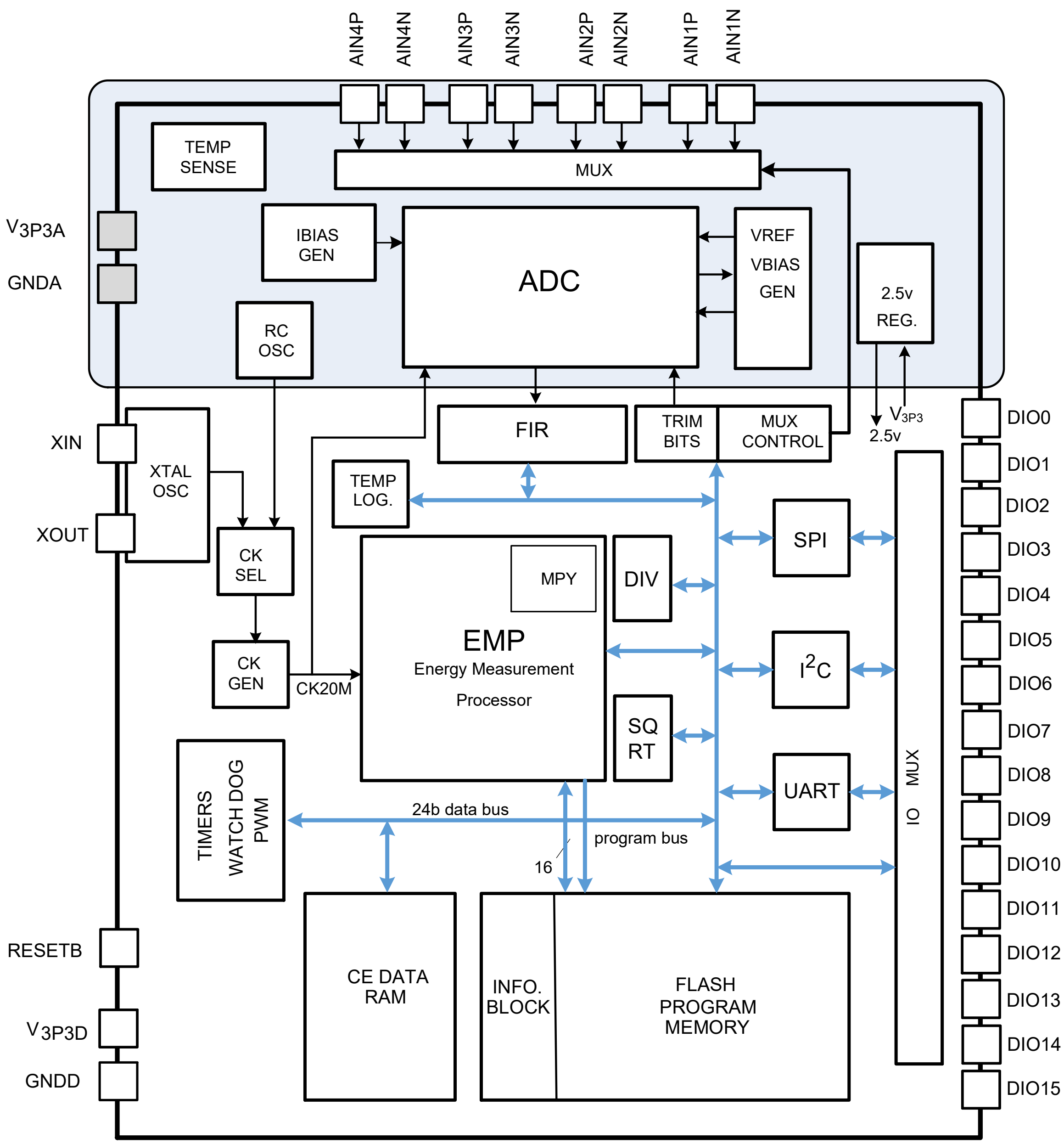


Figure 4-1. SY7T6xx/SY7T6xxE Functional Block Diagram

4.1 Clock Management, Power-On Reset, and WD Timer

Clock Management

The SY7T6xx/SY7T6xxE integrates a trimmed and temperature compensated RC oscillator. The device also includes the circuitry to handle an external crystal or ceramic resonator. The clock management unit of the SY7T6xx/SY7T6xxE automatically handles the clock sources logic and distributes the clock to the rest of the device.

Upon reset or power-on, the SY7T6xx/SY7T6xxE starts-up on the internal RC oscillator. After 1024 clock cycles of the internal RC oscillator, the clock management logic will switch to the external 20MHz clock (if available), allowing the external crystal an adequate start-up time. If no valid external clock is detected, the clock management logic will keep clocking the device using the internal RC oscillator. If the device is normally clocked using the external 20MHz crystal, the clock management logic continuously monitors the status of the clock. The clock management logic of the SY7T6xx/SY7T6xxE will automatically switch to the internal oscillator in the event of a failure of the external oscillator (or crystal not mounted).

The internal RC oscillator is trimmed and temperature compensated. It provides an accurate clock source, however for applications requiring highest accuracy of the time-based measurements (i.e. line frequency, energy, etc.), the use of an external crystal is recommended.

The SY7T6xx/SY7T6xxE external clock circuitry requires a 20.000MHz crystal. The circuitry includes two 18pF ceramic capacitors. Figure 4-2 shows the typical connection of the external crystal. This oscillator is self-biasing and therefore an external resistor should NOT be connected across the crystal.

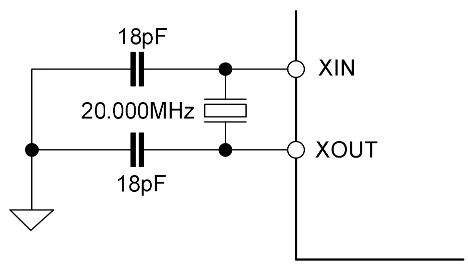


Figure 4-2: XTAL Connection

Alternatively, an external clock signal can be utilized instead of a crystal. In this case, the external clock should be connected to the XOUT pin while the XIN pin should be connected to GNDD.

If the external crystal is not utilized (not mounted), the XOUT pin should be connected to GNDD and the XIN pin left unconnected.

Power-On Reset (POR)

An on-chip Power-On Reset (POR) block monitors the supply voltage (V_{3P3D}) and initializes the internal digital circuitry at power-on. Once V_{3P3D} is above the minimum operating threshold, the POR circuit triggers and initiates a reset sequence. It will also issue a reset to the digital circuitry if the supply voltage falls below the minimum operating level.

Watchdog Timer (WDT)

A Watchdog Timer (WDT) block detects any software processing errors. The embedded software periodically refreshes the free-running watchdog timer to prevent it from timing out. If the WDT times out, it is an indication that software is no longer being executed in the intended sequence; thus, a system reset is initiated.

External Reset Pin (RESETB Pin)

In addition to the internal reset sources, a reset can be forced by applying a low level to the RESETB pin.

If the RESETB pin is pulled low, all digital activities in the device stop, except the clock management circuitry and oscillators, which continue to run. The external reset input is filtered to prevent spurious reset events in noisy environments. The reset does not occur until RESETB has been held low for at least 1 µs.

Once initiated, the reset mode persists until the RESETB is set high and the reset timer times out (4096 clock cycles). At the completion of the reset sequence, the internal reset is released and the processor (EMP) begins executing from address 0.

If not used, the RESETB pin can be connected either directly or through a pull-up resistor to V_{3P3D} supply. A simple connection diagram is shown in Figure 4-3.

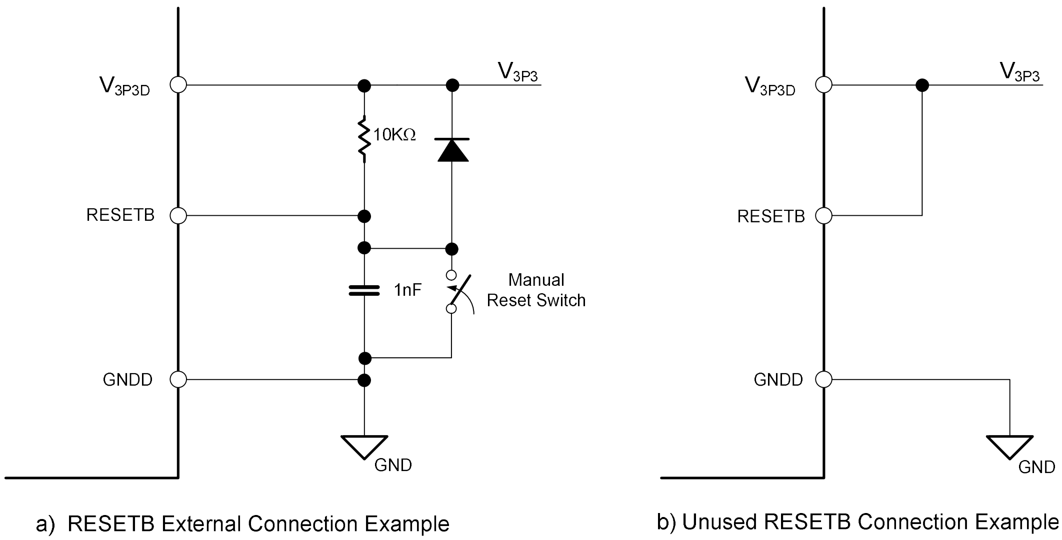


Figure 4-3: RESETB Pin Connections

4.2 Analog Front-End and Conversion

The Analog Front-End (AFE) of the SY7T6xx/SY7T6xxE includes an input multiplexer, delta-sigma A/D converter, bias current references, voltage references, a temperature sensor, and several voltage fault comparators.

Delta-Sigma A/D Converter

A second-order delta-sigma converter digitizes the analog inputs. The converted data is then processed through an FIR filter.

Voltage Reference

The device includes an on-chip precision bandgap voltage reference that incorporates auto-zero techniques as well as production trims to minimize errors caused by component mismatch and drift. The voltage reference is digitally compensated over temperature.

Die Temperature Measurement

The device includes an on-chip die temperature sensor used for digital compensation of the voltage reference. It is also used to report temperature information to the user.

Voltage and Current Inputs

The external voltage and current sensors are connected to analog input pins. The full-scale signal level that can be applied to the voltage input pins is V3P3A ±250mVpk. With a sinusoidal waveform, the maximum RMS voltage is:

$$\mathrm{VrmsMAX} = \frac{250mVpk}{\sqrt{2}} = 176.78\mathrm{mVRMS}$$

A common-mode voltage of less than ±25 mV is recommended to fully utilize the available dynamic range.

4.3 Energy Measurement Processor

The SY7T6xx/SY7T6xxE integrates a dedicated 24-bit processor that performs all the digital signal processing necessary for measurement, calibration, compensation, analysis, alarms generation, etc.

4.4 Flash and RAM

The SY7T6xx/SY7T6xxE includes on-chip flash memory for storing program code, coefficients, calibration data, and configuration settings. The SY7T6xx/SY7T6xxE also includes on-chip RAM which is used to store the values of input and output registers and utilized by the firmware for its operations.

4.5 Digital I/O

The SY7T6xx/SY7T6xxE features general purpose digital I/O. The digital I/O are either managed directly by the user, by embedded firmware, or multiplexed with the serial communication interfaces. The device also includes the necessary hardware to generate free-running PWM signals at either DIO7 or DIO8 with configurable period and pulse width. The following table summarizes the multiplexing and pin assignment on the SY7T6xx/SY7T6xxE.

<table>
<tr><th rowspan="2">Pin Name</th><th rowspan="2">Pin #</th><th rowspan="2">Function at Power-On Reset</th><th colspan="3">Function by Interface</th></tr>
<tr><th>SPI</th><th>UART</th><th>I²C</th></tr>
<tr><td>DIO15</td><td>2</td><td>--</td><td colspan="3">DIO15</td></tr>
<tr><td>DIO14</td><td>5</td><td>--</td><td colspan="3">DIO14</td></tr>
<tr><td>DIO13</td><td>7</td><td>--</td><td colspan="3">DIO13</td></tr>
<tr><td>DIO12</td><td>10</td><td>--</td><td colspan="3">DIO12</td></tr>
<tr><td>DIO11</td><td>19</td><td>--</td><td colspan="3">DIO11</td></tr>
<tr><td>DIO10</td><td>21</td><td>--</td><td colspan="3">DIO10</td></tr>
<tr><td>DIO9</td><td>22</td><td>--</td><td colspan="3">DIO9</td></tr>
<tr><td>DIO8</td><td>3</td><td>Interface Select</td><td colspan="3">DIO8</td></tr>
<tr><td>DIO7</td><td>4</td><td>--</td><td colspan="3">DIO7</td></tr>
<tr><td>DIO6</td><td>6</td><td>--</td><td colspan="3">DIO6</td></tr>
<tr><td>DIO5</td><td>8</td><td>--</td><td>SSB</td><td>DIO5</td><td>SCL</td></tr>
<tr><td>DIO4</td><td>9</td><td>--</td><td colspan="3">DIO4</td></tr>
<tr><td>DIO3</td><td>16</td><td>--</td><td>MISO</td><td>TX</td><td>SDAo</td></tr>
<tr><td>DIO2</td><td>17</td><td>--</td><td>MOSI</td><td>RX</td><td>SDAi</td></tr>
<tr><td>DIO1</td><td>18</td><td>--</td><td>SCK</td><td colspan="2">DIO1</td></tr>
<tr><td>DIO0</td><td>20</td><td>--</td><td colspan="3">DIO0</td></tr>
</table>

4.6 Serial Interfaces

The SY7T6xx/SY7T6xxE provides UART, I^2C, and SPI interface options, but only one interface can be active at a time. The pin DIO8 is sampled following a power-on reset to select between SPI interface or UART/ I^2C. The firmware that is loaded on the device will determine the selection between UART and I^2C interfaces. The user should allow at least 10ms from a power-on reset event for the selection pin status to be latched and the serial interface selected. During this time the status of DIO8 must not change.

Selected Interface	DIO8
SPI	0
UART or I^2C (1)	1

Note:

Refer to the relevant firmware documentation for information on the selection of the UART/I^2C interfaces.

> **Warning**
>
> **Where applicable, pins should be configured via pull-up and pull-down resistors as these pins could become outputs after initialization. Therefore, direct connection to GNDD/GNDA or V3P3D/V3P3A supplies must be avoided.**

4.6.1 UART Interface

The SY7T6xx/SY7T6xxE features a UART interface with a data rate ranging from 2400 up to 115k Baud. The UART interface has a fixed configuration supporting: 8-bit, one start bit, one stop bit and no-parity. The UART interface hardware does not provide handshaking hardware signals (i.e. RTS, CTS etc.). Refer to the firmware documentation for further details on the communication protocol.

The UART clock is derived from the 20MHz system clock. The error due to the clock division is reported in the following Table.

BAUD	Actual Baud	Percent error
2400	2399.808	0.008
4800	4800.768	0.016
9600	9596.929	-0.032
19200	19193.86	-0.032
38400	38461.54	0.160
57600	57541.26	-0.2235
115200	114942.5	-0.2235

4.6.2 SPI Interface

The SPI featured in the SY7T6xx/SY7T6xxE is slave only. Once the SPI interface is activated, it utilizes the following digital I/O as the SPI interface:

DIO5: Slave select (SSB) is an active low input signal.

DIO1: Serial Data Clock (SCK) input.

DIO3: Master Input, Slave Output (MISO), serial data output.

DIO2: Master Output, Slave Input (MOSI), serial data input.

The SPI interface allows read and write accessed to the data RAM specified in the command bit field ADDR[5:0]. The command limits the access to RAM locations 0x00 through 0x3F.

SPI Mode

The device operates in mode 3 (CPOL=1, CPHA=1) and as such the data is captured on the rising edge and propagated on the falling edge of the serial data clock (SCK). The figure below shows a single-byte transaction on the SPI bus. Bytes are transmitted/received MSB first.

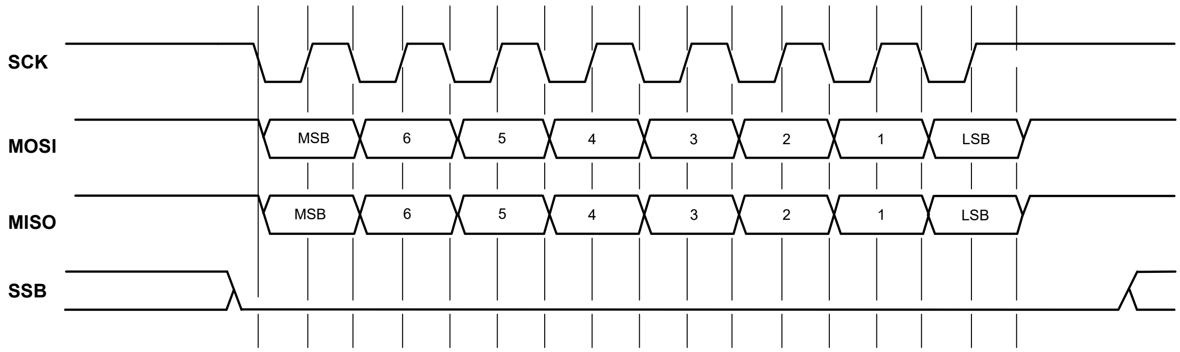


Figure 4-4. Signal Timing on the SPI Bus

Single Word SPI Reads

The device supplies direct read access to the device RAM memory. To read the RAM the master device must send a read command to the slave device and then clock out the resulting read data. SSB must be kept active low for the entire read transaction (command and response). SCK may be interrupted as long as SSB remains low. ADDR[5:0] is filled with the word address of the read transaction. RAM data contents are transmitted most significant byte first. ADDR[5:0] cannot exceed 0x3F. RAM words, and therefore the results, are natively 24 bits (3 bytes) long.

Single Word SPI Read Command (MOSI)

Byte #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	ADDR[5:0]						0x0	
1	0							
2	0							
3	0							

The slave responds with the data contents of the requested RAM addresses.

Single Word SPI Read Response (MISO)

Byte #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Hi-Z (during Read Command)							
1	DATA[23:16] @ ADDR							
2	DATA[15:8] @ ADDR							
3	DATA[7:0] @ ADDR							

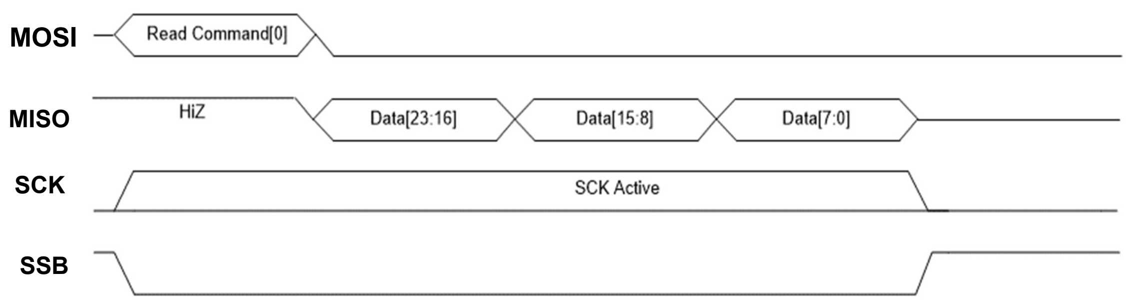


Figure 4-5. Single Word Read Access Timing

Single Word SPI Writes

The device supplies direct write access to the device RAM memory. To write the RAM the master device must send a write command to the slave device and then clock out the write data. SSB must be kept active low for the entire write transaction (command and data). SCK may be interrupted as long as SSB remains low. ADDR[5:0] is filled with the word address of the write transaction. RAM data contents are transmitted most significant byte first. ADDR[5:0] cannot exceed 0x3F. RAM words are natively 24-bit-long (3 bytes).

Single Word SPI Write Command and Data (MOSI)

Byte#	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	ADDR[5:0]						0x02	
1	DATA[23:16] @ ADDR							
2	DATA[15:8] @ ADDR							
3	DATA[7:0] @ ADDR							

The slave SDO remains Hi-Z during a write access.

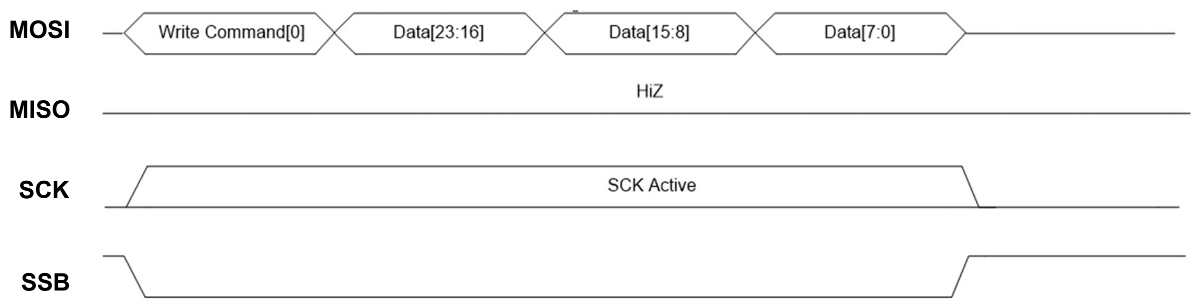


Figure 4-6. Single Word Write Access Timing

4.6.3 I²C Interface

The SY7T6xx/SY7T6xxE has an I²C interface available at the DIO2, DIO3, and DIO5 pins. The interface supports I²C slave mode with a 7-bit address and operates at a data rate up to 400kHz (Fast-mode). The SY7T6xx/SY7T6xxE has separate SD (serial data) input and output pins to allow the use of opto-couplers to isolate the serial bus.

The figure below shows two possible configurations. Configuration A is the standard configuration. The double pin for SDA allows the isolated configuration B.

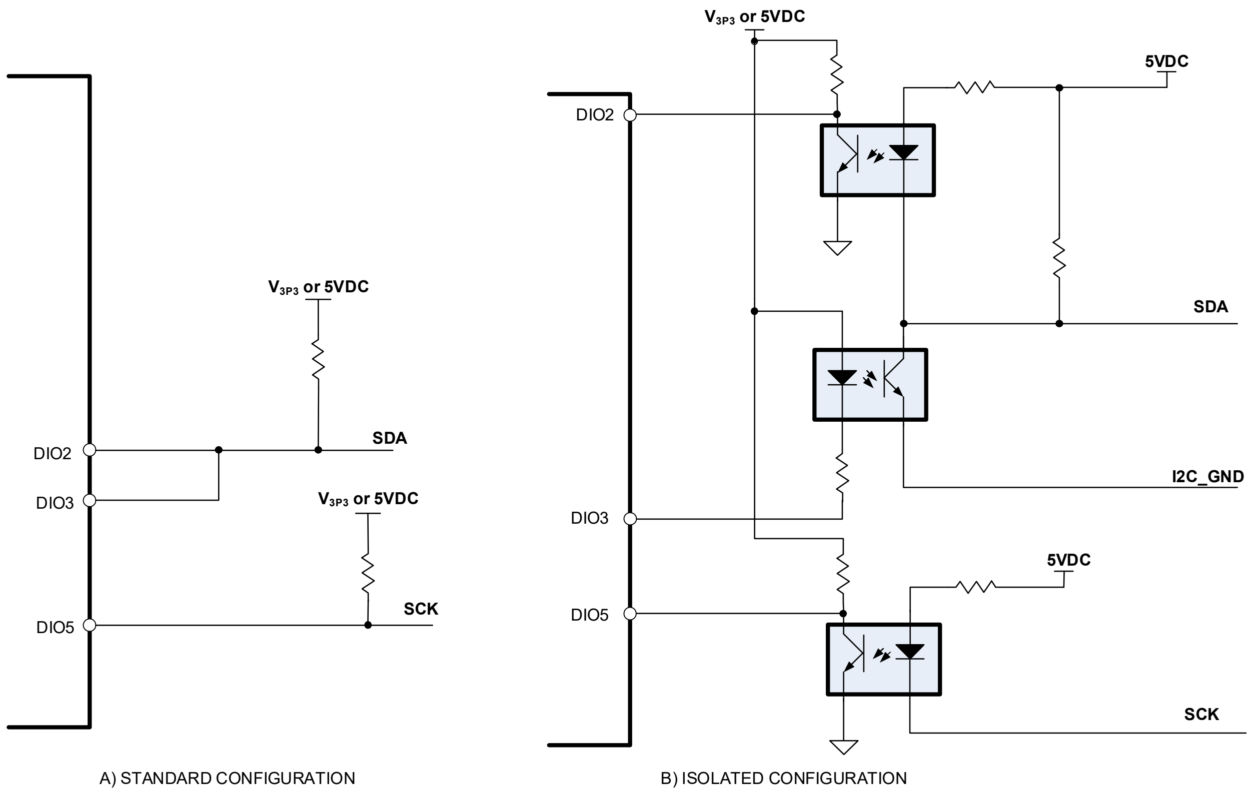


Figure 4-7. I2C Bus Connection in Standard (A) and Isolated (B) Configuration

The I²C interface allows access to read and write registers contained in a 256-word (24-bit) area of the on-chip RAM. The firmware documentation contains the address and assignment of each register.

Bus Characteristics

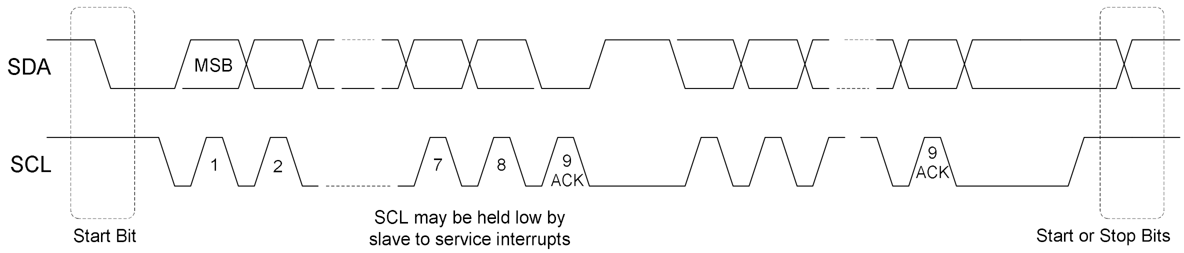
- A data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Bus Conditions

- **Bus not Busy (I):** Both data and clock lines are HIGH, indicating an Idle Condition.
- **Start Data Transfer (S):** a HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.
- **Stop Data Transfer (P):** a LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.
- **Data Valid:** The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be

changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition.

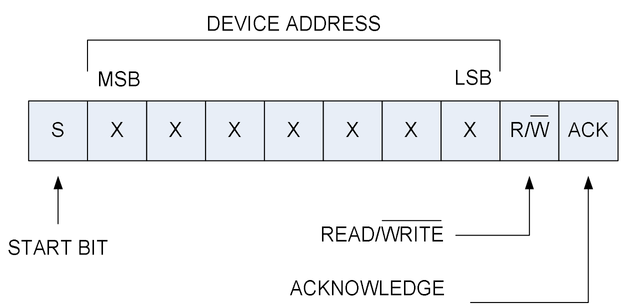
- **Acknowledge (A):** Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse, which is associated with this Acknowledge bit. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave SY7T6xx/SY7T6xxE will leave the data line HIGH to enable the master to generate the STOP condition.



Device Addressing

A control byte is the first byte received following the START condition from the master device.

The control byte consists of a seven-bit address and a bit (LSB) indicating the type of access (0=write; 1=read).



Write Operations

Following the START (S) condition from the master, the device address (7-bits) and the R/W bit (logic low for write) are clocked onto the bus by the master. This indicates to the addressed slave receiver that the register address will follow after it has generated an acknowledge bit (A) during the ninth clock cycle. Therefore, the next byte transmitted by the master is the register address and will be written into the address pointer of the SY7T6xx/SY7T6xxE. After receiving another acknowledge (A) signal from the SY7T6xx/SY7T6xxE, the master device will transmit the data byte(s) to be written into the addressed memory location. The data transfer ends when the master generates a STOP (P) condition. This initiates the internal write cycle. The example below shows a 3-byte data write (24-bit register write).

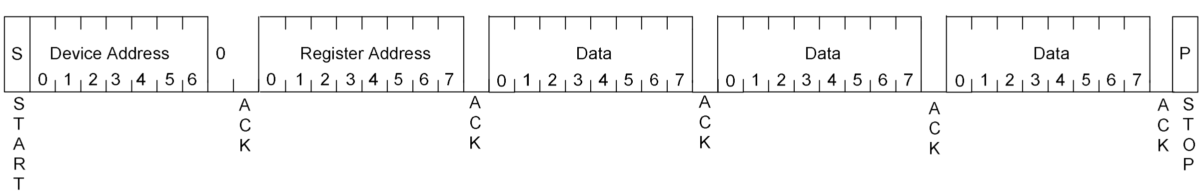


Figure 4-8. I2C Bus 3-byte Data Write

Upon receiving a STOP (P) condition, the internal register address pointer will be incremented.

The write access can be extended to multiple sequential registers. The figure below shows a transaction where multiple registers are written sequentially.

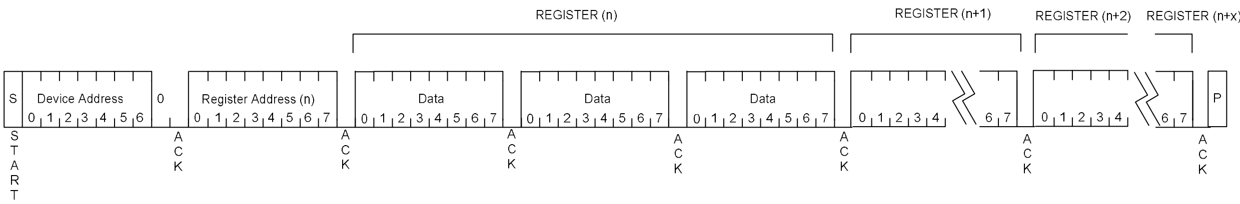


Figure 4-9. I2C Bus Multiple Sequential Register Write

Read Operations

Read operations are initiated in the same way as write operations with the exception that the R/W bit of the control byte is set to one. There are two basic types of read operations: current address read and random read.

Current Address Read: the SY7T6xx/SY7T6xxE contains an address counter that maintains the address of the last register accessed, internally incremented by one when the STOP bit is received. Therefore, if the previous read access was to register address n, the next current address read operation would access data from address n + 1.

Upon receipt of the control byte with R/W bit set to one, the SY7T6xx/SY7T6xxE issues an acknowledge (A) and transmits the eight-bit data byte. The master will not acknowledge the transfer, but generates a STOP condition to end the transfer and the SY7T6xx/SY7T6xxE will discontinue the transmission.

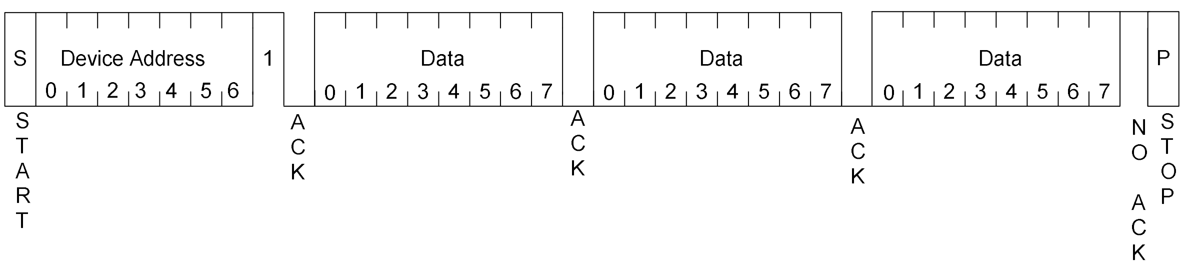
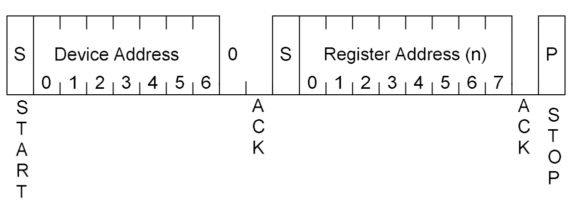


Figure 4-10. I2C Bus Current Address Read

This read operation is not limited to 3 bytes but can be extended until the register address pointer reaches its maximum value.

If the register address pointer has not been set by previous operations, it is necessary to set it by issuing a command as follows:



Random Read: random read operations allow the master to access any register in a random manner. To perform this operation, the register address must be set as part of the write operation. After the address is sent, the master generates a START condition following the acknowledge response. This sequence completes the write operation. The master should issue the control byte again this time, with the R/W bit set to 1 to indicate a read operation. The SY7T6xx/SY7T6xxE will issue the acknowledge response and transmit the data.

At the end of the transaction the master will not acknowledge the transfer and generate a STOP condition.

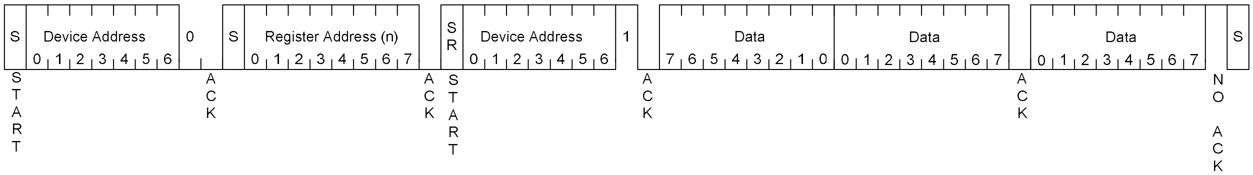


Figure 4-11. I2C Bus Random Read

This read operation is not limited to 3 bytes but can be extended until the register address pointer reaches its maximum value.

5 Electrical Specifications

5.1 Absolute Maximum Ratings

Supplies and Ground Pins:	
V_{3P3D}, V_{3P3A}	-0.5V to 4.6V
GNDD, GNDA	-0.5V to +0.5V
Analog Input Pins:	
AIN4P, AIN4N, AIN3P, AIN3N, AIN2P, AIN2N, AIN1P, AIN1N	-10mA to +10mA -0.5V to (V_{3P3} + 0.5V)
Digital Pins:	
DIO15, DIO14, DIO13, DIO12, DIO11, DIO10, DIO9, DIO8, DIO7, DIO6, DIO5, DIO4, DIO3, DIO2, DIO1	-30mA to +30mA, -0.5V to (V_{3P3D}+ 0.5V)
Temperatures:	
Operating Junction Temperature (peak, 100ms)	+140°C
Operating Junction Temperature (continuous)	+125°C
Storage Temperature	-45°C to +165°C
Soldering Temperature (10-second duration)	+250°C
ESD Stress on All Pins	±4kV

Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND.

5.2 Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
3.3V Supply Voltage (V_{3P3})	Normal Operation	3.0	3.3	3.6	V
Operating Temperature (non-E / E)		-40	–	+85 / +105	ºC

5.3 Performance Specifications

5.3.1 Input Logic Levels

Parameter	Condition	Min	Typ	Max	Unit
Digital high-level input voltage, V_{IH}		2	–	–	V
Digital low-level input voltage, V_{IL}		–	–	0.8	V

5.3.2 Output Logic Levels

Parameter	Condition	Min	Typ	Max	Unit
Digital high-level output voltage V_{OH}	I_{LOAD} = 1 mA	V_{3P3} –0.4	–	–	V
	I_{LOAD} = 10 mA	V_{3P3}-0.6	–	–	V
Digital low-level output voltage V_{OL}	I_{LOAD} = 1 mA	0	–	0.4	V
	I_{LOAD} = 10 mA	–	–	0.5	V

5.3.3 Supply Current

Parameter	Condition	Min	Typ	Max	Unit
V_{3P3D} and V_{3P3A} current (compounded)	Normal Operation, V3P=3.3V	–	8.1	10.3	mA

5.3.4 Internal RC Oscillator

Parameter	Condition	Min	Typ	Max	Unit
Nominal Frequency	V3P=3.3V, 25ºC	–	20.000	–	MHz
Accuracy		–	±1.5	–	%

5.3.5 ADC Converter, V_{3P3} Referenced

Parameter	Condition	Min	Typ	Max	Unit
Usable Input Range (Vin-V_{3P3})		-250	–	250	mV peak
THD (First 10 harmonics)	Vin=65Hz, 64kpts FFT, Blackman-Harris window	–	-85	–	dB
Input Impedance	Vin=65Hz	30	–	90	kΩ
Temperature coefficient of Input Impedance	Vin=65Hz	–	1.7[1]	–	Ω/°C
ADC Gain Error vs %Power Supply Variation $\frac{10^6\,\Delta Nout_{PK}\,357nV/V_{IN}}{100\,\Delta V3P3A/3.3}$	Vin=200mVpk, 65Hz V_{3P3}=3.0V, 3.6V	–	–	50	ppm/%
Input Offset (Vin-V_{3P3})		-10		10	mV

[1] Guaranteed by design, not subject to test.

5.4 Timing Specifications

5.4.1 SPI Slave Port

Parameter		Condition	Min	Typ	Max	Unit
t_{SPIcyc}	SPCK cycle time		1	–	–	µs
$t_{SPILead}$	Enable lead time		15	–	–	ns
t_{SPILag}	Enable lag time		0	–	–	ns
t_{SPIW}	SPCK pulse width: High Low		 250 250	–	–	 ns ns
t_{SPISCK}	SSB to first SPCK fall	Ignore if SPCK is low when SSB falls.	–	2[1]	–	ns
t_{SPIDIS}	Disable time		–	0[1]	–	ns
t_{SPIEV}	SPCK to Data Out (MISO)			–	25	ns
t_{SPISU}	Data input setup time (MOSI)		10	–	–	ns
t_{SPIH}	Data input hold time (MOSI)		5	–	–	ns

[1] Guaranteed by design, not subject to test.

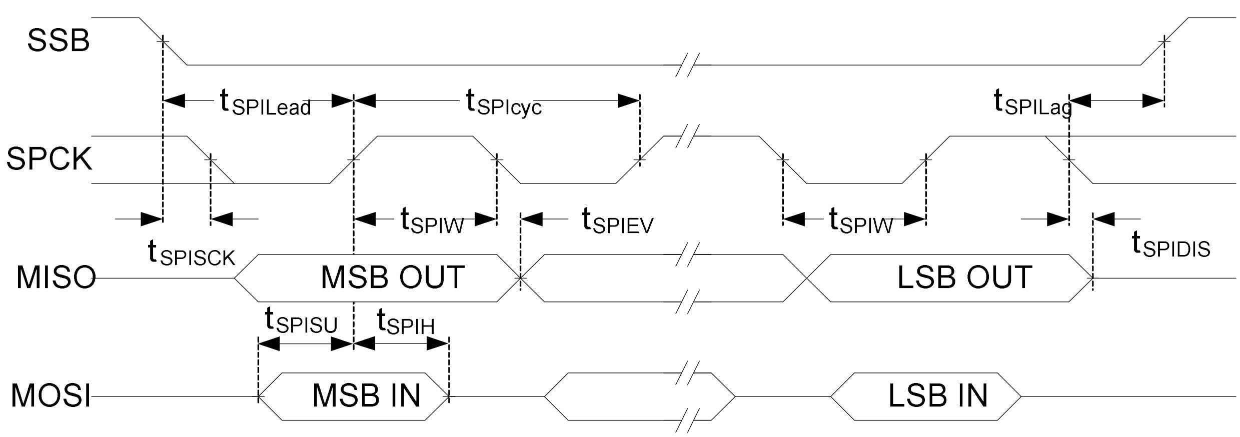


Figure 5-1: SPI Slave Port Timing

5.4.2 I²C Slave Port

Table 5-1: I²C Slave Port Timing[2]

Parameter	Condition	Min	Typ	Max	Unit
t_{BUF} Bus Idle (Free) time between transmissions (STOP/START)		1500	-	–	ns
t_{ICF} I²C input Fall Time		20[1]	–	300	ns
t_{ICR} I²C input Rise Time		20[1]	–	300	ns
t_{STH} I²C START or repeated START condition hold time		500	–	–	ns
t_{STS} I²C START or repeated START condition setup time		600	–	–	ns
t_{SCH} I²C clock high time		600	–	–	ns
t_{SCL} I²C clock low time		1300	–	–	ns
t_{SDS} I²C serial data setup time		100	–	–	ns
t_{SDH} I²C serial data hold time		10	–	–	ns
t_{VDA} I²C Valid data time: - SCL low to SDA output valid - ACK signal from SCL low to SDA (out) low		–	–	900	ns

Notes:

[1] Dependent on bus capacitance.

[2] Guaranteed by design, not subject to test.

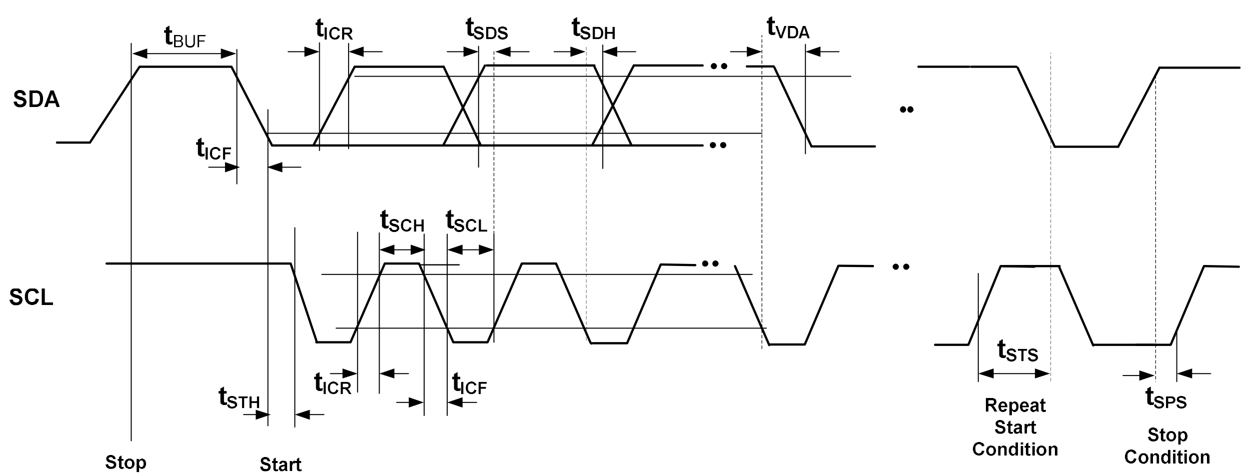
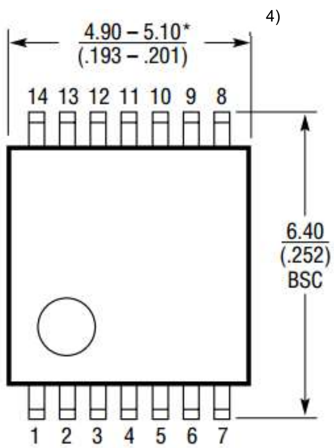


Figure 5-2: I²C (Slave) Port Timing

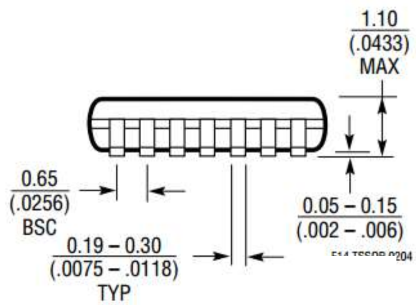
6 Mechanical Dimensions

6.1 SY7T609/SY7T609E

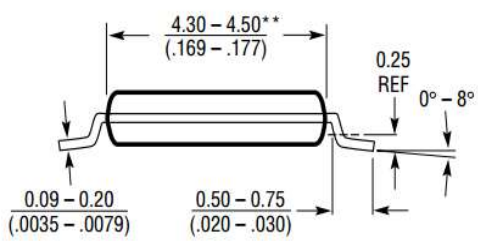
6.1.1 Package Outline Drawing



TOP-VIEW



SIDE-VIEW



FRONT-VIEW

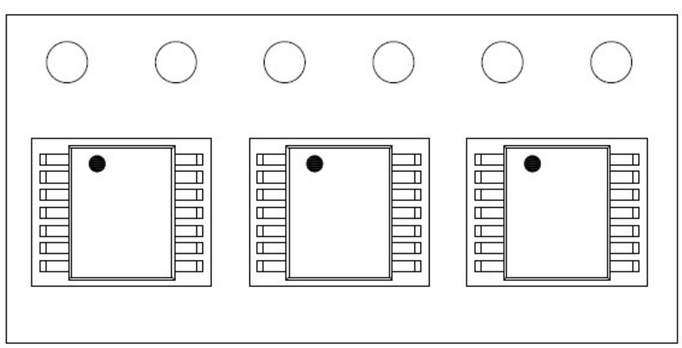
NOTES:

- Dimensions are in Millimeters/(Inches)
- Controlling Dimensions: Millimeters
- Drawing not to scale
- Dimensions not including mold-flash.

  Mold-flash not to exceed 0.152mm (.006'') per side.
- Dimensions do not include interlead flash.

  Interlead flash not to exceed 0.254mm (0.010'') per Side

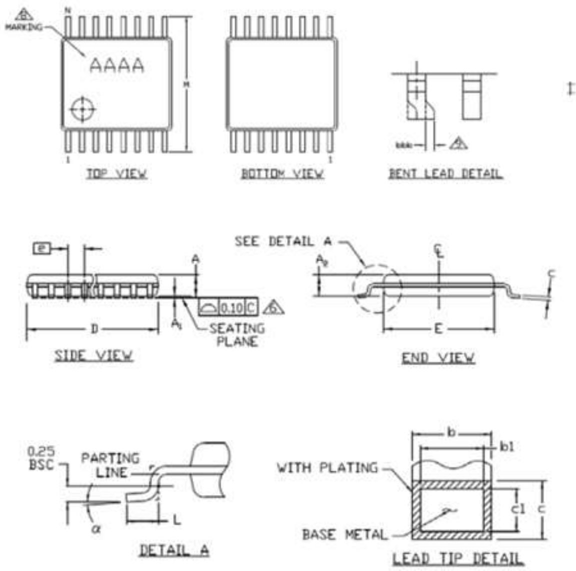
6.1.2 Tape & Reel Orientation



Feeding Direction →

6.2 SY7T610/ SY7T610E

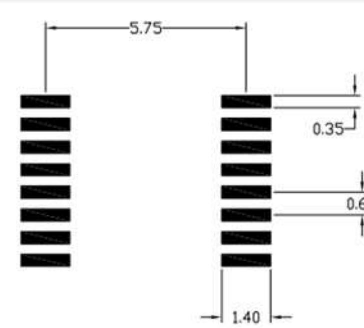
6.2.1 Package Outline Drawing



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	—	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	4.90	5.10	.193	.201
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
bbb	0.10 MAX			

NOTES
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. 'N' REFERS TO NUMBER OF LEADS
6. LEAD COPLANARITY 0.10 MM MAX.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
9. BENT LEAD 0.10 MM MAX.
10. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
11. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PBFREE (+) PKG. CODES.

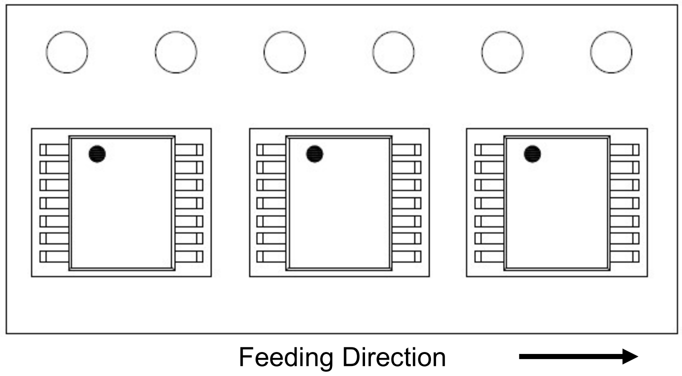
-DRAWING NOT TO SCALE-



NOTES:
1. LAND PATTERN COMPLIES TO: IPC7351A.
2. TOLERANCE: +/- 0.02 MM.
3. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.
4. ALL DIMENSIONS IN MM.

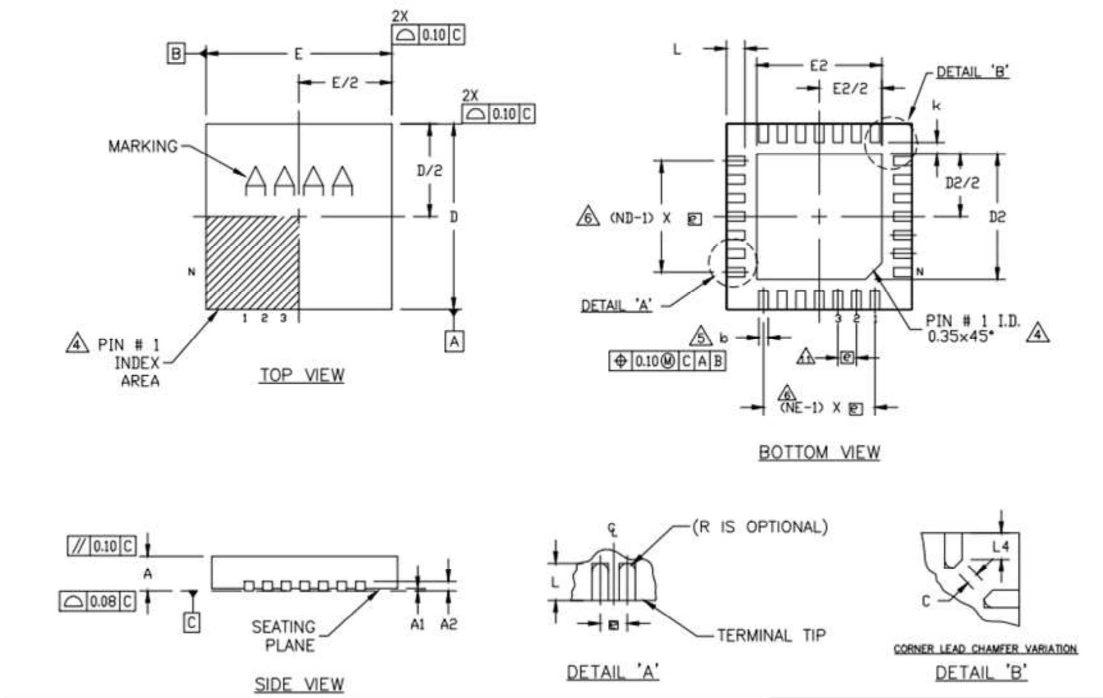
-DRAWING NOT TO SCALE-

6.2.2 Tape & Reel Orientation

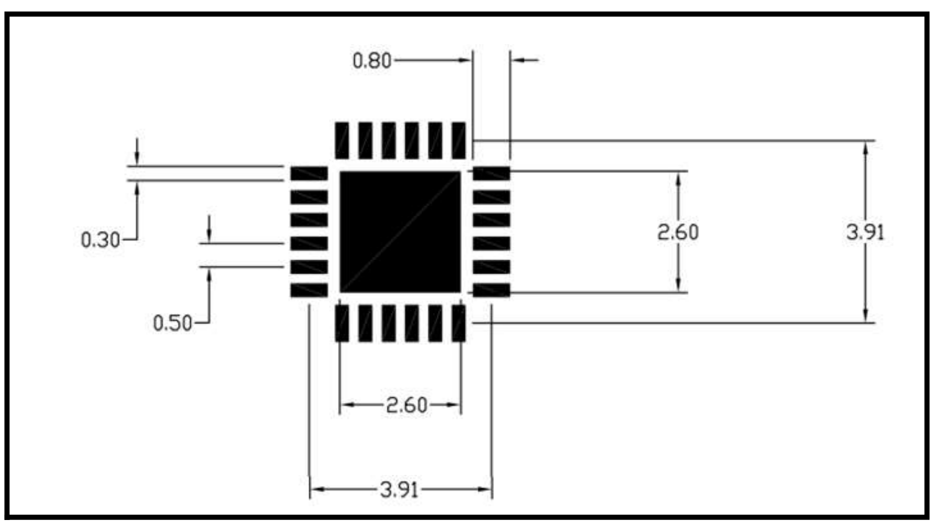


6.3 SY7T611/ SY7T611E

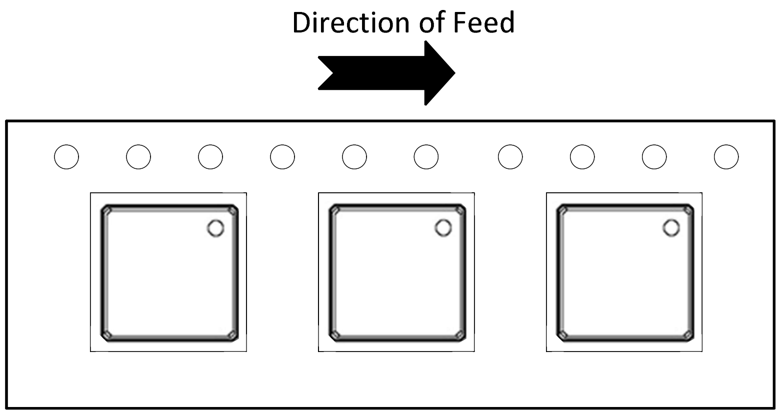
6.3.1 Package Outline Drawing



COMMON DIMENSIONS			
PKG	24L 4x4		
REF.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.0	0.02	0.05
A2	0.20 REF		
b	0.18	0.23	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e	0.50 BSC.		
k	0.25	-	-
L	0.30	0.40	0.50
N	24		
ND	6		
NE	6		
Jedec Var.	WGGD-2		

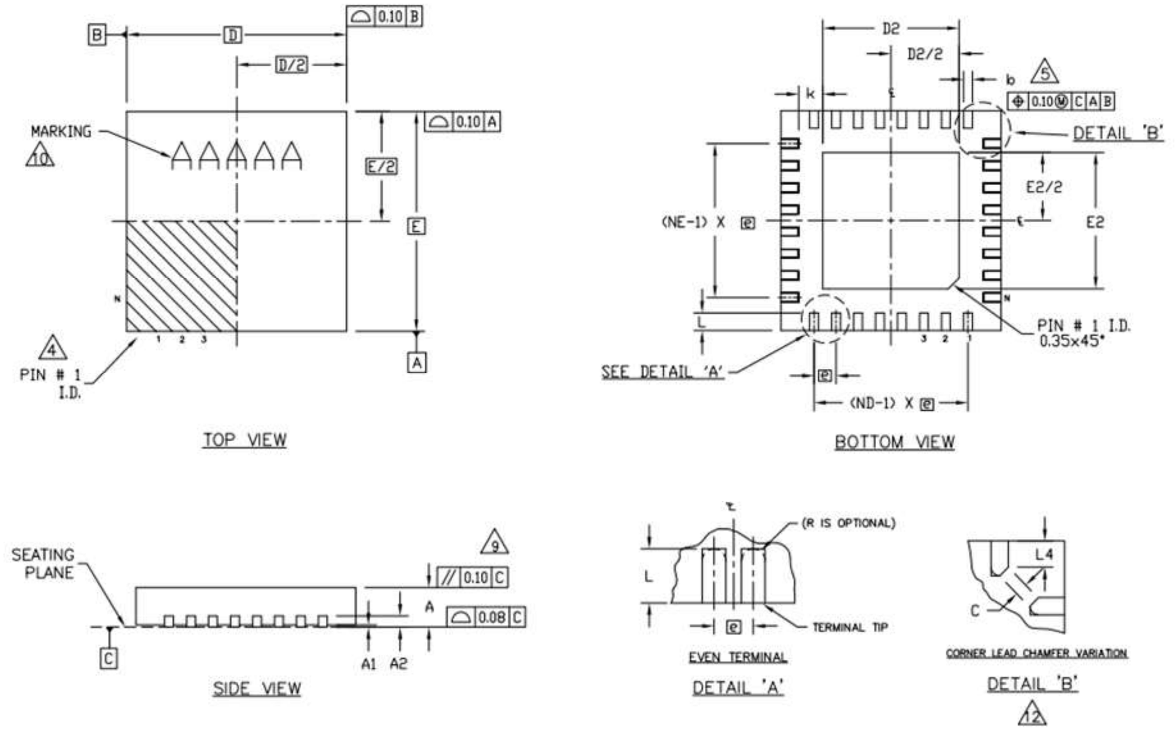


6.3.2 Tape & Reel Orientation

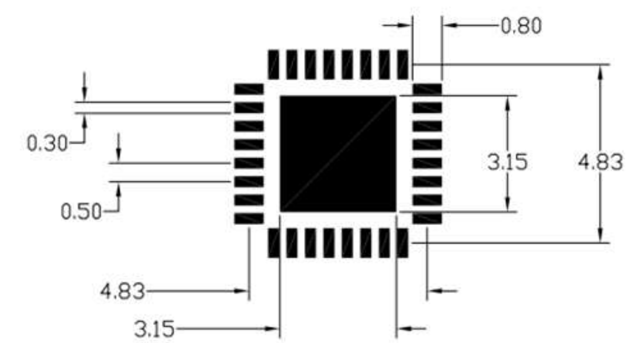


6.4 SY7T612 SY7T612E

6.4.1 Package Outline Drawing

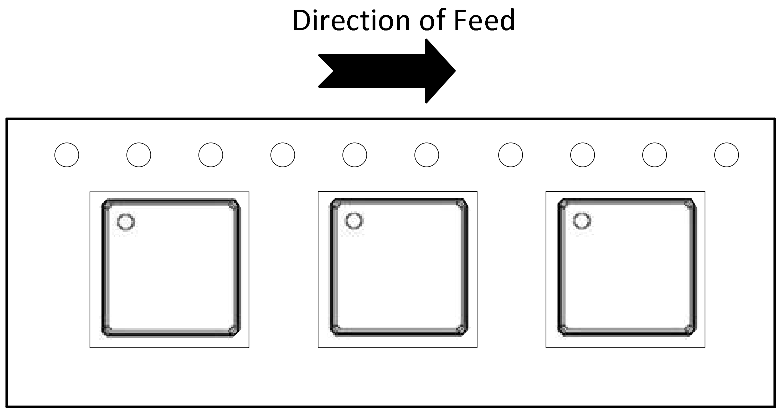


COMMON DIMENSIONS			
PKG.	32L 5x5		
SYMBOL	MIN.	NOM.	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	0.20 REF.		
b	0.20	0.25	0.30
D	5.00 BSC		
E	5.00 BSC		
e	0.50 BSC.		
k	0.25	-	-
L	0.30	0.40	0.50
N	32		
ND	8		
NE	8		
JEDEC	WHHD-2		



NOTES:
1. REFERENCE PKG. OUTLINE: 21-0140
2. LAND PATTERN COMPLIES TO: IPC7351A.
3. TOLERANCE: +/- 0.02 mm.
4. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.
5. ALL DIMENSIONS IN MM.

6.4.2 Tape & Reel Orientation



7 Contact Information

For more information about the SY7T6xx/SY7T6xxE, contact support.em@silergy.com

8 Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION
1.0	12/2025	Initial release. Combine all the SY7T6xx/SY7T6xxE into one datasheet.
1.1	01/2026	Minor corrections

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