SY7T108F/G
Electricity Metering SoC for Single-Phase Systems

General Description

The SY7T108F/G is a versatile electricity metering SoC for single-phase electricity meters and power monitoring systems. The SY7T108F/G contains one dedicated ADC (ADCS) and one multiplexed ADC (ADCM) to accommodate all single-phase metering configurations. Shunts, CTs, or Rogowski coils can be used as current sensors.

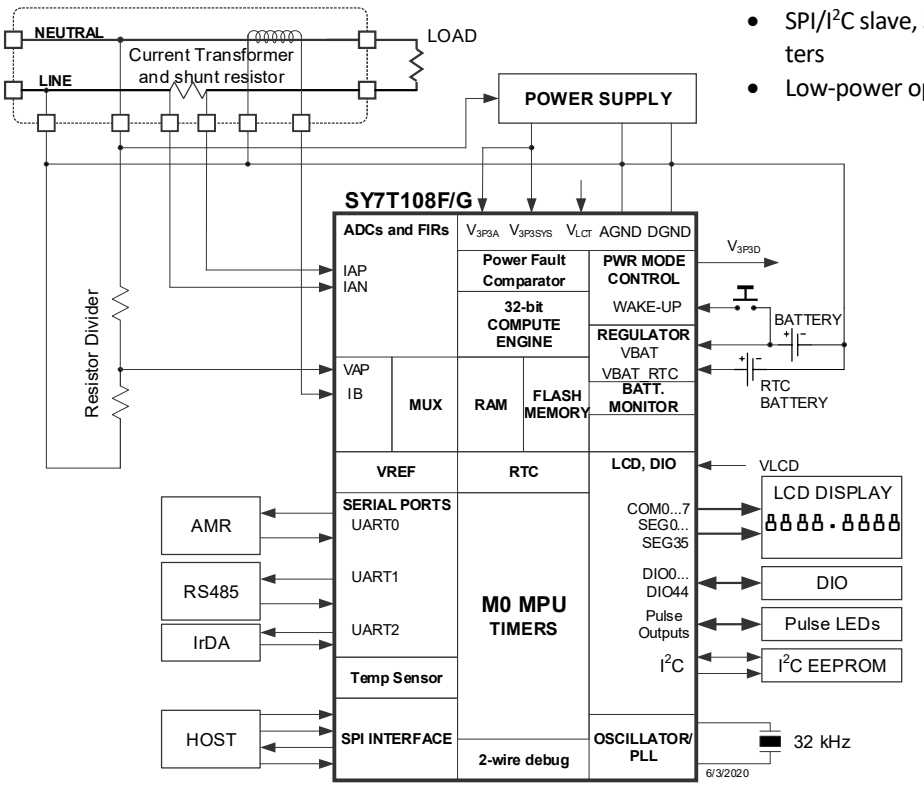
An embedded 32-bit Compute Engine (CE) performs all necessary computations and data formatting for accurate reporting of metrology parameters to the Cortex M0 core. With integrated flash memory for storing code, nonvolatile calibration coefficients and device configuration settings, the SY7T108F/G offers a completely autonomous solution and can interface to a host processor through its SPI, UART, or I^2C ports. The device is available in a 64-pin LQFP package.

Applications

- Smart Meters and sub-meters
- Building Automation Systems
- Inverters and Renewable Energy Systems
- Level 1 and 2 EV Charging Systems
- Grid-Friendly Appliances and Smart Plugs

Features

- Powerful 32-bit ARM Cortex M0 core
- 64KB (SY7T108F), 128KB (SY7T108G) of Flash memory
- 8KB (SY7T108F), 12KB (SY7T108G) data RAM, 128 bytes NV-RAM
- Up to 10MHz clock frequency
- Dedicated 32-bit 10MHz Compute Engine (CE) core
- Optimized CE code image provided by Silergy, suitable for most metering applications and adaptable to specific applications
- Compatible with capacitively coupled isolated remote sensors (SY7M007) – contact your Silergy representative for the SY7M007 data sheet.
- Brownout mode functional with 2.5V V_{BAT} supply
- On-chip digital temperature sensor
- Configurable ADC sampling rate, up to 16kHz (practical restrictions on CE cycles and resolution apply)
- On-chip RTC with accurate 1-second pulse output
- ±0.1% Wh accuracy over 5,000:1 current range with CT
- Large selection of on-chip features
- Single 32kHz crystal provides all operating clocks
- Internal 32kHz backup R/C clock generator
- Up to 36 LCD segment pins, up to 8 commons, 15 pages
- Up to 45 GPIO pins, all are interrupt-capable
- Pre-amp gain selectable 1 or 8 for ADCS
- SPI/I^2C slave, SPI master ports, three UARTs, four counters
- Low-power operation for line-cut tamper mode

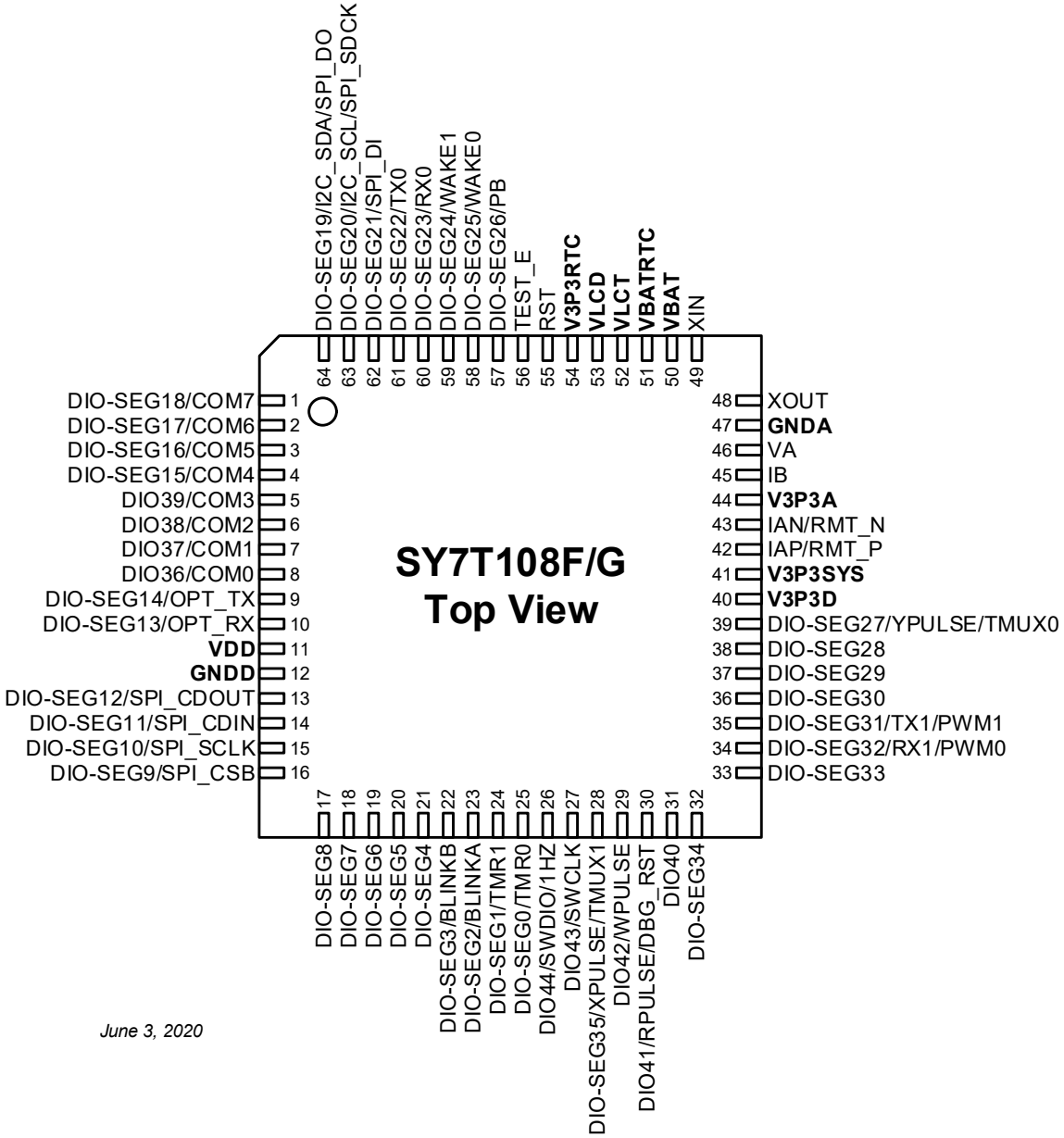


Ordering Information

Ordering Number	Carrier Type	Temperature Range	Package	Flash Memory	Top Mark
SY7T108FBGDF	Bulk/tray	-40°C to +85°C	64 LQFP	64KB	TERIDIAN SY7T108F RRyywwz †
SY7T108FGDF	Reel				
SY7T108GBGDF	Bulk/tray			128KB	TERIDIAN SY7T108G RRyywwz †
SY7T108GGDF	Reel				

† RR = die revision, yy = assembly year, ww = work week, z= assembly lot number code

Pinout (top view)



June 3, 2020

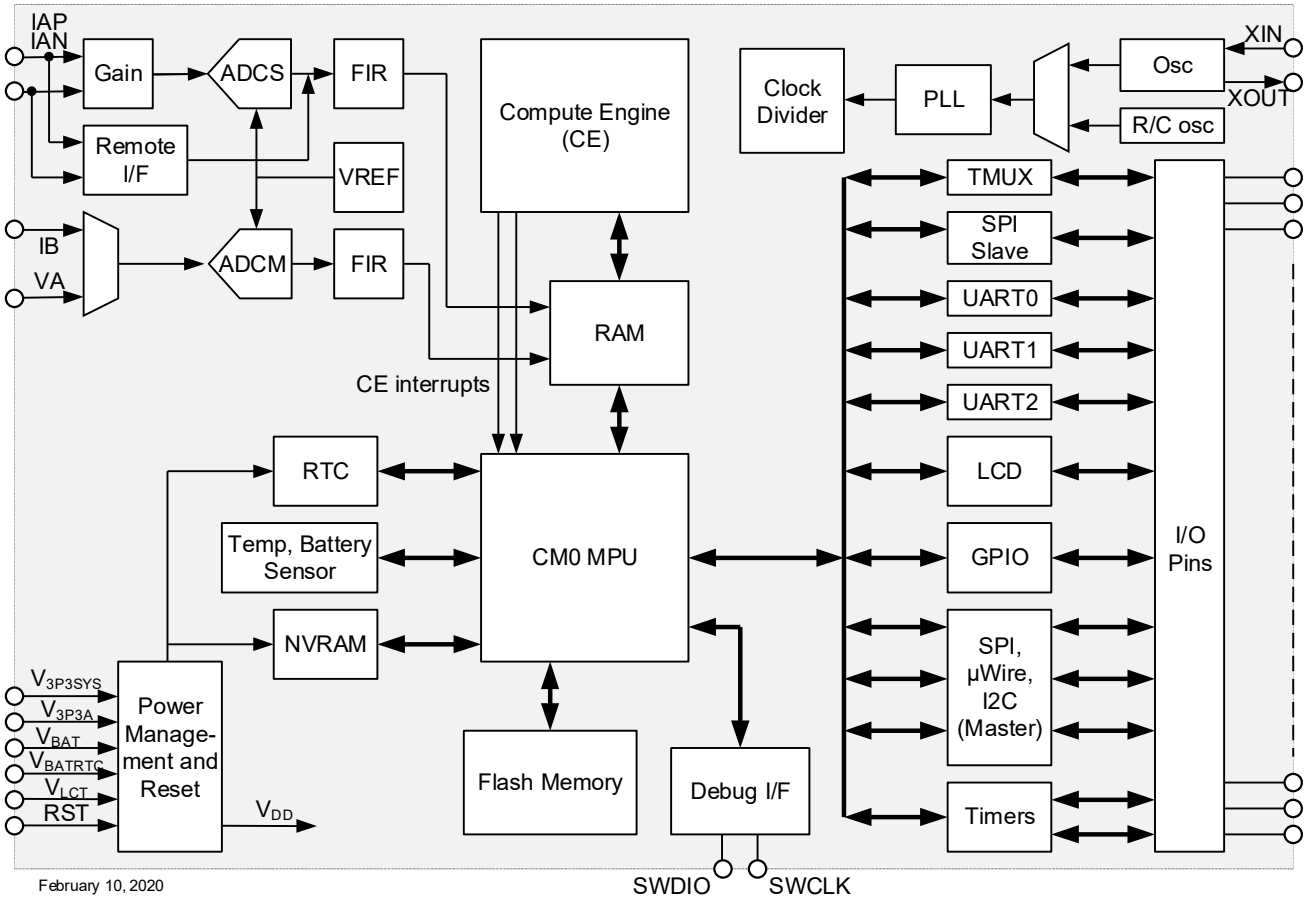
Pin List

Pin Name	Pin Number	Pin Description
DIO18/SEG18/COM7	1	GPIO, LCD segment, LCD common
DIO17/SEG17/COM6	2	GPIO, LCD segment, LCD common
DIO16/SEG16/COM5	3	GPIO, LCD segment, LCD common
DIO15/SEG15/COM4	4	GPIO, LCD segment, LCD common
DIO39/COM3	5	GPIO, LCD common
DIO38/COM2	6	GPIO, LCD common
DIO37/COM1	7	GPIO, LCD common
DIO36/COM0	8	GPIO, LCD common
DIO14/SEG14/OPT_TX	9	GPIO, LCD segment, optical UART TX
DIO13/SEG13/OPT_RX	10	GPIO, LCD segment, optical UART RX
VDD	11	Bypass point for the flash supply voltage. A capacitor to GND should be connected.
GNDD	12	Digital GND
DIO12/SEG12/SPI_CDOUT	13	GPIO, LCD segment, SPI slave data out
DIO11/SEG11/SPI_CDIN	14	GPIO, LCD segment, SPI slave data in
DIO10/SEG10/SPI_SCLK	15	GPIO, LCD segment, SPI slave clock
DIO9/SEG9/SPI_CSB	16	GPIO, LCD segment, SPI slave chip select
DIO8/SEG8	17	GPIO, LCD common
DIO7/SEG7	18	GPIO, LCD segment
DIO6/SEG6	19	GPIO, LCD segment
DIO5/SEG5	20	GPIO, LCD segment
DIO4/SEG4	21	GPIO, LCD segment
DIO3/SEG3/BLINKB	22	GPIO, LCD segment (blink)
DIO2/SEG2/BLINKA	23	GPIO, LCD segment (blink)
DIO1/SEG1/TMR1	24	GPIO, LCD segment, timer 1 input
DIO0/SEG0/TMR0	25	GPIO, LCD segment, timer 0 input
DIO44/SWDIO/1S_PLS	26	GPIO, data for debug interface (when enabled by TEST_E), 1 second pulse
DIO43/SWCLK	27	GPIO, debug clock (when enabled by TEST_E)
DIO35/SEG35/TMUX1/ XPULSE	28	GPIO, LCD segment, test multiplexer output (TMUX1), XPULSE
DIO42/WPULSE	29	GPIO, Wh (active) pulse
DIO41/RPULSE/ DBG_RSTB	30	GPIO, VARh (reactive) pulse, debug reset (when enabled by TEST_E)
DIO40	31	GPIO
DIO34/SEG34	32	GPIO, LCD segment
DIO33/SEG33	33	GPIO, LCD segment
DIO32/SEG32/PWM0/RX1	34	GPIO, LCD segment, PWM0 out, UART1 RX

DIO31/SEG31/PWM1/TX1	35	GPIO, LCD segment, PWM1 out, UART1 TX
DIO30/SEG30	36	GPIO, LCD segment
DIO29/SEG29	37	GPIO, LCD segment
DIO28/SEG28	38	GPIO, LCD segment
DIO27/SEG27/TMUX0/ YPULSE	39	GPIO, LCD segment, test multiplexer (TMUX0) output, CE pulse output
V_{3P3D}	40	Bypass point for GPIO supply. A capacitor to GND, but no external loads should be connected to this pin.
V_{3P3SYS}	41	Digital supply
IAP/RMT_P	42	Positive input for ADC0 or for capacitive interface to SY7M007
IAN/RMT_N	43	Negative input for ADC0 or for capacitive interface to SY7M007
V_{3P3A}	44	Analog supply
IB	45	Input for ADC1 (multiplexed)
VA	46	Input for ADC1 (multiplexed)
GNDA	47	Analog GND
XOUT	48	Crystal oscillator output
XIN	49	Crystal oscillator input
V_{BAT}	50	Main battery voltage input
V_{BAT_RTC}	51	RTC battery and NV-RAM voltage input
V_{LCT}	52	Line-cut voltage input to internal regulator
V_{LCD}	53	LCD supply input
V_{3P3RTC}	54	Bypass point for non-volatile supply
RST	55	Reset pin (active high)
TEST_E	56	Factory test and debug mode enable input (active high)
DIO26/SEG26/PB	57	GPIO, LCD segment, pushbutton input
DIO25/SEG25/WAKE0	58	GPIO, LCD segment, wake input (edge-triggered)
DIO24/SEG24/WAKE1	59	GPIO, LCD segment, wake input (edge-triggered)
DIO23/SEG23/RX0	60	GPIO, LCD segment, UART0 RX
DIO22/SEG22/TX0	61	GPIO, LCD segment, UART0 TX
DIO21/SEG21/SPI_DI	62	GPIO, LCD segment, master SPI data input
DIO20/SEG20/I2C_SCL/ SPI_SDCK	63	GPIO, LCD segment, I^2C clock, master SPI master clock
DIO19/SEG19/SPI_DO	64	GPIO, LCD segment, I^2C data, master SPI data out

1 Hardware Description

1.1 SY7T108F/G Functional Block Diagram



1.2 On-Chip Resources

Clock Management

For normal operation, an external 32kHz watch crystal is used to drive the internal oscillator. A PLL generates the master clock from the 32kHz signal. If the external crystal fails, an internal oscillator trimmed to 32kHz takes over for continuous operation. Since it is not as accurate as the crystal oscillator, the internal oscillator should not be used for metrology or timekeeping.

Power-On Reset (POR)

An on-chip power-on reset (POR) block monitors the supply voltage (VDD) and initializes the internal digital circuitry at power-on. Once VDD is above the minimum operating threshold, the POR circuit triggers and initiates a reset sequence. It also issues a reset to the digital circuitry if the supply voltage falls below the minimum operating level.

No external reset circuitry is necessary.

Watchdog Timer (WDT)

A watchdog timer (WDT) block detects any software processing errors. The embedded code periodically refreshes the free-running watchdog timer to prevent it from timing out. If the WDT times out, it is an indication that software is no longer being executed in the intended sequence; thus, a system reset is initiated. The WDT cannot be disabled by code.

External Reset Pin (RST Pin)

The RST pin can be used in test and evaluation to reset the SY7T108F/G. For proper reset, the RTS pin must be pulled high for at least 5µs.

32-Bit Compute Engine (CE)

The Compute Engine is 32-bit DSP that performs management and signal processing of the ADC samples. It can perform read and write operation in the dedicated memory space with no wait states. The CE is a programmable device, and Silergy typically provides binary code modules that the CE uses to perform energy computations. The CE calculations and processes may include:

- Multiplication of each current sample with its associated voltage sample to obtain the energy per sample (when multiplied with the constant sample time).
- 90° phase shifter (for VAR calculations).
- Pulse generation.
- Measurement of the input signal frequency (for frequency and phase information).
- Monitoring of the input signal amplitude (for sag detection).
- Scaling of the processed samples based on calibration coefficients.
- Scaling of samples based on MPU temperature compensation information.
- Creep processing
- Extraction, suppression or filtering of harmonics for special functions.
- Variable gain compensation.
- Variable phase compensation.

The CE Code image resides in flash as part of the Cortex M0 code image.

The CE is a fixed-function core and is not user programmable. Silergy Technology provides many different configurations for the CE as precompiled modules that can be linked into user programs. Please see the relevant *CE Code Reference Manual* for specific functional details.

Debug Interface

The part has an integrated debugger that allows real-time debugging of the code running on the Cortex M0 MPU core. Basic debug functionality includes processor halt, single-step, processor core register access, Reset and Hard Fault Vector Catch, four hardware breakpoints, and full system memory access.

The debug system uses Serial-Wire Debug (SWD), not JTAG.

RAM

The RAM accessible to the Cortex M0 MPU core is implemented as SRAM. A RAM controller manages simultaneous access requests from multiple SRAM clients. The clients are the CE (data), RTM, FIRs for ADCM and ADCS, LCD DMA, and the Cortex M0 MPU core.

The Cortex M0 MPU core can directly access a total of 8KB, or 2024 32-bit words.

NV-RAM

The 128 bytes of NV-RAM are not directly accessible and have their own address range. Each cell pointed to by the address pointer has access to 32 bits. The size of the NV-RAM is 32 words, or 128 bytes.

Flash Programming

The flash memory can be programmed via the debug interface.

Digital I/O Pins

The SoC contains 45 pins that can be configured as digital I/O (DIO0 – DIO44). When assigned for general-purpose I/O (GPIO), the user can select from different configurations. Pins configured for DIO provide the following properties:

- Programmable interrupt generation capability.
- Bit-masking support using address values.
- Registers for alternate function switching with pin multiplexing support.
- Thread-safe operation by providing separate set and clear addresses for control registers.
- Inputs are sampled using a double flip-flop to avoid meta-stability issues.

Individual pins can be configured for LCD or DIO functions using registers, and then can be controlled using two separate mechanisms:

- Using the *LCD_DIO* registers
- Using the register set provided by the Cortex M0 core, therefore taking advantage of masked access and advanced interrupt control. DIO0 – DIO31 can be managed by the Cortex M0 MPU core registers. To control DIO32 – DIO44, the *LCD_DIO* registers must be used.

External components such as LEDs, relay coils, etc. should be pulled low by a DIO pin, not driven high.

LCD System

The SY7T108F/G supports up to 45 DIO pins, up to 36 LCD SEG (segment) pins, and a total 8 COM pins (4 dedicated COM pins and 4 shared COM pins). The 4 shared COM pins are:

- COM4/SEG15
- COM5/SEG16
- COM6/SEG17
- COM7/SEG18

The *LCD.MAPH* register controls the configuration for pins SEG32/DIO32 through SEG35/DIO35 and DIO36/COM0 to DIO39/COM3, the *LCD.MAPL* register controls SEG0/DIO0 to SEG31/DIO31. Each bit in these registers controls the configuration of its associated pin: When the bit is set, the pin is in LCD mode and acts as an LCD segment or COM pin. When cleared, the pin is in DIO mode and its function is controlled by the corresponding LCD segment register.

Key features of the LCD System are:

- Automated blinking without MPU interference is possible on two pins: SEG2 and SEG3. With 8 COM pins, this allows for a maximum of 16 blinking segments. The blink rate can be programmed to be 0.5Hz or 1.0Hz.
- Multiple LCD display pages. The device can cycle through a maximum of 15 pages of data at a programmable time interval of up to 32 seconds with 0.25 seconds resolution when the page DMA is enabled.

Real-Time Clock (RTC)

The RTC keeps accurate time based on the direct output of the 32.768KHz crystal oscillator. The resolution of the RTC output is 1/256th of a second. The RTC output is guaranteed to be monotonic, i.e. the RTC only increments, and cannot decrement due to calibration or temperature compensation. To maintain accuracy across temperature the RTC can be configured to periodically make temperature measurements and compensate the rate at which the RTC accumulates time.

The real-time clock (RTC) block includes a time-of-day clock plus a set of ancillary features to keep the clock accurate and to provide additional services to the system. The RTC include the following features:

- Weekday, date, month, year, seconds, minutes, hours registers with corresponding shadow registers for safe read and write operations
- Eight-bit sub-seconds register.
- Alarm register.
- Wake MPU core from SLP mode on a variety of events.
- Temperature measurement for RTC compensation.
- Third-order (cubic) temperature compensation hardware.

Timers and Counters

The SY7T108F/G comprises two separate timer modules with two timers each:

- Generic timers, Timer0 and Timer1, with inputs accessible through DIO pins
- Dual-input timers, Dtimer0 and Dtimer1

Analog Features

- Reference Voltage
- The reference voltage is buffered. The buffer amplifier contains a chop circuit that eliminates temperature drift. The temperature coefficient of the reference voltage itself can be compensated. Typical CE Code features VREF compensation based on die temperature and typical VREF temperature coefficients using a quadratic equation.
- Temperature Sensor
- An on-chip temperature sensor is provided. The temperature sensor can be used by the Cortex M0 MPU as part of the application code, but it also can support automatic periodic measurements in SLP mode. Temperature limits can be defined to trigger automatic wake ups from SLP mode.
- Battery Monitor
- The part can monitor the voltage on the two battery pins (V_{BAT} and V_{BAT_RTC}).

Communication Interfaces

UARTs: Three UARTs are available. UART2 is equipped with an optional optical encoder in transmit (TX) direction and an optional IrDA decoder in the receive (RX) direction.

SPI/I²C/µWire Master: Three pins are configurable for operation as SPI, I²C, or µWire master interfaces that can be used to connect EEPROMs, display controllers, and other peripheral devices.

SPI Slave Port: The SPI slave port communicates directly with the internal AHB (Advanced High-Performance) bus. It can read and write RAM and register locations. The hardware interface of the SPI slave port uses the SPI_CSB, SPI_SCLK, SPI_CDIN, and SPI_CDOUT pins, which are multiplexed with LCD segment driver pins 9-12. To facilitate flash programming, cold start and reset cause the port pins to default to SPI mode. Interrupts to the Cortex M0 MPU core can be generated by the slave SPI port and both single-byte and multi-byte transactions are possible. In SSPI Safe Mode, SSPI write operations are disabled except for a 16-byte transfer region at address 0x2000_0400 to 0x2000_04FC.

1.3 Power Modes

The SoC supports five operational (power) modes:

- **Mission (MSN) mode:** The part is in *MSN Mode* when the primary power supply is within specification. Primary power is supplied via the V_{3P3SYS} (digital power) and V_{3P3A} (analog power) pins. Comparators on the V_{3PSYS} pin monitor the voltage level on this bus. If the voltage at the V_{3PSYS} pin falls below a set threshold, the part automatically enters *BRN Mode*.
- **Brownout (BRN) mode:** In *BRN Mode*, the voltages at V_{3P3A} and V_{3P3SYS} are too low to maintain MSN mode operation, and the supply for the I/O and other circuits is automatically switched to the V_{BAT} input. In BRN *Mode* the metrology blocks are functional, and the Cortex M0 MPU core continues to operate at full speed until the firmware selects a lower clock speed, and/or powers down the ADCs to reduce power consumption. BRN mode can be maintained until the voltage at the V_{BAT} pin falls below 2.5V.
- **LCD-ONLY mode:** This mode is commanded by the Cortex M0 MPU core. In this mode, the LCD can take its power from either V_{BAT} or from an external VLCD supply, depending on the LCD configuration. The Cortex M0 MPU core and the analog functions are not available in *LCD-ONLY* mode. It is possible to place up to 15 different images of the LCD in RAM, and step through them automatically without using the Cortex M0 MPU. To support this, RAM remains powered in *LCD-ONLY* mode.
- **Sleep (SLP) mode:** The *SLP Mode* is commanded by the Cortex M0 MPU core. In *SLP* mode, hardware shuts down all logic blocks except the RTC and non-volatile memory blocks. In SLP mode all power to the device except the NV domain (and the LCD domain if *LCD-ONLY* is selected) is removed. The only way to exit SLP mode is if a wake event occurs. Various events can be configured to cause a wake up from *SLP* mode, e.g. timer, UART0 RX, pushbutton, two wake pins, or temperature.
- **Line-Cut (LCT) mode**: In this mode, power is supplied via the V_{LCT} pin, and the metrology blocks of the part function at reduced accuracy. LCT mode is a counter measure for tampering attempts that involve removing the wires at the LINE and NEUTRAL terminals and connecting the LINE wire to the NEUTRAL terminal, while feeding the load with the NEUTRAL output of the meter. In this mode, one side of the load is connected to earth ground. An auxiliary CT in the NEUTRAL circuit typically provides a few milli-amperes that can be used to feed the SY7T108F/G via its LCT input. Alternatively, a battery or super-capacitor can be used. Once, the part is in LCT mode, it can continue to perform metrology at reduced sample rate and accuracy.

Hardware in the SoC and firmware control transitions between the power modes.

There are nine power-related pins in the part:

- **V_{3P3SYS}:** This is the primary digital supply input for the device. It is typically connected to the same supply as V_{3P3A}, but is separately bypassed.
- **V_{3P3A}:** This is the primary analog supply input for the device. In MSN mode, it provides power to the ADC blocks, to the voltage comparator blocks and to the bandgap voltage reference with its output buffer. In LCT mode, power for the metrology blocks is switched to the V_{LCT} Pin.
- **V_{LCT}:** This is a secondary supply pin for digital and analog blocks that can be used to power reduced-accuracy metering functions when the main board power source has been removed. Typically, this pin is supplied from an auxiliary CT or from a battery.
- **V_{BAT}:** The primary battery supply input. This input is selected to provide system power when the V_{3P3SYS} circuit falls below its threshold level.
- **V_{BAT_RTC}:** This pin provides the RTC and non-volatile memory backup power. It is typically connected to a lithium battery to maintain the RTC and NV memory elements.
- **V_{3P3RTC}:** This pin provides a bypass point for the non-volatile power domain.
- **V_{3P3D}:** The output from an internal switch that selects either V_{3P3SYS} (if the primary supply is above threshold) or V_{BAT} (if the primary supply is below threshold). This pin should always be bypassed and never be used to drive external loads.
- **V_{LCD}:** Usually, this is a bypass point for the LCD supply. Frequently the supply will be the LCD DAC, although it can also be the currently selected V_{BAT} or V_{3P3SYS} supply, directly. This pin can also be used as an input to provide an external voltage to the LCD system.
- **V_{DD}:** The bypass point for the power supply to the internal flash memory

1.4 Operation

1.4.1 Metering Operation and Processes

Metrology tasks are handled by the Compute Engine, which completely frees up the Cortex M0 MPU for communication, security, and household tasks.

Processing by the CE typically involves the following operations:

- DC offset removal
- Multiplication of each current sample with its associated voltage sample to obtain the energy per sample
- 90° phase shifter for VARh calculations
- Measurement of the input signal frequency and mains voltage zero crossing
- Monitoring of the signal amplitude for sag and swell detection
- Scaling of the processed samples based on calibration coefficients
- Monitoring of the die temperature
- Scaling of the processed samples based on temperature compensation information
- Accumulation of energy from all phases in fixed intervals for reporting to the host microcontroller
- Squaring and summation of voltage samples for V_{RMS} processing
- Squaring and summation of current samples for I_{RMS} processing
- Delay compensation for shunt sensors, phase compensation for CTs
- Pulse generation
- Extraction, suppression or filtering of harmonics

Metrology data are typically collected and integrated by the CE for one second and are then available to the Cortex M0 MPU in transfer registers. The integration time is configurable.

1.5 Calibration

The calibration process will largely depend on available calibration system hardware and implemented MPU code. All widely used calibration methods, e.g. absolute, ratiometric, multi-point, and auto-calibration, etc., are supported.

1.6 Temperature Compensation

It can be assumed that the part is trimmed at 22°C to produce a uniform voltage reference gain at that temperature. The voltage reference can be digitally compensated over changes in measured die temperature using a cubic equation. The coefficients for the compensation equation can be generated from fuse settings. See the CE Reference Manual for details on temperature compensation.

2 Electrical Specifications

2.1 Absolute Maximum Ratings (1)

Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

	Min	Max	Unit
Supply and Ground Pins			
V_{3P3SYS}, V_{3P3A}	-0.5	+3.8	V
V_{LCT}	-0.5	+6.0	V
V_{BAT}, V_{BAT_RTC}	-0.5	+3.8	V
GNDD, GNDA	-0.1	+0.1	V
Analog Output Pins			
V_{LCD}	-10	+10	mA
	-0.5	+3.8	V
V_{3P3D}	-10	+10	mA
	-0.5	+3.8	V
V_{DD}	-10	+10	mA
	-0.5	+3.0	V
V_{3P3RTC}	-10	+10	mA
	-0.5	+3.8	V
Analog Input Pins			
VA, IAP/IAN, IB	-10	+10	mA
	-0.5	V_{3P3A}+ 0.5	V
XIN, XOUT	-10	+10	mA
	-0.5	+3.0	V
LCD Segment and SEG-DIO Pins			
Configured as SEG or COM drivers	-1	+1	mA
	-0.5	V_{LCD}+ 0.5	V
Configured as Digital Inputs (all DIO pins except DIO23 – DIO26)	-10	+10	mA
	-0.5	V_{3P3D} +0.5	V
Configured as Digital Inputs (DIO pins DIO23 – DIO26)	-10	+10	mA
	-0.5	V_{3P3RTC} +0.5	V
Configured as Digital Outputs (all DIO pins except DIO23 – DIO26)	-10	+10	mA
	-0.5	V_{3P3D}+ 0.5	V
Configured as Digital Outputs (DIO pins DIO23 – DIO26)	-10	+10	mA
	-0.5	V_{3P3RTC} +0.5	V

	Min	Max	Unit
Test and Reset Pins			
TEST_E, RST	-10	+10	mA
	-0.5	V_{3P3RTC} + 0.5	V
Flash Memory			
Flash memory program/erase cycles	20,000		
Temperature			
Operating junction temperature, peak, 100ms		+140	°C
Operating junction temperature, continuous		+125	°C
Storage temperature	-45	+165	°C
Solder temperature, 10s duration		+250	°C

2.2 Thermal Information

θJA is measured in the natural convection at T_A = 25°C on a two-layer Silergy Evaluation Board.

		Unit
θJA Junction-to-ambient thermal resistance	55.4	°C/W
θJC Junction-to-case (bottom) thermal resistance	13	
PD Power dissipation T_A = 25°C	15	mW

2.3 Recommended Operating Conditions

The device is not guaranteed to function outside its operating conditions

Parameter	Conditions	Min	Max	Unit
Supply Voltages (V_{3P3A}, V_{3P3SYS})	Precision metering operation, V_{BAT} = 0 – 3.8V, V_{BAT_RTC} = 0 – 3.8V	3.0	3.6	V
Supply Voltages (V_{3P3A}, V_{3P3SYS})	Reduced accuracy metering mode	2.5	3.0	V
V_{BAT} Supply Voltage	BRN mode	2.5	3.8	V
V_{BAT_RTC} Voltage	SLP mode, LCD-ONLY mode	2.0	3.8	V
V_{LCT} Supply Voltage	Line-cut metering mode	4.1	5.5	V
Operating Temperature		-40	+85	°C

2.4 Recommended External Components

Name	From	To	Function	Value	Unit
XTAL	XIN	XOUT	32.768kHz	32.768	kHz
CXS	XIN	GND	Load capacitor for crystal. Exact value depends on crystal specifications and parasitic capacitance of board (4pF assumed).	20 ±10%	pF
CXL	XOUT	GND		20 ±10%	pF
CV3P3A	V_{3P3A}	GND	Analog supply bypass capacitor	1.0±30%	µF
CV3P3S	V_{3P3SYS}	GND	Digital supply bypass capacitor	1.0±30%	µF
CV3P3D	V_{3P3D}	GND	V_{3P3D} bypass capacitor	0.1±20%	µF

Name	From	To	Function	Value	Unit
CVDD	V_{DD}	GND	Flash supply bypass capacitor	1.0±20%	µF
CVLCD	V_{VLCD}	GND	LCD supply bypass capacitor	0.1±20%	µF
CVLCT	V_{LCT}	GND	LCT supply bypass capacitor	100±20%	µF
CVRTC	V_{3P3RTC}	GND	Non-volatile supply bypass capacitor	1.0±30%	µF

2.5 Electrical Characteristics

Note that production tests are performed at room temperature

Parameter	Symbol	Test Conditions [3]	Min	Typ	Max	Unit
Input Logic Levels						
Digital High-Level Input Voltage †	V_{IH}		2.3			V
Digital Low-Level Input Voltage †	V_{IL}				0.6	V
Input Current	I_H, I_{IL}		-1.5		+1.5	µA
Input Pull-Up Resistance	R_{pup}		20		160	kΩ
Input Pull-Down Resistance	R_{pdn}		15		100	kΩ
† In battery-powered modes, digital inputs should be below 0.1V or above V_{BAT}-0.1V to minimize battery current						
Output Logic Levels						
Digital High-Level Output Voltage, all DIO pins except DIO23 – DIO26	V_{OH}	I_{LOAD} = 1mA	V_{3P3D} -0.4			V
		I_{LOAD} = 5mA†	V_{3P3D} -0.6			V
Digital High-Level Output Voltage, pins DIO23 – DIO26	V_{OL}	I_{LOAD} = 0.1mA ††		V_{3P3RTC} – 0.1		V
Digital Low-Level Output Voltage	V_{OL}	I_{LOAD} = 1mA			0.4	V
		I_{LOAD} = 15mA			0.85	V
† Caution: The sum of all pull-up currents will cause a voltage drop across the relevant V_{3P3D} switch resistance, which will reduce V3P3D and the V_{OH} level, and will also decrease the margin to the V3P3D_OK threshold. $$V3P3D(I_{SUM}) = V3P3D(0) - I_{SUM} \cdot R_{SWITCH}$$ $$V_{OH}(I_{SUM}) = V_{OH}(0) - I_{SUM} \cdot R_{SWITCH}$$ †† Caution: The sum of all pull-up currents will cause a voltage drop across the relevant V_{3P3RTC} switch resistance, which will reduce the V_{OH} level.						
Input Spike Width Tolerance						
Reset Spike †	t_{RST}	Note 1	420	1100	1800	ns
TEST Pin Spike †	τ_{TEST}	Note 1	420	1100	1800	ns
Spike for DIO23 to DIO26 †		Note 1	420	1100	1800	ns
† Positive pulses narrower than Tspike_min will be ignored by these pins. When asserted high, these pins must be held at least for a duration of Tspike_max						
V3P3D SWITCH						
On-Resistance (V_{3P3SYS} to V_{3P3D})	RON	I(V_{3P3D}) ≤ 7mA		5	8	Ω
On-Resistance (V_{BAT} to V_{3P3D})	RON	I(V_{3P3D}) ≤ 7mA, V_{BAT} ≥ 2.5V		6	11	Ω
V_{3P3D} Current, MSN mode	I_{OH}	V_{3P3SYS} = 3.0V, V_{3P3D} = 2.9V	9			mA
V_{3P3D} Current, BRN mode	I_{OH}	V_{BAT} = 2.6V, V_{3P3D} = 2.5V	5			mA

Parameter	Symbol	Test Conditions [3]	Min	Typ	Max	Unit
Note that the sum of all pull-up currents in all DIOs except DIO23 – DIO26 will cause a voltage drop across the relevant V_{3P3D} switch resistance, which will reduce V_{3P3D} voltage and the V_{OH} level. $V3P3D(I_{SUM}) = V3P3D(0) - I_{SUM} \cdot R_{SWITCH}$ $V_{OH}(I_{SUM}) = V_{OH}(0) - I_{SUM} \cdot R_{SWITCH}$						
V3P3RTC SWITCH						
On-Resistance (V_{3P3SYS} to V_{3P3RTC})	RON	I($V_{3P3RTCD}$) ≤ 1mA			75	Ω
On-Resistance (V_{BAT} to V_{3P3RTC})	RON	I(V_{3P3RTC}) ≤ 1mA, V_{BAT} > 2.5V			75	Ω
On-Resistance (V_{BAT_RTC} to V_{3P3RTC})	RON	I(V_{3P3RTC}) ≤ 1mA, V_{BA_RTC} > 2.5V			100	Ω
Note that the sum of all pull-up currents in DIO23 – DIO26 will cause a voltage drop across the relevant V_{3P3RTC} switch resistance, which will reduce the V_{3P3RTC} voltage and the V_{OH} level. $V_{3P3RTC}(I_{SUM}) = V_{3P3RTC}(0) - I_{SUM} \cdot R_{SWITCH}$ $V_{OH}(I_{SUM}) = V_{OH}(0) - I_{SUM} \cdot R_{SWITCH}$						
Metrology Reference Voltage (VREF)						
Reference Voltage	VREF	TA = +22°C	1.21	1.213	1.216	V
Power Supply Rejection	PSRR	ΔVREF/ΔV_{3P3A}, V_{3P3A} = 3.0V to 3.6V	-1.5		+1.5	$\frac{mV}{V}$
Nominal Voltage Definition	VNOM	VNOM(S)=VREF22+ ((5.9790*10^{-5}-3.3866*10^{-06}*TRIMT+ 4.5681*10^{-08}*TRIMT^2) *(S-S_{22})) - 2.5406*10^{-09}*(S-S_{22})^2 $S = STEMP$, $S_{22} = STEMP(22)$ = *STEMP* at calibration (22°C)				V
Linear Temperature Coefficient	TC1	IC w/o temperature trim		-3.3866 *10^{-06} *TRIMT		$\frac{V}{°C}$
Quadratic Temperature Coefficient	TC2			4.5681 *10^{-8} *TRIMT^2		$\frac{V}{°C^2}$
VREF Deviation from VNOM(T) (IC w/o dual temperature trim)		$\frac{VREF(T) - VNOM(T)}{VNOM(T)} \frac{10^6}{62}$	-44		+44	$\frac{ppm}{°C}$
Supply Currents						
Digital Supply Current †	$I_{V3P3SYS}$	Normal operation, MPU @ 5MHz, ADCS @ 1.7MHz, ADCS bias < 2.5MHz, ADCM @ 5MHz, ADCM bias 5MHz		1	1.4	mA
Analog Supply Current †	I_{V3P3A}			3.3	4.2	mA
Digital Supply Current †	$I_{V3P3SYS}$	Normal operation, MPU @ 2.5MHz, ADCS @ 426kHz, ADCS bias < 500kHz, ADCM @ 2.5MHz, ADCM bias 2.5MHz		0.9	1.25	mA
Analog Supply Current †	I_{V3P3A}			1.75	2.2	mA
Digital Dynamic Supply Current †	$\frac{\Delta I_{V3P3SYS}}{\Delta f}$	Normal operation, but MPU clock speed varied	0.04	0.055	0.07	$\frac{mA}{MHz}$
† Conditions for supply currents: V_{3P3SYS} = 3.3V, V_{3P3A} = 3.3V, RTM off, CE on, both ADCS and ADCM enabled, no flash memory write						
Digital Supply Current	$I_{V3P3SYS}$	Normal Operation, except write Flash at maximum rate, *CE_E*=0, *ADC_E*=0		5.6	8.6	mA

Parameter	Symbol	Test Conditions [3]	Min	Typ	Max	Unit
Line Cut Supply Current (added current for LCT regulator)	I_{VLCT}	ADCS, ADCM, off, *adc_vls* = 1		0.2	0.3	mA
Battery Currents	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Battery Current (3.0V < V_{BAT} < 3.8V)	I_{VBAT}	MSN mode, V_{3P3SYS}, V_{3P3A} > 3.0V	-100		+100	nA
	I_{VBAT}	BRN mode, V_{3P3SYS}, V_{3P3A} = 0V		2.5	3.5	mA
	I_{VBAT}	LCD-ONLY mode, *LCD_MODE* = 11 (external VLCD)			14	µA
	I_{VBAT}	LCD-ONLY mode, LCD_ MODE = 10 (unused)			33	µA
	I_{VBAT}	LCD-ONLY mode, LCD_ MODE = 01 (V_{3P3D}, DAC)		20	33	µA
	I_{VBAT}	LCD-ONLY mode, *LCD_ MODE* = 00 (V_{3P3D}, no DAC)		7	14	µA
	I_{VBAT}	SLP mode		5	10	µA
V_{BAT_RTC} Current (3.0V < V_{BAT_RTC} < 3.8V)	I_{VBAT_RTC}	MSN mode		0	20	nA
	I_{VBAT_RTC}	BRN mode		0	20	nA
	I_{VBAT_RTC}	SLP mode		3	7	µA
Line-Cut Current		Current is equivalent to current in BRN or MSN mode, with I_{VLCT} added.				
Crystal Oscillator						
Maximum Output Voltage	V_{OUT}	V_{in}=0.2V-pp sine wave, 32.8kHz, no test load			1.5	V
Transconductance †		Vin=32.8kHz, 10mVpp sine, voltage measured across 100kΩ	4.5		130	µS
Peak Output Source Current	I_{OUT}	I_{XOUT} for V_{XOUT} = 0V	0.25		5.8	µA
Frequency Variation with Voltage, relative to frequency at +25°C, V_{3P3A} = 3.3V	$\frac{\Delta f}{\Delta V_{BAT\_RTC}}$	ΔV_{BAT_RTC} = 2.5V to 3.8V	-1		1	ppm
† Nominal relationship, not a measured parameter.						
Internal R/C Oscillator						
Nominal Frequency	f_{OSC}	V_{3P3SYS} = 3.3V, TA = 22°C		32.768		kHz
Accuracy		V_{3P3SYS} = 3.0V to 3.6V; TA = -40°C to +85°C	-4.5		+4.5	%
Frequency Variation with Supply	$\frac{\Delta f}{\Delta V_{BAT\_RTC}}$		-0.08		+0.08	$\frac{kHz}{V}$

Parameter	Symbol	Test Conditions [3]	Min	Typ	Max	Unit
Power Fault Comparators	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Analog Supply Threshold	V3A_OK	Rising			3.06	V
		Falling	2.86			V
		Hysteresis	32		88	mV
Digital Supply Threshold	V3_OK	Rising			2.76	V
		Falling	2.35			V
		Hysteresis	95		210	mV
Battery Supply Threshold	VBAT_OK	Rising			2.68	V
		Falling	2.3			V
		Hysteresis	20		70	mV
V_{3P3D} Threshold	V3P3D_OK	Rising			2.57	V
		Falling	2.13			V
		Hysteresis	65	80	97	mV
Power-up State Machine V_{3P3SYS} Comparator	SYS_COMP_OK	V_{3P3SYS} rising			2.75	V
		V_{3P3SYS} falling	2.31			V
		Hysteresis	100		200	mV
Power-up State Machine V_{BAT} Comparator	BAT_COMP_OK	V_{BAT} rising			2.59	V
		V_{BAT} falling	2.27			V
		Hysteresis	25		70	mV
ADCS – Staring ADC and Preamp						
Usable Input Range	V_{IN}	Gain = 1	-250		250	mV
		Gain = 8	-31.25		31.25	mV
Preamp Gain	G	Gain = 8, V_{3P3A} = 3.3V, +25°C, preamp enabled	7.88	8.0	8.1	$\frac{V}{V}$
Input Impedance	Z_{IN}	Gain = 8	3.7	6.4	8.5	kΩ
		Gain = 1	22	40	60	kΩ
Preamp Gain Variation vs. Supply	$\frac{\Delta G}{\Delta V}$	V_{3P3A} = 3.0V to 3.6V	-150		+150	$\frac{ppm}{\%}$
Preamp Gain Variation vs. Temperature	$\frac{\Delta G}{\Delta T}$	TA = -40°C…+85°C	-50		+50	$\frac{ppm}{°C}$
Preamp Supply Current	I_{PA}	ADCS clock = 825kHz, bias = 0100		0.18	0.23	mA
Preamp Phase Shift		25°C, V_{3P3A} = 3.3V		19		m°
Phase Shift Variation vs. Temperature		TA = -40°C…+85°C	-0.25		+0.25	$\frac{m°}{°C}$
Phase Shift Variation vs. Supply		V_{3P3A} = 3.0V to 3.6V	-60		+60	$\frac{m°}{V}$
Preamp Input-Referred Offset	V_{OFF}	With divide by 8	-1.5		+1.5	mV
		Without divide by 8	-12		+12	mV

Parameter	Symbol	Test Conditions [3]	Min	Typ	Max	Unit
ADCS Gain Error vs. Supply Voltage	$\frac{\Delta G}{\Delta V}$	preamp disabled	-90		+90	$\frac{ppm}{\%}$
Total Channel Gain Error vs. Supply Voltage	$\frac{\Delta G}{\Delta V}$	preamp enabled	-143		+143	$\frac{ppm}{\%}$
Total Harmonic Distortion	THD	Gain = 8, V_{in}=20mVpk, 55Hz		-82		dB
Total Harmonic Distortion	THD	Gain = 1, V_{in}=250mVpk, 55Hz		-75		dB
Differential Noise, Gain = 1	N0	FIR_LEN = 0x00, f_S = 2520Hz, V_{in} = 24mV pk, 60Hz		200		LSB
Differential Noise, Gain = 1	N1	FIR_LEN = 0x0B, f_S = 2520Hz, V_{in} = 24mV pk, 60Hz		425		LSB
Preamp Input Equivalent Noise Density $Noise/\sqrt{Hz} = \frac{NP * LSB\_SIZE}{8\sqrt{1260}}$					100	$nV/\sqrt{Hz}$
ADC Input Equivalent Noise Density $\frac{Noise}{\sqrt{Hz}} = \frac{N0 * LSB\_SIZE}{\sqrt{1260}}$		FIR_LEN = 0x0B		300		$nV/\sqrt{Hz}$
ADC Input Equivalent Noise Density, $\frac{Noise}{\sqrt{Hz}} = \frac{N1 * LSB\_SIZE}{\sqrt{1260}}$		FIR_LEN0 = 0x0F		300		$nV/\sqrt{Hz}$
ADCM – Multiplexed ADC						
Usable Input Range	V_{IN}		-250		250	mV
ADCM Supply Current	I_{ADCM}	ADCS disabled		1.2	1.45	mA
Input Impedance	R_{IN}	At 65Hz	17		60	kΩ
LSB size (assumes full scale input 310mV-pk)		FIR_LEN setting = 11		290		$\frac{nV}{LSB}$
		FIR_LEN setting = 15		122.6		$\frac{nV}{LSB}$
Digital Full Scale		FIR_LEN setting = 11		±1105920		LSB
		FIR_LEN setting = 15		±2621440		LSB
Input Offset	V_{OFF}	V_{IN} = 0V (GNDA)	-14		+14	mV
ADC Gain Error vs %Power Supply Variation $\frac{10^6 \cdot \Delta Nout_{PK} \cdot 357nV/V_{IN}}{100 \cdot \Delta V3P3A/3.3}$	PSRR	Vin=200mV$_{pk}$, 65Hz, V_{3P3A}=3.0V, 3.6V			120	$\frac{ppm}{\%}$
ADC Gain Error over Temperature		40°C to +85°C	-13		+13	$\frac{LSB}{°C}$
Total Harmonic Distortion	THD	V_{in} = 20mVpk		-80		dB
		V_{in} = 250mVpk		-70		dB
ADC Noise		V_{in}=20mVpk, 55Hz, FIR_LEN=11		153		LSB

Parameter	Symbol	Test Conditions [3]	Min	Typ	Max	Unit
ADC Input Equivalent Noise Density		V_{in}=20mVpk, 55Hz, FIR_LEN = 11		200		$\frac{nV}{\sqrt{Hz}}$
Battery Monitor						
BNOM, Nominal Value, T_A = +22°C		V_{3P3A} = V_{3P3SYS} = 3.3V, V_{BAT} = 3.0V, TEMP_PWR=1	121	125	130	LSB
LSB Value (Definition)	BLSB	T_A = +22°C		24		$\frac{mV}{LSB}$
Measurement Equation (Definition)		$VBAT = -0.024 + 0.024 \cdot \text{BSENSE} + 3.953 \cdot 10^{-5} - 5(\text{STEMP} - \text{STEMP22})$				
Measurement Error		V_{BAT}, V_{BAT_RTC} = 2.0V to 3.8V			80	mV
BCURR Load		V_{3P3A} = V_{3P3SYS} = 3.3V	82	100	105	µA
Temperature Monitor						
Nominal Value for T_A = +22°C (the value measured at calibration is stored as STEMP22)	TNOM	V_{3P3A} = V_{3P3SYS} = 3.3V	3600		3900	LSB
LSB Value for Temperature (definition, not measured)	TLSB	V_{3P3A} = V_{3P3SYS} = 3.3V		12.4		$\frac{°C}{LSB}$
Temperature Equation		Based on STEMP22 measured at calibration time	T = 21.40 +(0.0806*(STEMP-STEMP22))+(-1.8184*10^{-6} * (STEMP-STEMP22)^2)			°C
Relative Temperature Error at	TE	T_A=-40°C to +85°C	-2		+2	°C
Measurement Time	t_T	TEMP_PWR=0, SLP mode, TEMP_PER=111, VRTC=3.6V, V3P3D=1.0V		50		ms
LCD System						
V_{LCD} Current	I_{VLCD}	V_{LCD} = 3.3V			4	µA
VLC2 Voltage		Relative to V_{LCD}	-0.1		+0.1	V
VLC1 Voltage, 2/3 bias		relative to 2*VLC2/3	-4.5		+4.2	%VLC2
VLC1 Voltage, 1/2 bias		relative to VLC2/2	-3.8		+4.2	%VLC2
VLC0 Voltage, 1/3 bias		relative to VLC2/3	-2		+2.3	%VLC2
VLC0 Impedance		ΔILOAD=10 µA, -10µA		8	17	kΩ
VLC1 Impedance		ΔILOAD=10 µA, -10µA		8	17	kΩ
VLCD Generator						
LCD DAC Full Scale, MSN Mode (LCD_DAC = 1F, LCD_VMODE = 01)	$VLCD_{FS}$	V_{3P3SYS} = 3.6V	3.5	3.6	3.6	V
		V_{3P3SYS} = 3.0V	2.9	3.0	3.0	V
LCD DAC Full Scale, BRN Mode (LCD_DAC = 1F, LCD_VMODE = 01)	$VLCD_{FS}$	V_{BAT} = 3.8V, V_{3P3SYS} = 0V	3.7	3.8	3.8	V
		V_{BAT} = 2.5V, V_{3P3SYS} = 0V	2.4	2.5	2.5	V
LCD DAC Mid Scale, MSN Mode (LCD_DAC = 0F, LCD_VMODE = 01)	$VLCD_{ZS}$	V_{3P3SYS} = 3.6V	3.5	3.6	3.6	V
LCD DAC Mid Scale, MSN Mode (LCD_DAC = 0F, LCD_VMODE = 01)	$VLCD_{ZS}$	V_{3P3SYS} = 3.6V	2.9	3.0	3.0	V

Parameter	Symbol	Test Conditions [3]	Min	Typ	Max	Unit
LCD DAC Mid Scale, BRN Mode (LCD_DAC = 0F, LCD_VMODE = 01)	$VLCD_{ZS}$	V_{BAT} = 3.8V, V_{3P3SYS} = 0V	3.5	3.73	3.97	V
LCD DAC Mid Scale, BRN Mode (LCD_DAC = 0F, LCD_VMODE = 01)	$VLCD_{ZS}$	V_{BAT} = 2.5V, V_{3P3SYS} = 0V	2.4	2.5	2.5	V
LCD DAC Zero Scale, MSN Mode (LCD_DAC = 00, LCD_VMODE = 01)	$VLCD_{ZS}$	V_{3P3SYS} = 3.6V	2.2	2.6	3.0	V
		V_{3P3SYS} = 3.0V	2.0	2.6	3.2	V
LCD DAC Zero Scale, BRN Mode (LCD_DAC = 00, LCD_VMODE = 01)	$VLCD_{ZS}$	V_{BAT} = 3.8V, V_{3P3SYS} = 0V	2.2	2.6	3.0	V
		V_{BAT} = 2.5V, V_{3P3SYS} = 0V	2.38	2.5	2.52	V
SPI Slave Port						
SPI Setup Time	t_{SU}	SPI DIN to SPI CLK rise	10			ns
SPI Hold Time	t_{HLD}	SPI CLK rise to SPI DIN	10			ns
SPI Output Delay	t_{DEL}	SPI CLK fall to SPI DOUT		20		ns
SPI Recovery Time	t_{REC}	SPI SSB fall to SPI CLK rise	10			ns
SPI Removal Time	t_{REM}	SPI CLK rise to SPI SSB rise	15			ns
SPI Clock High Time	t_H		80			ns
SPI Clock Low Time	t_L		80			ns
SPI Clock Frequency Ratio	Rf_{CLK}	MPU Frequency/SPI Frequency	2			$\frac{MHz}{MHz}$
SPI Transaction Space	t_{TRA}	SPI_SSB rise to SPI_SSB fall	4.5			MPU cycles
I2C, µWire, SPI Master Port						
I^2C Interface SCL Frequency				$\frac{f_{MPU}}{12}$		kHz
3-Wire Interface Frequency				$\frac{f_{MPU}}{10}$		kHz
Flash Memory						
Sector Endurance			20,000			cycles
Data Retention Time		+25°C	100			Years
		+85°C	25			Years
		+125°C	10			Years
Flash Supply Current		Read, 10MHz		1.7	2.1	mA
		Write, 6µs to 7.5µs †			3.5	mA
		Sector erase (4ms to 5ms)			2.0	mA
		Mass erase (20ms to 40ms)			2.0	mA
† Write program time is 6µs to 7.5µs						

Parameter	Symbol	Test Conditions [3]	Min	Typ	Max	Unit
Remote Receiver						
Supply Current	I_{rem}	V_{cm} = 1.8V		700	950	µA
Input Bias Voltage	V_{bias}	V_{cm} = open	1.73	1.84	1.93	V
Differential Input Resistance for Vin = 100mV	R_{in}	*R2K_EN*=1, V_{cm} = 1.8V	3	4.7	6	kΩ
		R2K_EN=0, V_{cm} = 1.8V	100	170	220	kΩ
Input Resistance Mismatch		V_{cm} = 0V, *R2K_EN*=0	-1.2		+1.2	%
		V_{cm} = 3.3V, *R2K_EN*=0	-1.2		+1.2	%
Propagation Delay, RX Rising	T_R	V_{in} = 10mV peak, V_{cm} = 1.8V		23		ns
Input Offset	V_{OFF}	V_{cm} = 0V	-12		+12	mV
		V_{cm} = 1.8V	-12		+12	mV
		V_{cm} = V_{3P3A}	-12		+12	mV

Note 1: Guaranteed by design, not subject to test.

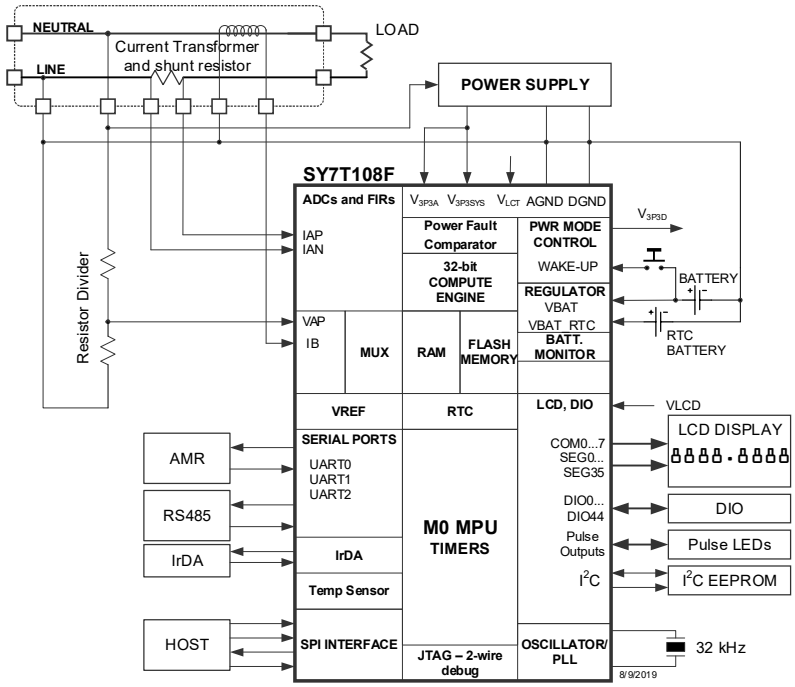
Note 2: Dependent on bus capacitance.

Note 3: Register settings contributing to test conditions are described in the Hardware Reference Manual (HRM)

3 Application Information

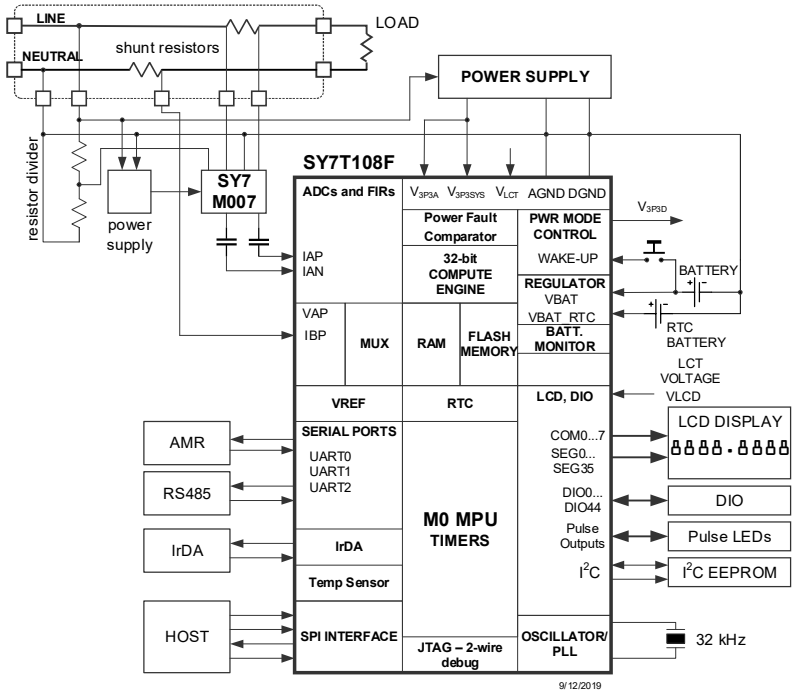
3.1 Typical Application with Shunt and CT Sensors

In a configuration with a local shunt sensor (non-isolated) and a CT for neutral current, the built-in ADCs of the SY7T108F/G are used. Single-ended voltages at IAP and IAN should not exceed 0.5V with respect to GND. Differential voltages should not exceed 3V.



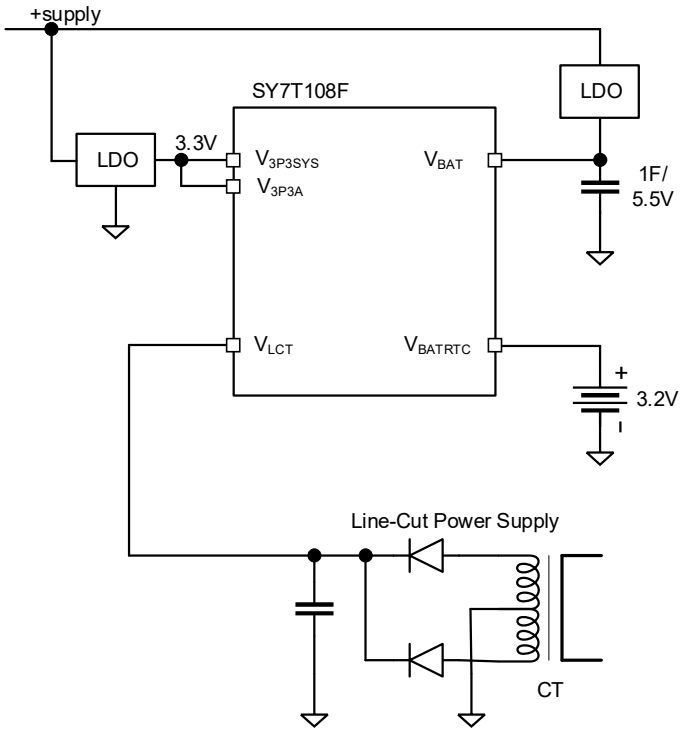
3.2 Typical Application with two Shunts

In this configuration, the two ADCs of the external remote sensor IC (SY7M007) are used. The IB analog input is used for the local shunt.

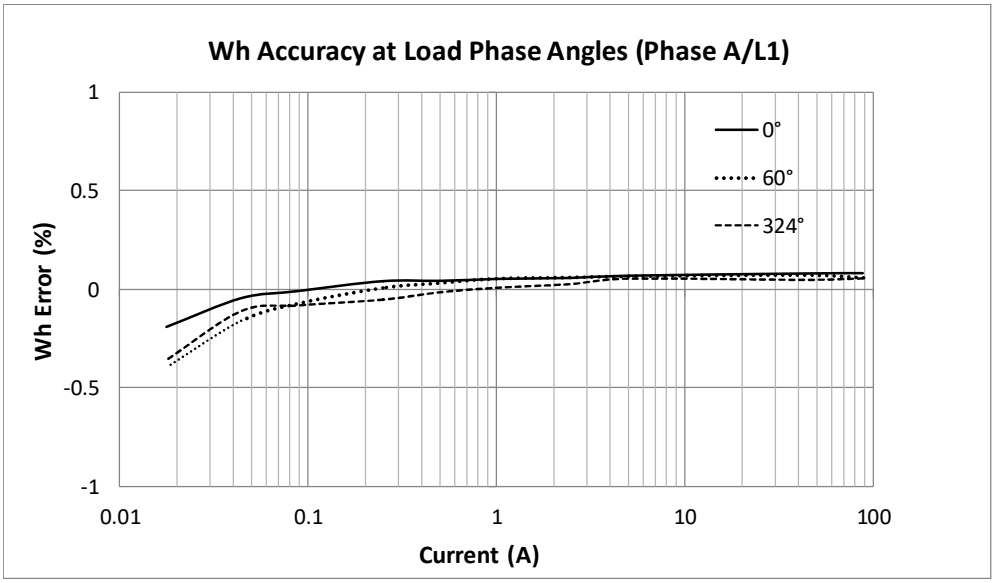


3.3 Line-Cut Operation

In a neutral-cut tampering condition (LCT), the main meter power supply is not active. In this case, the meter can be powered by a secondary CT that is connected to the V_{LCT} pin of the SY7T108F/G via a rectifier. Alternatively, a battery can be used.

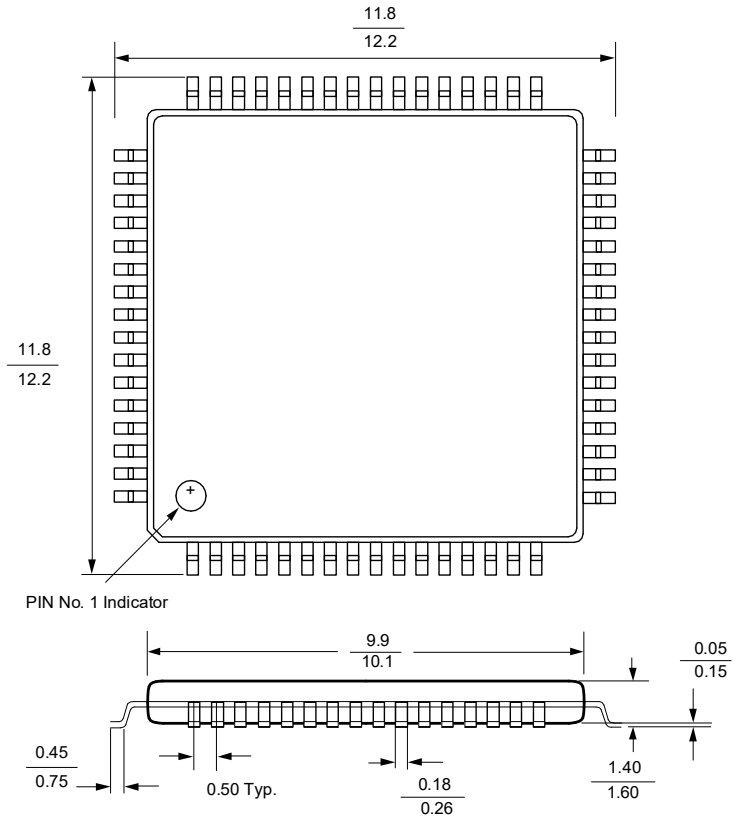


3.4 Typical Performance Characteristics

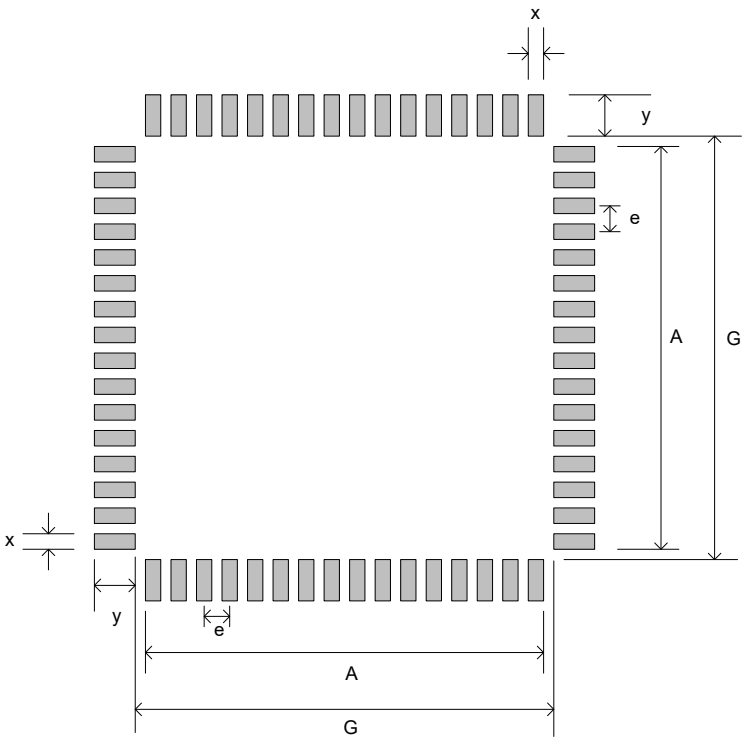


Measured at 240V/50Hz with 250μΩ shunt, ADC gain of 8 selected.

4 Mechanical Drawings



LQFP-64 Package Outline Drawing



PCB Land Pattern

Recommended PCB Land Pattern Dimensions

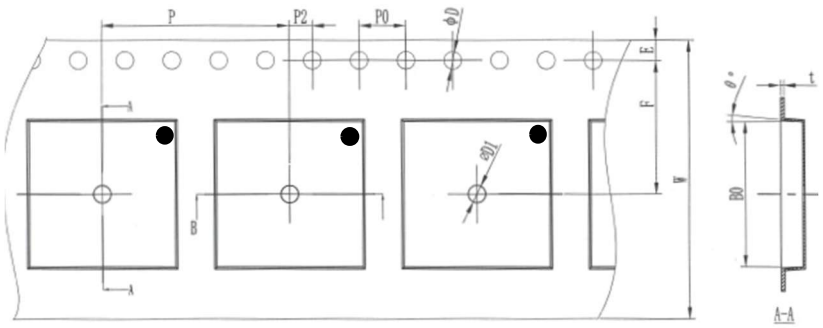
Symbol	Description	Typical Dimension
e	Lead pitch	0.5 mm
x	Pad width	0.25 mm
y	Pad length. See Note.	2.0 mm
A		7.75 mm
G		9.0 mm

Note: The y dimension has been elongated to allow for hand soldering and reworking. Production assembly may allow this dimension to be reduced if the G dimension is maintained.

Taping & Reel Specification

Taping Orientation

LQFP10x10-64

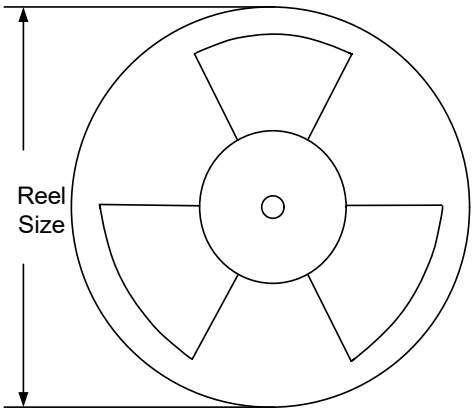


外观	尺寸（mm）
E	1.75±0.10
F	11.50±0.10
P2	2.00±0.10
D	$1.50^{+0.10}_{0}$
D1	1.50MIN
P0	4.00±0.10
10P0	40.00±0.20

外观	尺寸（mm）
W	24.00±0.10
P	16.00±0.10
A0	12.50±0.10
B0	12.50±0.10
K0	2.0±0.10
t	0.30±0.05
θ	5° TYP

Feeding Direction ⟶

Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
LQFP10x10-64	16	16	13"	800	1600	1500

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5 Revision History

Revision Number	Revision Date	Description	Pages changed
0.9	07/23/2020	First release	All
0.9a	07/29/2020	T&R specifications added	24
0.9b	9/24/2021	Added usable input range for ADCS Clarified LTC currents definition Relaxed limits for preamp phase variation over supply Changed VBAT_OK Hysteresis minimum to 20mV	16 15 16 16
1.0	9/25/2021	Official Release	