SQ52104x

Small Size, Low-Power, Unidirectional, Zero-Drift Current-sense Amplifier

General Description

The SQ52104x is a high-side voltage output current-sense amplifier that can sense drops across shunts at common-mode voltages from +1.8V to +5.5V with the fixed gains. The miniature size is paramount for applications in cell phones, mobile accessories, notebooks, portable medical, and all battery-operated portable devices where the precision and space of current sensing are critical.

These device operates from a single +1.8V to +5.5V power supply, drawing 18μA (typical) of supply current. The SQ52104x is specified over the temperature range of －40°C to +125°C. Supply voltage for the device is shared with the IN+ pin to fit the SQ52104x in a 4-bump, ultra-thin CSP package.

Features

- Voltage-output, Current-sense Amplifier
- Common-mode Range: +1.8V to +5.5V
- Fixed Gains:
  - SQ52104: 100V/V
  - SQ52104E: 200V/V
- Low offset Voltage: ±7μV (typical)
- Offset Drift: 0.2 μV/°C (maximum)
- Gain Error: 0.06% (typical)
- Gain Drift: 1 ppm/°C (maximum)
- Quiescent Current: 18μA (typical)
- Buffered Voltage Output: No Additional OP-AMP Needed
- Compact Package: CSP0.76×0.76-4

Applications

- Notebook Computers
- Cell Phones
- Telecom Equipment
- Power Management
- Battery Chargers

Typical Application and Block Diagram

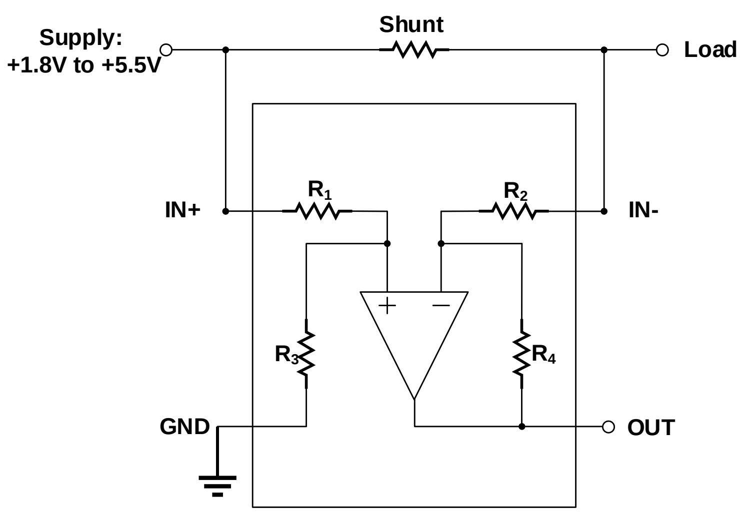


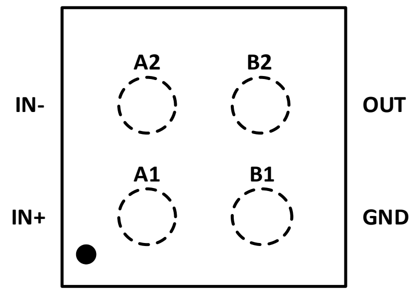
Figure 1. Simplified Application Circuit

Ordering Information

Ordering Part Number	Package Type	Top Mark	Gain
SQ52104WMS	CSP0.76×0.76-4	**GQQ*xyz***	**100V/V**
SQ52104EWMS	CSP0.76×0.76-4	**LHH*xyz***	**200V/V**

x=year code, y=week code, z= lot number code.

Pinout (Top View)



(CSP0.76×0.76-4)

Pin Description

Pin Name	Pin No.	Pin Description
IN+	A1	Supply voltage and positive sense input.
IN-	A2	Negative sense input.
GND	B1	Ground.
OUT	B2	Output Voltage.

Absolute Maximum Ratings

Parameter (Note 1)Note 1)	Min	Max	Unit
Supply Voltage		6	V
Differential V_{IN+} - V_{IN-}	-5.5	5.5	
Common mode, V_{IN+} - V_{IN-}	GND-0.3	5.5	
Output	GND-0.3	V_{IN+}+0.3	
Input Current into Any Pin		5	mA
Operating Temperature	-40	125	°C
Storage Temperature	-65	150	
ESD: HBM (Human Body Model)	± 2500		V
ESD: CDM (Charged Device Model)	± 1000		V

Thermal Information

Parameter (Note 2)	Max	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	315	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	3.5	
ψ_{JT} Junction-to-top characterization parameter	2.5	
θ_{JB} Junction-to-Case Thermal Resistance	70	
P_D Power Dissipation T_A = 25°C	0.32	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Supply Voltage	1.8	5.5	V
Common mode, V_{IN+} - V_{IN-}	1.8	5.5	
Operating Free-Air Temperature	-40	125	°C

Electrical Characteristics

T_A=25℃, V_{CM}= V_{IN+}=4.2V, unless otherwise noted. (Note 4)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input						
Common Mode Input Voltage	V_{CM}	T_A= –40°C to 125°C	1.8		5.5	V
Common-mode Rejection Ratio, RTI (Note 5)	CMRR	V_{IN+}= +1.8V to +5.5V T_A= –40°C to 125°C	100	120		dB
Offset Voltage, RTI(Note 5)	V_{OS}	SQ52104		±7	±45	µV
		SQ52104E		±5	±32	
Offset Voltage Drift	dV_{OS}/dT	SQ52104, T_A= –40°C to 125°C		0.02	0.2	µV/°C
		SQ52104E, TA= –40°C to 125°C		0.01	0.1	
Power-supply Rejection Ratio, RTI (Note 5)	PSRR	T_A= –40°C to 125°C	100	120		dB
Input Bias Current	I_{N-}			3		µA
Output						
Gain	G	SQ52104		100		V/V
		SQ52104E		200		
Gain Error		SQ52104		0.06	±0.18	%
		SQ52104E		0.02	±0.16	
		SQ52104, T_A= –40°C to 125°C		0.23	1	ppm/°C
		SQ52104E, T_A= –40°C to 125°C		1	1.5	
Non-linearity Error(Note 6)		GND + 10mV≤V_{OUT}≤V_S–200mV		±0.01		%
Maximum Capacitive Load (Note 6)		No sustained oscillation		2		nF
Voltage Output						
Swing to V_S Power-supply Rail		R_L=10kΩ to GND, T_A = –40°C to 125°C		(V+)–0.1	(V+)-0.3	V
Swing to GND		R_L=10kΩ to GND, T_A= –40°C to 125°C		(V_{GND})+1	(V_{GND})+2	mV
Frequency Response						
Bandwidth (Note 6)	BW	SQ52104, C_{LOAD}=10pF		5		kHz
		SQ52104E, C_{LOAD}=10pF		2.5		
Slew Rate (Note 6)	SR			0.03		V/µs
Noise (Input Referred)						
Voltage Noise Density (Note 6)				70		nV/√Hz
Power Supply						
Supply Voltage	V_{IN+}	T_A= –40°C to 125°C	1.8		5.5	V
Quiescent Current	I_Q			18	22	µA
		I_Q vs temperature, T_A= –40°C to 125°C			30	
Turn-on Time (Note 6)		V_{IN+} = 0 to +2.5V; V_{SENSE} = 10mV; V_{OUT} ±0.5%		200		µs
Specified Temperature Range			-40		125	°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25˚C on a low effective single-layer test board per JESD51-3. $\theta_{JC(top)}$ is measured in accordance with JESD51-14.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested at $T_A \approx T_J$ = 25°C. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

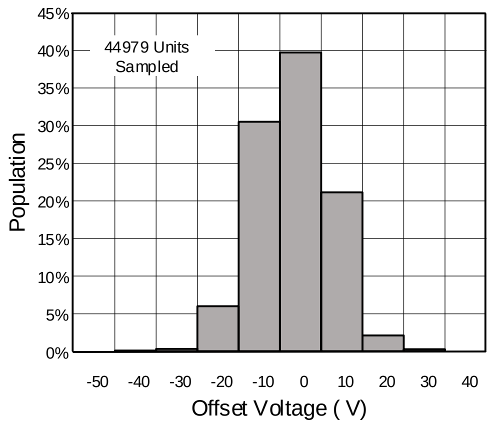
Note 5: Referred to Input.

Note 6: Guaranteed by design or statistical correlation and not production tested.

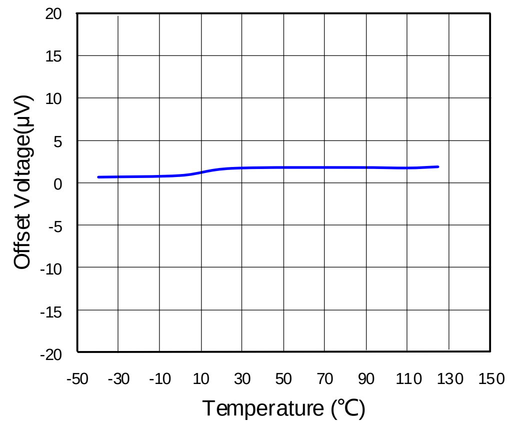
Typical Performance Characteristics

(The SQ52104WMS is used for typical characteristic measurements at T_A=25℃, V_{CM}= V_{IN+}=4.2V, unless otherwise noted.)

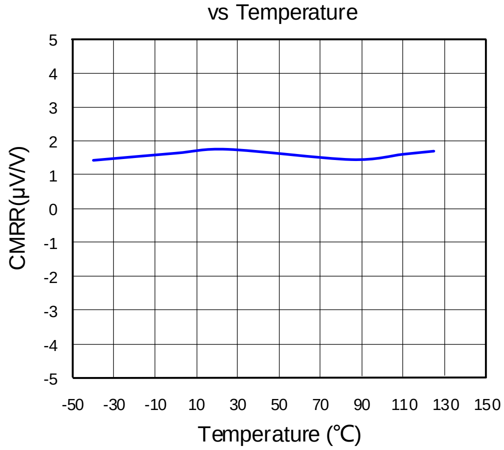
Input Offset Voltage Production Distribution



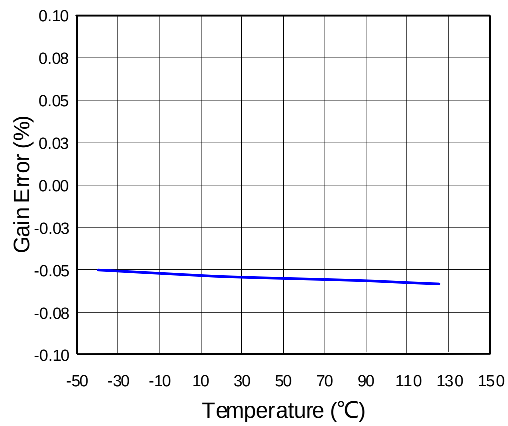
Offset Voltage vs Temperature



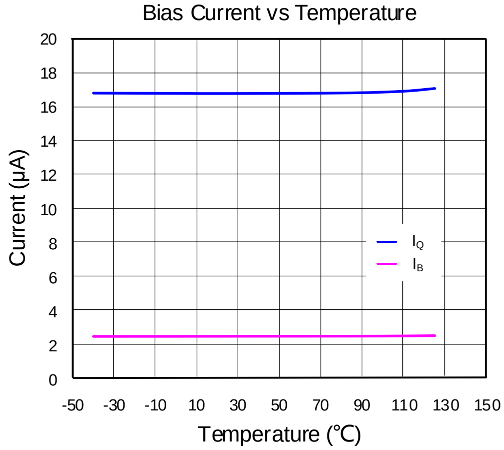
Common-mode Rejection Ratio vs Temperature



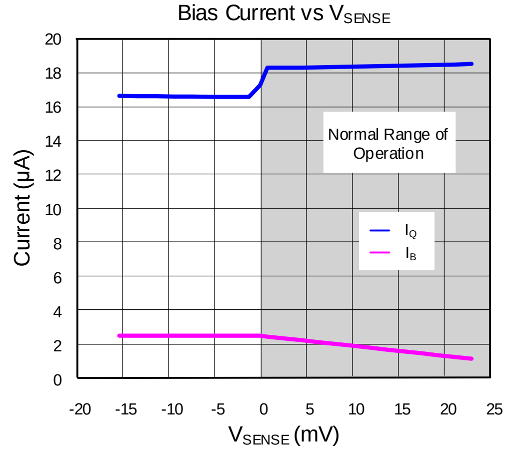
Gain Error vs Temperature

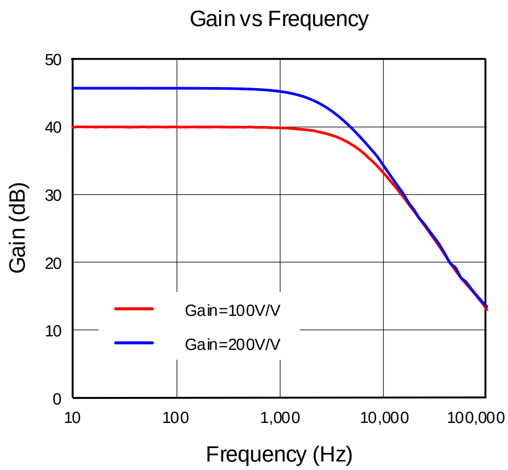


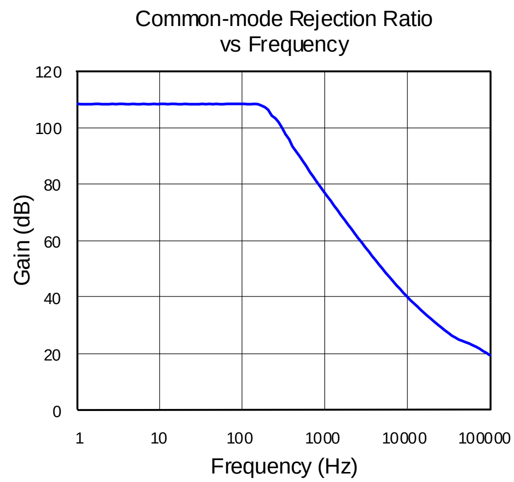
Quiescent Current and Negative Input Bias Current vs Temperature

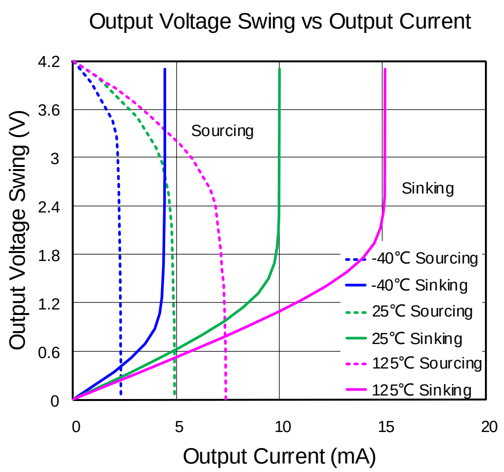


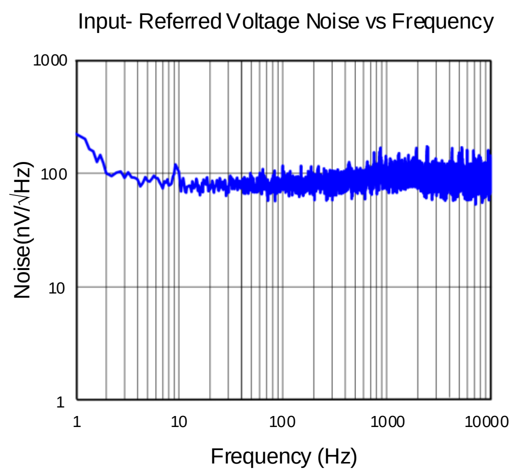
Quiescent Current and Negative Input Bias Current vs V_{SENSE}



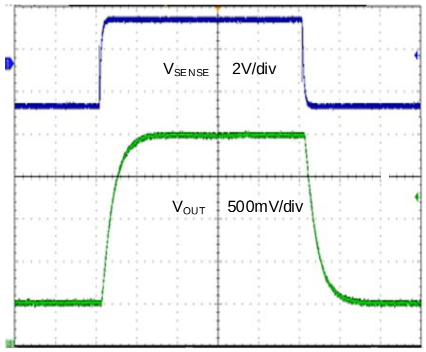

Gain vs Frequency
Gain (dB)
Frequency (Hz)
Gain=100V/V
Gain=200V/V


Common-mode Rejection Ratio vs Frequency
Gain (dB)
Frequency (Hz)


Output Voltage Swing vs Output Current
Output Voltage Swing (V)
Output Current (mA)
Sourcing
Sinking
-40℃ Sourcing
-40℃ Sinking
25℃ Sourcing
25℃ Sinking
125℃ Sourcing
125℃ Sinking

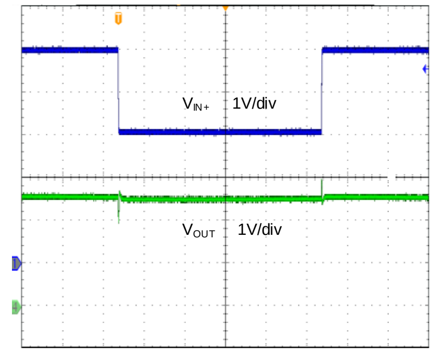

Input- Referred Voltage Noise vs Frequency
Noise(nV/√Hz)
Frequency (Hz)

Step Response



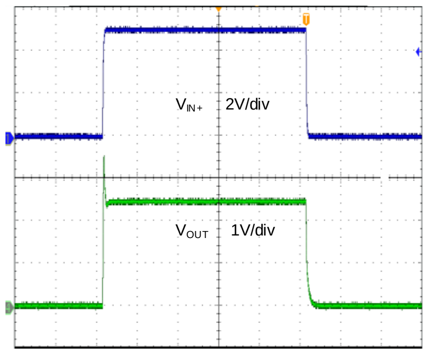
Time (100μs/div)

Common-Mode Voltage Transient



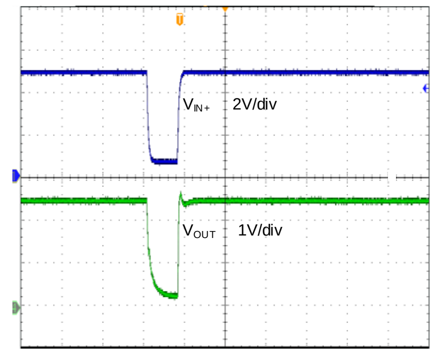
Time (1ms/div)

Startup Response



Time (1ms/div)

Brownout Recovery



Time (400μs/div)

Application Information

The SQ52104x is a high-side voltage output current-sense amplifier that offers chip-scale package, low-power, unidirectional, zero-drift and can sense drops across shunts at common-mode voltages from +1.8V to +5.5V without the need for an extra supply voltage terminal.

Basic Connections

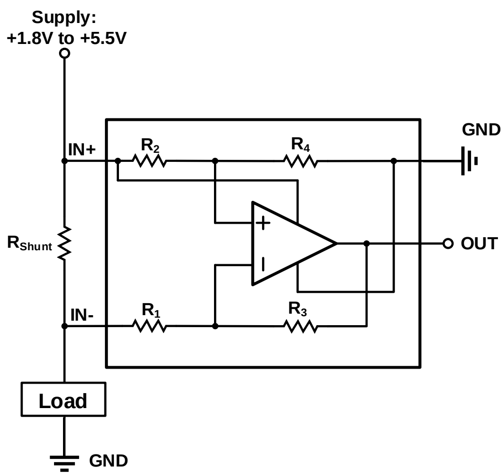


Figure 2. Typical Application

The Figure 2 shows the basic connections of the SQ52104x. The input pins, IN+ and IN–, should be connected as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistance.

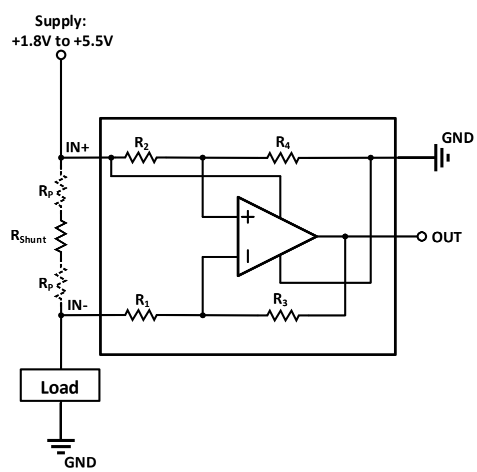


Figure 3. Shunt Resistance Measurement Including Trace Resistance

Figure3 illustrates the SQ52104x connected to a shunt resistor with additional trace resistance in series with the shunt placed between the positions of the current shunt monitor input pins. Since the typically low shunt resistor values are commonly used in these applications, even small amounts of additional impedance in series with the shunt resistor can significantly affect the differential voltage at the SQ52104x input pins.

Kelvin Connections

In order to eliminate the effect of voltage drop on the lead wire in the circuit, a four-terminal current detection resistor or Kelvin is usually used, shown as Figure 4. This connection helps ensure that the only impedance between the current monitor input pins is the shunt resistor.

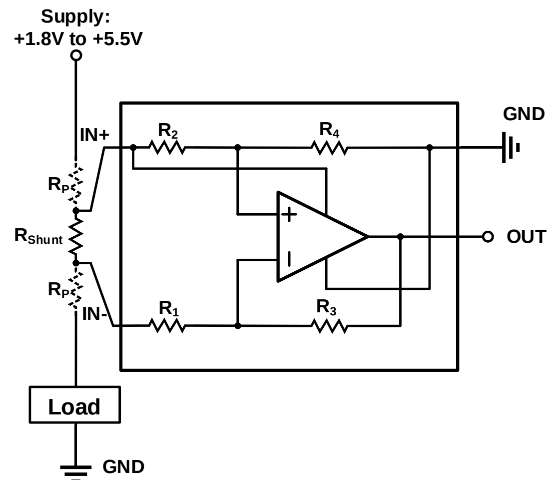


Figure 4. Kelvin Connection

Power Supply

The SQ52104x does not have a dedicated power-supply pin. Instead, the IN+ pin with an internal connection serves as the power supply for this device. Because the SQ52104x is powered from the IN+ pin, the common-mode input range is limited on the low end to 1.8V. Therefore, the SQ52104x cannot be used as a low-side current shunt monitor.

Selecting Shunt Resistor

The selection of the value of the shunt resistor used in the SQ52104x is based on the specific operating conditions and requirements of the application. The starting point for selecting the resistor is to firstly determine the desired full-scale output from the SQ52104x. The SQ52104x provides 100V/V and 200V/V gains and maintains high-performance levels with very low offset, allowing the use of lower shunt resistor values to achieve lower power dissipation and meet high system performance specifications. Most applications have an allowable maximum drop to ensure that the load can receive the required voltage to operate. Assuming that there are now multiple shunt voltages that are acceptable, the choice of what value shunt resistor to use can be made based on accuracy.

Two important factors need to be considered when finalizing the current-sensing resistor value: the required current measurement accuracy and the maximum power dissipation across the resistor. A high shunt resistor value allows lower currents to be measured more accurately because offsets are less significant. When the sense voltage is larger, for extremely low input offset voltage and gain error that this part offers, this output voltage error will be insignificant. At high current levels, the losses in resistor can be significant, this need to be considered when choosing the resistor value and its power dissipation rating. Furthermore, the shunt resistor value might drift if it is allowed to heat up excessively. Due to the precise offset voltage of the SQ52104x, the device is allowed to sense very low current using small sense resistors, which reduces power dissipation and hot spots. Dynamic range of the current that can be sensed will rise with low V_{OS} and low sense resistors

Input Filtering

An ideal location to implement filtering is at the inputs of a device. Placing an input filter in front of the SQ52104x, though, is not recommended, but it can be implemented if necessary. This location is not recommended for filtering because adding input filters induces an additional gain error to the device, which can easily exceed the device maximum gain error specification of 0.18%. In the SQ52104x, the nominal current into the IN+ pin will be in the range of 18μA when the bias current into the IN– pin is in the range of approximately 3μA. The current flowing into the IN+ pin includes both the input bias current and the quiescent current. The issue of input filtering begins to become a bigger problem because the quiescent current of the SQ52104x flows through the IN+ pin, and when the output starts driving the current, this additional current also flows through the IN+ pin, creating a greater error.

A typical common-mode filter of 10Ω is placed in series with each input and a 0.1μF capacitor across the input pins, as shown in Figure 5, which introduces an additional gain error into the system. If an application uses the SQ52104x with a full-scale output of 4V, the device will not drive any output current. To create the 4V output with a gain of 100, the shunt voltage needs to be 40mV. With 10Ω filter resistors on each input, there is a generated differential voltage that subtracts from the 40mV full-scale differential current.

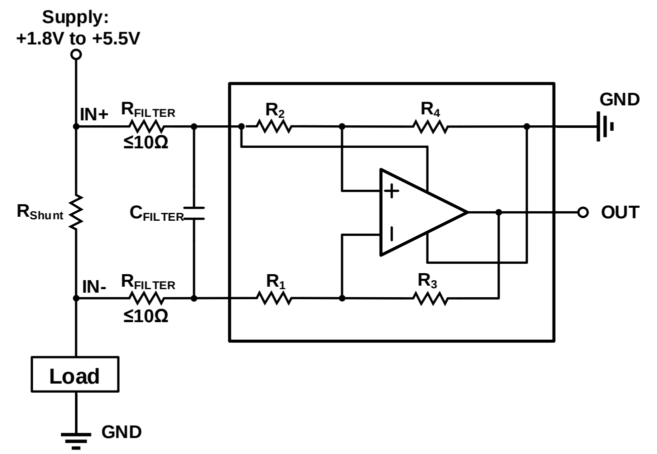
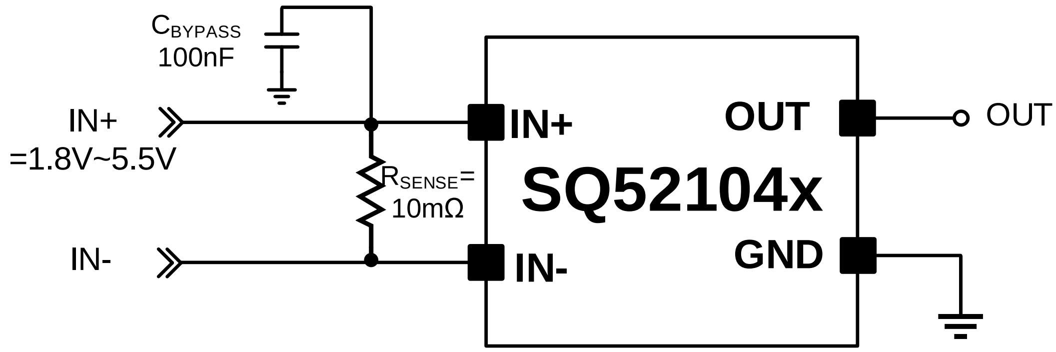


Figure 5. Input Filtering

If filtering is required for the application and the gain error introduced by the input filter resistors exceeds the available error budget for this circuit, a filter can be implemented following the SQ52104x. Placing a filter at the output of the current shunt monitor is not typically the ideal location because the benefit of the low impedance output of the amplifier is lost. Applications that require the low impedance output require an additional buffer amplifier that follows the post current shunt monitor filter.

Application Schematic



BOM List

Designator	Description	Part Number	MFR
C_{BYPASS}	100nF/50V/X7R, 0603	GCJ188R71H104KA12D	muRata
R_{SENSE}	10mΩ/1W, 2512, 1%	RL2512FK-070R01L	YAGEO

Layout Guidelines

For optimal performance, follow these PCB layout considerations:

- Use a Kelvin connection to connect the input pins to the current-sense resistor (R_{SENSE}). Due to the low resistance values of R_{SENSE}, poor PCB routing often leads to additional parasitic resistance between input pins, resulting in significant measurement errors. The Kelvin connection ensures that only R_{SENSE} impedance is detected between the input pins.
- Minimize the loop formed by these connections.
- Place the bypass capacitor (0.1μF MLCC is recommended) as close as possible to the IN+ and GND pins.

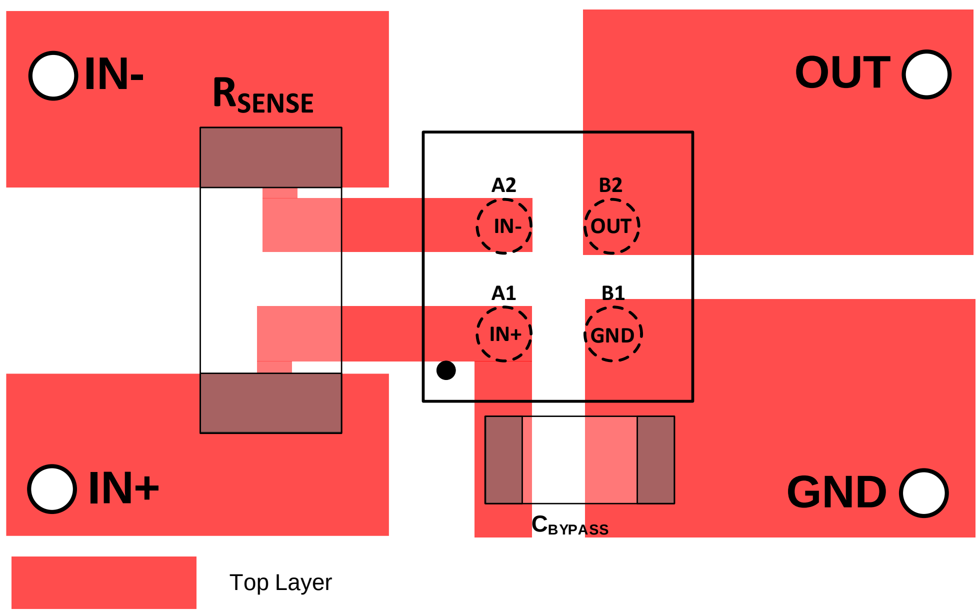
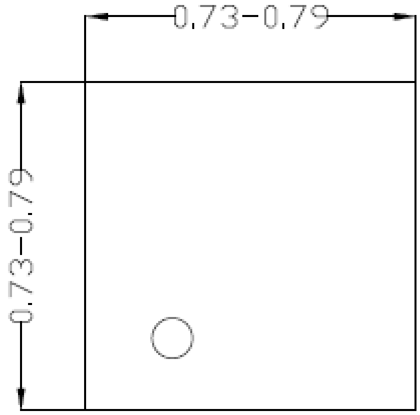
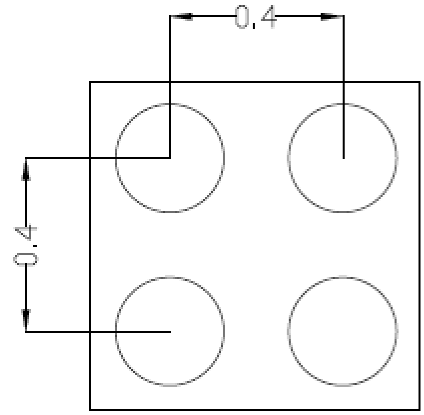


Figure 8. Recommended Layout

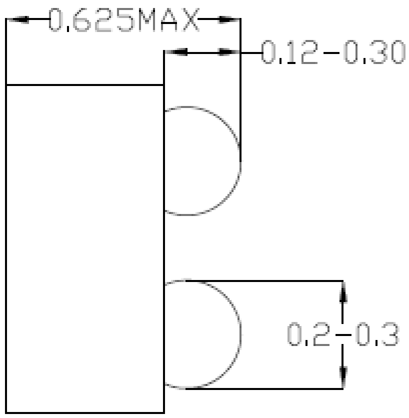
CSP0.76×0.76-4 Package Outline Drawing



Top View



Side View

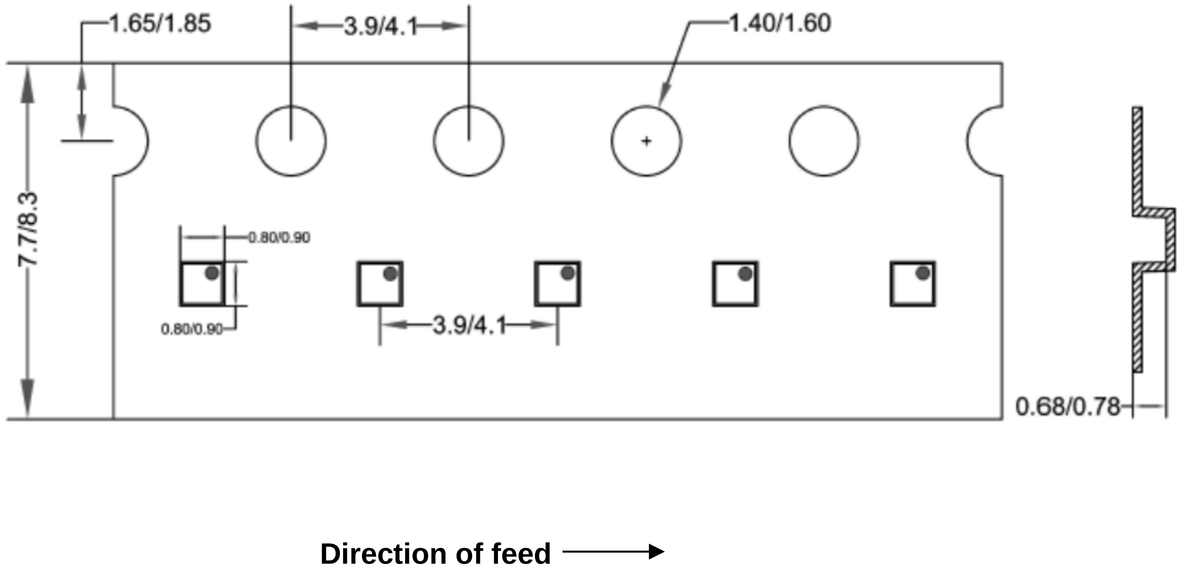


Front View

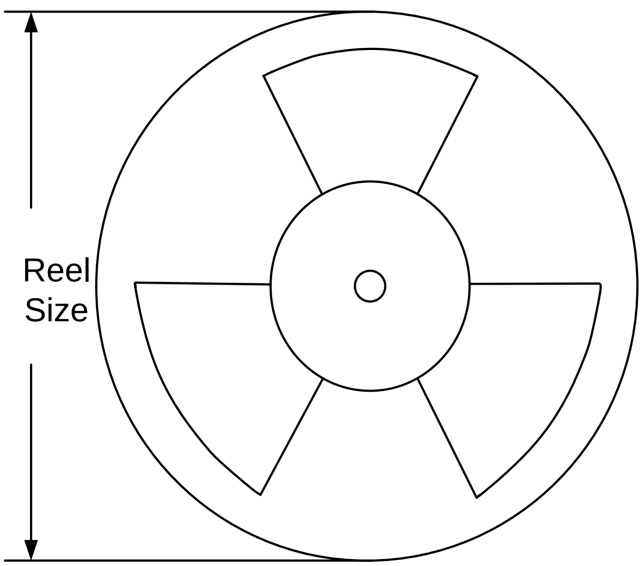
Note: All dimensions are in millimeters and exclude mold flash and metal burr.

Tape and Reel Information

1. CSP0.76x0.76-4 Tape Dimensions and Pin 1 Orientation



2. Reel Dimensions



Package types	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Trailer length (mm)	Leader length (mm)	Qty per reel (pcs)
CSP0.76x0.76-4	8	4	7"	400	160	3000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Aug. 31, 2023	Revision 0.9	Initial Release
Aug. 31, 2024	Revision 1.0	Production Release
Jan. 15, 2026	Revision 1.0A	Add SQ52104EWMS information

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