SY5055E

PFC+LLC Controller

General Description

The SY5055E PFC+LLC controller integrates a boost PFC controller and a resonant half-bridge controller.

The boost converter operates in critical conduction mode (CrM) or discontinuous conduction mode (DCM) to minimize switching losses and improve EMI performance. It uses a proprietary control method to achieve unity power factor (PF) and minimal total harmonic distortion (THD). The burst function enhances efficiency at low load conditions. The SY5055E ensures safe boost converter operation with reliable protection against output overvoltage (OVP), undervoltage (UVP), and overcurrent (OCP), as well as input brown-out (BO).

The LLC converter with proprietary control achieves a fast dynamic response and simplifies the design of loop compensation parameters. The number of external components is significantly reduced, resulting in lower BOM costs. The SY5055E ensures safe LLC converter operation with reliable protection against output overvoltage (OVP), overtemperature (OTP), and overload (OLP).

Features

- PF > 0.95, THD < 5%
- Support DC/AC input
- Boost Quasi-Resonant (QR) Operation
- Boost Burst Operation at Light Load
- LLC Fast Dynamic Response
- LLC Integrated Half-Bridge Driver
- Input Brown-In (BI) and Brown-Out (BO) Protection
- Boost FBB, LLC Output Overvoltage Protection (OVP)
- Cycle-by-Cycle Peak Current Protection
- Overtemperature Protection
- LLC Capacitive Mode Protection
- MSL3
- SOP14 package

Applications

- LCD TVs
- Chargers
- Printers

Typical Application

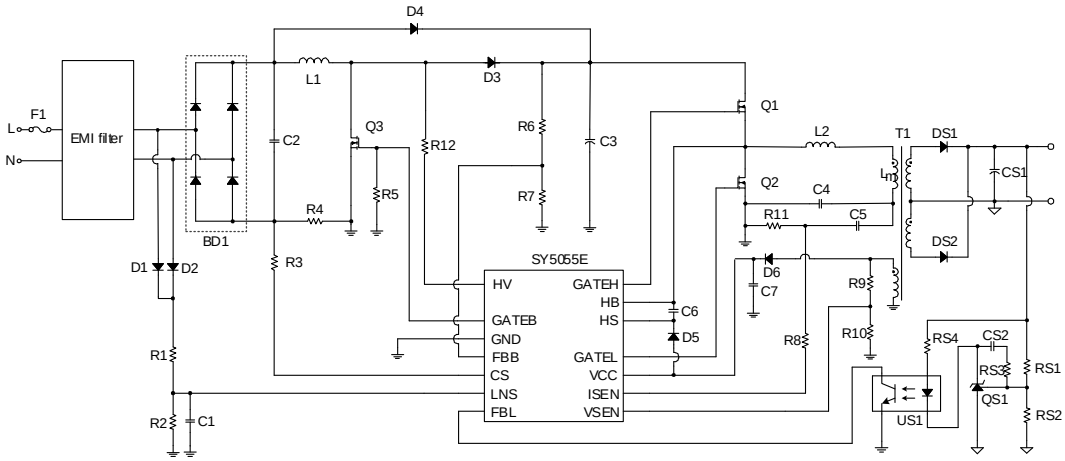


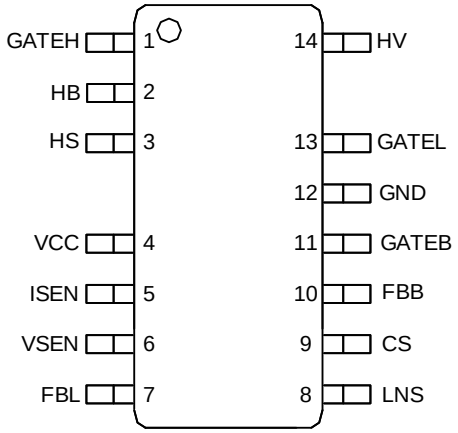
Figure 1. Typical Application Circuit

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY5055EHXP	SOP14	**AAGExyz**

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	GATEH	Half-bridge controller high side drive pin. Connect to high-side MOSFET gate.
2	HB	Half-bridge controller high side return path. Connect to the high-side MOSFET source.
3	HS	Half-bridge controller high side bias supply pin. Connect to a bootstrap capacitor.
4	VCC	Bias supply pin.
5	ISEN	Half-bridge controller resonant current sense pin.
6	VSEN	Half-bridge controller output voltage sense pin.
7	FBL	Half-bridge controller control input pin.
8	LNS	PFC controller input voltage sense pin.
9	CS	PFC controller input current sense pin.
10	FBB	PFC controller output feedback pin. Connect to external resistor divider to set the LLC voltage.
11	GATEB	PFC controller gate drive pin. Connect to the LLC external MOSFET gate.
12	GND	Ground pin.
13	GATEL	Half-bridge controller low side drive pin. Connect to the low-side MOSFET gate.
14	HV	HV startup pin.

Block Diagram

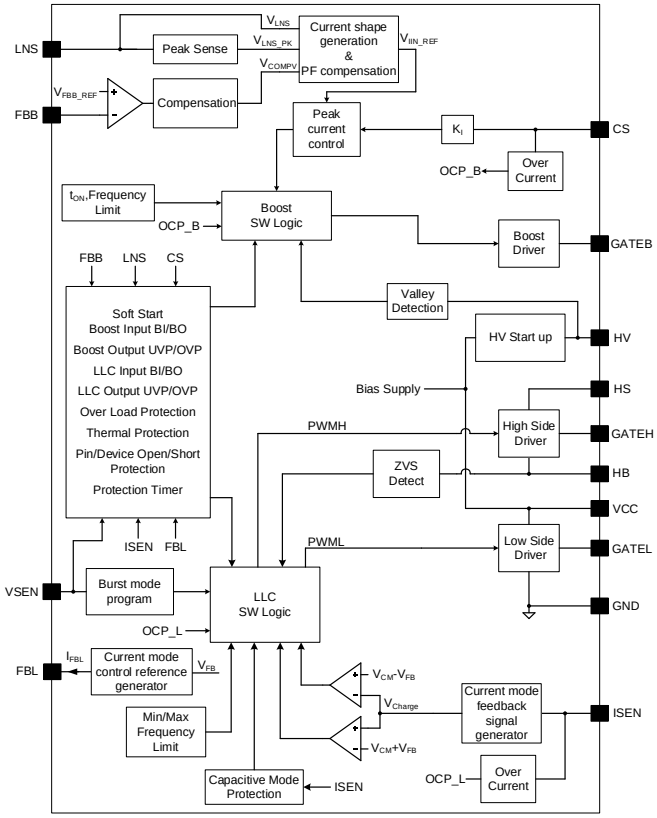


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
HV	-0.3	650	V
HB	-3	650	
HS	HB - 0.3	HB + 30	
GATEH	HB - 0.3	HB + 15	
VCC	-0.3	30	
I_{CS} (Note 6)	-20	20	mA
I_{VSEN} (Note 6)	-10		
I_{ISEN} (Note 6)	-20	20	
CS/ISEN (Note 6)	-1.1	1.1	V
FBB/LNS/FBL/VSEN	-0.3	3.6	V
GATEB/GATEL	-0.3	15	V
Junction Temperature, Operating	-45	150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Max	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	122	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	11.5	
PD Power Dissipation T_A = 25°C	1.02	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VCC	10	24	V
HS-HB	9	24	V

Electrical Characteristics

(V_{VCC} = 15V, T_J = 25°C unless otherwise specified (Note 4))

Parameter (Note 7)		Symbol	Test Conditions	Min	Typ	Max	Unit
VCC	VCC Turn-On Threshold	V_{VCC_ON}	Voltage rising	23	24	25	V
	VCC Turn-Off Threshold	V_{VCC_OFF}	Voltage falling	8.5	9	9.5	V
	VCC Low for HV Start Threshold	V_{VCC_LO}		8.9	9.5	10	V
	VCC Short-Circuit Protection	V_{VCC_SCP}		0.6	0.8	1	V
	VCC Shunt Voltage Protection	V_{VCC_SHUNT}		25.4	26.4	27.4	V
	VCC OVP Threshold	V_{VCC_OVP}		V_{VCC_SHUNT} + 0.4	V_{VCC_SHUNT} + 0.75	V_{VCC_SHUNT} + 1.1	V
	VCC OVP Trigger Number of Switching Cycles	N_{VCC_OVP}			4		
	Quiescent Current	I_Q		1.5	1.85	2.15	mA
	Standby Current	I_{SDY}		370	430	490	μA
	Enable-Off Current	I_{ENOFF}		100	170	250	μA
	VCC Maximum Shunt Current (Note 5)	I_{SHUNT}	VCC > 26V	8	11	14.5	mA
	VCC Fault Restart Timer	$t_{VCC\_TIMEOUT}$		0.84	1.12	1.46	s
HV	HV Startup Current at VCC SCP	I_{ST_L}	VCC < 0.7V	0.4	0.5	0.6	mA
	HV Startup Current at Normal State	I_{ST_N}		4.2	5.6	7	mA
	Maximum Charge Time	t_{VCC_CHARGE}		45	67	90	ms
	Boost Second OVP Threshold	V_{HV_OVPTH}		480	505	530	V
	HV OVP Number of Consecutive Off-Times for Trigger	n_{HV_OVP}			4		
	QR dV/dt Sense Threshold (Note 5)	V_{HV_TH}			40		V/μs
	QR Timeout Time	t_{ZCS}		2.2	3.3	4.4	μs

FBB	Boost Output Regulation Reference	V_{FBB_REF}		1.18	1.2	1.22	V
	Boost Output UVP Threshold	V_{FBB_UVP}	16.7% of boost V_{OUT}	170	200	230	mV
	Boost Output OVP Threshold	V_{FBB_OVP}	107.5% of boost V_{OUT}	1.245	1.29	1.335	V
	Boost and LLC Disable Threshold	V_{FBB_ENB}		2.2	2.4	2.6	V
	LLC Input BO Threshold	V_{FBB_BO}		690	740	800	mV
	LLC Input BI Threshold	V_{FBB_BI}		990	1050	1110	mV
	Pin Open Detection Source Current	I_{FBB_OPEN}	For open pin	50	100	200	nA
CS	Boost Peak Current Limit	V_{CS_LIMIT}		-740	-700	-660	mV
	Inductor Saturation or Short-Circuit Protection Limit	V_{LS_LIMIT}		-900	-850	-800	mV
	Inductor Saturation or Short-Circuit Protection Trigger Number	n_{LS_TIMER}			4		
	Boost Current Sense Resistor Short-Circuit Protection Threshold	V_{CS_RSCP}		-65	-50	-35	mV
	Boost Current Sense Resistor Short-Circuit Protection Timer (Note 5)	t_{CS_RSCP}			4		µs
	Voltage Threshold at Boost Overpower Protection (Note 5)	V_{COMPV_OPP}			1.33		V
	Calculated Coefficient of Boost Overpower Protection (Note 5)	k_{PFCOPP}			0.073		
	Boost Overpower Protection Timer	t_{COMPV_OPP}		220	300	380	ms
LNS	X-Cap Maximum Discharge Time	t_{X_MAX}		54	72	100	ms
	X-Cap Discharge Debounce Time	t_{XDIS_DBT}		54	72	100	ms
	Boost Input Brown-Out Timer	$t_{PROT\_LNS\_BO}$		70	90	115	ms
	Boost Input Brown-Out Threshold	V_{LNS_BO}		374	395	425	mV
	Boost Input Brown-In Threshold	V_{LNS_BI}		450	475	500	mV
	Pin Open Detection Source Current	I_{LNS_OPEN}		50	100	200	nA
GATEB	Drive Limit Voltage	V_{GATEB_DRV}		10.1	10.9	11.6	V
	Drive Voltage within $t_{ON\_MIN\_B}$	V_{GATEB_TH}			8.5		V
	Source Current	I_{SOURCE_GATEB}	V_{GATEB} = 8.5V	400	600	800	mA
	Sink Current (Note 5)	I_{SINK_GATEB}	V_{GATEB} = 2V	0.3			A
			V_{GATEB} = 11V	1	1.4	1.8	A
	Boost Minimum On-Time	t_{ON,MIN_B}		200	300	400	ns
	Boost Maximum On-Time	t_{ON,MAX_B}		20	33	45	µs
	Boost Minimum Off-Time	t_{OFF,MIN_B}		0.7	1	1.5	µs

	Boost Maximum Off-Time	t_{OFF,MAX_B}		20	30	40	μs
	t_{OFF_MAX} if CS ≤ 850mV, within $t_{LLC,DELAY}$	$t_{OFF,MAX}$		75	110	145	μs
	Boost Minimum Switching Period(Note 5)	t_{SW,MIN_B}			8.33		μs
FBL	Open Loop Protection Threshold Current	$I_{FBL\_250\%}$		16	22	28	μA
	Open Loop Protection Trigger Time	t_{OLP}		110	150	200	ms
	Overpower Protection Trigger Time	t_{OPP}		220	300	380	ms
	Regulated Burst Frequency for Burst Mode(Note 5)	f_{BURST}		0.33	0.45	0.6	kHz
ISEN	Resonant Current Sample Resistor Calculation Coefficient (Note 5)	k			1.23×10^{-6}		
	LLC Current Sense Resistor Short-Circuit Protection Threshold	V_{ISEN_RSCP}		30	45	60	mV
	LLC Current Sense Resistor Short-Circuit Protection Timer (Note 5)	t_{ISEN_RSCP}			4		μs
	ISEN Max Current Limit	V_{ISEN_L}		±700	±750	±800	mV
	ISEN Max Current Limit Protection Timer	$t_{IL\_PROTECT}$		27	35	47	ms
VSEN	LLC Output OVP Counter	N_{OVP_COUNT}			4		
	LLC Output OVP Reference	V_{VSEN_OVP}		1.42	1.47	1.54	V
	LLC Disable Threshold	V_{VSEN_ENB}		1.9	2.2	2.5	V
	LLC Output UVP Reference	V_{VSEN_UVP}		370	390	425	mV
	LLC Output UVP Timer	t_{VSEN_UVP}		27	35	47	ms
	Pin Open Detection Source Current	I_{VSEN_OPEN}		50	100	200	nA
GATEL	Drive Limit Voltage	V_{GATEL_DRV}		10.5	11.5	12.5	V
	Source Current	I_{SOURCE_GATEL}	V_{GATEL} = 4V	200	350	500	mA
	Sink Current	I_{SINK_GATEL}	V_{GATEL} = 2V	0.3			A
			V_{GATEL} = 11V	1	1.4	1.8	A
	LLC Minimum On-Time	$t_{ON\_MIN\_L}$		250	400	550	ns
	LLC Maximum On-Time	$t_{ON\_MAX\_L}$		12	20	28	μs
	Bootstrap Charge Time	t_{BST}		3	5	7	μs
HB	dV/dt Threshold for HB ZVS (Note 5)	dV/dt_{ZVS}		52	80	108	V/μs
	Minimum Dead Time for ZVS	t_{D_MIN}		120	185	250	ns
	Maximum Dead Time for ZVS	t_{D_MAX}		0.7	1	1.3	μs
HS	HS Turn-On Threshold	V_{HS_ON}		6.2	7	7.8	V
	HS Turn-Off Threshold	V_{HS_OFF}		5.8	6.4	7.1	V
	HS Quiescent Current	I_{Q_HS}		9	16	28	μA
GATEH	Drive Limit Voltage	V_{GATEH_DRV}		10.5	11.5	12.6	V

	Source Current	I_{SOURCE_GATEH}	V_{GATEH} - V_{HB} = 4V	200	350	500	mA
	Sink Current	I_{SINK_GATEH}	V_{GATEH} - V_{HB} = 2V	0.3			A
			V_{GATEH} - V_{HB} = 11V	1	1.4	1.8	A
OTP	Thermal Shutdown Temperature (Note 5)	T_{SD}			150		°C
	Thermal Shutdown Temperature Hysteresis (Note 5)	T_{SD_HSY}			20		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a four-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test , or statistical correlation.

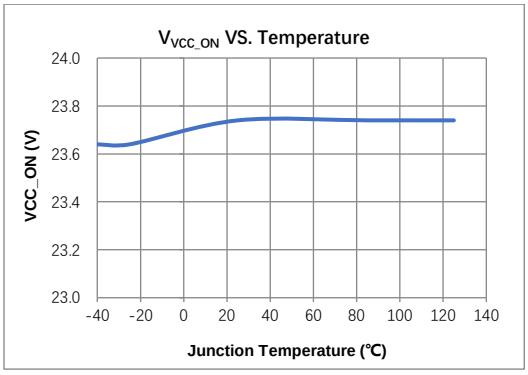
Note 5: Guaranteed by design or statistical correlation and not production tested.

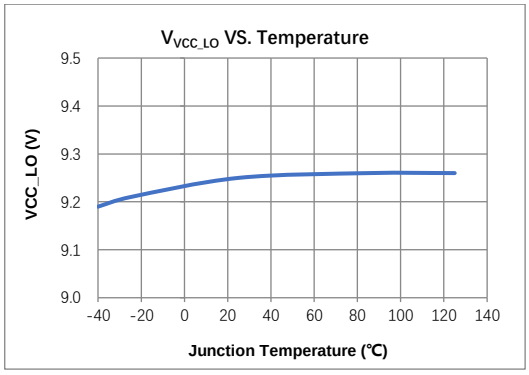
Note 6: The IC internal diode clamps the CS pin voltage. During normal operation, I_{CS} should not exceed ±20mA if V_{CS} reaches ±1.1V. The internal diode clamps the ISEN pin voltage. During normal operation, I_{ISEN} should not exceed ±20mA if V_{ISEN} reaches ±1.1V. The internal diode clamps the negative voltage at the VSEN pin. During normal operation, I_{VSEN} should not exceed -10mA if V_{VSEN} reaches -0.3V.

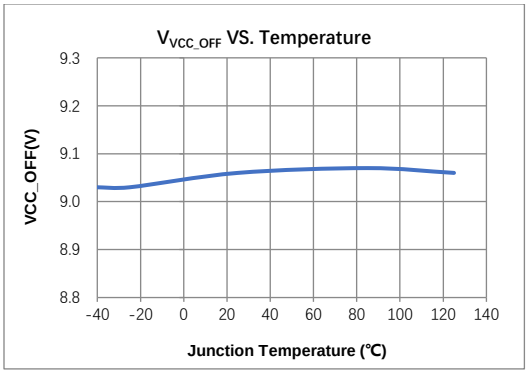
Note 7: Increase VCC pin voltage gradually to a level higher than V_{VCC_ON} threshold, then turn down to 15V.

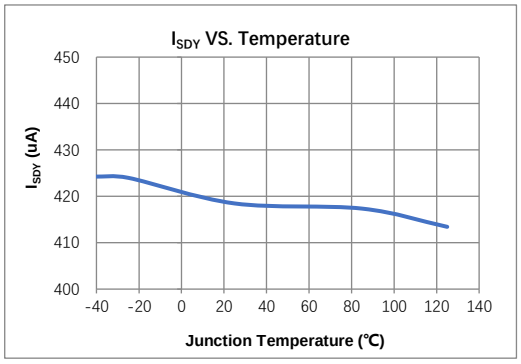
Typical Performance Characteristics

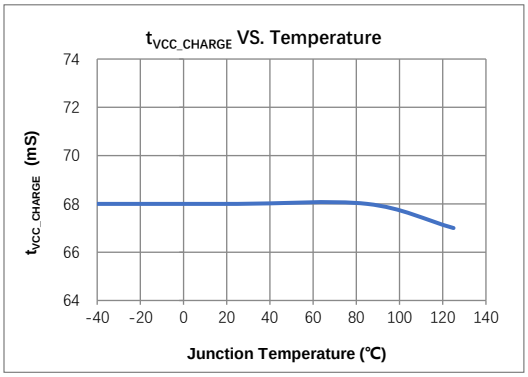
V_{IN} = 90V_{AC}–264V_{AC}, V_{OUT} = 24V, I_{OUT} = 10A,T_A = 25°C

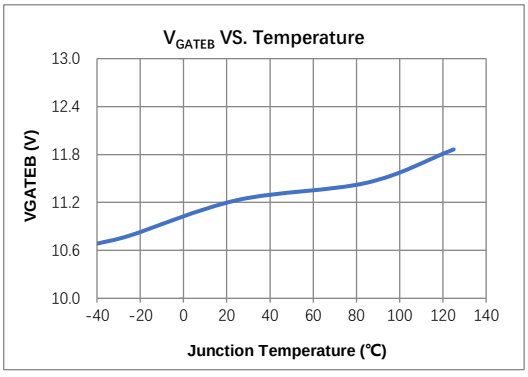


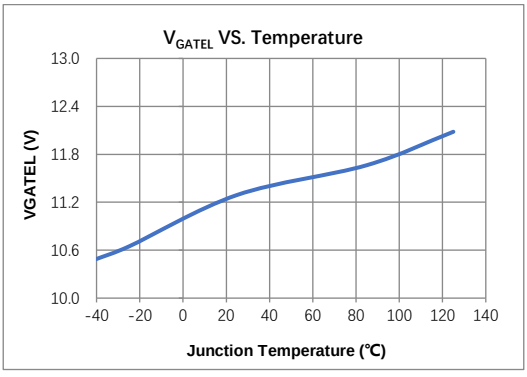


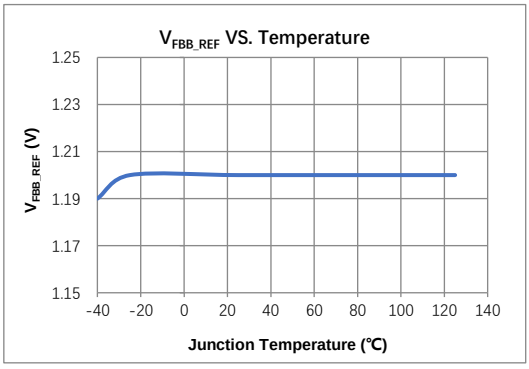


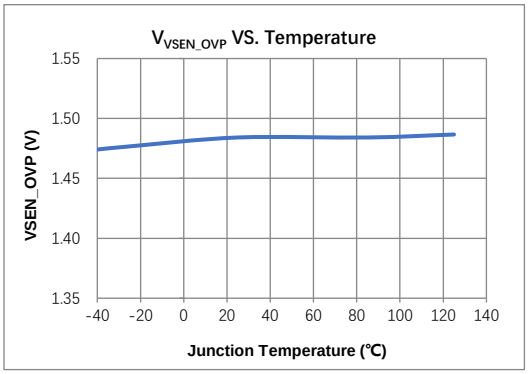


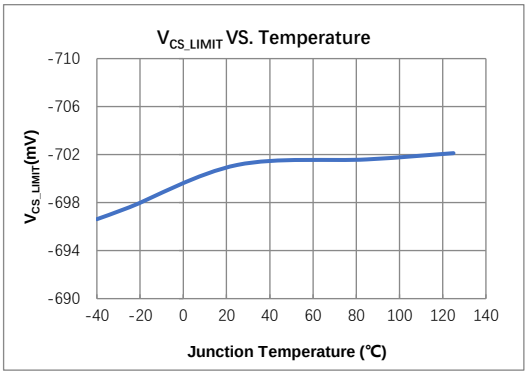


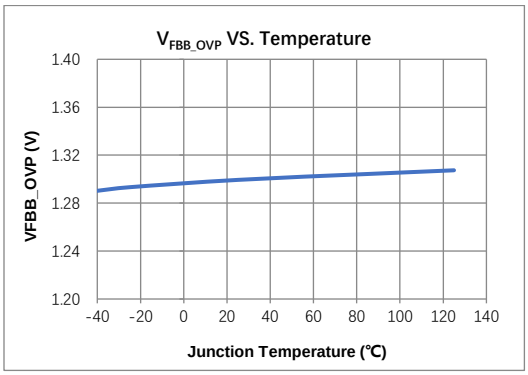


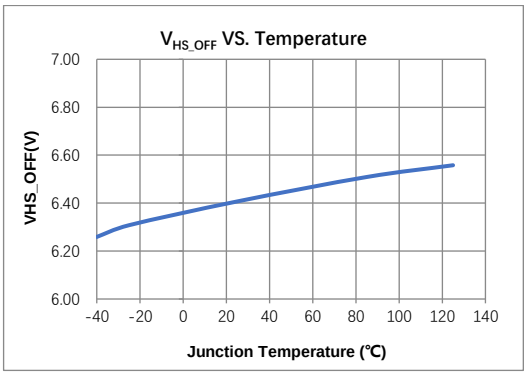


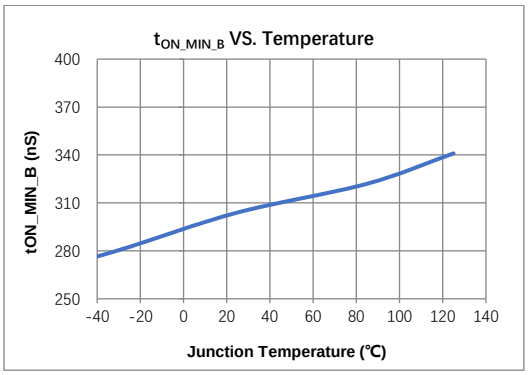


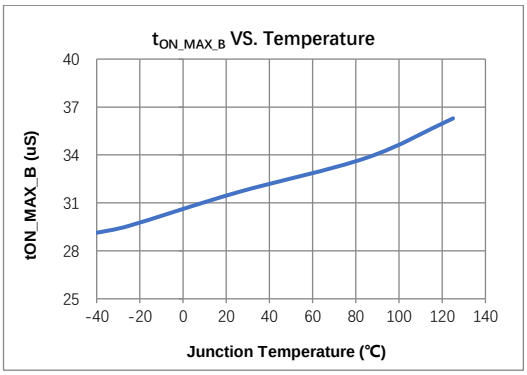






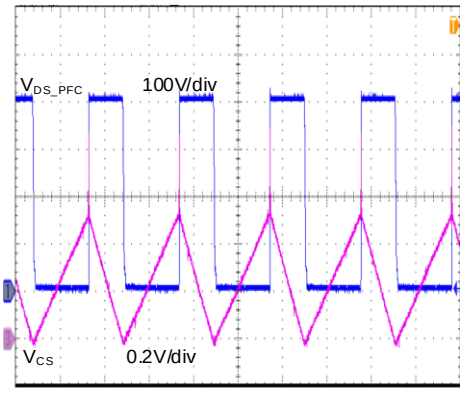






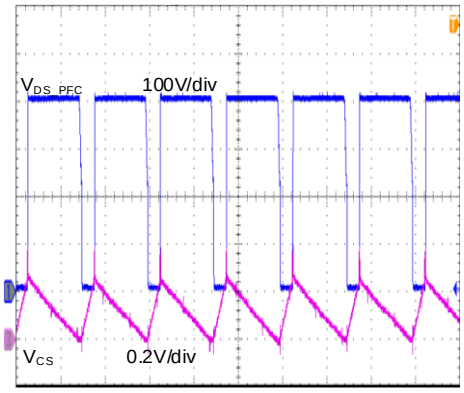
Typical Performance Characteristics

Steady State
(V_{IN}=115V)



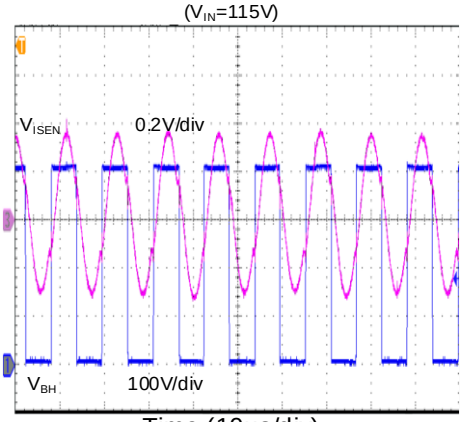
Time (10μs/div)

Steady State
(V_{IN}=230V)



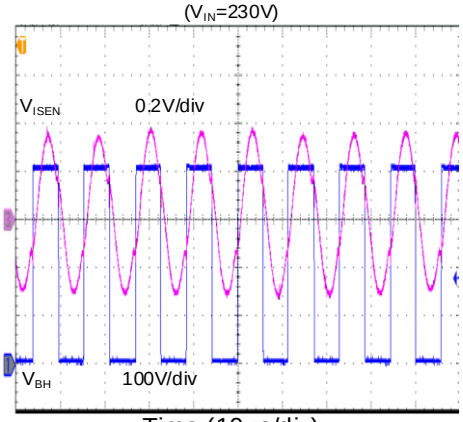
Time (10μs/div)

Steady State
(V_{IN}=115V)



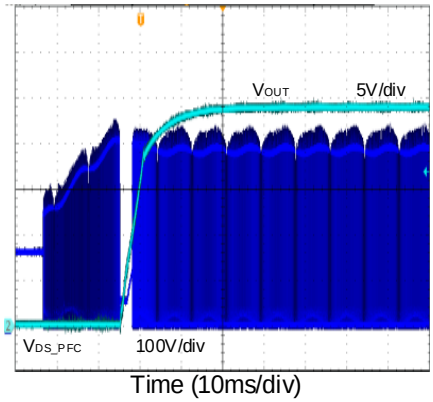
Time (10μs/div)

Steady State
(V_{IN}=230V)



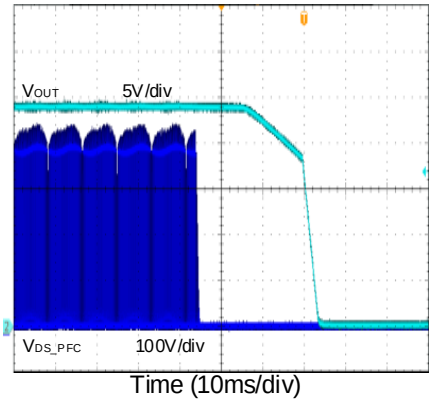
Time (10μs/div)

Start up
(V_{IN}=115V)



Time (10ms/div)

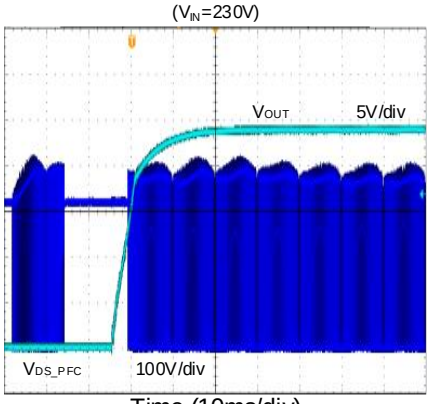
Shut down
(V_{IN}=115V)



Time (10ms/div)

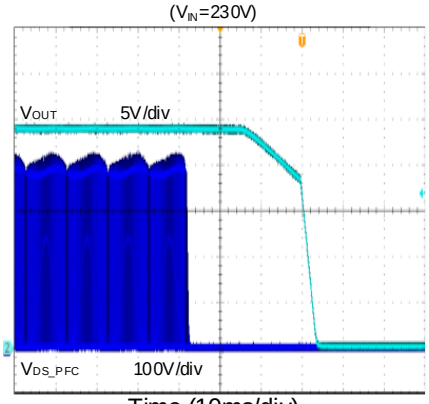
Typical Performance Characteristics (cont.)

Start up
(V_{IN}=230V)



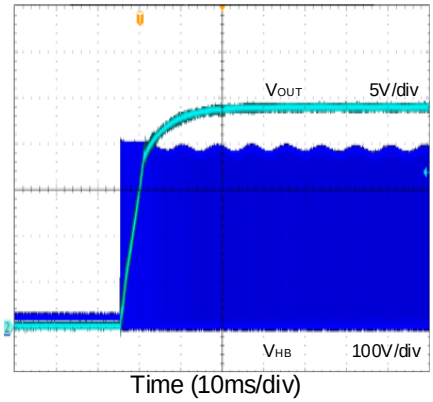
Time (10ms/div)

Shut down
(V_{IN}=230V)



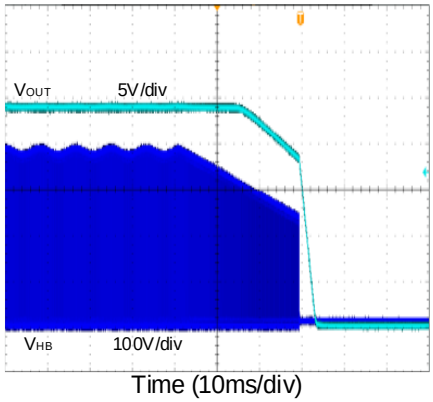
Time (10ms/div)

Start up
(V_{IN}=115V)



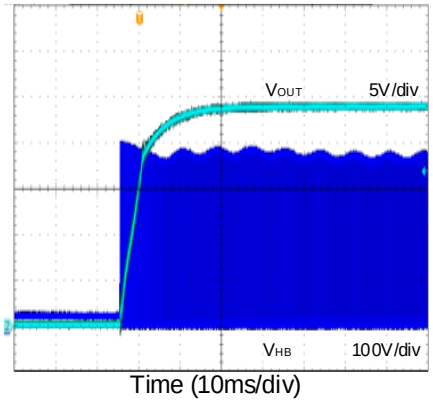
Time (10ms/div)

Shut down
(V_{IN}=115V)



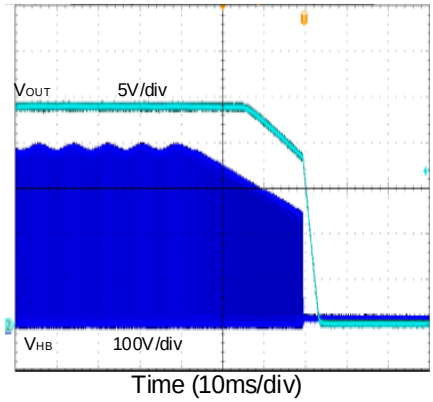
Time (10ms/div)

Start up
(V_{IN}=230V)



Time (10ms/div)

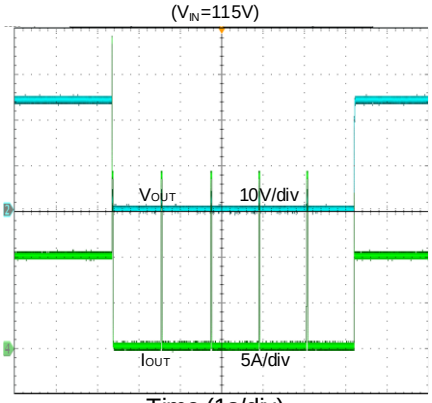
Shut down
(V_{IN}=230V)



Time (10ms/div)

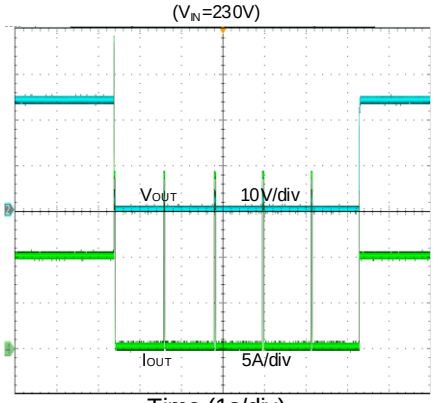
Typical Performance Characteristics (cont.)

Short Circuit Protection
(V_{IN}=115V)



Time (1s/div)

Short Circuit Protection
(V_{IN}=230V)



Time (1s/div)

Detailed Description

The SY5055E PFC+LLC controller integrates a boost PFC controller and a resonant half-bridge LLC controller. The boost converter operates in critical conduction mode (CrM) or discontinuous conduction mode (DCM) to minimize switching losses and improve EMI performance. It uses average current control to achieve unity power factor (PF) and minimal total harmonic distortion (THD). The burst function enhances efficiency at low loads. The SY5055E ensures safe boost converter operation with reliable protection against output overvoltage (OVP), undervoltage (UVP), and overcurrent (OCP), as well as input brown-out (BO).

The LLC converter uses integrated current mode control to provide a fast dynamic response along with eliminating the need for the capacitor sense circuit, to simplify the design of loop compensation parameters. The converter maintains high efficiency and low audible noise throughout the entire load range. The SY5055E ensures safe LLC converter operation with reliable protection against output overvoltage (OVP), overtemperature (OTP), and overload (OLP) events.

PFC Operation

The Power Factor Correction (PFC) operates in quasi-resonant (QR) or discontinuous conduction mode (DCM) using valley detection to reduce switch turn-on losses. The PFC is designed as a boost converter with a fixed output voltage. One advantage of a fixed boost converter is that the LLC can be designed for high input voltages, simplifying the LLC design process. Another advantage is the option to use a smaller boost capacitor value or to achieve a significantly longer hold-up time. The system can operate in Burst mode to improve efficiency at low output loads.

Boost PFC Basic Control

The SY5055E uses average current mode control, which can automatically compensate for parasitic parameters to achieve optimal PF/THD. The average current control block is shown in Figure 3.

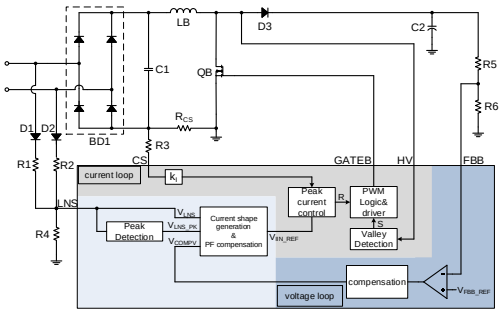


Figure 3. PFC Control Block

In the block diagram, the voltage loop generates the compensation signal V_{COMPV}. The current shaping circuit produces a current reference with power factor (PF) compensation. The current loop regulates the input current to follow the sine wave reference.

Power Curve and Modes of Operation

Under heavy load, the PFC operates in CrM mode. The duty cycle D_{SW} is 100%. To increase efficiency under light load, the boost converter operates in DCM mode. As the PFC output power decreases, the V_{COMPV} generated by the PFC output voltage control loop will decrease. When V_{COMPV} falls below V_{COMPV_D}, the DCM time increases as V_{COMPV} decreases. The circuit controls the time the inductor current (t_L) flows, as a portion of the switching period (t_{SW}). If R_{CS} is designed to the typical value indicated in the peak current control section, the duty cycle D_{SW} decreases from 100% to 10% as the PFC output power P_{OUT} drops from 25% to 5%.

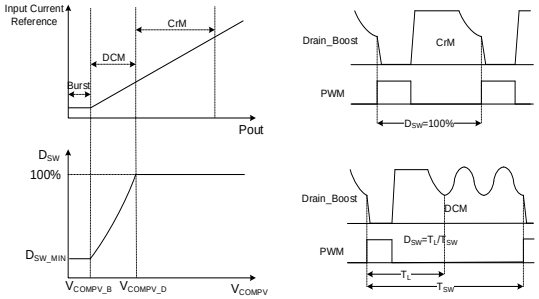


Figure 4. Power Curve and Modes of Operation

When the PFC output power drops below 5% of the nominal power, the PFC operates in Burst mode to improve efficiency.

Valley Detection

The boost stage operates in quasi-resonant mode to reduce switching power losses. The power MOSFET QB turns on at the resonant valley, which is detected by sensing the drain voltage via the HV pin. To prevent damage to the SY5055E during an input power surge, connect a 1kΩ–5kΩ resistor in series between the HV pin and the MOSFET drain. An integrated V_{DRAIN} slope detection circuit monitors the zero crossing of the PFC inductor current (ZCS). After detecting ZCS and following a fixed delay time of t_{QR_DELAY} (300ns), the MOSFET QB turns on. The AC valley detection circuit is shown in Figure 5.

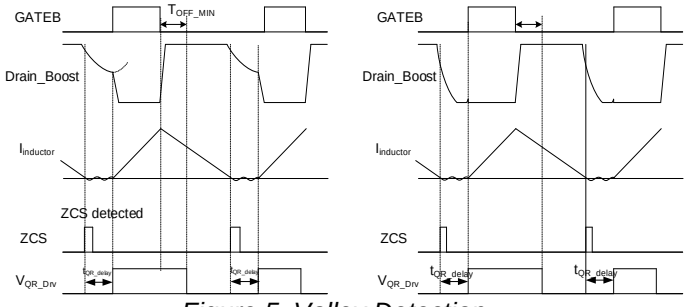


Figure 5. Valley Detection

AC Mains Sensing

AC mains sensing occurs through the LNS pin. The LNS pin senses both the constant and the peak values of the AC mains power source. The AC mains peak value is used as a feed-forward mechanism to adjust the input current reference. Typically, the AC mains peak value is detected every half line cycle.

Add 100μs filter time to the LNS pin to improve noise immunity. The AC mains sensing circuit is shown in Figure 6.

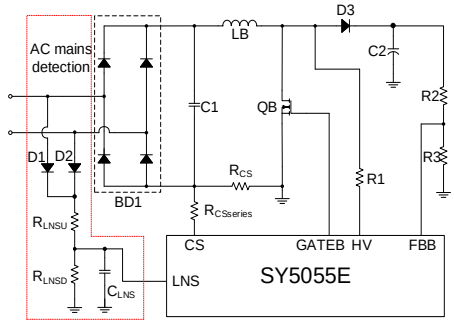


Figure 6. AC Mains Sensing Circuit

PFC Output Voltage Regulation

The PFC output voltage is set by the resistance voltage divider connected between the FBB and GND pins.

The regulated PFC output voltage can be calculated as follows:

$$V_{PFC} = \frac{R_{FBBU} + R_{FBBD}}{R_{FBBD}} \times V_{FBB\_REF}$$

Typical values for most applications are as follows: R_{FBBU} = 6MΩ–12MΩ, V_{FBB_REF} = 1.2V. Adding a filter with a time constant of 200μs to the FBB pin is recommended for improved noise immunity.

For example, to obtain a nominal PFC output of 390V with R_{FBBU} set to 6MΩ, R_{FBBD} should be 18.5kΩ. It is recommended that C_{FBB} is chosen to be in the range of 10nF to 22nF, and C_{FBB} should be placed as close as possible to the FBB pin.

PFC Current Sensing

To achieve a unity power factor (PF), the input current must be in phase with the input voltage. To minimize input current distortion caused by V_{COMPV} ripple under high line input conditions, the peak input voltage information (V_{LNS_PK}) is fed forward to the current reference. The input voltage is sensed through a resistor divider as V_{LNS}, and the peak input voltage V_{LNS_PK} detection is also integrated. The value k_i represents an internal transfer coefficient. The input current reference V_{IIN_REF} can be calculated using the following equation:

$$V_{IIN\_REF} = \frac{V_{COMPV} \times V_{LNS}}{k_i \times V_{LNS\_PK}^2}$$

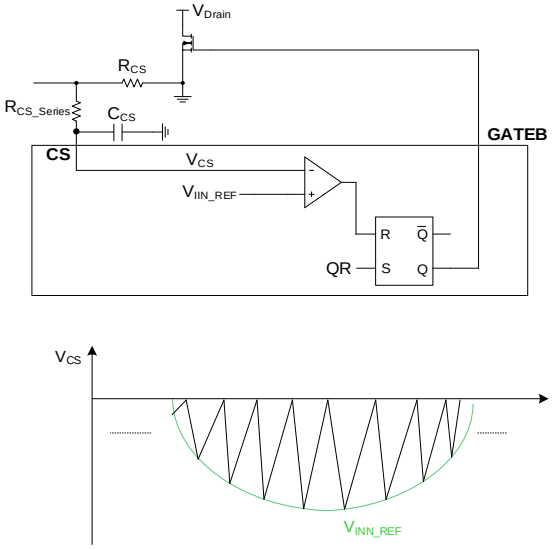


Figure 7. Peak Current Control

As shown in Figure 7, V_{CS} is compared with V_{IIN_REF}. When the peak current is reached, the MOSFET will turn off. After the inductor current decreases to 0, the QR signal initiates the next switching cycle.

To design for the lowest AC input and full load, the PFC operates in CrM mode. The R_{CS} can be determined as follows:

$$R_{CS} \approx \frac{V_{CS\_LIMIT} \times V_{AC\_MIN}}{2\sqrt{2} \times P_{IN}}$$

where the V_{CS_LIMIT} is the current limit point of PFC.

The SY5055E provides overpower protection at the PFC stage to improve system reliability. When V_{COMPV} exceeds V_{COMPV_OPP} for a duration of t_{COMPV_OPP}, the PFC OPP will be triggered. To improve efficiency of the LLC stage, the PFC overpower protection value is set to $\frac{P_{OUT\_MAX}}{\eta_{\_LLC}}$.

To ensure the PFC OPP cannot be triggered during normal operation, the chosen R_{CS} value should satisfy the following equation:

$$R_{CS} < \frac{V_{COMPV\_OPP} \times k_{PFCOPP}}{\frac{P_{OUT\_MAX}}{\eta_{\_LLC}}} \times \frac{R_{LNSD}}{R_{LNSU} + R_{LNSD}}$$

where V_{COMPV_OPP} is an internal voltage threshold (1.33V) and k_{PFCOPP} is a calculated coefficient (0.073).

The PFC OPP value is calculated using the above formula at the minimum input voltage.

For example, selecting R_{LNSD} = 25kΩ, R_{LNSU} = 6MΩ, P_{OUT_MAX} = 120W, η_{LLC} = 95%, then R_{CS} < 185mΩ.

Due to the PFC gate turn-off delay, the PFC OPP value will increase as the input voltage increases. Typically, the PFC OPP value at 264 VAC input is 1.2 to 1.4 times that of the 90 VAC input.

If there is no NTC in the AC input loop, a large surge current, typically exceeding 100A, may occur during the

startup stage, potentially causing a significant voltage drop across R_{CS}. Resistor R_{CS_SERIES} is designed to protect the CS pin from this surge current. The recommended value for R_{CS_SERIES} is between 200Ω and 800Ω. The circuit is shown in Figure 8.

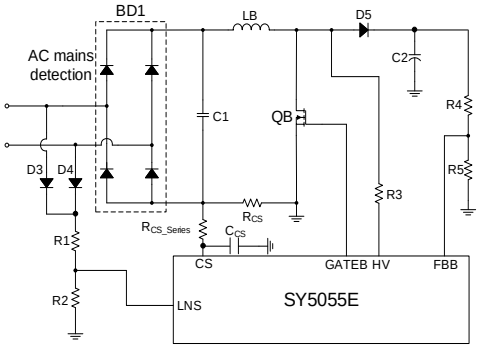


Figure 8. V_{RCS} Limit Circuit

When VSEN_OVP protection is triggered, the protection behavior can be controlled in the following ways:

- If R_{CS_SERIES} is between 200Ω and 240Ω, the device will stop switching and restart after the $t_{VCC\_TIMEOUT}$.
- If R_{CS_SERIES} is between 510Ω and 800Ω, the device will stop switching and latch.

For improved noise immunity and signal delay trade-off considerations, place a 100pF to 470pF capacitor (C_{CS}) as close as possible to the CS pin.

PFC Driver

To achieve optimal EMI performance, the SY5055E uses an optimized two-stage gate driver method. In the first stage, GATEB rises to V_{GATEB_TH} (8.5V). In the second stage, after the minimum on-time $t_{ON\_MIN\_B}$ has elapsed, GATEB rises from V_{GATEB_TH} to V_{GATEB_DRV} (11V). The gate voltage is illustrated in Figure 9.

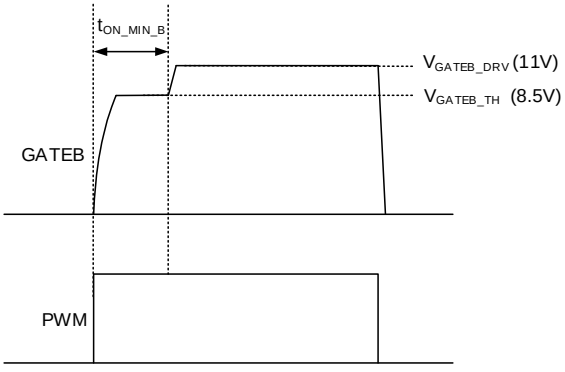


Figure 9. GATEB Waveform

PFC Fault Protection

PFC Brown-In and Brown-Out Protection

To prevent the boost converter from operating at very low input voltages, which can cause excessive heat and significantly reduced efficiency, input brown-out (BO) is monitored by the LNS pin. When V_{LNS_PK} is less than V_{LNS_BO} continuously for longer than $t_{PROT\_LNS\_BO}$, an input brown-out is detected. Consequently, the protected minimum input voltage $V_{AC\_MIN(RMS)}$ is as follows:

$$V_{AC\_MIN} = \frac{V_{LNS\_BO}}{\sqrt{2}} \times \frac{R_{LNSU} + R_{LNSD}}{R_{LNSD}}$$

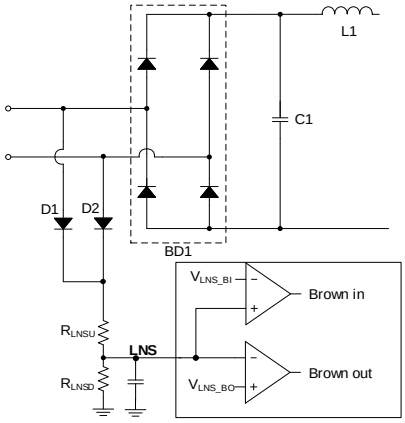


Figure 10. Input Voltage BO/BI Circuit

After the input BO protection is triggered, the PFC and LLC will stop switching. The device enables the restart timer, and the HV will begin to draw current to prevent LNS from floating high. Once the restart timer is overflows, if V_{LNS_PK} is greater than V_{LNS_BI}, the boost converter will initiate soft-start as shown in Figure 11.

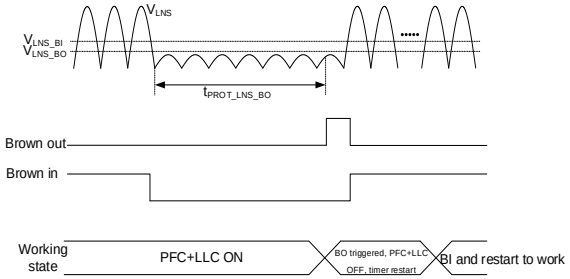


Figure 11. Brown-Out Protection

The recommended value range for R_{LNSU} is 6MΩ to 12MΩ. For example, if the brown-out point is set at 70V (AC RMS) and the R_{LNSU} is set to 6MΩ, then the R_{LNSD} can be calculated as 24.3kΩ. Add a 1nF capacitor between the LNS pin and GND to improve noise immunity.

X-Cap Discharge

When no rising edge is detected on the LNS pin for the duration of the X-cap discharge debounce time t_{XDIS_DBT}, X-cap discharge protection will be enabled. In this mode, both stages cease operation, and the HV pin sinks current to VCC to discharge all input capacitors. VCC is clamped high during the discharge period. If all input capacitors are discharged, VCC will gradually drop to the undervoltage lockout (UVLO) threshold. If AC power is connected before the capacitors are fully discharged, X-cap

discharge protection will exit immediately, and the system will restart once VCC has charged to V_{VCC_ON}. The maximum discharge time t_{X_MAX} protects the HV discharge circuit. If the maximum discharge time is reached, discharge will stop for t_{X_MAX} before restarting the discharge process. When the input voltage is DC, the X-cap function is disabled.

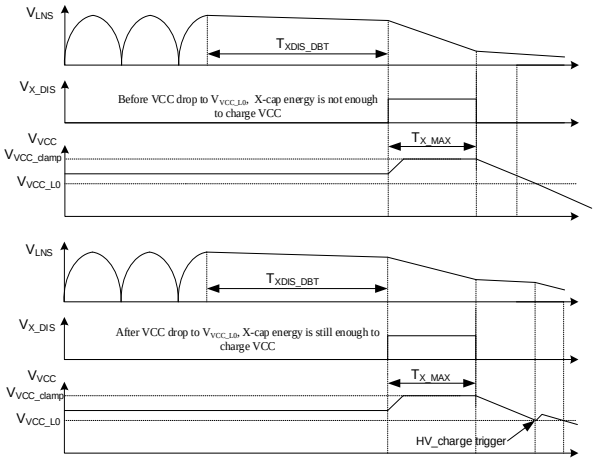


Figure 12. AC Power Disconnected

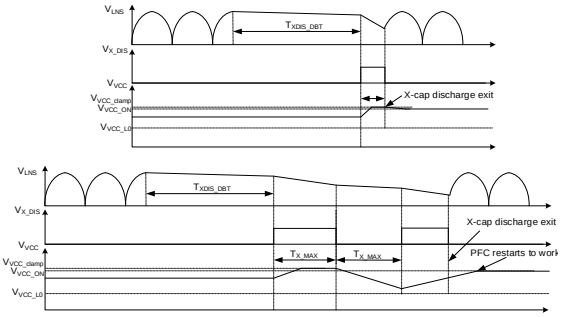


Figure 13. AC Disconnected and Reconnected before X-Cap is Fully Discharged

PFC Output UVP and OVP

PFC output undervoltage protection (UVP) prevents short circuits at the FBB low side resistor or FBB pin during output undervoltage conditions.

If $V_{FBB} < V_{FBB\_UVP}$, the boost stage stops switching unless $V_{FBB} > V_{FBB\_UVP} + V_{HYS}$, as shown in Figure 14.

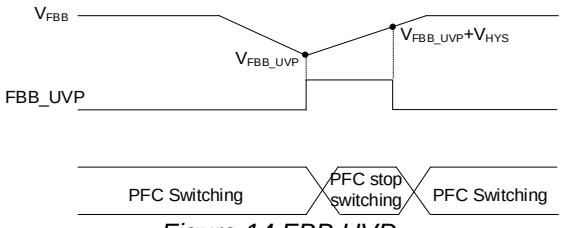


Figure 14.FBB UVP

PFC output overvoltage protection (FBB OVP) safeguards against the following cases:

- Output voltage overshoot caused by slow loop response or rapid load steps
- Input overvoltage resulting from line voltage jitter, incorrect line voltage connections, or surge tests
- Low side resistor failure or open circuit conditions at the FBB pin

If $V_{FBB} > V_{FBB\_OVP}$, the boost stage stops switching unless $V_{FBB} < V_{FBB\_OVP} - V_{HYS}$, as shown in Figure 15.

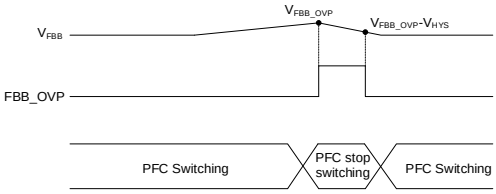


Figure 15. FBB OVP

PFC HV OVP

HV overvoltage protection detects FBB feedback loop failure during PFC output overvoltage conditions, in case FBB OVP is not triggered. This protection is integrated into the HV pin. If V_{HV_SENSE} exceeds V_{HV_OVPTH} and the PFC output OVP is not triggered, both stages will stop switching, and the device timeout will restart. If the PFC output overvoltage protection is triggered, the HV OVP will be disabled and will only stop the PFC stage. To avoid noise interference, the HV OVP can only be triggered if V_{HV_SENSE} exceeds V_{HV_OVPTH} during four consecutive PFC OFF periods when the PFC output overvoltage protection has not been triggered.

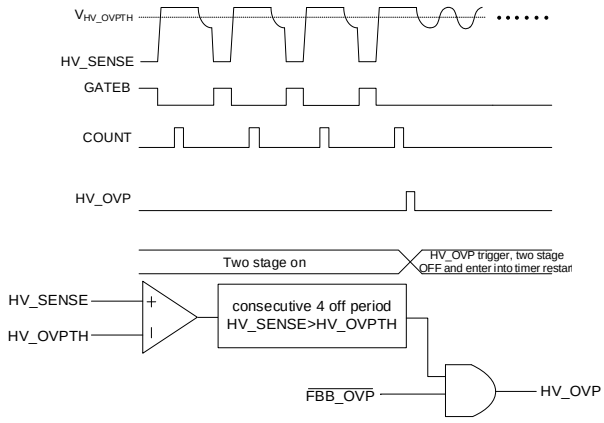


Figure 16. HV OVP

PFC Inductor Short-Circuit or Saturation Protection

The SY5055E includes inductor short circuit protection to prevent damage to the device and external MOSFET. If V_{CS} reaches the -850mV limit continuously four times during each PFC switching cycle, inductor short circuit protection is triggered, both stages shut down, and the device initiates a timeout restart.

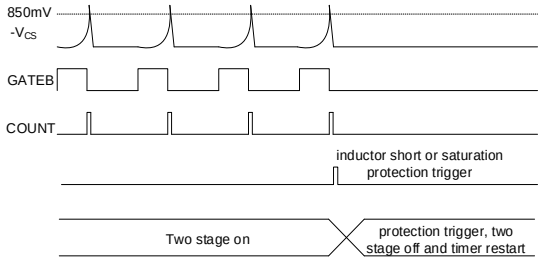


Figure 17. Inductor Short or Saturation Protection

PFC+LLC Two-Stage Disable Function

To achieve extremely low standby power requirements, both the PFC and LLC stages can be disabled by applying a voltage greater than 2.3V to the FBB pin.

LLC Operation

Current Mode Control

The SY5055E uses current mode control in the LLC stage inner loop to achieve fast dynamic response.

The outer loop controls the output voltage through the amplifier or TL431 regulator in various applications. The compensation information is transferred to the primary side via a compensation circuit and an optocoupler to obtain I_{FBL}. V_{CCOMP} is the internal compensation voltage. Figure 18 shows the current mode control block.

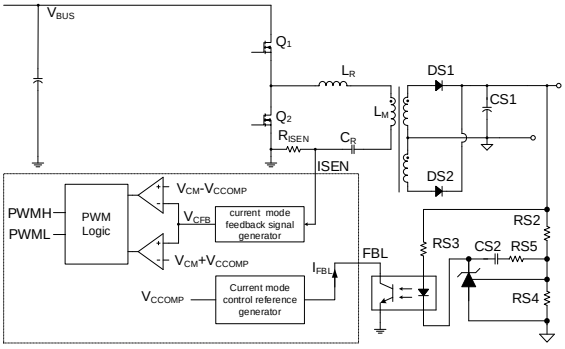


Figure 18. Control Mode Control Block

The internal signal V_{CFB} acts as a current loop feedback signal and has a linear relationship with the output power. The V_{CFB} voltage changes are a result of the primary current that drives power conversion.

V_{CFB} is compared with V_{CM} - V_{CCOMP} and V_{CM} + V_{CCOMP} for MOSFETs control as follows:

- If $V_{CFB} < V_{CM} - V_{CCOMP}$, PWMH = 1, PWML = 0, high-side MOSFET is turned on
- If $V_{CFB} > V_{CM} + V_{CCOMP}$ PWMH = 0, PWML = 1, low side MOSFET is turned on

The typical waveforms are shown in Figure 19. When load increases, V_{CCOMP} increases. Otherwise, V_{CCOMP} decreases.

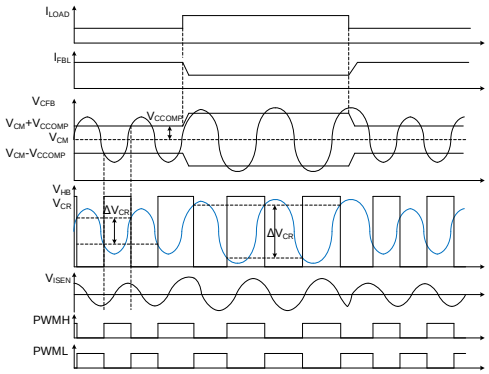


Figure 19. Current Mode Control Waveform

R_{ISEN} Selection

The control design parameters are shown below:

$$P_{IN} = V_{BUS} \times C_R \times \Delta V_{CR} \times f_{SW} + C_j \times {V_{BUS}}^2 \times f_{SW}$$

Where C_J represents the total junction capacitance; P_{IN} denotes the LLC input power; C_R is the resonant capacitor; ΔV_{CR} indicates the voltage change across the C_R during the PWMH = 1 stage.

$$\Delta V_{CR} = \frac{P_{IN} - C_j \times {V_{BUS}}^2 \times f_{SW}}{V_{BUS} \times C_R \times f_{SW}}$$

The relationship between V_{CCOMP} and ΔV_{CR} is

$$\Delta V_{CR} = V_{CCOMP} \times \frac{2 \times k}{C_R \times R_{ISEN}}$$

and the current sense resistor R_{ISEN} is chosen as follows:

$$R_{ISEN} = \frac{2 \times V_{CCOMP\_OPP} \times k \times V_{BUS} \times f_{SW}}{P_{IN} - C_j \times {V_{BUS}}^2 \times f_{SW}}$$

where k is the R_{ISEN} calculation coefficient.

The value of k can be adjusted to suit different operating frequency applications. V_{CCOMP_OPP} represents the internal voltage threshold of the device, with a typical value of 330mV. See the External Settings section for more information. Figure 20 shows a recommended resonant current sensing method for typical applications.

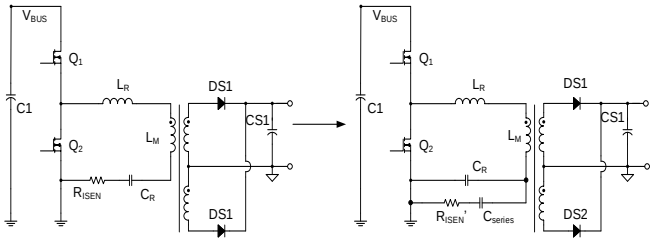


Figure 20. Resonant Current Sense Circuit

$$R'_{ISEN} = \frac{C_R}{C_{series}} R_{ISEN}$$

This approach decreases the sensing resistor loss.

For example, if the selected operating frequency (f_{SW}) is 100 kHz, the input voltage (V_{BUS}) is 400V, the maximum

input power (P_{IN_OPP}) is 120 W, the resonant capacitor (C_R) is 33nF, the current split capacitor (C_{SERIES}) is 200pF, the junction capacitance (C_J) is 200pF, and the output compensation voltage (V_{CCOMP_OPP}) is 330mV.

$$R_{ISEN} = \frac{2 \times V_{CCOMP\_OPP} \times k \times V_{BUS} \times f_{SW}}{P_{IN} - C_j \times {V_{BUS}}^2 \times f_{SW}} = 0.278\Omega$$

Therefore, R_{ISEN}' = (33/0.2) × R_{ISEN} = 47Ω.

Power Curve and Operation Modes

The power curve is shown as below.

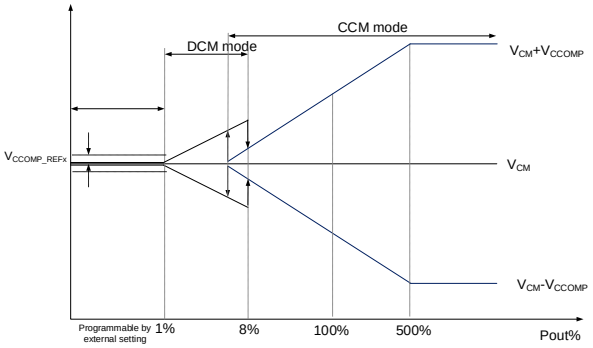


Figure.21 Power Curve and Modes of Operation

There are three operational modes, ranging from heavy load to light load: Continuous Conduction Mode (CCM), Discontinuous Conduction Mode (DCM) and Burst Mode.

In CCM mode, the system operates in continuous switching with a 50% duty cycle, similar to traditional LLC operation via frequency control. In all operating modes, current mode control is employed, and the adaptive non-overlap function, based on the HB end-of-slope detection, activates the gate driver.

The DCM mode is a type of burst mode that operates at a high repetition frequency. In this mode, the energy in each pulse is maintained at a relatively high level to enhance conversion efficiency.

In Burst mode, each Burst cycle consists of a series of DCM cycles followed by a sleep period. The Burst mode frequency is well regulated to a maximum of 0.4kHz to avoid audible noise. The transition level for entering Burst mode can be preset using the VSEN pin. This preset principle will be demonstrated in the external setting principle section.

DCM Mode Switching

One DCM cycle consists of five PWM pulses that follow a Low-High-Low-High-Low sequence, along with a sleep time controlled by the internal power curve. Upon the first entry into DCM mode, the LLC first activates the low side to ensure that the high side power supply remains sufficient even after an extended sleep period. The low side will turn off once V_{CFB} reaches V_{CM}-V_{CCOMP}. The subsequent three switching cycles will operate the same as in CCM mode. The last low side switch will turn off when the resonant current crosses zero. During the non-switching period, The DCM ring number is locked at 2. Once the first DCM cycle concludes, the next DCM cycle will begin by detecting the falling slope end of HB for QR, with the following logic mirroring that of the previous DCM cycle.

The working principle of the DCM mode is shown as below:

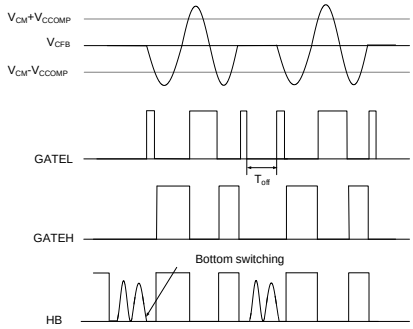


Figure.22a DCM Modes Working Principle

To accurately set the V_{CCOMP} value during DCM operation, SY5055E adopt compensation current strategy, as shown in Fig. 22b; the Vccomp value can be equivalently decreased or increased by increasing or decreasing the compensation current;

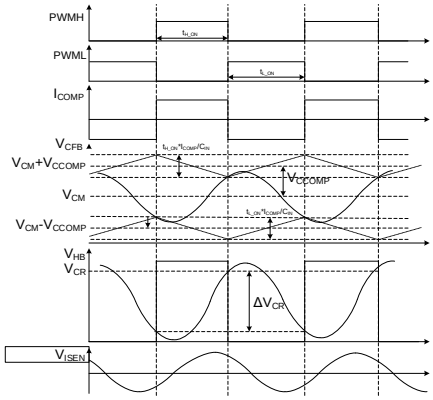


Fig.22b DCM Compensation Current Working Principle

Burst Mode Operation

As the output power decreases, when the I_{FBL} rises above the Burst mode entry threshold, which can be set through an external resistor connected to the VSEN pin, the IC enters sleep mode and the LLC stops switching.

When the compensation voltage on the secondary side rises and the I_{FBL} drops below the Burst-on threshold, the LLC wakes up to operate. The number of DCM cycles is adjusted by detecting the Burst frequency. During the current Burst cycle, if the duration of the Burst cycle is less than t_{BURST_REF}, the number of DCM cycles will increase

by one in the next Burst cycle. Conversely, if the duration of the Burst cycle is greater than t_{BURST_REF} the number of DCM cycles will decrease by one in the next Burst cycle. Each Burst cycle modifies the number of DCM cycles only once. When the output power increases and the I_{FBL} falls below the Burst mode entry level minus a specific level of hysteresis, the LLC exits Burst mode and reverts to DCM mode. For instance, the operational principle of Burst mode under load increase is illustrated below.

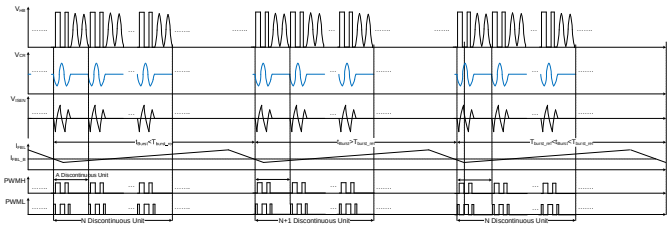


Figure.23 Burst Modes Working Principle

Adaptive Non-Overlap ZVS Operation

To minimize switching power loss, adaptive zero voltage switching (ZVS) is implemented in every switching period. HB rising/falling slope are detected via a slope detection circuit.

When ZVS is enabled, the dead time begins. If the end of the rising or falling slope of HB is detected after the minimum dead time T_{D_MIN}, the high side or low side MOSFET will be turned on again. If T_{D_MAX} expires without a slope end detected, the MOSFET will be turned on directly.

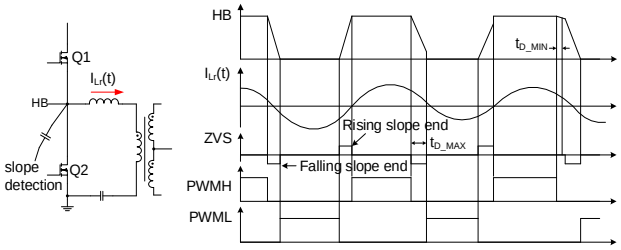


Figure 24. Adaptive Non-Overlap ZVS Operation

External Settings

Three pins are used to preset the LLC operating characteristics:

- GATEB determines whether DC input is supported
- ISEN sets the LLC DCM compensation current
- VSEN establishes the burst entry level

Figure 25 shows the external settings circuit.

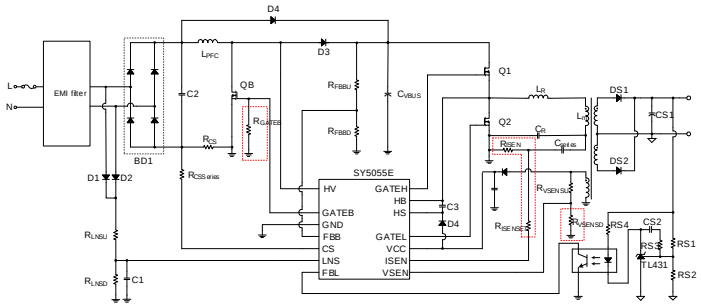


Figure 25. External LLC Settings

Table 1. Input Voltage Setting

R_{GATEB}	DC input
9kΩ–11kΩ	Y
27kΩ–33kΩ	N

Table 2. LLC DCM Compensation Current Setting

$R_{ISENSET}$ + R_{ISEN}	Compensation Current (Note 8)
0Ω < $R_{ISENSET}$ +R_{ISEN} < 125Ω	**Big**
125Ω < $R_{ISENSET}$ +R_{ISEN} < 375Ω	**Middle**
375Ω < $R_{ISENSET}$ +R_{ISEN} < 520Ω	**Small**

Note 8: Set the resistance value to adjust the compensation current.

Table 3. Burst Power Level Setting

RVSEND	Burst Power Level (Note 9)
3.9kΩ < R_{VSEND} < 5.1kΩ	Approximately 1%
9.1kΩ < R_{VSEND} < 11kΩ	Approximately 2%
22kΩ < R_{VSEND} < 30kΩ	Approximately 3%

Note 9: Percentage of designed 100% load when 375Ω < $R_{ISENSET}$ +R_{ISEN} < 520Ω.

LLC Fault Protection

Capacitive Mode Protection

Capacitive mode should be avoided to prevent high switching losses and control logic errors. The SY5055E uses improved adaptive non-overlap zero-voltage switching (ZVS) logic to eliminate capacitive mode switching. Figure 26 shows capacitive mode operation.

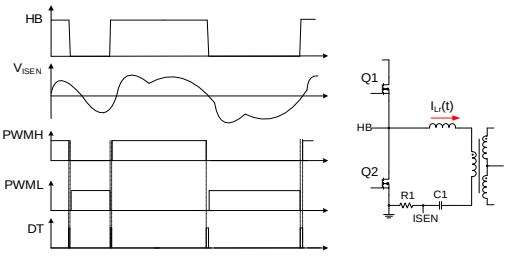


Figure 26. Capacitive Mode Operation

When the high side MOSFET enters capacitive mode, it will be turned off immediately. After T_{D_MAX} expires or when zero-voltage switching (ZVS) is detected after T_{D_MIN}, the low side MOSFET will turn on. This prevents hard switching and shoot-through of the low side MOSFET. The logic operates in the same manner when the low-side MOSFET is turned off. Figure 27 shows this switching logic.

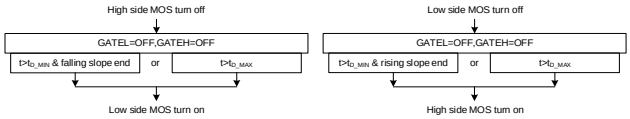


Figure 27. MOSFET Switching Logic

LLC Input Brown-In and Brown-Out Protection

The LLC input voltage is sensed via the FBB pin, and LLC switching is controlled as follows:

- If $V_{FBB} < V_{FBB\_BO}$, the LLC stops switching
- If $V_{FBB} > V_{FBB\_BI}$, the LLC begins to switch

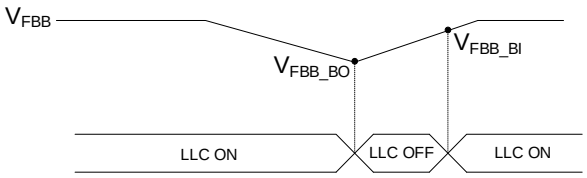


Figure 28. LLC BO and BI Protection

LLC Output OVP

The LLC output OVP is sensed via the VSEN pin. Figure 29 shows the VSEN pin sensing circuit.

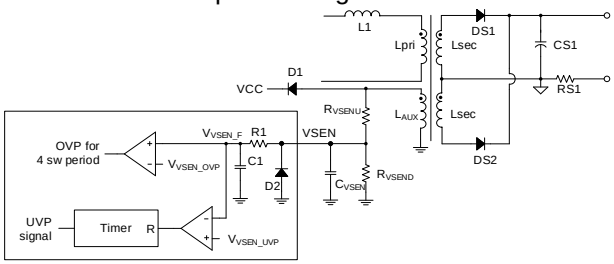


Figure 29. Output OVP and UVP Sensing Directly from AUX Winding

If $V_{VSEN\_F} > V_{VSEN\_OVP}$ for eight consecutive LLC switching cycles, LLC output OVP is triggered as shown in Figure 30.

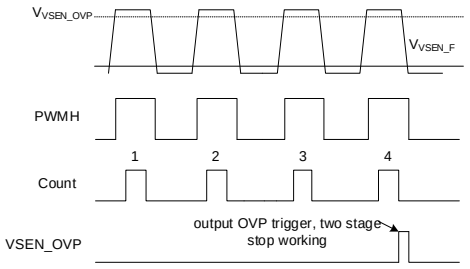


Figure 30. LLC Output OVP Logic

For example, if the output voltage is regulated at Vo and a 20% overvoltage range is acceptable, R_{VSEND} is selected for the burst entry level. R_{VSENU} can be calculated using the following equation:

$$R_{VSENU} = R_{VSEND} \times \left(\frac{120\% \times N_{AUX} \times Vo}{V_{VSEN\_OVP} \times N_{sec}} - 1 \right)$$

To improve noise immunity, place a 100pF to 200pF capacitor between the VSEN pin and GND. The capacitor should be positioned as close as possible to the device.

Figure 31 shows another type of VSEN circuit that can be used. The voltage across the AUX winding is first rectified to obtain the DC component, which is then divided by a resistor before connecting to the VSEN pin. R_{VSEND}, R_{EVSEU}, and C_{VSEN} can be selected as described above. It is recommended to select a value of 1µF for C_{REC}.

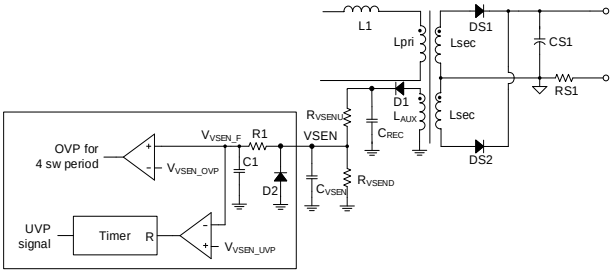


Figure 31. Output OVP and UVP Sensing via Rectified Voltage of AUX Winding

LLC Output UVP

The VSEN pin is also used to monitor voltage for LLC output undervoltage protection (UVP). If V_{VSEN_F} is less than V_{VSEN_UVP} continuously for the duration of t_{VSEN_UVP}, LLC output UVP is activated.

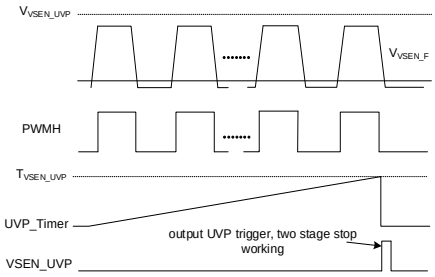


Figure 32. LLC Output UVP Logic

LLC Cycle-by-Cycle Current Limit Protection

$V_{ISEN\_L}(+)$ and $V_{ISEN\_L}(-)$ are the maximum current limits for the LLC stage.

When $V_{ISEN\_L(+)}$ is reached, the high side MOSFET will be turned off immediately, and the low side MOSFET will be turned on after a delay. When $V_{ISEN\_L(-)}$ is reached, the low side MOSFET will be turned off immediately, and the high side MOSFET will be turned on after a delay. Figure 33 shows LLC cycle-by-cycle current limit protection.

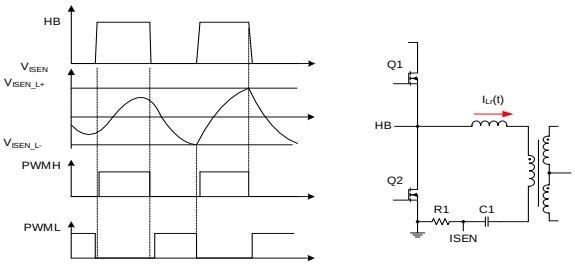


Figure 33. LLC Cycle-by-Cycle Current Limit Protection

When the output of the LLC is short circuited, and V_{ISEN_L} has been activated cycle-by-cycle for a duration of $t_{IL\_PROTECT}$, then output short-circuit protection will be triggered.

LLC Overpower Protection (OPP)

When the output power exceeds the maximum value, then LLC OPP will be triggered to ensure that I_{FBL} remains below $I_{FBL\_130\%}$ continuously for the duration of t_{OPP}.

LLC Open Loop Protection (OLP)

If the secondary side feedback loop is damaged, as in the case of a short circuit in the optocoupler, and it causes I_{FBL} to fall below $I_{FBL\_250\%}$ continuously for the duration of t_{OLP}, then open loop protection will be triggered.

VCC Overvoltage Protection (VCC OVP)

Before VCC rises to V_{VCC_OVP}, if VCC exceeds V_{VCC_SHUNT}, the VCC shunt current I_{VCC_SHUNT} will activate to reduce VCC. If VCC cannot be lowered and continues to rise to V_{VCC_OVP}, and if V_{VCC} remains greater than V_{VCC_OVP} for four continuous LLC switching cycles, then VCC overvoltage protection (OVP) will be triggered.

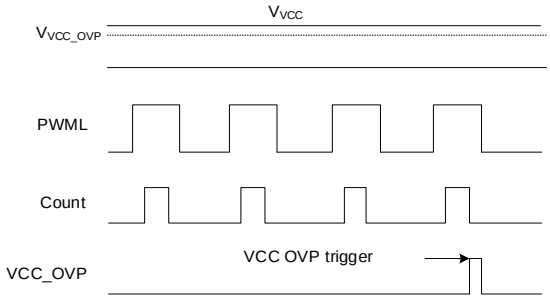


Figure 34. VCC OVP

In the LLC transformer design, the output voltage must be regulated at V_O. Therefore, the following design criteria should be met:

$$\frac{N_{AUX}}{N_{sec}} Vo < V_{VCC\_shunt}$$

Overtemperature Protection

Internal thermal protection operates by monitoring the junction temperature (T_J). If T_J reaches thermal shutdown temperature (T_{SD}), all switching ceases, and the device enters a timeout state. It will resume operation when T_J falls below T_{SD} - T_{HYS} (the hysteresis threshold), at which point switching will be re-enabled.

Startup and Power Supply

High Voltage Charge and VCC Management

The SY5055E controller features a high voltage startup current source that enables fast startup times and extremely low standby power consumption. The system provides two startup current levels (I_{ST_L} and I_{ST_N}) for safety in the event of a short circuit between the VCC and GND pins. The HV startup current source charges the VCC capacitor prior to device startup. The VCC startup sequence is as follows:

1) When $V_{VCC} < V_{VCC\_SCP}$, the startup current is limited to I_{ST_L}. This logic prevents the device from overheating in the event of a VCC short circuit to GND (VCC capacitor short circuit).
2) $V_{VCC\_SCP} < V_{VCC} < V_{VCC\_ON}$, startup current is I_{ST_N}, and V_{VCC} rises quickly to V_{VCC_ON} to satisfy startup time.
3) When V_{VCC} exceeds V_{VCC_ON}, the HV charge current pauses, allowing other logic functions to operate (sensing external parameters, initiating boost switching, and starting LLC switching). If VCC drops below V_{VCC_LO}, the charge current resumes to recharge VCC. The maximum charge time after VCC starts is defined as t_{VCC_CHARGE} to prevent overheating. This logic ensures that V_{VCC} remains between V_{VCC_LO} and V_{VCC_ON} before the load voltage rises.
4) When V_{OUT} rises sufficiently, VCC will be supplied by the auxiliary winding and will not drop below V_{VCC_LO},

causing the startup current to stop. If an output short circuit or other errors occur, the auxiliary winding supply will cease, allowing the HV startup to activate again to ensure VCC remains above V_{VCC_LO}.

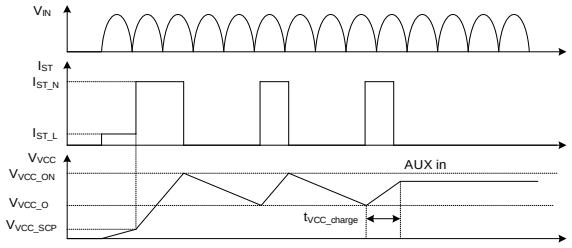


Figure 35. HV Charge Logic

High Side Driver Power Supply

An external bootstrap buffer capacitor supplies the high side driver. The bootstrap capacitor is connected between the high side reference HB pin and the HS pin of the high side driver supply input. When HB is low, an external diode charges this capacitor from the VCC pin.

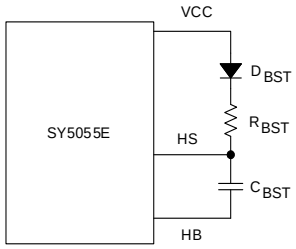


Figure 36. High Side Driver Power Supply Circuit

External diode D_{BST} should be a fast recovery, low voltage-drop diode. The series resistor R_{BST} is used to limit the charge current to protect D_{BST}. Typically, R_{BST} is set to 4.7Ω–10Ω.

Capacitor Values on VCC Pin and HS Pin

Generally, two types of capacitors are used on the VCC pin: an SMD ceramic capacitor with a smaller value, located close to the device to filter noise, and an electrolytic capacitor to supply the device's operating power.

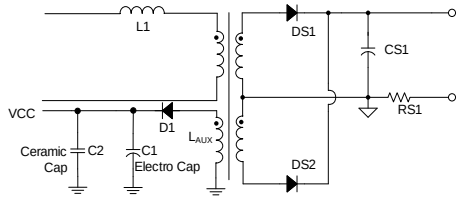


Figure 37. VCC Power Supply Circuit

The typical C_{VCC} values are $C_{VCC\_ELECTROLYTICAL}$ = 47μF and $C_{VCC\_CERAMIC}$ = 1μF.

The VCC capacitor must be sufficient to handle the startup period from when the LLC initiates until the auxiliary winding takes over the supply for the VCC pin.

For example, during startup, if the consumption current of the IC is I_{OPER} = 25mA and the time at which the auxiliary winding begins to take over the VCC supply is Δt = 15 ms, then the allowable VCC drop during startup is given by V_{VCC_ON} - V_{VCC_LO}, which results in ΔU = 15V.

Then the VCC capacitor should be:

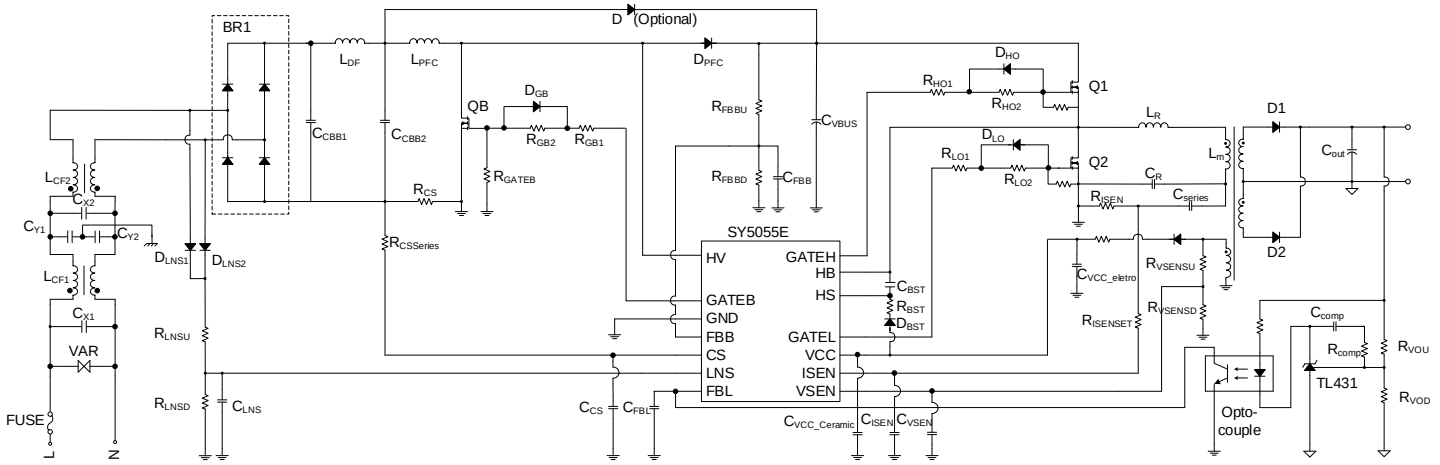
$$C_{VCC} > \frac{i_{oper} \times \Delta t}{\Delta U} = 25\mu F$$

To support charging the high side MOSFET gate, the value of the HS capacitor must be significantly higher than the gate capacitance. This prevents a substantial decrease in voltage on the HS due to gate charges. Typically, the recommended capacitor value across HS and HB ranges from 100nF to 470nF.

Table 4. Protection Action Summary

PFC Protection Action		LLC Protection Action	
Item	**Action**	**Item**	**Action**
AC BI/BO	Two stages stop switching, restart after $T_{VCC\_TIMEOUT}$	LLC BI/BO	LLC stop switching
PFC Output Second OVP		Output OVP	Both stages stop switching, restart after $T_{VCC\_TIMEOUT}$ or Latch (decided by CS series resistor)
PFC Inductor SCP		Output UVP	Two stages stop switching, restart after $T_{VCC\_TIMEOUT}$
CS resistor SCP		Output OPP	
PFC OPP		Output SCP	
PFC Output UVP	PFC not operating, all variables reset to initial value	Optocoupler OLP	
PFC Output OVP	PFC stops switching	ISEN current limit	
OTP	Both stages stop switching	ISEN resistor SCP	

Typical Application



Layout Design

FBL Track Shielded by GND Tracks or Plane

The FBL function operates at low current levels to minimize energy consumption during no-load conditions, making this signal more sensitive to disturbances.

Disturbances caused by capacitive coupling to converter switching tracks (HB or PFC DRAIN) can lead to unstable regulation.

To avoid disturbances in FBL, the FBL track must be positioned at a sufficient distance from the power section of the converters (LLC and PFC). Tracks along the FBL track must also be grounded for shielding, along with a ground plane if the design utilizes a double-sided copper layout. Additionally, the FBL track should be as short as possible.

Place FBB, LNS, CS, ISEN, and VSEN Sensing Resistor Close to the Device

For all input sensing pins, the sensing resistors should be placed close to the device to minimize disturbance caused by capacitive coupling.

Separate GND Connections for LLC and PFC

To prevent mutual disturbances, the grounding of the PFC and LLC controllers must be separated in the PCB layout. Current pulses through ground tracks can result in incorrect values or signals on pins that reference the ground level. The primary sources of disturbance are the substantial energy switching of the PFC and LLC converters, as well as the MOSFET gate drive currents generated by the controllers.

Figure 38 illustrates the energy flows. It also demonstrates that a special grounding structure can keep them separated to avoid disturbances.

Keep the energy flow loops for each converter as small as possible, in terms of track length and surface area. Minimize the track lengths of A and B, as shown in Figure 38. Minimize disturbances caused by the converter by connecting the device to the shared bulk capacitor through a separate ground track.

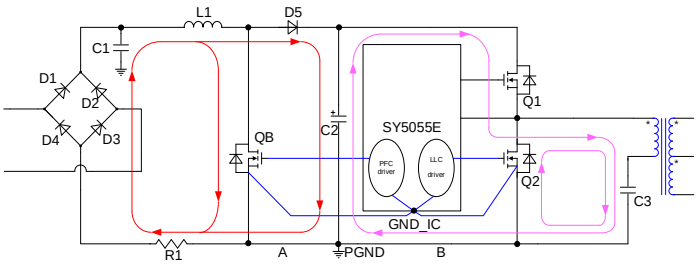


Figure 38. PFC and LLC Energy Flow Loops

Connect the primary ground as shown in Figure 39. The ground traces, marked in red, should be as short and wide as possible.

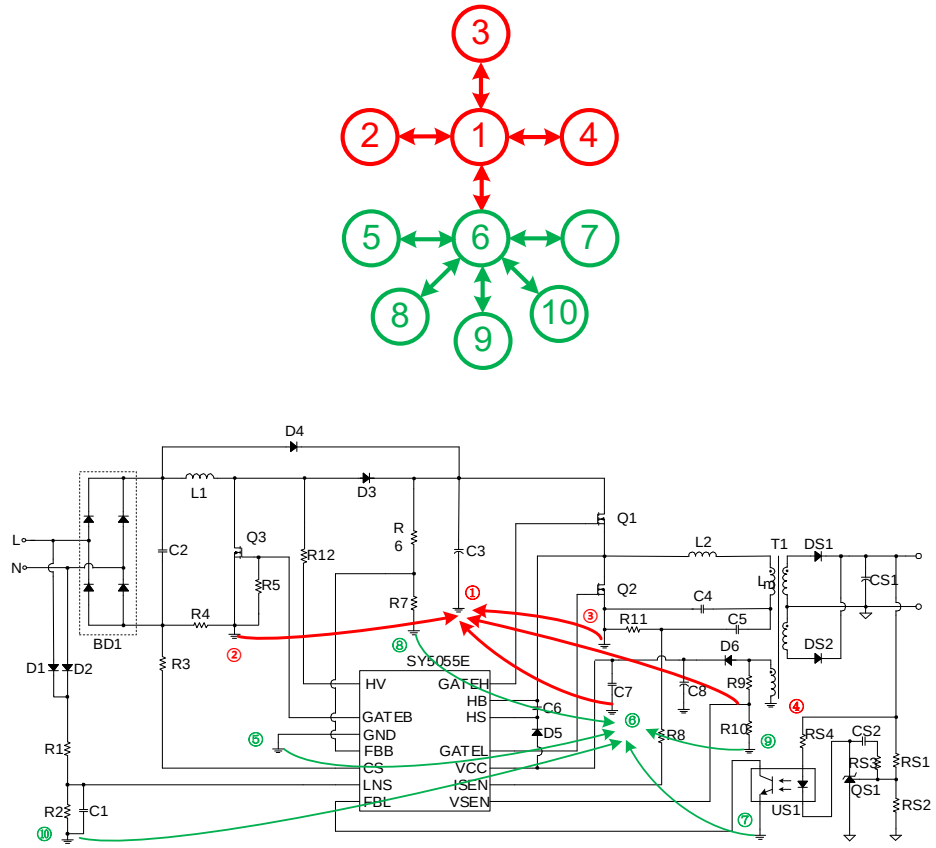


Figure 39. Recommended Ground Connection

①: Ground node of PFC bulk capacitor

②: Ground node of CS resistor and source of PFC MOS

③: Ground node of LLC resonant capacitor and source of LLC low side MOS

④: Ground node of transformer auxiliary winding

⑤: Ground node of IC GND

⑥: Ground node of VCC capacitor

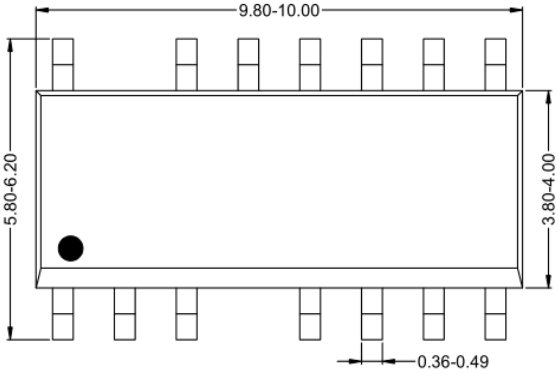
⑦: Ground node of opto-coupler

⑧: Ground node of FBB pin lower resistor

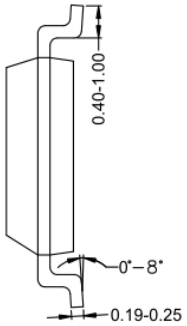
⑨: Ground node of VSEN pin lower resistor

⑩: Ground node of LNS pin lower resistor

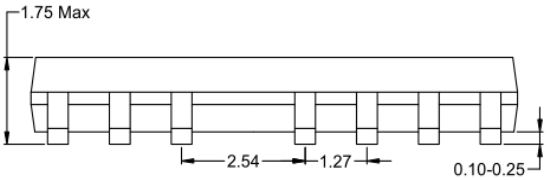
SOP14 Package Outline Drawing and PCB Layout



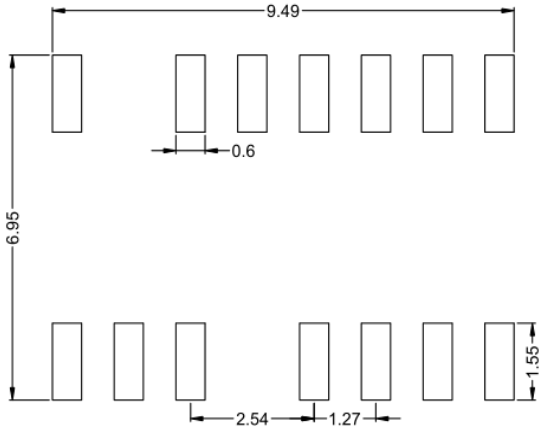
Top view



Side view



Front view

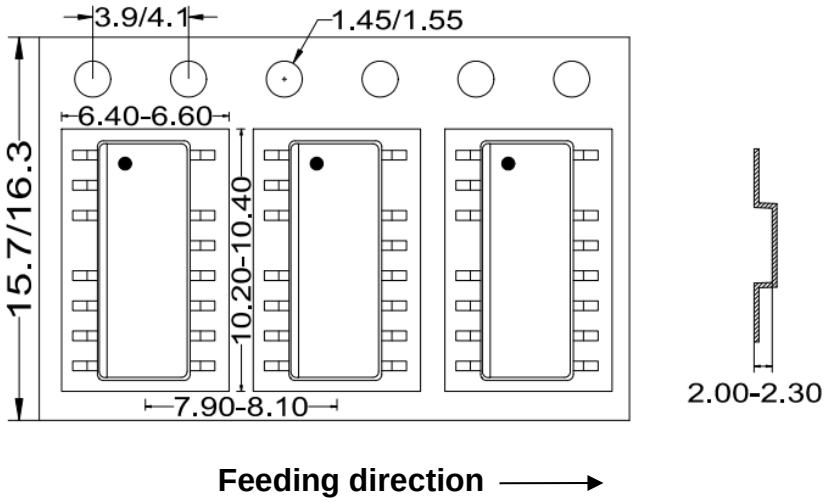


Recommended Pad Layout (Reference Only)

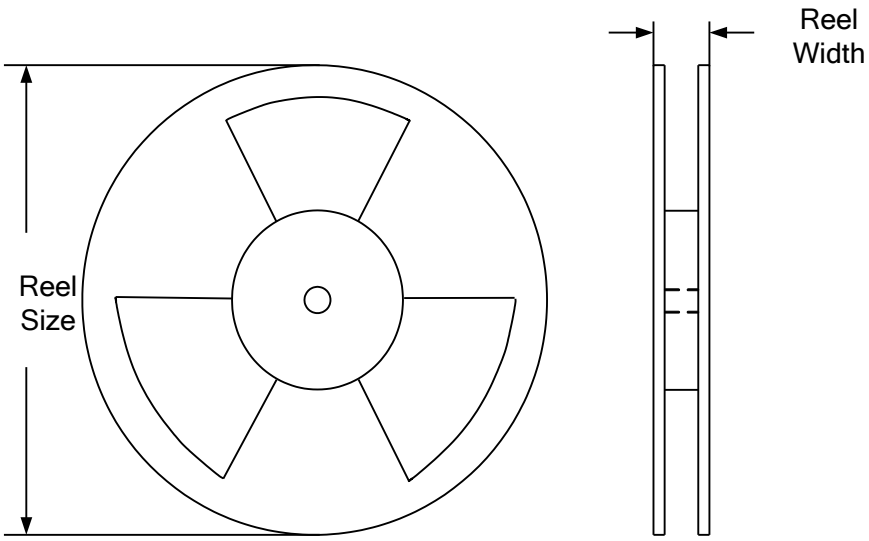
Notes: All dimensions are in millimeters and exclude mold flash and metal burr.

Tape and Reel Specification

Tape dimensions (SOP14)



Reel dimensions



Package types	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Trailer length (mm)	Leader length (mm)	Qty per reel
SOP14	16	8	13"	400	400	2500

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
October 21,2025	Revision 1.0	Initial Release

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