SQ52212

70V, Dual Channel, 16-Bit, Current, Voltage, Power, and Energy Monitor With an I²C Interface

General Description

The SQ52212 is a 2-channel, 16-bit digital current monitor with an I²C/SMBus-compatible interface, supporting digital bus voltages from 1.2 V to 5.5 V. It measures the voltage across an external sense resistor and reports values for shunt voltage, bus voltage, current, power, and energy on each channel.

The SQ52212 offers programmable ADC conversion times and averaging, applied uniformly across all channels. Each channel has a programmable calibration value and an internal multiplier, enabling direct readout of current in amperes, power in watts, and energy in joules. It also monitors the bus voltage at the VBUS pin and can trigger alerts for overcurrent, undercurrent, overvoltage, undervoltage, and overpower conditions. With high input impedance in current measurement mode, the device supports the use of larger current sense resistors, which are necessary for measuring low system currents.

The SQ52212 operates with common-mode bus voltages ranging from 0V to 70V, independent of supply voltage. It runs on a single supply voltage of 2.7 V to 5.5 V, with a typical supply current of 335μA during normal operation. The device can be placed in a low-power standby mode, reducing the typical operating current to 6 μA, and can be fully disabled via the enable pin, resulting in a supply current of less than 50 nA. The device is specified for an operating temperature range of –40°C to 125°C and supports up to 16 programmable addresses.

Features

- High-side or low-side current sensing
- Operates from a 2.7 V to 5.5 V power supply
- Reports current, voltage, power, and energy
- Programmable Vshunt full scale range: 20.48 mV / 81.92 mV
- Programmable Vbus full scale range:52.42 V / 78.64 V
- Input common mode range: -0.3V to 70V
- Current monitoring accuracy:
  - 16-bit ADC resolution
  - 0.25% gain error (maximum)
  - 10 μV offset (maximum)
- Power monitoring accuracy:
  - 0.7% full scale (maximum)
- Energy monitoring accuracy:
  - 1.2% full scale (maximum)
- Low input bias currents: 5 nA (maximum)
- Low disable current: 50 nA (maximum)
- Configurable averaging options
- Alert limits for over and under current events
- 1.2V compliant I²C, SMBus interface
- 16-pin selectable addresses
- CSP1.51×1.51-16

Applications

- Notebook computers
- Security cameras
- Retail automation
- Power management
- Battery cell monitors and balancers
- Rack servers
- eFuse current and power monitoring

Typical Application

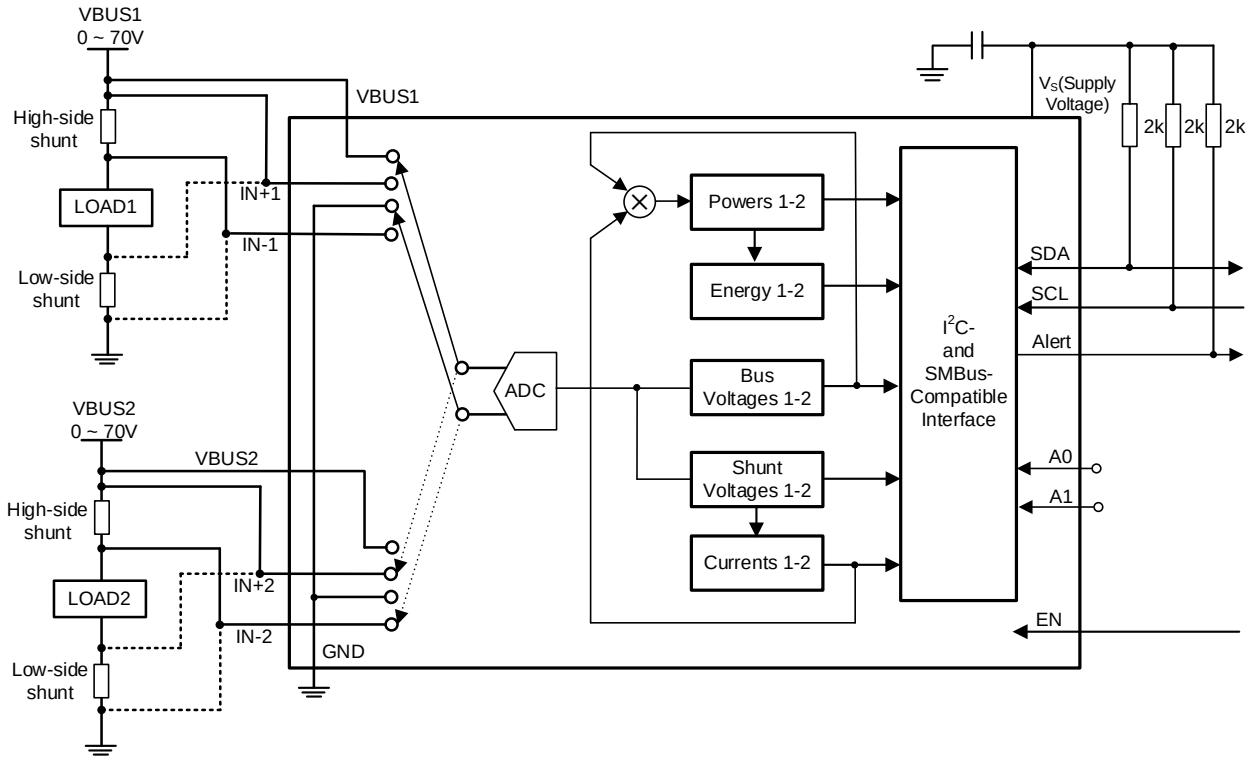


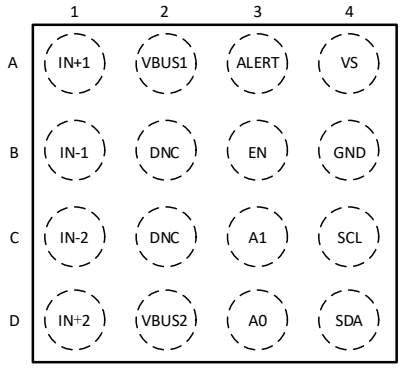
Figure 1. Typical Application Circuit

Ordering Information

Ordering Number	Package Type	Top Mark
SQ52212XFS	CSP1.51×1.51-16	**LFP*xyz***

x=year code, y=week code, z= lot number code.

Pinout (Top View)



CSP1.51×1.51-16

Pin Description

Pin Num.	Pin Name	I/O	Pin Description
A0	D3	Digital input	Address pin. Connect to GND, SCL, SDA, or VS. Table 1 lists the pin settings and corresponding addresses.
A1	C3	Digital input	Address pin. Connect to GND, SCL, SDA, or VS. Table 1 lists the pin settings and corresponding addresses.
ALERT	A3	Digital output	Multifunctional alert, open-drain output. This pin alerts to report fault conditions or can be configured to notify host when a conversion is complete.
EN	B3	Digital input	Enable pin. A logic high level enables the device; a logic low level disables the device.
GND	B4	Ground	Ground for both analog and digital.
IN-1	B1	Analog input	Channel 1 current sensing negative input. For high-side applications, connect to load side of sense resistor. For low-side applications, connect to ground side of sense resistor.
IN+1	A1	Analog input	Channel 1 current sensing positive input. For high-side applications, connect to bus voltage side of sense resistor. For low-side applications, connect to load side of sense resistor.
VBUS1	A2	Analog input	Channel 1 bus voltage input.
IN-2	C1	Analog input	Channel 2 current sensing negative input. For high-side applications, connect to load side of sense resistor. For low-side applications, connect to ground side of sense resistor.
IN+2	D1	Analog input	Channel 2 current sensing positive input. For high-side applications, connect to bus voltage side of sense resistor. For low-side applications, connect to load side of sense resistor.
VBUS2	D2	Analog input	Channel 2 bus voltage input.
SCL	C4	Digital input	I^2C serial bus clock line, open-drain input.
SDA	D4	Digital input/output	I^2C serial bus data line, open-drain input/output.
VS	A4	Power Supply	Power supply, 2.7V to 5.5V.
DNC	B2/C2	-	

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VS	-0.3	6	V
Differential Analog Input (VIN+ – VIN-)	-40	40	
Common Mode	-0.3	72	
VBUS	-0.3	72	
VSDA/VSCL/VA0/VA1	-0.3	6	
Input Current into Any Pin	-5	+5	mA
Open-Drain Digital Output Current	-10	+10	mA
Junction Temperature, Operating	-40	150	°C
Storage Temperature	-65	150	
ESD: HBM (Human Body Model)	± 2000		V
ESD: CDM (Charged Device Model)	± 1000		V

Thermal Information

Parameter (Note 2)	Value	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	38	°C/W
$\theta_{JC\text{-}TOP}$ Junction-to-Case (Top) Thermal Resistance	18	
$\theta_{JC\text{-}BOTTOM}$ Junction-to-Case (Bottom) Thermal Resistance	2	
θ_{JB} Junction-to-Case (Bottom) Thermal Resistance	3.4	
ψ_{JT} Junction-to-Top Characterization Parameter	1.4	
ψ_{JB} Junction-to- Board Characterization Parameter	2.8	
P_D Power Dissipation T_A = 25°C	2.63	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VS	2.7	5.5	V
Common Mode Analog Input	-0.3	70	V
Operating Ambient Temperature Range	-40	125	°C

Electrical Characteristics

At T_A = 25 °C, V_S = 3.3 V, V_{SENSE} = V_{IN+} – V_{IN-} = 0 V, V_{BUS} = V_{IN-} = 12 V (unless otherwise noted). (Note 4)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input						
Common-Mode Input Range	V_{CM}	T_A = -40°C to +125°C	-0.3		70	V
Bus Voltage Input Range	V_{BUS}		-0.3		70	V
Common-Mode Rejection	CMRR	0 V < V_{CM} < 70V, T_A = -40°C to +125°C	130	150		dB
Shunt Voltage Input Range		Vshunt ADCRANGE = 0	-81.9175		81.92	mV
		Vshunt ADCRANGE = 1	-20.4794		20.48	mV
Bus Voltage Input Range		Vbus ADCRANGE = 0	0		52.4	V
		Vbus ADCRANGE = 1	0		70	V
Shunt Offset Voltage	V_{OS}	V_{CM} = 12V		±2	±10	μV
Shunt Offset Voltage Drift	dV_{OS}/dT	T_A = -40°C to +125°C		±20	±100	nV/°C
Shunt Offset Voltage vs Power Supply	$PSRR_{SH}$	V_S = 2.7V to 5.5V		±0.5		μV/V
V_{BUS} Offset Voltage	V_{OS_BUS}			±1	±20	mV
V_{BUS} Offset Voltage Drift	dV_{OS}/dT	T_A = -40°C to +125°C		±10	±40	μV/°C
V_{BUS} Offset Voltage vs Power Supply	$PSRR_{BUS}$	V_S = 2.7V to 5.5V		±1		mV/V
Input Bias Current	I_B	IN+, IN-, Current Measurement Mode		0.1	5	nA
VBUS Pin Input Impedance	Z_{VBUS}	Bus Voltage Measurement Mode		1		MΩ
Input differential impedance	R_{DIFF}	V_{IN+} - V_{IN-} < 82mV		140		kΩ
DC Accuracy						
Shunt Voltage Gain Error	G_{SERR}			±0.02	±0.25	%
Shunt Voltage Gain Error Drift	G_{S_DRFT}	T_A = -40°C to +125°C			40	ppm/°C
V_{BUS} Voltage Gain Error	G_{BERR}			±0.02	±0.35	%
V_{BUS} Voltage Gain Error Drift	G_{B_DRFT}	T_A = -40°C to +125°C			40	ppm/°C
Power Total Measurement Error (TME)	P_{TME}	At full scale voltage and current		±0.04	±0.7	%
Energy Total Measurement Error (TME)	E_{TME}	At full scale voltage and current		±0.3	±1.2	%
ADC Resolution				16		Bits
1 LSB Step Size		Shunt Voltage, Vshunt ADCRANGE = 0		2.5		μV
		Shunt Voltage, Vshunt ADCRANGE = 1		625		nV
		Bus Voltage, Vbus ADCRANGE = 0		1.6		mV
		Bus Voltage, Vbus ADCRANGE = 1		2.4		mV
ADC Conversion Time	t_{CT}	CT bit = 000		140		μs
		CT bit = 001		204		μs
		CT bit = 010		332		μs
		CT bit = 011		588		μs
		CT bit = 100		1.100		ms
		CT bit = 101		2.116		ms
		CT bit = 110		4.156		ms
		CT bit = 111		8.244		ms

Integral Non-Linearity	INL	Vshunt ADCRANGE = 0, Linear best fit.		±2	±10	m%
Differential Non-Linearity	DNL			±0.2		LSB
Clock Source						
Internal Oscillator Frequency	f_{OSC}			500		kHz
Internal Oscillator Frequency Tolerance	f_{OSC_TOL}	T_A = 25°C			±0.5	%
		T_A = -40°C to +125°C			±1	%
Enable						
Input leakage current	I_{EN}	0 V ≤ V_{EN} ≤ V_S		1	50	nA
Logic input level, high	V_{IH}	V_S = 2.7V to 5.5V, T_A = -40°C to +125°C	1.4		5.5	V
Logic input level, low	V_{IL}	V_S = 2.7V to 5.5V, T_A = -40°C to +125°C	0		0.4	V
Hysteresis	V_{HYS}			250		mV
Power Supply						
Operating Supply Range			2.7		5.5	V
Quiescent Current	I_Q			335	370	µA
		I_Q vs temperature, TA = -40°C to +125°C			500	µA
Quiescent Current, Shutdown	I_{QSD}	Shutdown mode		6	10	µA
Quiescent current disabled	I_Q	V_{EN} = 0V		5	50	nA
Power-on reset threshold	V_{PON}	V_S falling		2.2		V
Digital Input / Output						
Logic Input Level, High	V_{IH}	V_S = 2.7V to 5.5V, T_A = -40°C to +125°C	0.9		5.5	V
Logic Input Level, Low	V_{IL}	V_S = 2.7V to 5.5V, T_A = -40°C to +125°C	0		0.4	V
Logic Output Level, Low	V_{OL}	I_{OL} = 3mA, V_S = 2.7V to 5.5V, T_A = -40°C to +125°C	0		0.3	V
Hysteresis voltage	V_{hys}			130		mV
Digital Leakage Input Current	I_{IO_LEAK}	0 V ≤ V_{SCL} ≤ V_S, 0 V ≤ V_{SDA} ≤ V_S		0.1	1	µA
Address Pin Input Current	I_{addr}	V_{A0} = V_S, V_{A1} = V_S		15		µA
I²C BUS (Fast Mode)						
I²C clock frequency	$F_{(SCL)}$		1		400	kHz
Bus-free time between STOP and START conditions	$t_{(BUF)}$		600			ns
Hold time following a repeated START condition. After this time, the first clock pulse is generated.	$t_{(HDSTA)}$		100			ns
Repeated START condition setup time	$t_{(SUSTA)}$		100			ns
STOP condition setup time	$t_{(SUSTO)}$		100			ns
Data hold time	$t_{(HDDAT)}$		10		900	ns
Data setup time	$t_{(SUDAT)}$		100			ns
SCL clock low period	$t_{(LOW)}$		1300			ns
SCL clock high period	$t_{(HIGH)}$		600			ns
Data fall time	t_F				300	ns
Clock fall time	t_F				300	ns
Clock rise time	t_R				300	ns
I²C BUS (High-Speed Mode)						

I²C clock frequency	$F_{(SCL)}$		1		3400	kHz
Bus-free time between STOP and START conditions	$t_{(BUF)}$		160			ns
Hold time following a repeated START condition. After this time, the first clock is generated.	$t_{(HDSTA)}$		100			ns
Repeated START condition setup time	$t_{(SUSTA)}$		100			ns
STOP condition setup time	$t_{(SUSTO)}$		100			ns
Data hold time	$t_{(HDDAT)}$		10		125	ns
Data setup time	$t_{(SUDAT)}$		20			ns
SCL clock low period	$t_{(LOW)}$		200			ns
SCL clock high period	$t_{(HIGH)}$		60			ns
Data fall time	t_F				80	ns
Clock fall time	t_F				40	ns
Clock rise time	t_R				40	ns

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured under still air and chip mounted on high effective four layer test board with thermal via in accordance with JESD51-2,7,-14.

Note 3: The device is not guaranteed to function outside its recommended operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A = T_J = 25°C$. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Timing Diagram

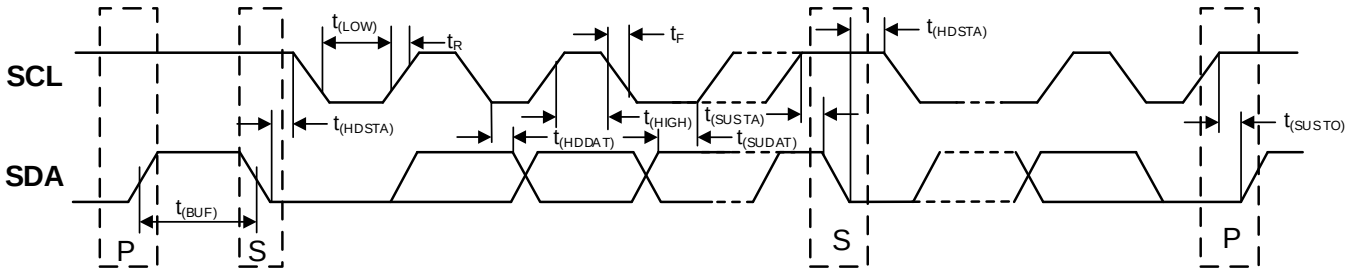


Figure 2. I²C Timing Diagram

Detailed Description

Overview

The SQ52212 is a 2-channel digital current-sense amplifier featuring an I²C- and SMBus-compatible interface. It provides real-time measurements of current, voltage, power, and energy for each channel. The device includes programmable out-of-range limits, enabling alert notifications when monitored parameters exceed the predefined operational thresholds. The integrated analog-to-digital converter (ADC) offers multiple averaging modes and can be configured for either continuous or triggered operation. Comprehensive register information for the SQ52212 is available in the Register Maps section.

Block Diagram

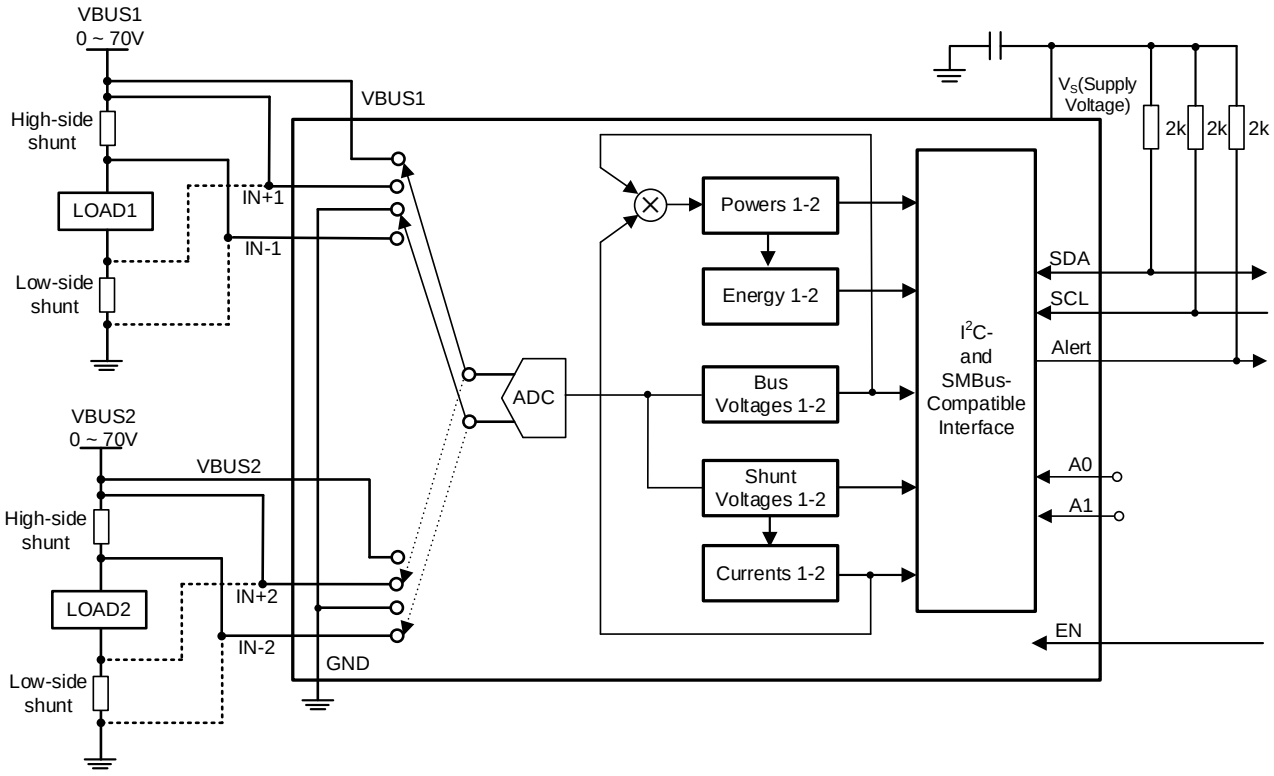


Figure 3. Functional Block Diagram

Feature Description

Integrated Analog-to-Digital Converter (ADC)

The SQ52212 integrates a low-offset, 16-bit delta-sigma (ΔΣ) ADC, which is multiplexed for each channel to measure both shunt and bus voltages. Bus voltage measurements are referenced to the BUS and GND, while the shunt voltage is measured differentially across the IN+ and IN– pins for each channel, capturing the voltage developed by the load current flowing through a shunt resistor. The shunt voltage measurement offers a maximum offset voltage of just 10μV and a maximum gain error of 0.25%. The low offset voltage enhances measurement accuracy under light load conditions for a given shunt resistor value. This also enables the accurate sensing of lower voltage drops across the sense resistor, allowing the use of lower-value shunt resistors. These lower-value shunt resistors help minimize power loss in the current-sensing circuit, thereby improving the overall power efficiency of the end application.

No special power-supply sequencing is required, as the common-mode voltage at the IN+ and IN- pins and the power-supply voltage at the VS pin are independent. As a result, the bus common-mode voltage can be present even when the supply voltage is off.

Internal Measurement and Calculation Engine

The internal round-robin measurement scheme for the SQ52212 is illustrated in Figure 4. For each channel, the current, power, and energy registers are calculated based on the shunt and bus voltage measurements, and these calculations are

not directly influenced by ADC conversion times. Register values are updated for each channel before proceeding to the next one. When averaging is enabled, the register updates occur once the specified number of averages is completed. Fault conditions are evaluated immediately after conversions or calculations, based on the ADC conversion time, and are independent of the averaging settings.

Reducing conversion times leads to faster alert responses, but at the cost of lower effective resolution due to increased noise. Longer conversion times result in slower alert responses but provide greater immunity to noise. Channels or measurements that are disabled are skipped in the round-robin cycle. The conversion-ready flag is set once the conversions are complete and the selected number of averages has been reached.

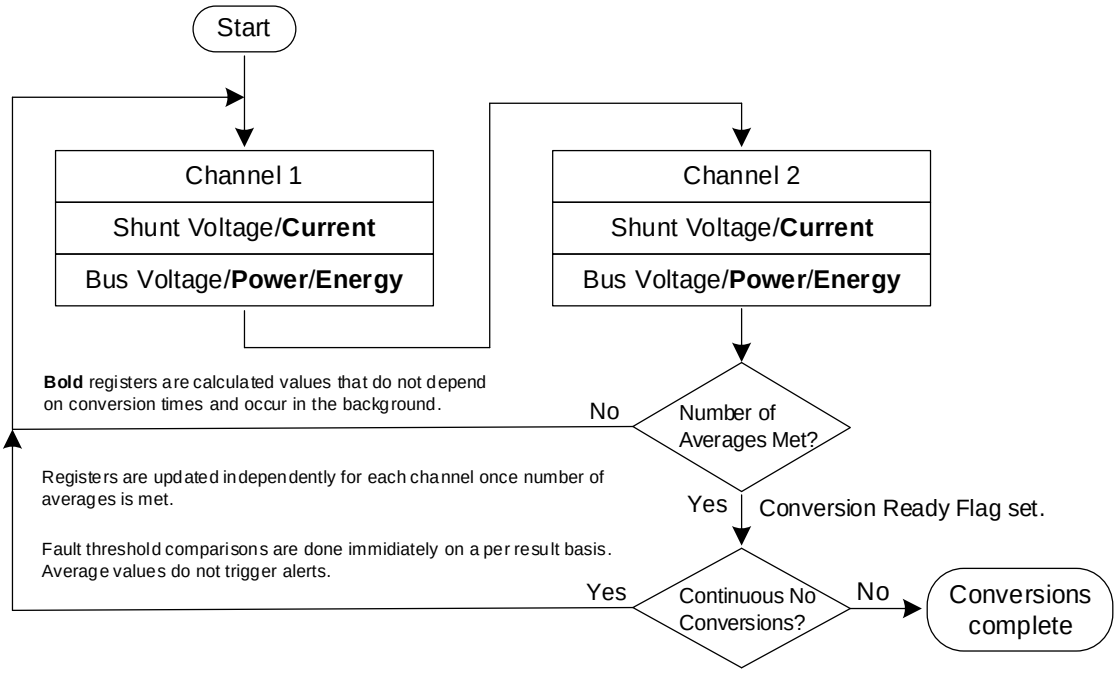


Figure 4. Internal Measurement and Calculation Scheme

The current is determined from the shunt voltage measurements and the value stored in the corresponding calibration register. Power is then calculated based on the previously determined current and the most recent bus voltage measurement. Energy is accumulated by multiplying the previously calculated power by the current time-base interval and adding this value to the total energy. If the value in the corresponding calibration register is zero, the reported current, power, and energy values will also be zero. When averaging is enabled, register values are updated once the specified number of averages has been reached. These calculations are performed in the background and do not impact the overall conversion time.

Low Bias Current

The SQ52212 offers several advantages due to its very low input bias current when performing current measurements. One key benefit is the reduction in current consumption by the device, both in active and shutdown states. Additionally, the low input bias current enables the use of input filters that can effectively reject high-frequency noise before the signal is converted to digital data. In traditional digital current-sense monitors, adding input filters typically compromises accuracy. However, with the SQ52212's low bias current, the impact on accuracy from the use of these filters is minimized. Another advantage is the ability to use a larger shunt resistor, which allows for accurate measurement of smaller currents. This makes it possible for the device to monitor currents in the sub-milliampere range with high precision. The bias current in the SQ52212 is at its lowest when the sensed current is zero. As the current increases, the voltage drop across the shunt resistor also rises, which leads to an increase in the bias current.

Low Voltage Supply and Wide Common-Mode Voltage Range

The SQ52212 operates within a supply voltage range of 2.7V to 5.5V. Despite a minimum supply voltage of 2.7V, the device is capable of monitoring currents on voltage rails as high as 70V. This wide common-mode voltage range enables the SQ52212 to be used in a variety of applications where the common-mode voltage exceeds the supply voltage.

ALERT Pin

The SQ52212 features two Alert Configuration Registers, each of which can be assigned to one of the two channels as needed. Each register includes a channel assignment field and an alert mask field. The alert mask field allows users to select one of five available functions for the alert response. Depending on the monitored function, a corresponding value can be set in the Alert Limit Registers to define the threshold that triggers the ALERT pin.

The ALERT pin is used to monitor one of several alert functions and detect when a user-defined threshold is exceeded. The five available alert functions are:

- Shunt voltage overlimit (SOL)
- Shunt voltage underlimit (SUL)
- Bus voltage overlimit (BOL)
- Bus voltage underlimit (BUL)
- Power overlimit (POL)

The ALERT pin is an open-drain output that is asserted when the alert function selected in the Alert Configuration registers exceeds the threshold programmed in the Alert Limit register. Up to two alert functions can be enabled and monitored simultaneously.

In addition to monitoring alert functions, the ALERT pin can also signal the device's conversion-ready state, indicating when the previous conversion is complete and the device is ready for a new conversion. The Conversion Ready Flag (CVRF) bit can be monitored on the ALERT pin, alongside one of the alert functions.

If no alert function is in use, the ALERT pin can be left floating without affecting the operation of the device.

The alert function compares the programmed alert limit to the result of each corresponding conversion. As a result, an alert can be triggered during a conversion cycle, even if the averaged signal value does not exceed the alert limit. By issuing an alert based on this intermediate conversion, out-of-range events can be detected more quickly than the averaged output data registers are updated. This fast detection enables the creation of alert limits for rapidly changing conditions using the alert function, while also allowing for limits on longer-duration conditions through software monitoring of the averaged output values.

Device Functional Modes

Continuous Versus Triggered Operation

The SQ52212 operates in three modes: continuous and triggered. These modes determine how the ADC functions after completing conversions.

In continuous mode, which is the default operating mode (when the MODE bits of the CONFIG1 register are set to '111'), the device continuously converts a shunt voltage reading followed by a bus voltage reading for each channel.

In triggered mode, selecting any of the triggered conversion modes (i.e., setting the MODE bits of the CONFIG1 register to '001', '010', or '011') initiates a single-shot conversion of the chosen parameters. This results in one set of measurements. To trigger another single-shot conversion, the Configuration register must be written to again, even if the mode remains unchanged.

Although the SQ52212 can be read at any time, and data from the last conversion remains available, the Conversion Ready Flag (CVRF bit) in the FLAGS register helps coordinate single-shot or triggered conversions. The CVRF bit is set after all conversions, averaging, and multiplication operations are completed for a single round-robin cycle.

The CVRF bit is cleared under the following conditions:

- Writing to the CONFIG1 register, unless the MODE bits are configured for power-down mode;
- Reading the FLAGS register.

Device Low Power Modes

In addition to the two operating modes (continuous and triggered), the SQ52212 also has two low power modes. In shutdown the device reduces the quiescent current and input bias current but is able to process I^2C bus communications. In this state the quiescent current is reduced to less than 4μA. Full recovery from shut-down mode requires 40μs. The device remains in shut-down mode until one of the active modes settings are written into the Configuration register. An even lower power mode is the disabled mode, which is initiated by forcing a logic low on the enable pin. In this mode the quiescent current is the lowest, with the device only drawing 50nA (max) of supply current, but the device does not recognize any I^2C bus

communications in this state. Also the device configuration gets reset when in the disabled state and needs to be reprogrammed when enabled. Recovery from the disabled state requires 100µs.

Power-On Reset

The Power-On Reset (POR) is asserted when the supply voltage (VS) drops below 2.2V (typical). At this point, all registers are reset to their default values. The default power-up values for each register are listed in the reset column of the register descriptions.

Averaging and Conversion Time Considerations

The SQ52212 offers programmable conversion times for both shunt voltage and bus voltage measurements, applicable across all channels. These conversion times can be selected from as fast as 140µs to as long as 8.244ms. With these configurable conversion times, along with the programmable averaging mode, the SQ52212 can be tailored to meet the timing requirements of specific applications. Additionally, the SQ52212 allows for different conversion time settings for shunt and bus voltage measurements, which is particularly useful in applications where the bus voltage is relatively stable. In such cases, the measurement time for the bus voltage can be reduced compared to the shunt voltage measurement.

There are trade-offs to consider when configuring the conversion times and averaging mode. The averaging feature significantly enhances measurement accuracy by filtering out noise, improving the quality of the signal. A higher number of averages further reduces noise, resulting in more accurate measurements.

The selected conversion times also impact measurement accuracy. For the highest possible accuracy, it is recommended to use the longest allowable conversion times combined with the maximum number of averages, depending on the system's timing requirements.

Programming

I²C Serial Interface

The SQ52212 offers compatibility with both I²C and SMBus interfaces. The I²C and SMBus protocols are essentially compatible with one another.

The I²C interface is used throughout this data sheet as the primary example, with the SMBus protocol specified only when a difference between the two systems is discussed. Two I/O lines, the serial clock (SCL) and data signal line (SDA), connect the SQ52212 to the bus. Both SCL and SDA are open-drain connections.

The device that initiates a data transfer is called a master, and the devices controlled by the master are slaves. The bus must be controlled by the master device that generates the SCL, controls the bus access, and generates start and stop conditions.

To address a specific device, the master initiates a start condition by pulling SDA from a high to a low logic level while SCL is high. All slaves on the bus shift in the slave address byte on the SCL rising edge, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an acknowledge bit and pulling SDA low.

Data transfer is then initiated and eight bits of data are sent, followed by an acknowledge bit. During data transfer, SDA must remain stable while SCL is high. Any change in SDA while SCL is high is interpreted as a start or stop condition.

After all data are transferred, the master generates a stop condition by pulling SDA from low to high while SCL is high. The SQ52212 includes a 28-ms timeout on the interface to prevent locking up the bus.

Serial Bus Address

To communicate with the SQ52212, the master must first address slave devices with a slave address byte. This byte consists of seven address bits and a direction bit to indicate whether the intended action is a read or write operation.

The SQ52212 has two address pins, A0 and A1. Table 1 describes the pin logic levels for each of the four possible addresses. The state of the A0 and A1 pin is sampled on every bus communication and must be set before any activity on the interface occurs.

Table 1 Address Pins and Secondary Device Addresses

A1	A0	TARGET ADDRESS
GND	GND	1000000
GND	VS	1000001

GND	SDA	1000010
GND	SCL	1000011
VS	GND	1000100
VS	VS	1000101
VS	SDA	1000110
VS	SCL	1000111
SDA	GND	1001000
SDA	VS	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	VS	1001101
SCL	SDA	1001110
SCL	SCL	1001111

Serial Interface

The SQ52212 only operates as a slave device on the I^2C bus and SMBus. Bus connections are made using the open-drain I/O lines, SDA and SCL. The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. While there is spike suppression integrated into the digital I/O lines, use proper layout to minimize the amount of coupling into the communication lines. Noise introduction occurs from capacitively coupling signal edges between the two communication lines themselves, or from other switching noise sources present in the system. Routing traces in parallel with ground between layers on a printed circuit board (PCB) typically reduces the effects of coupling between the communication lines. Shield communication lines to reduce the possibility of unintended noise coupling into the digital I/O lines that could be incorrectly interpreted as start or stop commands.

The SQ52212 supports a transmission protocol for Fast (1 kHz to 400 kHz) and High-speed (1 kHz to 3.4 MHz) modes. All data bytes are transmitted MSB first.

Writing To and Reading From the SQ52212

To access a specific SQ52212 register, write the appropriate value to the register pointer. See Table 1 for a complete list of registers and corresponding addresses. The value for the register pointer, as shown in Figure 5 is the first byte transferred after the slave address byte with the R/W bit low. Every write operation to the SQ52212 requires a register pointer value.

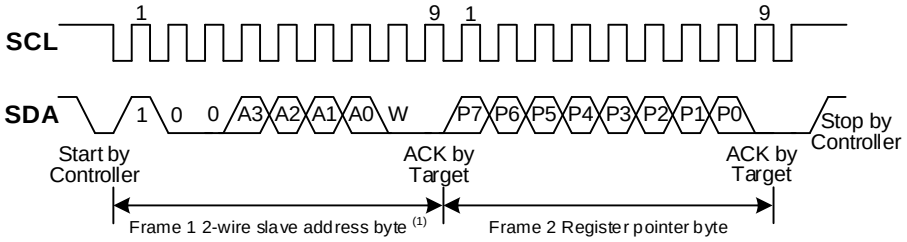


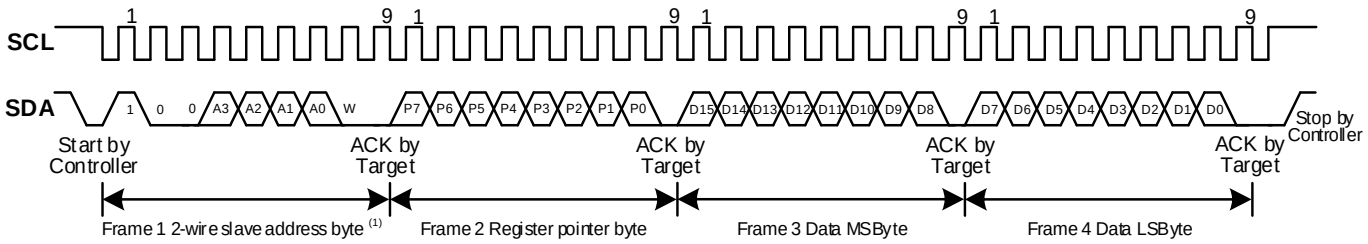
Figure 5. Typical Register Pointer Set

Register writes begin with the first byte transmitted by the master. This byte is the slave address, with the R/W bit low. The SQ52212 then acknowledges receipt of a valid address. The next byte transmitted by the master is the register address that data are written to. This register address value updates the register pointer to the desired register. The next two bytes are written to the register addressed by the register pointer. The SQ52212 acknowledges receipt of each data byte. The master terminates data transfer by generating a start or stop condition.

When reading from the SQ52212, the last value stored in the register pointer by a write operation determines which register is read during a read operation. To change the register pointer for a read operation, write a new value to the register pointer. This write is accomplished by issuing a slave address byte with the R/W bit low, followed by the register pointer byte. No additional data are required. The master then generates a start condition and sends the slave address byte with the R/W bit high to initiate the read command. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the register pointer. This byte is followed by an acknowledge from the master; then the slave transmits the least

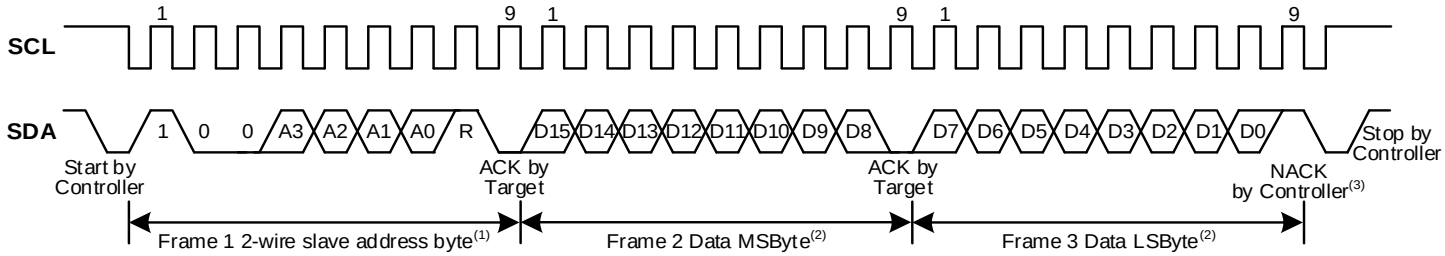
significant byte. The master acknowledges receipt of the data byte. The master terminates data transfer by generating a not-acknowledge after receiving any data byte, or generating a start or stop condition. If repeated reads from the same register are desired, it is not necessary to continually send the register pointer bytes; the SQ52212 retains the register pointer value until it is changed by the next write operation.

Figure 6 and Figure 7 show the write and read operation timing diagrams, respectively. Note that register bytes are sent most-significant byte first, followed by the least significant byte.



1. The value of the Secondary Device Address byte is determined by the settings of the A0 and A1 pins. Refer to Table 1.

Figure 6 Timing Diagram for Write Word Format



1. The value of the Secondary Device Address byte is determined by the settings of the A0 and A1 pins. Refer to Table 1.

2. Read data is from the last register pointer location. If a new register is desired, the register pointer must be updated. See Table 1

3. ACK by the main device can also be sent.

Figure 7 Timing Diagram for Read Word Format

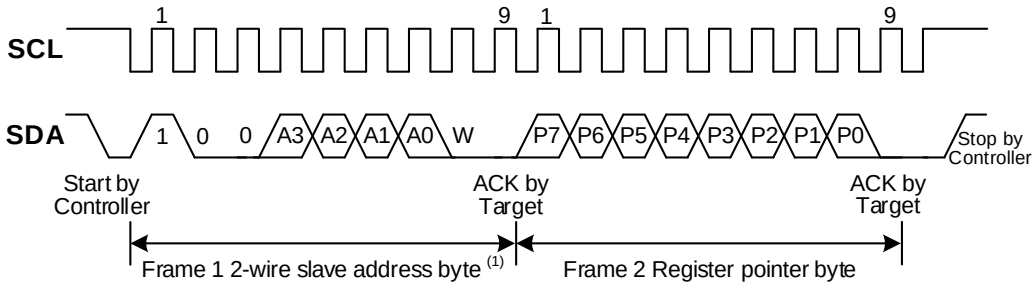


Figure 8 Typical Register Pointer Set

High-Speed I²C Mode

When the bus is idle, the SDA and SCL lines are pulled high by the pull-up resistors. The master generates a start condition followed by a valid serial byte with the high-speed (HS) master code 00001XXX. This transmission is made in fast (400 kHz) or standard (100 kHz) (F/S) mode at no more than 400 kHz. The SQ52212 does not acknowledge the Hs master code, but does recognize it and switches its internal filters to support 3.4-MHz operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 3.4 MHz are allowed. Instead of using a stop condition, the master uses a repeated start conditions to secure the bus in Hs mode. A stop condition ends the HS mode, and switches all internal SQ52212 filters to support F/S mode.

General Call Reset

A general call reset for multiple devices is triggered by addressing the general call address (0000 000) with the last R/W bit set to 0, followed by the data byte 0000 0110 (06h).

Upon receiving this 2-byte sequence, all devices configured to respond to the general call address are reset. All SQ52212 devices on the bus will perform a soft reset and return to their default power-up conditions.

SMBus Alert Response

The SQ52212 is designed to respond to the SMBus Alert Response address, which provides quick fault identification for simple targets. When an Alert occurs, the controller broadcasts the Alert Response target address (0001 100) with the Read/Write bit set high. After this Alert Response, any target that generates an alert acknowledges the response and sends its address on the bus.

The Alert Response can activate multiple target devices simultaneously, similar to the I^2C General Call. If more than one target attempts to respond, bus arbitration rules are applied. The device that is not prioritized during arbitration will not generate an acknowledge. It will continue to hold the Alert line low until it is prioritized through the arbitration process.

Register Map

Device Registers

Table 2 lists the SQ52212 registers. All register locations not listed in the table are considered as reserved locations and the register contents must not be modified.

Table 2 Registers Map

Address	Register Name	Reset Value	Size (bits)	Register Type
0x10	CONFIG1	3127h	16	R/W
0x11	CONFIG2	0000h	16	R/W
0x05, 0x0D	CALIBRATION (CH1 - CH2)	0000h	16	R/W
0x07, 0x0F	ALERT_CONFIG (1 - 2)	0000h	16	R/W
0x06, 0x0E	ALERT_LIMIT (1 - 2)	0000h	16	R/W
0x00, 0x08	SHUNT_VOLTAGE_(CH1 - CH2)	0000h	16	R
0x01, 0x09	BUS_VOLTAGE_(CH1 - CH2)	0000h	16	R
0x02, 0x0A	CURRENT_(CH1 - CH2)	0000h	16	R
0x03, 0x0B	POWER_(CH1 - Ch2)	0000h	16	R
0x04, 0x0C	ENERGY_(CH1 - CH2)	0000h	32	R
0x12	FLAGS	0000h	16	R
0x20	CONFIG3	0000h	16	R/W
0x7E	MANUFACTURER_ID	190Fh	16	R
0x7F	DEVICE_ID	2120h	16	R

CONFIG1 Register (Address = 10h) [reset = 3127h]

The configuration register is shown in Table 3.

Table 3. CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	Reserved	R	00b	Reserved
13-12	ACTIVE_CHANNEL	R/W	11b	These 2 bits determine which channels are active. Set this bit to '1' to enable each channel. Disabled channels are skipped in the round robin cycle. Bit13 = Channel 2 measurement enable/disable.

				Bit12 = Channel 1 measurement enable/disable. Power up default: 11b = All channels active.
11-9	AVG2-0	R/W	000b	Averaging mode. These bits set the number of samples that are collected and averaged together. 000 = 1 (default) 001 = 4 010 = 16 011 = 64 100 = 128 101 = 256 110 = 512 111 = 1024
8-6	VBUSCT2-0	R/W	100b	Bus-voltage conversion time. These bits set the conversion time for the bus-voltage measurement. 000 = 140 μs 001 = 204 μs 010 = 332 μs 011 = 588 μs 100 = 1.1 ms (default) 101 = 2.116 ms 110 = 4.156 ms 111 = 8.244 ms
5-3	VSHCT2-0	R/W	100b	Sets the conversion time of the SHUNT measurement. 000b = 140μs 001b = 204μs 010b = 332μs 011b = 588μs 100 = 1.1 ms (default) 101b = 2116μs 110b = 4156μs 111b = 8244μs
2-0	MODE3-1	R/W	111b	Operating mode. These bits select continuous, single-shot (triggered), power-down mode or low power mode of operation. These bits default to continuous shunt and bus mode. 000 = Power-down 001 = Shunt voltage, single-shot (triggered) 010 = Bus voltage, single-shot (triggered) 011 = Shunt and bus, single-shot (triggered) 100 = Power-down 101 = Shunt voltage, continuous 110 = Bus voltage, continuous 111 = Shunt and bus, continuous (default)

CONFIG2 Register (address = 11h) [reset = 0000h]

The configuration register is shown in Table 4.

Table 4 CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RST	R/W	0b	Set this bit to '1' to generate a system reset that is the same as power- on reset. Resets all registers to default values and then self-clears.
14-10	Reserved	R	000b	These bits always read 0.
9-8	ACC_RST	R/W	0000b	Writing a one to these bits resets the energy registers and clears any overflow flags. Bit9 = Channel 2 energy reset, overflow clear.

				Bit8 = Channel 1 energy reset, overflow clear. Power up default: 00b = All channels active. Bits are reset back to 0 after write.
7	CNVR_MASK	R/W	0b	Setting this bit high configures the ALERT pin to be asserted when conversions are complete. 0b = Disable conversion ready flag on ALERT pin. 1b = Enables conversion ready flag on ALERT pin. ALERT remains asserted until the CVRF field in the flags register is read.
6	ENOF_MASK	R/W	0b	When set to 1, the Alert pin toggles when an energy overflow condition occurs on any of the enabled channels.
5	ALERT_LATCH	R/W	0b	When set to 1 the state of the Alert pin latches during fault conditions. To clear the alert the alert flags register must be read and the fault condition removed.
4	ALERT_POL	R/W	0b	When this bit is set to 1, the alert pin toggles from low to high during a fault condition. When set to 0 (default), the alert pin toggles from high to low during faults.
3-2	Reserved	R	00b	These bits always read 0.
1-0	Vshunt RANGE	R/W	00b	Enables the selection of the shunt full scale input range for each channel. Bit1 = Channel 2 range selection. Bit0 = Channel 1 range selection. range selection bit = 0 selects ±81.92mV. range selection bit = 1 selects ±20.48mV. 00b = all channels set to ±81.92mV range.

CALIBRATION Registers (address = 05h, 0Dh) [reset = 0000h]

The calibration registers shown in Table 5 must be programmed to receive valid current, power, and energy results after initial power up, power cycle events, or on device enable.

Table 5 Calibration Registers

Address	Register Name	Register Type	Register Size (bits)
0x05	CALIBRATION_CH1	R/W	16
0x0D	CALIBRATION_CH2	R/W	16

This register provides the device with the value of the shunt resistor that are present to create the measured differential voltage. This register also sets the resolution of the Current Register. Programming this register sets the Current_LSB and the Power_LSB.

Table 6 Calibration Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	
14-0	SHUNT_CAL	R/W	0000h	Programmed value needed for doing the shunt voltage to current conversion.

Alert Configuration Registers (address = 07h, 0Fh) [reset = 0000h]

The alert configuration registers are shown in Table 7.

Table 7 ALERT_CONFIG Registers

Address	Register Name	Register Type	Register Size (bits)
0x07	ALERT1	R/W	16
0x0F	ALERT2	R/W	16

The format of each alert configuration register is shown in Table 8.

These registers configure what triggers an alert for each of the channels. The alert mask field sets the active alert. Up to 2 alerts can be assigned to a given channel or spread equally across all channels depending on the needs of the application.

Table 8 Alert Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	Reserved	R	000000000000b	Reserved
3	CHANNEL	R/W	0b	Selects 0b = Channel 1 1b = Channel 2
2-0	ALERT_MASK	R/W	000b	Sets the active alert for the assigned channel 000b = reserved, no effect 001b = Shunt Voltage over limit (SOL) 010b = Shunt Voltage under limit (SUL) 011b = Bus Voltage over limit (BOL) 100b = Bus Voltage under limit (BUL) 101b = Power over limit (POL) 110b = reserved, no effect 111b = reserved, no effect

The alert configuration registers set what triggers an alert for each of the channels. The alert mask field sets the active alert. Up to 2 alerts can be assigned to a given channel or spread as required across all channels depending on the application.

Alert Limit Registers (address = 06h, 0Eh) [reset = 0000h]

The alert configuration registers are shown in Table 9.

Table 9 ALERT_LIMIT Registers

Address	Register Name	Register Type	Reset	Register Size (bits)
0x06	LIMIT1	R/W	0000h	16
0x0E	LIMIT2	R/W	0000h	16

The format of the alert limit register follows the format of the corresponding result register.

Shunt voltage limits are represented as signed 16 bit, bus voltage limits are unsigned 15 bit, and power limits are unsigned 16 bit values.

Shunt Voltage Registers (address = 00h, 08h) [reset = 0000h]

The Shunt Voltage Registers store the current shunt voltage reading, VSHUNT. The shunt voltage measurement for each channel has a unique address as shown in Table 10.

Table 10 SHUNT_VOLTAGE Registers

Address	Register Name	Register Type	Register Size (bits)
0x00	SHUNT_VOLTAGE_CH1	R	16
0x08	SHUNT_VOLTAGE_CH2	R	16

The format of each shunt voltage register is shown in Table 11.
If averaging is enabled, these registers contain the averaged shunt voltage value.

Table 11 Shunt Voltage Register Field Description

Bit	Field	Type	Reset	Description
15-0	VSHUNT	R	0000h	Differential voltage measured across the shunt output. 2's complement value.

Negative numbers are represented in two's complement format. Generate the two's complement of a negative number by complementing the absolute value binary number and adding 1. An MSB = '1' denotes a negative number.

Example: For a value of VSHUNT = –80mV:

1. Take the absolute value: 80mV
2. Translate this number to a whole decimal number (80mV ÷ 2.5μV) = 32000
3. Convert this number to binary = 0111 1101 0000 0000
4. Complement the binary result = 1000 0010 1111 1111
5. Add '1' to the complement to create the two's complement result = 1000 0011 0000 0000 = 8300h

Return to the Summary Table.

Bus Voltage Registers (address = 01h, 09h) [reset = 0000h]

The bus voltage registers store the voltage measured at the bus pin for each of the channels. Bus voltage measurements are stored in an unique register addresses as shown in Table 12.

Table 12 BUS_VOLTAGE Registers

Address	Register Name	Register Type	Register Size (bits)
0x01	BUS_VOLTAGE_CH1	R	16
0x09	BUS_VOLTAGE_CH2	R	16

The format of each bus voltage register is shown in Table 13.

The bus voltage registers only return positive values. If averaging is enabled, this register displays the averaged value.

Table 13 Bus Voltage Register Field Description

Bit	Field	Type	Reset	Description
15-0	VBUS	R	0000h	Bus voltage output. 2's complement value, however always positive.

CURRENT Registers (address = 02h, 0Ah) [reset = 0000h]

The current registers store the calculated current value for each of the channels. Current measurements are stored in an unique register addresses as shown in Table 14.

Table 14 Current Registers

Address	Register Name	Register Type	Register Size (bits)
0x02	CURRENT_CH1	R	16
0x0A	CURRENT_CH2	R	16

The format of each current register is shown in Table 15.

If averaging is enabled, this register displays the averaged value. The value of the Current Register is calculated by multiplying the decimal value in the Shunt Voltage Register with the decimal value of the Calibration Register.

Table 15 Current Register Field Description

Bit	Field	Type	Reset	Description
15-0	CURRENT	R	0000h	Calculated current output in Amperes. 2's complement value.

POWER Registers (address = 03h, 0Bh) [reset = 0000h]

The power registers store the multiplied value of the bus voltage and current for each of the channels. Power measurements are stored in an unique register addresses as shown in Table 16

Table 16 Power Registers

Address	Register Name	Register Type	Register Size (bits)
0x03	POWER_CH1	R	16
0x0B	POWER_CH2	R	16

The format of each power register is shown in Table 17.

If averaging is enabled, this register displays the averaged value. The Power Register records power in Watts by multiplying the decimal values of the Current Register with the decimal value of the Bus Voltage Register. This is an unsigned result.

Table 17 Power Register Field Description

Bit	Field	Type	Reset	Description
15-0	POWER	R	0000h	This bit returns a calculated value of power in the system. This is an unsigned result.

Energy Registers (address = 09h) [reset = 0000h]

The energy registers accumulate data from the power registers and with the internal precision timebase calculate and store the energy for each of the channels. Energy measurements are stored in an unique register addresses as shown in Table 18.

Table 18 Energy Registers

Address	Register Name	Register Type	Register Size (bits)
0x04	ENERGY_CH1	R	32
0x0C	ENERGY_CH2	R	32

The format of each energy register is shown in Table 19.
The Energy register records energy in Joules and utilizes the precision oscillator as a timebase. This is an unsigned result.

Table 19 Energy Register Field Description

Bit	Field	Type	Reset	Description
31-0	ENERGY	R	00000000h	This bit returns a calculated value of energy in the system. This is an unsigned result.

Flags Register (address = 12h) [reset = 0000h]

The Flags Register is shown in Table 20.

Table 20 Flags Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	Reserved	R	00b	Reserved, will return 0.
13	LIMIT2_ALERT	R	0b	Indicates the second alert limit has been exceeded. This alert is independent of channel.
12	LIMIT1_ALERT	R	0b	Indicates the first alert limit has been exceeded. This alert is independent of channel.
11-10	Reserved	R	00b	Reserved, will return 0.
9	ENERGYOF_ CH2	R	0b	Indicates an the energy register has overflowed for channel 2
8	ENERGYOF_ CH1	R	0b	Indicates an the energy register has overflowed for channel 1
7	CVRF (Conversion Ready Flag)	R	0b	Although the device can be read at any time, and the data from the last conversion is available, the Conversion Ready Flag bit is provided to help coordinate one-shot or triggered conversions. The Conversion Ready Flag bit is set after all conversions, averaging, and multiplications are complete. Conversion Ready Flag bit clears under the following conditions: 1.) Writing to the Configuration Register (except for Power-Down selection) 2.) Reading the Flags Register

6	OVF (Math Over-flow)	R	0b	This bit is set to '1' if an arithmetic operation results in an overflow error. This bit indicates that current and power data can be invalid.
5-0	Reserved	-	000000b	Reserved

CONFIG3 Register (address = 20h) [reset = 0000h]

The configuration register is shown in Table 21.

Table 21 CONFIG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	Vbus RANGE	R/W	00b	Enables the selection of the bus full scale input range for each channel. Bit15 = Channel 2 range selection. Bit14 = Channel 1 range selection. range selection bit = 0 selects 52.4V range selection bit = 1 selects 78.6V 00b = all channels set to 52.4V range
13-0	Reserved	R	000b	These bits always read 0.

Manufacturer ID Register (address = 7Eh) [reset = 190Fh]

The manufacturer ID register is shown in Table 22.

Table 22 Manufacturer ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MANUFACTURE_ID	R	190Fh	

Die ID Register (address = 7Fh) [reset = 2120h]

The DEVICE_ID register is shown in Table 23.

Table 23 Die ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	DIE_ID	R	0x212	Stores the device identification bits
3-0	REV_ID	R	0h	Device revision identification.

Application and Implementation

The SQ52212 is a multi-channel current shunt monitor with an I²C- and SMBus-compatible interface. The device monitors a shunt voltage drop to calculate the current and bus voltage at IN- pin to determine power and energy for up to two measurement channels. Programmable calibration value, conversion times, and averaging (combined with an internal multiplier) enable direct readouts of current in amperes, power in watts, and energy in joules.

Device Measurement Range and Resolution

The SQ52212 device supports two input ranges for the shunt voltage measurements for each channel. The supported full scale differential input across the IN+ and IN– pins can be either ±81.92mV or ±20.48mV depending on the Vshunt RANGE field in the CONFIG2 Register (address = 11h) [reset = 0000h]. The range for the bus voltage measurement at the VBUS pins is from 0V to 52.42V or 0V to 78.64V depending on the Vbus RANGE field in the CONFIG2 Register (address = 11h) [reset = 0000h], but is limited by process ratings to the maximum operating voltage.

Table 24 provides a description of full scale voltage on shunt and bus voltage measurements, along with the associated resolution.

Table 24 ADC Full Scale Values

Parameter	Full Scale Value	Resolution
Shunt voltage	±81.92mV (Vshunt ADCRANGE = 0)	2.5μV/LSB
	±20.48mV (Vshunt ADCRANGE = 1)	625nV/LSB
Bus voltage	0V to 52.4V (Vbus ADCRANGE = 0)	1.6mV/LSB

	0V-78.6V(Limit usable range to recommended operating voltage) (Vbus ADCRANGE = 1)	2.4mV/LSB

The device shunt voltage and bus voltage measurements are read through the Shunt Voltage registers and Bus Voltage registers, respectively. The digital output in shunt voltage and bus voltage registers is 16 bits. The shunt voltage measurement can be positive or negative due to bidirectional currents in the system; therefore the data value in shunt voltage register can be positive or negative. The bus voltage register data value is always positive. The output data can be directly converted into voltage by multiplying the digital value by the respective resolution size.

Furthermore, the device provides the flexibility to report calculated current in Amperes, power in Watts, energy in Joules, as described in Current, Power and Energy Calculations.

Current, Power and Energy Calculations

In order to report the current and power values properly, several registers should be configured as the steps followed. The following is an example of channel 1. Vshunt ADCRANGE = 0 and Vbus ADCRANGE = 0.

For the SQ52212 to report current values in Amperes, a constant conversion value must be written in each of the calibration registers that is dependent on the selected CURRENT_LSB and the shunt resistance used in the application for each channel. The value of the calibration register is calculated based on Equation 1. The term CURRENT_LSB is the chosen LSB step size for the CURRENT register where the current is stored. Equation 2 shows the minimum value of CURRENT_LSB is based on the maximum expected current, and the equation directly defines the maximum resolution of the CURRENT register. While the smallest CURRENT_LSB value yields highest resolution, this value is common for selecting a higher round-number (no higher than 8x) value for the CURRENT_LSB to simplify the conversion of the CURRENT.

The RSHUNT term is the resistance value of the external shunt used to develop the differential voltage across the IN+ and IN– pins.

$$CAL[R] = \frac{2048 \times Shunt\_LSB}{Current\_LSB \times R_{Shunt}} \quad (1)$$

where

2048 is an internal fixed value used to verify that scaling is maintained properly.

- CURRENT_LSB is a selected value for the current step size in amperes. Must be greater than or equal to CURRENT_LSB (minimum), but less than 8 x CURRENT_LSB(minimum) to reduce resolution loss.
- The value of Shunt_LSB is 2.5uA for Vshunt ADCRANGE = 0 and the value of Shunt_LSB is 625nA for Vshunt ADCRANGE = 1.

$$Current\_LSB = \frac{Maximum\ Expected\ Current}{2^{15}} \quad (2)$$

Note that the current is calculated following a shunt voltage measurement based on the value set in the SHUNT_CAL field. If the value loaded into the SHUNT_CAL field is zero, the current value reported through the CURRENT register is also zero.

After programming the SHUNT_CAL field with the calculated value, the measured current in Amperes can be read from the CURRENT register. Use Equation 3 to calculate the final value scaled by the CURRENT_LSB:

$$Current\ [A] = CURRENT\_LSB \times CURRENT \quad (3)$$

Where

- CURRENT is the value read from the CURRENT register

The power value can be read from the POWER register as an unsigned 16-bit value. Use Equation 4 to convert the power to Watts:

$$Power\ [W] = 32 \times CURRENT\_LSB \times POWER,\ Vbus\ ADCRANGE = 0$$
$$Power\ [W] = 48 \times CURRENT\_LSB \times POWER,\ Vbus\ ADCRANGE = 1 \quad (4)$$

Where

- POWER is the value read from the POWER register.
- CURRENT_LSB is chosen lsb size for the selected channel.

The energy values can be read from the each ENERGY register as a 32-bit unsigned value. Use Equation 5 to convert the energy to Joules:

$$\text{Energy [J]} = 32 \times \text{CURRENT\_LSB} \times \text{ENERGY, Vbus ADCRANGE} = 0$$
$$\text{Energy [J]} = 48 \times \text{CURRENT\_LSB} \times \text{ENERGY, Vbus ADCRANGE} = 1 \quad (5)$$

Where

- ENERGY is the value read from the each ENERGY register.
- CURRENT_LSB is chosen lsb size for the selected channel.

Configuration Example

When Load = 10 A, RSHUNT=2mΩ, and VBUS=12V, a nominal 10A load that creates a differential voltage of 20mV across 2mΩ shunt resistor. The bus voltage for The SQ52212 is measured at the VBUS pin, which in this example is connected to the VBUS pin to measure the voltage level delivered to the load. The configuration is as follows: Vshunt ADCRANGE = 0 , and Vbus ADCRANGE = 0.

For this example, assuming a maximum expected current of 15 A, the Current_LSB is calculated to be 457.7μA/bit using Equation (2). Using a value for the Current_LSB of 500μA/Bit or 1mA/Bit would significantly simplify the conversion from the Current Register (02h) and Power Register (03h) to amperes and watts. For this example, a value of 1mA/bit was chosen for the Current_LSB. Using this value for the Current_LSB does trade a small amount of resolution for having a simpler conversion process on the user side. Using Equation (1) in this example with a Current_LSB value of 1mA/bit and a shunt resistor of 2mΩ results in a Calibration Register value of 2560 or A00h.

The Current Register (02h) is then calculated through the Shunt Voltage Register (01h) and Calibration Register(05h). For this example, the Shunt Voltage Register contains a value of 1F40h (representing 20mV), and Current Register (02h) contains a value of 2710h, or a decimal equivalent of 10000. Multiplying this value by 1mA/bit results in the original 10A level stated in the example.

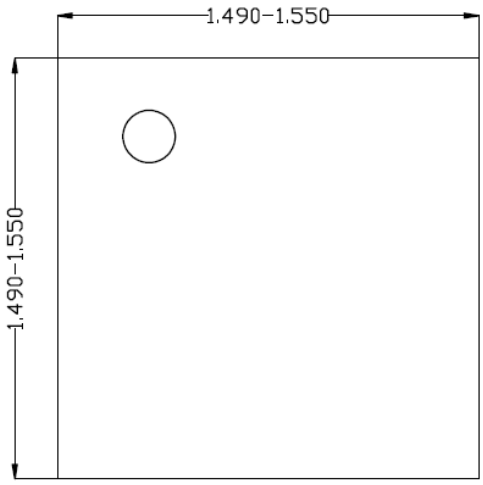
The LSB for the Bus Voltage Register (01h) is a fixed 1.6mV/bit, which means that the 12V present at the VBUS pin results in a register value of 1D4Ch, or a decimal equivalent of 7500. Note that the MSB of the Bus Voltage Register (01h) is always zero because the VBUS pin is only able to measure positive voltages.

For this example, the result for the Power Register (03h) is 0EA0h, or a decimal equivalent of 3750. Multiplying this result by the power LSB (32 times Current_LSB) results in a power calculation of (3750 × 32mW/bit), or 120W. The power LSB has a fixed ratio to the Current_LSB of 32. For this example, 1mA/bit Current_LSB results in a power LSB of 32mW/bit. This ratio is internally programmed to ensure that the scaling of the power calculation is within an acceptable range. A manual calculation for the power being delivered to the load would use a bus voltage of 12V multiplied by the load current of 10 A to give a result of 120W.

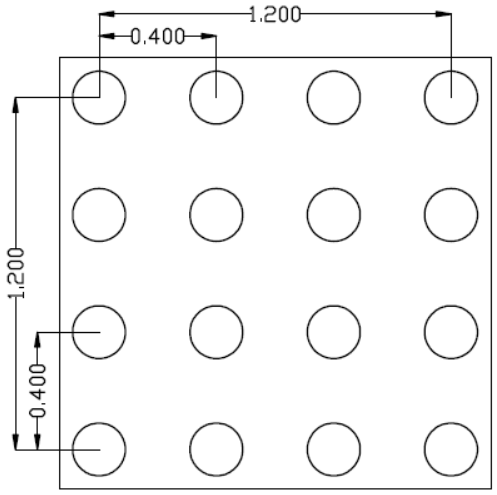
The following table lists the results of configuring, measuring, and calculating the values for current and power for The SQ52212.

Register Name	Address	Contents	DEC	LSB	Value
Configuration Register	10h	3127h			
Shunt Register	00h	1F40h	8000	2.5μV	20mV
Bus Voltage Register	01h	1D4Ch	7500	1.6mV	12V
Calibration Register	05h	0A00h	2560		
Current Register	02h	2710h	10000	1mA	10A
Power Register	03h	0EA0h	3750	32mW	120W

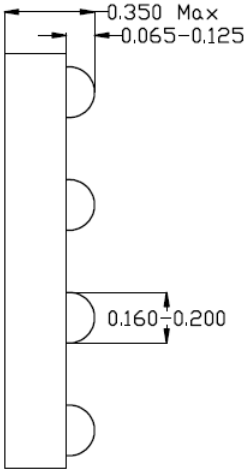
CSP1.51×1.51-16 Package Outline Drawing



Top View



Bottom View



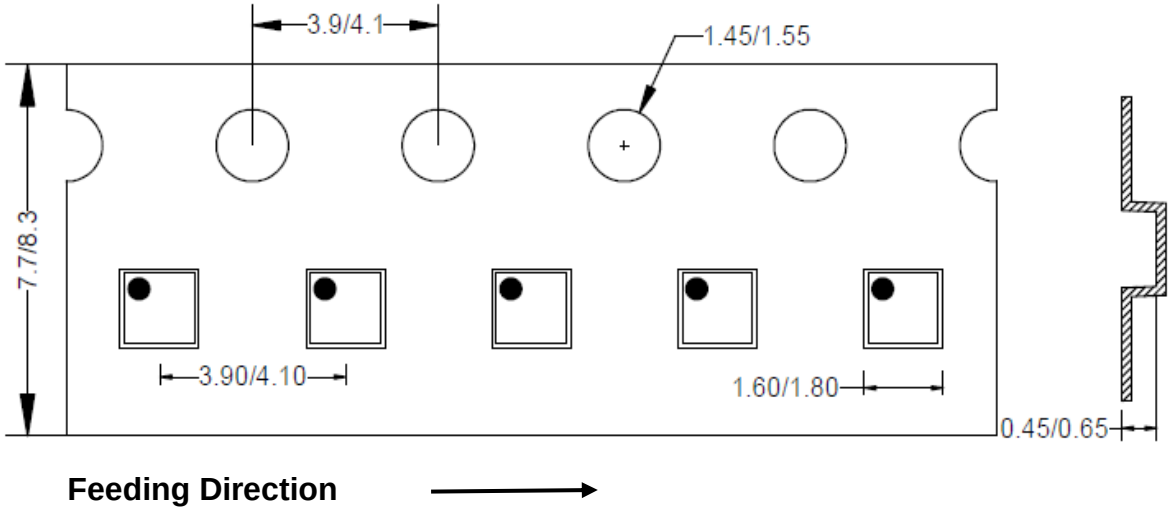
Side View

Note: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

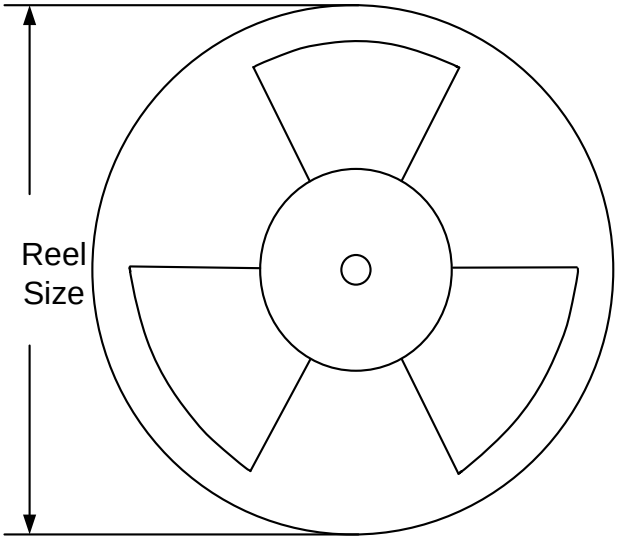
1. Taping Orientation

CSP1.51×1.51



Feeding Direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
CSP1.51×1.51	8	4	7”	400	400	3000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Mar. 25, 2026	Revision 1.0	Initial Release.

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