SQ52201QDQ

36V High-accuracy Current/Power Monitor with Programmable Alert Function

General Description

The SQ52201 which has an I²C or SMBUS-compatible interface, is a high accuracy device with the features of current shunt, bus voltage and power monitor.

The shunt voltage and the bus supply voltage could be sampled accurately at the same time and will be processed inside the device to generate the power data with programmable calibration, averaging technique and internal multiplier. It makes the application system more reliable because of abundant alert sources settings provided by programmable alert function.

The current on common mode bus voltages can be monitored by SQ52201. The common mode bus voltages can vary from 0V to 36V, which is independent of the supply voltage, ranging from 2.7V to 5.5V. The operating temperature of SQ52201 ranges between -40°C and +125°C. The SQ52201 is available in the QFN3*3-16 package and features 16 programmable addresses on the I²C-compatible interface.

Features

- Senses Bus Voltages from 0 V to 36 V
- High-Side or Low-Side Sensing
- Bi-directional Current Sensing
- Reports Current, Voltage, and Power
- High Accuracy:
  - 0.02% Gain Error (Typ) for Shunt Voltage
  - 0.02% Gain Error (Typ) for Bus Voltage
  - 2.5μV Offset (Typ) for Shunt Voltage
  - 1.25mV Offset (Typ) for Bus Voltage
- Configurable Averaging Options
- Configurable Conversion Time
- Abundant Alert Sources Setting
- 16 Programmable Addresses
- High Speed I²C Mode Compatible
- 3.3V I²C Interface Compatible
- Operates from 2.7V to 5.5V Power Supply
- Package: QFN3×3-16
- MSL Rating: MSL1

Applications

- Servers
- Telecom Equipment
- Computing
- Power Management
- Battery Chargers
- Power Supplies
- Test Equipment

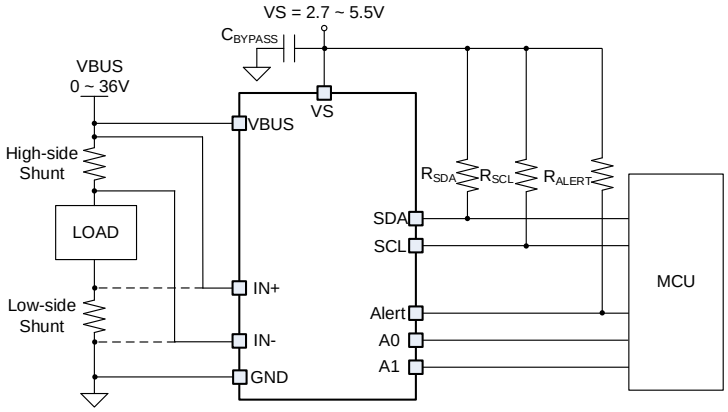


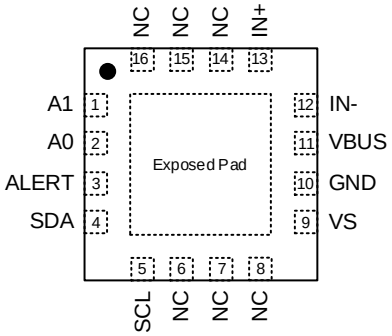
Figure 1. Typical Application

Ordering Information

Ordering Part Number	Package type	Top Mark
SQ52201QDQ	QFN3×3-16	**LMK*xyz***

x=year code, y=week code, z= lot number code

Pinout (Top View)



(QFN3×3-16)

Pin Description

Pin No	Pin Name	Pin Description
1	A1	Address pin. Connect to GND, SCL, SDA, or VS.
2	A0	Address pin. Connect to GND, SCL, SDA, or VS.
3	ALERT	Multi-functional alert, open-drain output.
4	SDA	Serial bus data line, open-drain input/output.
5	SCL	Serial bus clock line, open-drain input.
6, 7, 8, 14, 15, 16	NC	No internal connection
9	VS	Power supply, 2.7 V to 5.5 V.
10	GND	Ground.
11	VBUS	Bus voltage input.
12	IN–	Negative differential voltage input. Connect to load side of shunt resistor.
13	IN+	Positive differential voltage input. Connect to supply side of shunt resistor.
	Exposed Pad	This pad can be connected to ground or left floating.

Block Diagram

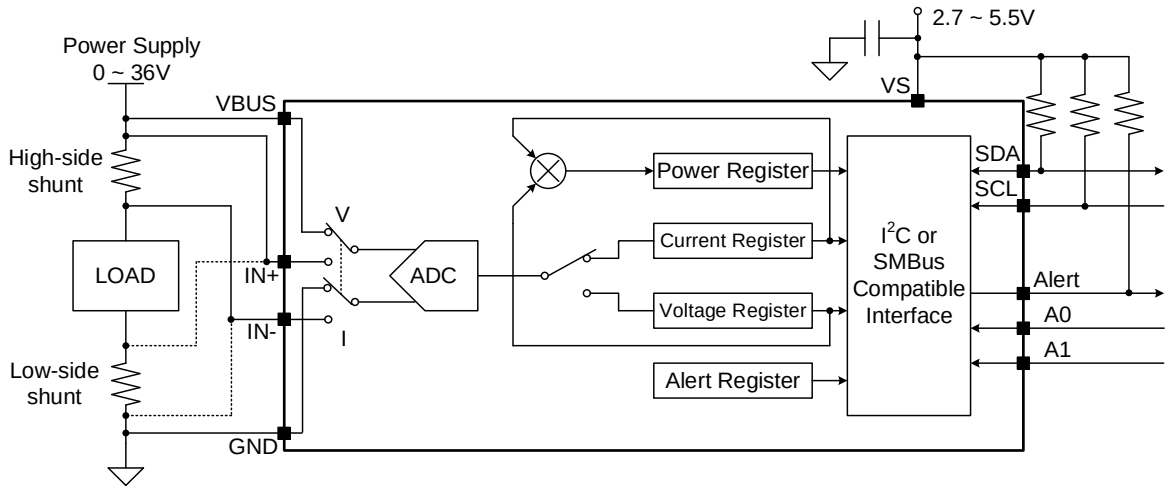


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VS	-0.3	6	V
Differential Analog input (V_{IN+} – V_{IN-})	-40	40	
Common Mode Analog input (V_{IN+} + V_{IN-}) / 2	-0.3	40	
BUS	-0.3	40	
SDA, ALERT,SCL, A0, A1	-0.3	6	
Input current into any pin		5	mA
Open-drain digital output current (SDA, SCL, ALERT)		10	
Junction Temperature, Operating	-40	150	°C
Storage Temperature	-65	150	
ESD: HBM (Human Body Mode)	± 2000		V
ESD: CDM (Charged Device Model)	± 1000		V

Thermal Information

Parameter (Note 2)	Max	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	118	°C/W
θ_{JC}-TOP Junction-to-Case (Top) Thermal Resistance	19	
ψ_{JT} Junction-to-Top Characterization Parameter	3	
P_D Power Dissipation TA = 25°C	0.847	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VS	2.7	5.5	V
Differential Analog input (V_{IN+} – V_{IN-})	-81.92	+81.91	mV
Common Mode Analog input (V_{IN+} + V_{IN-}) / 2	0	36	V
BUS	0	36	
Junction Temperature Range	-40	125	°C

Electrical Characteristics

VS = 3.3V, V_{IN+} = 12V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0mV and V_{VBUS} = 12V, T_A = 25°C, unless otherwise specified. (4)

Parameter(4)		Symbol	Test condition	Min	Typ	Max	Unit
Input	Shunt Voltage Input Range			-81.92		+81.9175	mV
	Bus Voltage Input Range (Note 5)			0		36	V
	Common-Mode Rejection	CMRR	0V≤V_{IN+}≤36V	126	140		dB
	Shunt Offset Voltage, RTI (Note 6)	V_{OS}			±2.5	±10	μV
	Shunt Offset Voltage, RTI vs. Temperature		-40°C≤T_A≤125°C		0.02	0.1	μV/°C
	Shunt Offset Voltage, RTI vs. Power Supply	PSRR	2.7V≤VS≤5.5V		2.5		μV/V
	Bus Offset Voltage, RTI	V_{OS}			±1.25	±10	mV
	Bus Offset Voltage, RTI vs. Temperature		-40°C≤T_A≤125°C		10	40	μV/°C
	Bus Offset Voltage, RTI vs. Power Supply	PSRR			0.5		mV/V
	Input Bias Current (I_{IN+}, I_{IN})	I_B			7		μA
	VBUS Input Impedance				830		kΩ
	Input Leakage (Note 7)		(IN+ pin) + (IN– pin), Power-down mode		0.1	0.5	μA
DC Accuracy	ADC Native Resolution				16		Bits
	1 LSB Step Size		Shunt voltage		2.5		μV
			Bus voltage		1.25		mV
	Shunt Voltage Gain Error				0.02	0.2	%
	Shunt Voltage Gain Error vs. Temperature		-40°C≤T_A≤125°C		10	50	ppm/°C
	Bus Voltage Gain Error				0.02	0.25	%
	Bus Voltage Gain Error vs. Temperature		-40°C≤T_A≤125°C		10	50	ppm/°C
	Differential Nonlinearity				±0.1		LSB
	ADC Conversion Time	t_{CT}	CT bit = 000		140	165	μs
			CT bit = 001		204	232	
			CT bit = 010		332	366	
			CT bit = 011		588	633	
			CT bit = 100		1.1	1.165	ms
			CT bit = 101		2.116	2.224	
			CT bit = 110		4.156	4.349	
			CT bit = 111		8.244	8.608	
SMBus	SMBus Timeout (Note 8)				28	35	ms
Digital Input/Output	Input Capacitance				3		pF
	Leakage Input Current		0V≤V_{SCL}≤VS, 0V≤V_{SDA}≤VS, 0V≤V_{Alert}≤VS, 0V≤V_{A0}≤VS, 0V≤V_{A1}≤VS		0.1	1	μA
	High Level Input Voltage	V_{IH}		0.7×VS		6	V
	Low Level Input Voltage	V_{IL}		-0.3		0.3×VS	V
	Low Level Output Voltage, SDA, Alert	V_{OL}	I_{OL}=3mA	0		0.4	V
	Hysteresis				400		mV
Power Supply	Operating Supply Range			2.7		5.5	V
	Quiescent Current	I_Q			396	460	μA
			Power down (shutdown) mode		0.5	1	μA
	Power-on Reset Threshold	V_{POR}			2		V

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured under still air and chip mounted on high effective two-layer test board in accordance with JESD51-2,-14.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Production testing is performed at 25˚C; limits at -40°C to +125°C are guaranteed by design, test or statistical correlation.

Note 5: While the input range is 36 V, the full-scale range of the ADC scaling is 40.96 V. Do not apply more than 36 V.

Note 6: RTI = Referred-to-input.

Note 7: Input leakage is positive (current flowing into the pin) for the conditions shown at the top of this table. Negative leakage currents can occur under different input conditions.

Note 8: SMBus timeout in the SQ52201 resets the interface any time SCL is low for more than 28ms.

Detailed Description

Bus Voltage and Current Sample

The bus voltage and shunt voltage could be measured directly on the power supply bus of interest in the SQ52201. The power supply bus voltage can be taken at the VBUS pin, while the shunt voltage representing the current is measured by the IN+ and IN– pins. The differential shunt voltage is measured with respect to the IN– pin while the bus voltage and the shunt voltage are measured with respect to ground and IN– pin, respectively.

Operation Mode

The continuous and triggered operating modes for data conversions in the device will determine how the ADC operates following these conversions.

Continuous Operating Mode:

The continuous operating mode of the SQ52201 will be adopted as the MODE bits of the Configuration Register (00h) are set to '111'. At first, the number of averages should be set in the Configuration Register. The shunt voltage and then the bus voltage will be sampled and converted in each sampling sequence. Next, the current value is calculated based on the shunt voltage to get the power result. All the values will be stored in an accumulator and the above measurement/calculation sequence repeats until the number of averages set in the Configuration Register is reached. At the end of each sequence, the newly acquired set of values is added to previously gathered values. When all the averaging finishes, the final values of shunt voltage, bus voltage, current, and power will be renewed in the corresponding resisters, which could read without any affect by the conversion in progress. These values will be covered when another fully completed conversion results is stored in the same register.

All the calculations are performed in the background, which has no influence on conversion time.

The shunt voltage or the bus voltage can be converted solely with proper setting by the mode control in the Conversion Register (00h) to fit the user's explicit application conditions.

Triggered Operating Mode:

The triggered mode of the SQ52201 will be adopted as the MODE bits of the Configuration Register (00h) are set to '001', '010', or '011'. A single-shot conversion will be fulfilled to produce a single set of measurements as any triggered convert modes are wrote into the Configuration Register. Thus, another single-shot conversion can be only executed under the condition that the Configuration Register is written to a second time, even if the mode does not change.

Power-Down Mode:

Furthermore, the power-down mode of the SQ52201 is designed to reduce the quiescent current and turn off current into the device inputs, which can reduce impact of supply drain when the device is not being used. During the power-down mode, the values in the registers can be replaced and read. The power-down mode will exit with any active mode settings written into the Configuration Register. Notes: The exit procedures need 40μs.

Conversion Ready Flag

To help coordinate one-shot or triggered conversions, the Conversion Ready flag bit (CVRF bit, Mask/Enable Register) is provided, though the SQ52201 can be read at any time, and the data from the last conversion remain available. The CVRF bit will be set after the completion of all conversions, averaging, and multiplication operations. The Conversion Ready flag (CVRF) bit clears under these conditions:

• Writing to the Configuration Register (00h) , except when configuring the MODE bits for power-down mode.

• Reading the Mask/Enable Register (06h)

Averaging and Conversion Time

The conversion times (t_{CT}) for both the shunt voltage and bus voltage measurements can be selected from as fast as 140μs to as long as 8.244ms independently. This way is useful in applications because the bus voltage tends to be quite stable. This setting makes sure that more time will be adopted to measure the shunt voltage rather than the bus voltage.

There is a compromise between the settings for conversion time and the used averaging mode. The averaging feature could effectively filter the signal, resulting in dramatic modification of the measurement accuracy. Any kind of noise, even if it is coupled into the signal, could be suppressed by employing this approach in the device. With a vast average, the device could get more accurate signals by suppressing the noise.

The selected conversion times is another key point to improve the measurement accuracy. The highest accuracy measurement can be reached by a cooperation of the longest accessible conversion times and highest number of averages, under the timing requirements of the system.

Power Calculation

After the measurements of the shunt voltage and bus voltage, the Current and Power could be calculated, as shown in *Figure 3*. Current is equal to a shunt voltage divided by a value set in the Calibration Register. The current value will be set to zero when no value loaded in the Calibration Register. Similarly, Power is calculated following the bus voltage measurement, which is equal to Current multiply by the bus voltage. Also, the power will be set to zero when no value loaded in the Calibration Register. Remarkably, all the calculations are carried out in the background with no additional conversion time raise. The values of the current and power are regarded as intermediate results (unless the averaging is set to 1) and saved in an internal accumulation register rather than the corresponding output registers. Following every sampling, the newly-calculated values of current and power will be added to this accumulation register until all the samplings have been finished and averaged based on the number of averages set in the Configuration Register (00h).

Meanwhile, the values of the shunt and bus voltage are also registered. When all the sample measurements and corresponding calculations of the current and power are completed, the final average of each parameter will be loaded to the corresponding output registers, where users can read them.

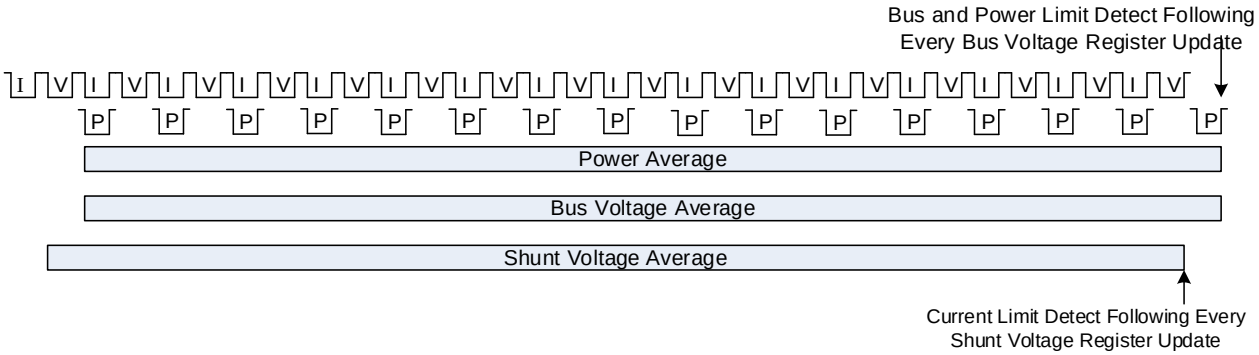


Figure 3. Power Calculation Scheme

Interrupt Generation

A single Alert Limit Register (07h) is equipped in the SQ52201. The function of the register is to allow the Alert pin being programmed in order to respond to a single user-defined event or to a Conversion Ready notification if necessary. The user can choose one of five possible functions to monitor and/or set the Conversion Ready bit to control the response of the Alert pin in the Mask/Enable Register. On account of the function being monitored, a value needs to be written into the Alert Limit Register to set the corresponding threshold value that asserts the Alert pin.

The Alert pin allows for one of several available user-programmable thresholds to be monitored:

- Current Over-Limit (COL)
- Current Under-Limit (CUL)
- Bus Over-Voltage (BOV)
- Bus Under-Voltage (BUV)
- Power Over-Limit (POL)

The alert pin is an open-drain output. This pin will be asserted when the function selected in the Mask/Enable Register meets the trigger criteria programmed into the Alert Limit Register. Among all the alert functions, only one could be enabled and kicked in at a time. If multiple Alert Functions are enabled, the selected function in the highest significant bit position will take priority and determine the behavior of the Alert pin. For instance, when the Current Over-Limit function and the Current Under-Limit function are both enabled, the alert pin will be asserted only at the time while the Shunt Voltage Register overtakes the value in the Alert Limit Register.

When the SQ52201 has completed the prior conversion and is ready to start a new conversion, the Conversion Ready state of the device can be also be monitored at the Alert pin to remind the user. The Alert pin can be used to monitor the Conversion Ready when it has another alert function. If an alert function and the Conversion Ready are both enabled at the Alert pin, when the Alert pin is asserted, the Conversion Ready Flag (CVRF, bit 3), and the Alert Function Flag (AFF, bit 4) in the Mask/Enable Register should be read following the alert to determine the source of the alert. If the Conversion Ready feature is not expected and the CNVR bit is not set, the Alert pin will only respond to the alert function.

Figure 3 shows the time that the value in the Alert Limit Register is compared to the corresponding converted value.

The measured shunt voltage will be compared with the Alert Limit Register following every shunt voltage register update and assert the AFF bit and Alert pin if the limit threshold is overtaken.

The measured bus voltage will be compared with the Alert Limit Register following every bus voltage register update and assert the AFF bit and Alert pin if the limit threshold is overtaken.

The calculated power value will also be compared following every bus voltage register update and asserts the AFF bit and Alert pin if the limit threshold is overtaken.

For instance, if the alert function of Current Over-Limit (COL) is enabled, when each shunt voltage conversion is completed, the measured value will be compared to the value programmed in the Alert Limit Register to determine whether the sampled has overtaken the set limit. Once the measured value overtakes the programmed one in the Alert Limit Register, the AFF, bit 4 of the Mask/Enable Register, will assert high. Except for the AFF being asserted, the Alert Polarity Bit (APOL, bit 1 of the Mask/Enable Register) can also make the alert pin assert. If the Alert Latch is enabled, the AFF and Alert pin will remain asserted until either the Mask/Enable Register is read or the Configuration Register (00h) is written to.0h) is written to or the Mask/Enable Register is read.

If the Alert pin is not used in a design, it can be left floating.

Device Configuration

In order to report the current and power values properly, several registers should be configured using the following steps:

Step1: select the resolution of the Current Register (04h): Current_LSB.

The user can obtain the highest resolution for Current Register (04h) by adopting the smallest allowable Current_LSB based on the maximum expected current IMAX as shown in Equation (1). Select a value for the Current_LSB to the nearest round number above this value to obtain the conversion of the Current Register (04h) and Power Register (03h) to amperes and watts respectively.

$$Current\_LSB = \frac{I_{MAX}}{2^{15}} \quad (1)$$

Where Current_LSB is the resolution of the Current Register (04h); I_{MAX} is the maximum expected current.

Moreover, this value of the shunt resistor is selected based on the shunt voltage measurement range and I_{MAX}.

Step2: configure the Calibration Register (05h)

The Calibration Register enables the user to scale the Current Register (04h) and Power Register (03h) values. With the correct configuration of the Calibration Register (05h), the current flowing through the shunt resistor can be read out by simply multiply the Current Register and Current_LSB. The value of the Calibration Register (05h), CAL[R], can be calculated using the equation (2) below:

$$CAL[R] = \frac{2048 \times Shunt\_LSB}{Current\_LSB \times R_{Shunt}} \quad (2)$$

Where CAL[R] is the value of the Calibration Register (05h), Shunt_LSB is the resolution of the Shunt Voltage Register (01h), Shunt_LSB is 2.5uV/LSB; Current_LSB is the resolution of the Current Register (04h); R_{Shunt} is the shunt resistor.

After programming the Calibration Register, the Current Register (04h) and Power Register (03h) will update accordingly based on the corresponding shunt voltage and bus voltage measurements on every measurement cycle. Before programming the Calibration Register, the Power Register (03h) and Current Register (04h) keeps at zero.

Step3: Current Register (04h)

The value of the Shunt Register (01h) can be calculated using the equation (3)

$$Shunt[R] = \frac{Current \times R_{Shunt}}{Shunt\_LSB} \quad (3)$$

In the device, based on the value in Calibration Register(05h) and the Shunt Voltage Register (01h), the Current Register value is calculated as shown in the equation (4).

$$Current[R] = \frac{Shunt[R] \times CAL[R]}{2048} \quad (4)$$

Where Current[R] is the value of the Current Register (04h); Shunt[R] is the value of the Shunt Register (01h); CAL[R] is the value of the Calibration Register (05h)

The Current Register value represents the current in Amperes as described by the equation (5)

$$Current = Current[R] \times Current\_LSB \quad (5)$$

Step4: Bus Voltage Register

The bus voltage is read by the equation (6)

$$Bus = Bus[R] \times Bus\_LSB \quad (6)$$

Where Bus_LSB is the resolution of the Bus Voltage Register(02h), which is a fixed 1.25mV/LSB.

Step5: Power Register

The value of the Power Register (03h) is calculated according the equation (7)

$$Power[R] = \frac{Current[R] \times Bus[R]}{20000} \quad (7)$$

Where Current[R] is the value of the Current Register (04h); Bus[R] is the value of the Bus Voltage Register (02h); Power[R] is the value of the Power Register(03h).

Based on equations (1)~(7), the resolution of the Power Register is fixed as 25 times of the resolution of the Current Register. The resulting power value obtained based on equation (8)

$$Power = Power[R] \times Power\_LSB \quad (8)$$

Configuration Example

In *Figure4*, a nominal 10A load creates a differential voltage of 20mV across a 2mΩ shunt resistor. In this example, the external VBUS input pin is used to measure the bus voltage in the SQ52201. In order to measure the voltage level delivered to the load, the IN–pin is connected to the external VBUS input pin. In this example, the VBUS pin measures less than 12 V because the voltage at the IN– pin is 11.98 V as a result of the voltage drop across the shunt resistor.

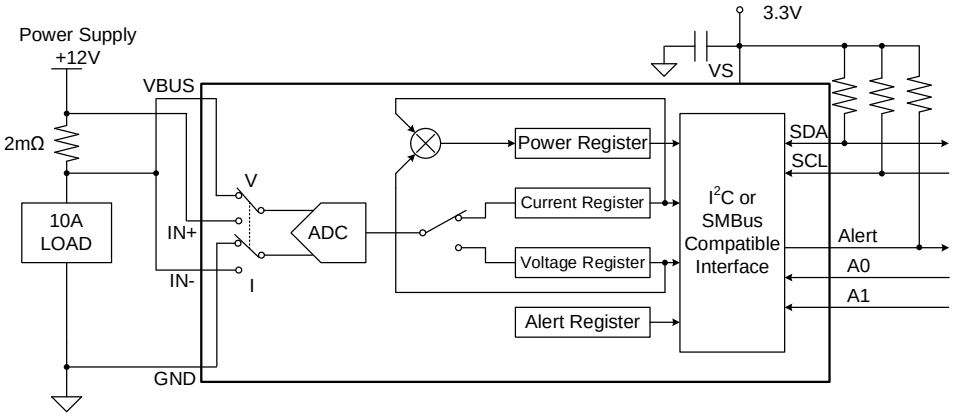


Figure 4. High-Side Sensing Circuit Application Example

Assuming a maximum expected current of 15A, the Current_LSB is calculated to be 457.7μA/bit using Equation (1). The Current_LSB value could be rounded up to 500μA/Bit or 1mA/Bit, to simplify the conversion from the Current Register (04h) and Power Register (03h) to amperes and watts. As for this example, the value of 1mA/bit was used for the Current_LSB. Using this value for the Current_LSB will significantly simplify the conversion process on the user side with trading a small amount of resolution. Using the equation (2) with a Current_LSB value of 1mA/bit and a shunt resistor value of 2mΩ results in a Calibration Register value of 2560 (A00h).

As shown in Equation (4), the Current Register (04h) is calculated by multiplying the value of the Shunt Voltage Register (01h) contents by the value of the Calibration Register and then dividing by 2048. It is noted that the values of the Shunt Voltage Register (01h) and the Calibration Register are decimal numbers. As for this example, the value for the Current Register (04h) of 10000 (decimal value), or 2710h can be obtained by multiplying the Shunt Voltage Register value of 8,000 (representing 20mV) by the Calibration Register value of 2560 and then divided by 2048. Multiplying this value by 1mA/bit results in the original 10A current level to be measured.

The 11.98V in the VBUS pin results in a decimal value of 9584 and a register equivalent of 2570h because of a fixed 1.25mV/bit in the LSB for the Bus Voltage Register (02h). Significantly, the VBUS pin cannot measure negative voltage, so the MSB of the Bus Voltage Register (02h) is invariably zero.

As defined in Equation (7), the Power Register (03h) can be calculated as follow: firstly, multiply the value of the Current Register, 10000 (decimal value) by the value of the Bus Voltage Register (02h), 9584 (decimal value); next, the front result

is divided by 20,000. As a result, the value for the Power Register (03h) is 4792 (decimal value) or 12B8h. A power calculation of (4792 × 25mW/bit), or 119.82W is the result of multiplying the value for the Power Register (03h) by the power LSB (25 times Current_LSB]). A fixed ratio of 25 between the power LSB and Current_LSB is internally programmed to ensure that the power calculation is just in an acceptable range. As for this example, the Current_LSB of 1mA/bit results in a power LSB of 25mW/bit. A simple calculation for the power on the load could use the load current of 10A multiplied by the bus voltage of 11.98V to get a result of 119.8W.

Table 1 lists the results of the values for current and power for the SQ52201 at the condition of Load = 10 A, V_{CM}=12V, R_{SHUNT}=2mΩ, and V_{VBUS}=12V.

Table 1. Calculating Current and Power

Register Name	Address	Contents	Dec	Lsb	Value
Configuration Register	00h	4127h			
Shunt Register	01h	1F40h	8000	2.5μV	20mV
Bus Voltage Register	02h	2570h	9584	1.25mV	11.98V
Calibration Register	05h	0A00h	2560		
Current Register	04h	2710h	10000	1mA	10A
Power Register	03h	12B8h	4792	25mW	119.82W

Simple Monitor Usage

If only reading a shunt voltage drop and bus voltage on the condition of the default power-on reset configuration and continuous conversion of shunt and bus voltages, the user can use the device with no programming.

Notably, not only a valid current but also a power value cannot be provided by the device, with no programming in the Calibration Register. This is because that these outputs are generated by the values loaded into the Calibration Register.

Basic I²C/SMBus Overview

The SQ52201 is compatible with I²C and SMBus interfaces. There are two lines, SCL and SDA, connecting the device to the bus, which are open-drain connections.

A master is the device that initiates a data transfer. The slaves are the devices controlled by the master. A master device will control the bus to generate the serial clock (SCL), control the bus access and generate START and STOP conditions.

In order to address a given device, a start condition will be initiated by the master though pulling the data signal line (SDA) from a high to a low logic level when SCL is high. On the rising edge of SCL, all salves on the bus shift in the salve address byte, where the last bit indicates whether a read or write operation is intended. The addressed salves respond to the master by producing an Acknowledge and pulling SDA low during the ninth clock pulse.

After an Acknowledge bit, data transfer will be initiated and eight of data will be sent. The most significant byte of the Register bytes is sent firstly and followed by the least significant byte. SDA must keep stable during data transfer with SCL high. Any change in SDA with SCL high will be regard as a start or stop condition.

With all data transmission finished, a stop condition is generated by the master with the symptom of pulling SDA from low to high keeping SCL high. To prevent locking up the bus, a 28ms timeout on the interface of the device is involved.

The SQ52201 supports fast mode (1kHz to 400kHz) and high-speed mode (1kHz to 3.4MHz) transmission protocols. All data transmitted are most significant byte first.

Programming

Serial Bus Address

To communicate with multiple devices on the bus, SQ52201 has 16 programmable slave addresses, which consists of seven address bits and a function bit that determines read or write operation.

The programmable address is determined by two address pins, A0 and A1. The following table lists the corresponding relationship between pins and addresses. The device samples the state of pins A0 and A1 on every bus communication. Establish the pin states before any activity on the interface occurs.

Table 2. Address Pins and Slave Addresses

A1	A0	Slave Address
GND	GND	1000000
GND	VS	1000001
GND	SDA	1000010
GND	SCL	1000011
VS	GND	1000100
VS	VS	1000101
VS	SDA	1000110
VS	SCL	1000111
SDA	GND	1001000
SDA	VS	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	VS	1001101
SCL	SDA	1001110
SCL	SCL	1001111

Writing Command

To access a specific register on SQ52201 the user should write an appropriate value to the register pointer. The first byte transferred after the slave address byte is the value for the register pointer while the R/W bit is low. A value for the register pointer is desired to the device for each write operation.

As the master transmits the first byte, which is the salve address with R/W bit low, writing to a register will start. Then the receipt of a valid address is acknowledged by the device. The master transmits the next byte, which is the address of the register, where the data is written. The register pointer to the desired register is updated by this register address. The next two bytes are written to the register addressed by the register pointer. The receipt of each data byte is acknowledged by the device. The data transfer may be terminated as a start or stop condition is generated by the master.

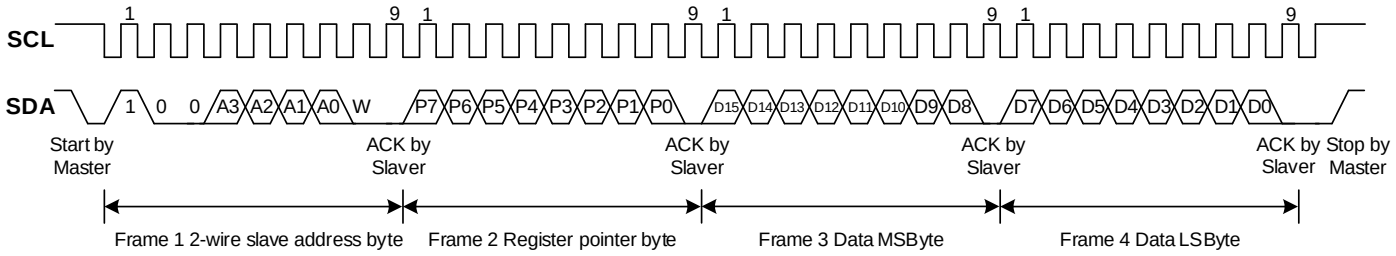


Figure 5. Timing Diagram for Write Word Format

Read Command

When reading from the device, the last value stored in the register pointer by a write operation determines which register is read during a read operation. To change the register pointer for a read operation, a new value must be written to the register pointer. This write is accomplished by issuing a slave address byte with the R/W bit low, followed by the register pointer byte, as shown in *Figure 6*. No additional data are required.

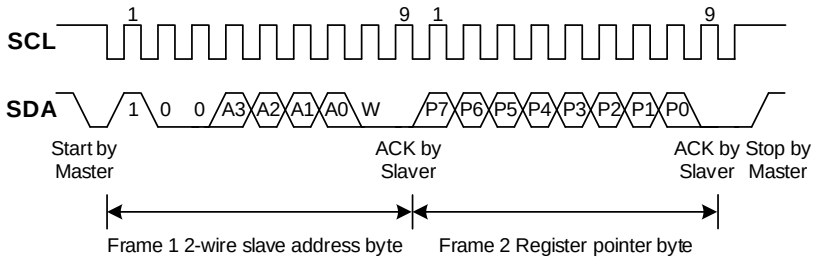


Figure 6. Typical Register Pointer Set

To initiate the read command, a start condition is generated and the slave address byte is sent by the master, while the R/W bit is high. And then the slave transmits the most significant byte of the register indicated by the register pointer, which is followed by an Acknowledge from the master; the last byte is the least significant byte transmitted by slave. The receipt of the data byte is acknowledged by the master. The data transfer may be terminated as a Not-Acknowledge after receiving any data byte, or a start or stop condition is generated by the master.

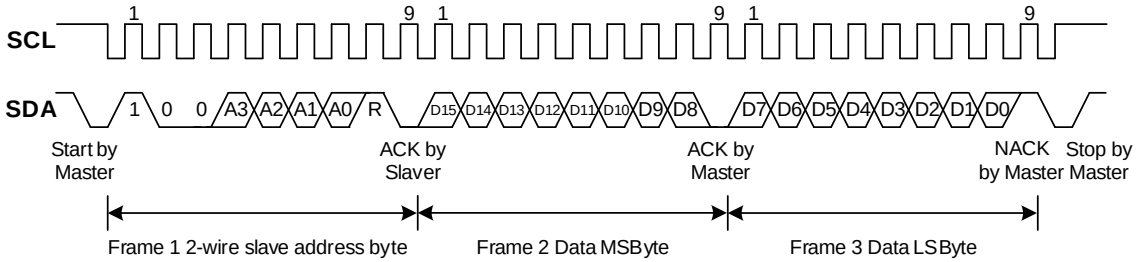


Figure 7. Timing Diagram for Read Word Format

High-Speed I²C Mode

The pull-up resistors will pull high the SDA and SCL lines, if the bus is free. A start condition is generated by the master followed by a valid serial byte, which contains high-speed (HS) master code 00001XXX. In both fast (400kHz) or standard (100kHz) (F/S) mode, this transmission can be executed at no more than 400kHz. The device does recognize the HS master code and switches its internal filters to support 3.4MHz operation, even if no HS master code is acknowledged.

A repeated start condition, which has the same timing as the start condition, is then generated by the master. After this repeated start condition, the protocol is almost identical to F/S mode while the transmission speeds cannot be up to 3.4MHz. Rather than a stop condition, the use of the repeated start conditions could repeated start conditions. The stop condition could escape the HS-mode and make all the internal filters of the device support the F/S mode.

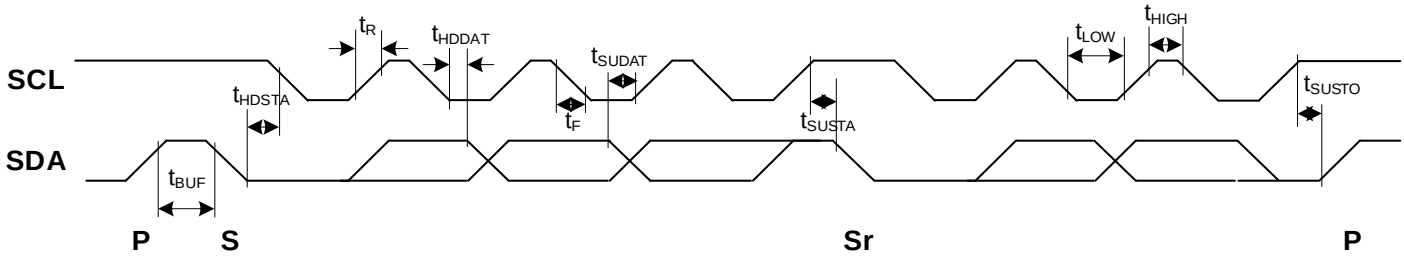


Figure 8. Bus Timing Diagram

Table 3. Bus Timing Diagram Definitions

Parameters	Symbol	Fast Mode		High-Speed Mode		Units
		MIN	MAX	MIN	MAX	
SCL operating frequency	f_{SCL}	0.001	0.4	0.001	3.4	MHz
Bus free time between stop and start conditions	t_{BUF}	600		160		ns
Hold time after repeated START condition. After this period, the first clock is generated.	t_{HDSTA}	100		100		ns
Repeated start condition setup time	t_{SUSTA}	100		100		ns
STOP condition setup time	t_{SUSTO}	100		100		ns
Data hold time	t_{HDDAT}	10	900	10	100	ns
Data setup time	t_{SUDAT}	100		20		ns
SCL clock low period	t_{LOW}	1300		200		ns
SCL clock high period	t_{HIGH}	600		60		ns
Data fall time	t_F		300		80	ns
Clock fall time	t_F		300		40	ns
Clock rise time	t_R		300		40	ns
Clock/data rise time for SCLK≤100kHz	t_R		1000			ns

SMBus Alert Response

The SQ52201 can respond to the SMBus Alert Response address, which provides a quick fault identification for simple slave devices. With an Alert arising, the Alert Response slave address (0001 100) will be broadcasted by the master and the Read/Write bit will be set high. After this Alert Response, the slave device, which generates an alert identifies itself by acknowledging the Alert Response, will send its address on the bus.

Like the I²C General Call, several different slave devices could be activated by the Alert Response at the same time. The bus arbitration rules will be applied is more than one slave tries to respond. The losing device will not produce an Acknowledge and keep the Alert line low until the interrupt is cleared.

The timing diagram for the SMBus Alert response operation is shown below.

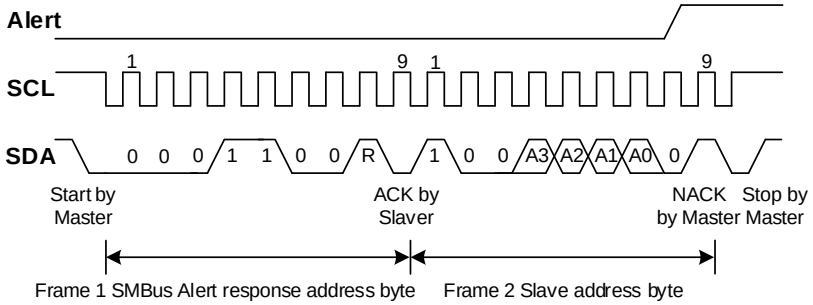


Figure 9. Timing Diagram for SMBus ALERT

Register Maps

SQ52201 uses a bank of registers for holding configuration settings, status information and storing measurement and internal calculation results.

The following table summarizes the device registers. All 16-bit device registers can be accessed using two 8-bit bytes via the I²C interface.

Register Set Summary				
Register Address (Hex)	**Register Name**	**Function**	**Power-On Reset (Hex)**	**Type**
00h	Configuration Register	All-register reset, shunt voltage and bus voltage ADC conversion times, averaging and operating mode.	4127h	R/W
01h	Shunt Voltage Register	Shunt voltage measurement data.	0000h	R
02h	Bus Voltage Register	Bus voltage measurement data.	0000h	R
03h	Power Register	Power transmitted by load.	0000h	R
04h	Current Register	Contains the value of the calculated current flowing through the shunt resistor.	0000h	R
05h	Calibration Register	Sets full-scale range and LSB of current and power measurements. Overall system calibration.	0000h	R/W
06h	Mask/Enable Register	Alert configuration and Conversion Ready flag.	0000h	R/W
07h	Alert Limit Register	Contains the limit value to compare to the selected Alert function.	0000h	R/W
FEh	Manufacturer ID Register	Contains unique manufacturer identification number.	190Fh	R
FFh	Die ID Register	Contains unique die identification number.	0000h	R

Configuration Register (00h) (Read/Write)

The Configuration Register controls system reset and the operating modes for the device, the conversion time settings for the shunt and bus voltage measurements as well as the averaging mode used. The program of the operating mode that decides which signals are selected to be measured is also in the Configuration Register.

The Configuration Register can be read from at any time without changing the device configuration and conversion progress. Any one ongoing conversion will be stopped by writing to the Configuration until the write operation is finished, causing a new conversion beginning based on the new contents in the Configuration Register (00h). This break will avoid any uncertainty in the conditions used for the next completed conversion.

<table>
<tr><th colspan="4">Configuration Register (00h) (Read/Write) Descriptions</th></tr>
<tr><th>Bit No.</th><th>Bit Name</th><th>Por Value</th><th>Description</th></tr>
<tr><td>D15</td><td>RST</td><td>0</td><td>Reset Bit
Setting this bit to '1' resets all registers to default values; this bit self-clears.</td></tr>
<tr><td>D14</td><td></td><td>1</td><td></td></tr>
<tr><td>D13</td><td></td><td>0</td><td></td></tr>
<tr><td>D12</td><td></td><td>0</td><td></td></tr>
<tr><td>D11</td><td>AVG2</td><td>0</td><td rowspan="3">Averaging Mode
Roles in the number of samples that are collected and averaged. The following table displays all the AVG bit settings and related number of averages for each bit setting.
<table>
<tr><th>AVG[2:0]</th><th>NUMBER OF AVERAGES</th></tr>
<tr><td>000</td><td>1</td></tr>
<tr><td>001</td><td>4</td></tr>
<tr><td>010</td><td>16</td></tr>
<tr><td>011</td><td>64</td></tr>
<tr><td>100</td><td>128</td></tr>
<tr><td>101</td><td>256</td></tr>
<tr><td>110</td><td>512</td></tr>
<tr><td>111</td><td>1024</td></tr>
</table></td></tr>
<tr><td>D10</td><td>AVG1</td><td>0</td></tr>
<tr><td>D9</td><td>AVG0</td><td>0</td></tr>
<tr><td>D8</td><td>VBUSCT2</td><td>1</td><td rowspan="3">Bus Voltage Conversion Time
Gives the conversion time for the bus voltage measurement. The following table displays the VBUSCT bit options and related conversion times for each bit setting.
<table>
<tr><th>VBUSCT[2:0]</th><th>CONVERSION TIME</th></tr>
<tr><td>000</td><td>140us</td></tr>
<tr><td>001</td><td>204us</td></tr>
<tr><td>010</td><td>332us</td></tr>
<tr><td>011</td><td>588us</td></tr>
<tr><td>100</td><td>1.1ms</td></tr>
<tr><td>101</td><td>2.116ms</td></tr>
<tr><td>110</td><td>4.156ms</td></tr>
<tr><td>111</td><td>8.244ms</td></tr>
</table></td></tr>
<tr><td>D7</td><td>VBUSCT1</td><td>0</td></tr>
<tr><td>D6</td><td>VBUSCT0</td><td>0</td></tr>
</table>

<table>
<tr><td>D5</td><td>VSHCT2</td><td>1</td><td rowspan="3">Shunt Voltage Conversion Time
Gives the conversion time for the shunt voltage measurement. The following table displays the VSHCT bit options and related conversion times for each bit setting.
<table><tr><th>VSHCT[2:0]</th><th>CONVERSION TIME</th></tr><tr><td>000</td><td>140us</td></tr><tr><td>001</td><td>204us</td></tr><tr><td>010</td><td>332us</td></tr><tr><td>011</td><td>588us</td></tr><tr><td>100</td><td>1.1ms</td></tr><tr><td>101</td><td>2.116ms</td></tr><tr><td>110</td><td>4.156ms</td></tr><tr><td>111</td><td>8.244ms</td></tr></table></td></tr>
<tr><td>D4</td><td>VSHCT1</td><td>0</td></tr>
<tr><td>D3</td><td>VSHCT0</td><td>0</td></tr>
<tr><td>D2</td><td>MODE2</td><td>1</td><td rowspan="3">Operating Mode
Selects continuous, triggered, or power-down mode of operation. These bits default to continuous shunt and bus measurement mode. The mode settings are shown as below.
<table><tr><th>MODE[2:0]</th><th>MODE</th></tr><tr><td>000</td><td>Power-Down (or Shutdown)</td></tr><tr><td>001</td><td>Shunt Voltage, Triggered</td></tr><tr><td>010</td><td>Bus Voltage, Triggered</td></tr><tr><td>011</td><td>Shunt and Bus, Triggered</td></tr><tr><td>100</td><td>Power-Down (or Shutdown)</td></tr><tr><td>101</td><td>Shunt Voltage, Continuous</td></tr><tr><td>110</td><td>Bus Voltage, Continuous</td></tr><tr><td>111</td><td>Shunt and Bus, Continuous</td></tr></table></td></tr>
<tr><td>D1</td><td>MODE1</td><td>1</td></tr>
<tr><td>D0</td><td>MODE0</td><td>1</td></tr>
</table>

Shunt Voltage Register (01h) (Read-Only)

The Shunt Voltage Register stores voltage reading across the shunt resistor, V_{SHUNT}, which is represented in two's complement format. This register will display the averaged value on condition that it is set by the user.

Full-scale range = 81.9175mV (hexadecimal= 7FFF); LSB= 2.5μV.

Shunt Voltage Register (01h) (Read-Only) Description																
BIT NO.	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	SIGN	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bus Voltage Register (02h) (Read-Only)

The Bus Voltage Register is used to store the most recent bus voltage reading, VBUS. Notes: this register displays the averaged value, when averaging is enabled.

Full-scale range = 40.96V (hexadecimal = 7FFF); LSB = 1.25mV.

Bus Voltage Register (02h) (Read-Only) Description																
BIT NO.	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	-	BD14	BD13	BD12	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Power Register (03h) (Read-Only)

This register displays the averaged value, when averaging is enabled.

The value of the Power Register LSB is internally programmed 25 times than the programmed value of the Current_LSB.

The power in Watts recorded by the Power Register is equal to multiply the decimal values of the Bus Voltage Register with the decimal values of the Current Register, as shown in Equation (7).

Power Register (03h) (Read-Only) Description																
BIT NO.	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Current Register (04h) (Read-Only)

If averaging is enabled, this register displays the averaged value. As shown in Equation (4), the value of the Current Register is equal to multiply the decimal value of the Calibration Register with the decimal value of the Shunt Voltage Register.

Current Register (04h) (Read-Only) Register Description																
BIT NO.	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	CSIGN	CD 14	CD 13	CD 12	CD 11	CD 10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Calibration Register (05h) (Read/Write)

This register has four main functions: (1) store the value of the shunt resistor which is used to produce the measured differential voltage; (2) set the resolution of the Current Register; (3) set the Current_LSB and the Power_LSB; (4) the overall system calibration.

Calibration Register (05h) (Read/Write) Description																
BIT NO.	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	-	FS14	FS13	FS12	FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mask/Enable Register (06h) (Read/Write)

The Mask/Enable Register controls the Alert pin as well as how that pin functions. If multiple functions are enabled, the higher significant bit position Alert Function (D15-D11) takes the higher priority and responds to the Alert Limit Register.

Mask/Enable Register (06h) (Read/Write)			
BIT NO.	**BIT NAME**	**POR VALUE**	**DESCRIPTION**
D15	COL	0	**Current Over-Voltage** Setting this bit high configures the Alert pin to be asserted if the shunt voltage measurement following a conversion exceeds the value programmed in the Alert Limit Register.
D14	CUL	0	**Current Under-Voltage** Setting this bit high configures the Alert pin to be asserted if the shunt voltage measurement following a conversion drops below the value programmed in the Alert Limit Register.
D13	BOL	0	**Bus Voltage Over-Voltage** Setting this bit high configures the Alert pin to be asserted if the bus voltage measurement following a conversion exceeds the value programmed in the Alert Limit Register.
D12	BUL	0	**Bus Voltage Under-Voltage** Setting this bit high configures the Alert pin to be asserted if the bus voltage measurement following a conversion drops below the value programmed in the Alert Limit Register.
D11	POL	0	**Power Over-Limit** Setting this bit high configures the Alert pin to be asserted if the Power calculation made following a bus voltage measurement exceeds the value programmed in the Alert Limit Register.
D10	CNVR	0	**Conversion Ready** Setting this bit high configures the Alert pin to be asserted when the Conversion Ready Flag, Bit 3, is asserted indicating that the device is ready for the next conversion.
D9	-	0	
D8	-	0	
D7	-	0	
D6	-	0	
D5	-	0	
D4	AFF	0	**Alert Function Flag** While only one Alert Function can be monitored at the Alert pin at a time, the Conversion Ready can also be enabled to assert the Alert pin. Reading the Alert Function Flag following an alert allows the user to determine if the Alert Function was the source of the Alert. When the Alert Latch Enable bit is set to Latch mode, the Alert Function Flag bit clears only when the Mask/Enable Register is read. When the Alert Latch Enable bit is set to Transparent mode, the Alert Function Flag bit is cleared following the next conversion that does not result in an Alert condition.
D3	CVRF	0	**Conversion Ready Flag** Although the device can be read at any time, and the data from the last conversion is available, the Conversion Ready Flag bit is provided to help coordinate one-shot or triggered conversions. The Conversion Ready Flag bit is set after all conversions, averaging, and multiplications are complete. Conversion Ready Flag bit clears under the following conditions: 1.) Writing to the Configuration Register (except for Power-Down selection) 2.) Reading the Mask/Enable Register

D2	OVF	0	**Math Overflow Flag** This bit is set to '1' if an arithmetic operation resulted in an overflow error. It indicates that current and power data may be invalid.
D1	APOL	0	**Alert Polarity bit; sets the Alert pin polarity.** 1 = Inverted (active-high open collector) 0 = Normal (active-low open collector) (default)
D0	LEN	0	**Alert Latch Enable** Configures the latching feature of the Alert pin and Alert Flag bits. 1 = Latch enabled 0 = Transparent (default) When the Alert Latch Enable bit is set to Transparent mode, the Alert pin and Flag bit resets to the idle states when the fault has been cleared. When the Alert Latch Enable bit is set to Latch mode, the Alert pin and Alert Flag bit remains active following a fault until the Mask/Enable Register has been read.

Alert Limit Register (07h) (Read/Write)

The Alert Limit Register contains the limit value for the alert event selected in the Mask/Enable Register. If the corresponding register exceeds the limit value, an alarm occurs.

Alert Limit Register (07h) (Read/Write) Description																
BIT NO.	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	AUL15	AUL14	AUL13	AUL12	AUL11	AUL10	AUL9	AUL8	AUL7	AUL6	AUL5	AUL4	AUL3	AUL2	AUL1	AUL0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Manufacturer ID Register (FEh) (Read-Only)

The Manufacturer ID Register stores a unique identification number for the manufacturer.

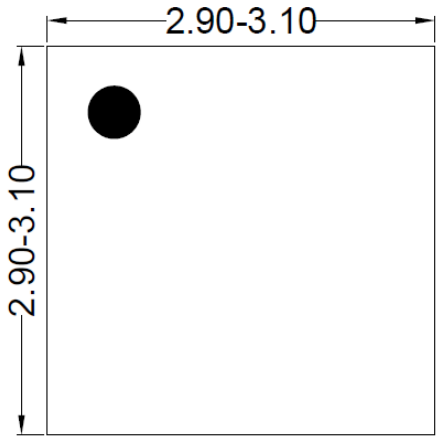
Manufacturer ID Register (FEh) (Read-Only) Description																
BIT NO.	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
POR VALUE	0	0	0	1	1	0	0	1	0	0	0	0	1	1	1	1

Die ID Register (FFh) (Read-Only)

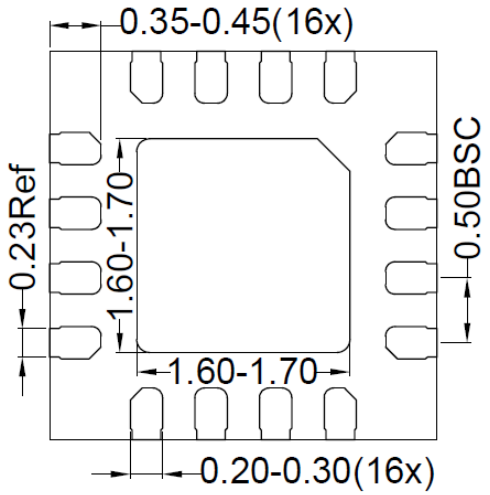
The Die ID Register stores a unique identification number and the revision ID for the die.

Die ID Register (FFh) (Read-Only) Description																
BIT NO.	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	DID11	DID10	DID9	DID8	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0	RID3	RID2	RID1	RID0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

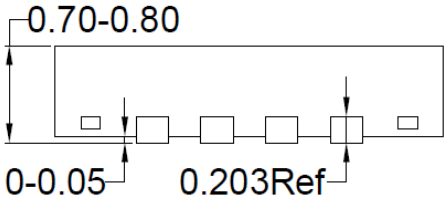
QFN3x3-16 Package outline



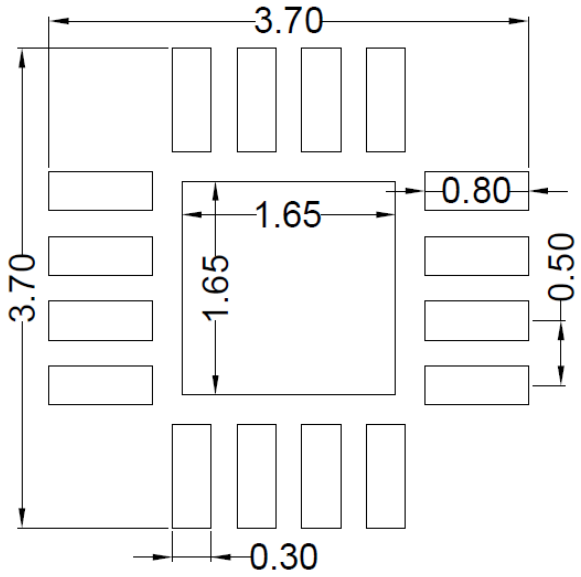
Top View



Bottom View



Front View

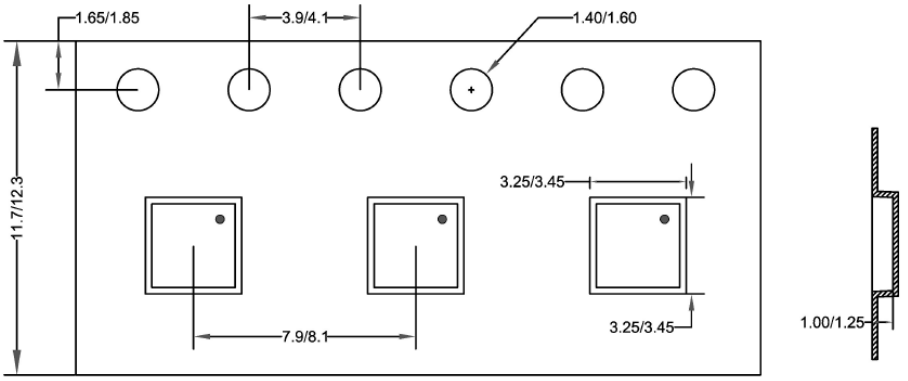


Recommended PCB layout
(reference only)

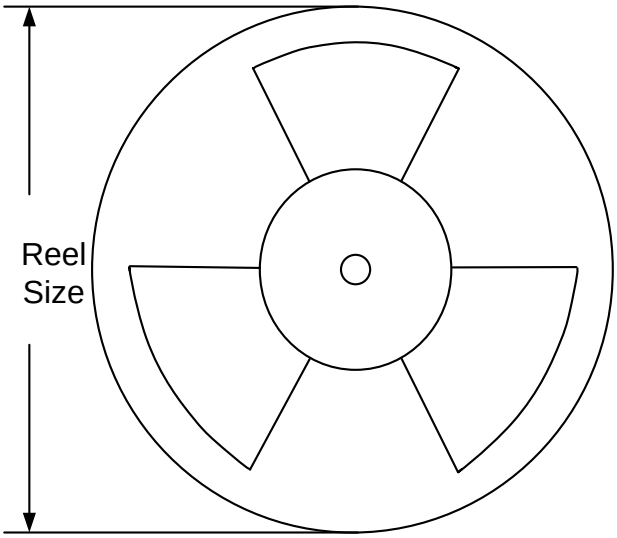
Note: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

1. Taping Orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
QFN3x3-16	**12**	**8**	**12"**	**400**	**400**	**5000**

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
March. 15, 2026	Revision 1.0	Initial Release.

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