SY50428

PWM/PFM Mode SSR Flyback Converter

General Description

The SY50428 is an SSR (Secondary Side Regulation) flyback converter featuring PWM/PFM (Pulse Width Modulation/Pulse Frequency Modulation) operating mode and a 100kHz rated switching frequency. It integrates a 800V power MOSFET within a DIP7 package. HV (High Voltage) start up is integrated on DRAIN pin to minimize load loss. It uses a pseudo-fixed frequency control strategy to avoid sub-harmonic oscillation under CCM (Continuous Conduction Mode). SY50428 enters frequency fold-back mode when the load decreases to achieve a high average efficiency. Under light load conditions, it enters burst mode for high efficiency. The device uses switching frequency modulation function to reduce EMI (Electro-Magnetic Interference) noise, and features a soft-start process to reduce current on the power MOSFET during Vin start up.

The SY50428 provides reliable protections including programmable input BO (Brown Out) / OVP (Over Voltage Protection), VCC OVP, OLP (Over Load Protection), OTP (Over Temperature Protection), and secondary diode SCP (Short Circuit Protection).

The SY50428 is available in a compact DIP7 package.

Features

- Secondary Side Regulation
- Integrated 800V Power MOSFET
- HV Start-Up
- 100kHz Switching Frequency
- Pseudo-Fixed Frequency Control to Eliminate Slope Compensation for CCM (Duty Cycle>50%)
- PFM Control for High Average Efficiency
- Burst Mode Control for High Light Load Efficiency
- 23.5kHz Minimum Switching Frequency to Eliminate Audible Noise
- Frequency Modulation to Reduce EMI Noise
- Internal Soft-Start Process
- Programmable Input BO/OVP Through PRT Pin
- OLP, VCC OVP, OTP, Secondary Diode SCP
- Compact Package: DIP7

Applications

- Home Appliances
- AC/DC Adapters

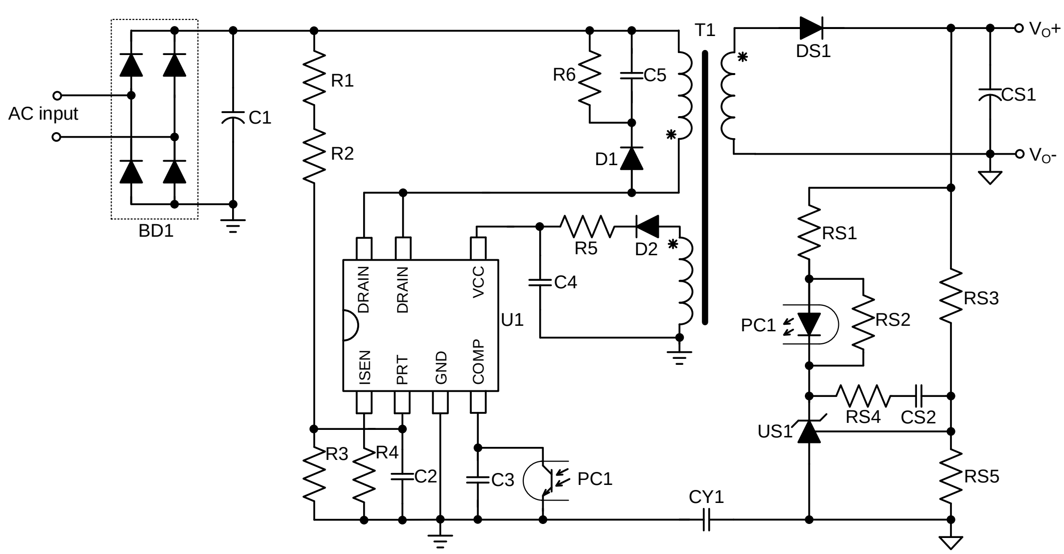


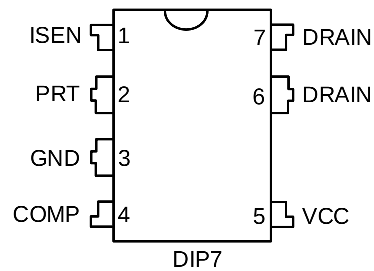
Fig. 1. Typical Application Circuit

Ordering Information

Ordering Part Number	Package type	Top Mark
SY50428FIB	DIP7 RoHS-Compliant and Halogen-Free	**AAWRxyz**

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin number	Pin Name	Pin Description
1	ISEN	Primary current sensing pin.
2	PRT	BO/input OVP protection, programmable by external resistor divider. Short this pin to GND if BO/input OVP is not used.
3	GND	Ground pin.
4	COMP	Output feedback pin. Directly connect to an opto-coupler.
5	VCC	IC supply pin.
6,7	DRAIN	DRAIN terminal of internal power MOSFET, HV start up.

Block Diagram

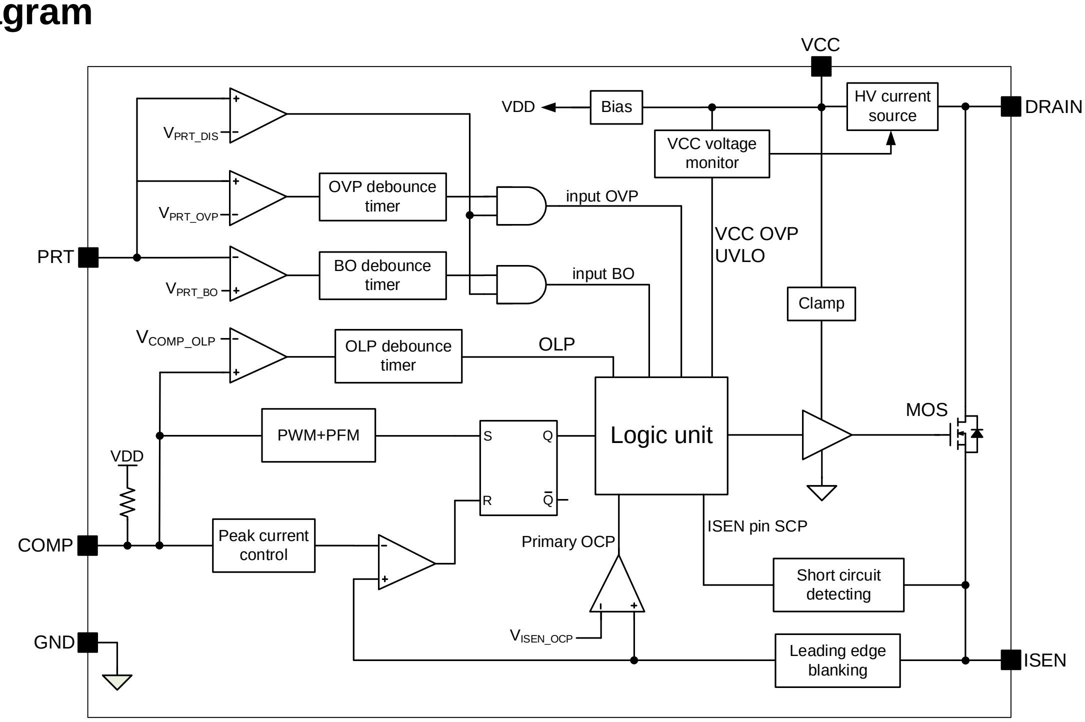


Fig.2 Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
DRAIN	-0.3	800	V
VCC	-0.3	32	
ISEN	-0.3	20	
COMP	-0.3	25	
PRT	-0.3	3.5	
Continuous Drain Current (T_A=25℃)		4	A
Pulsed Drain Current (Note 6)		16	
Junction Temperature, Operating	-45	150	°C
Lead Temperature (Soldering, 10 sec.)		260	
Storage Temperature	-60	150	

Thermal Information

Parameter (Note 2)	Min	Max	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance		111.5	°C/W
θ_{JC} Junction-to-Case Thermal Resistance		22	
P_D Power Dissipation T_A = 25°C		1.1	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VCC	10	26	V
Junction Temperature	-40	125	°C
Ambient Temperature	-40	105	

Electrical Characteristics

(V_{VCC}=12V, T_J=25°C unless otherwise specified (Note 4))

Parameter		Symbol	Test conditions	Min	Typ	Max	Unit
DRAIN	BV of Power MOSFET	V_{DS_BV}	V_{COMP}=0V, I_{DRAIN}=250μA	800			V
	ON Resistance of Power MOSFET	R_{DSON}	I_{DRAIN}=200mA,		2.8	3.5	Ω
	Leakage Current	I_{DRAIN_LK}	V_{DRAIN}=800V_{DC}, V_{COMP}=0V			1	μA
	HV Current Source	I_{HV}	V_{DRAIN}=100V_{DC}, V_{VCC}=5V	2.0	2.5	3.0	mA
VCC	Start-Up Current	I_{VCC_ST}	V_{VCC}=V_{VCC_ON}-0.5V	30	40	50	μA
	Turn on Threshold	V_{VCC_ON}	V_{VCC} rising up	15	16	17	V
	HV Current Source Turn on Threshold	V_{VCC_MIN}	V_{VCC} falling down	8.1	9	9.9	V
	Turn Off Threshold	V_{VCC_OFF}	V_{VCC} falling down	7.5	8	8.5	V
	OVP Threshold	V_{VCC_OVP}	V_{VCC} rising up	26	29	32	V
	Current Sink to Clamp VCC	I_{VCC_SINK}	V_{VCC}=V_{VCC_OVP}	4	5	6	mA
	Operating Current	I_{VCC_OPRT}	V_{COMP}=1.8V,(Note 5)		2		mA
	Quiescent Current	I_{VCC_Q}	V_{COMP}=0V	220	250	280	μA
	Current Sink under Fault	I_{VCC_FAULT}		550	650	750	μA
ISEN	Maximum Peak Current Limit	V_{ISEN_MAX}		0.855	0.9	0.945	V
	Primary OCP threshold	V_{ISEN_OCP}		1.0	1.1	1.2	V
	Minimum Peak Current Limit	V_{ISEN_MIN}		165	205	245	mV
	Leading Edge Blanking Time	T_{ISEN_LEB}		300	410	520	ns
	Blanking Time for Pin Short Detection	$T_{ISENSCP\_BLK}$		2.5	3.25	4.0	μs
	Pin Short Threshold	V_{ISEN_SCP}		40	50	60	mV
COMP	Internal Pull Up Voltage	V_{COMP_HIGH}		2.2	2.5	2.8	V
	Internal Pull Up Resistor	R_{COMP}		20	24	28	kΩ
	Threshold to Enter Sleep Mode	V_{COMP_ENSLP}	V_{COMP} falling down	350	400	450	mV
	Threshold to Exit Sleep Mode	V_{COMP_EXSLP}	V_{COMP} rising up	450	500	550	mV
	OLP Threshold	V_{COMP_OLP}	V_{COMP} rising up	2.0	2.15	2.3	V
	OLP Debounce Time	T_{OLP_DBT}	(Note 5)		64		ms
PRT	Brown Out Threshold	V_{PRT_BO}		450	500	550	mV
	Brown In Threshold	V_{PRT_BI}		550	600	650	mV
	Brown Out Debounce Time	T_{BO_DBC}	(Note 5)		64		ms
	OVP Threshold	V_{PRT_OVP}		1.95	2.15	2.35	V
	PRT Function Disable Threshold	V_{PRT_DIS}		80	100	120	mV
Switching Frequency	Rated Switching Frequency	F_{SW_RATE}	V_{COMP}=1.8V	90	100	110	kHz
	Maximum On Time	T_{ON_MAX}		8.5	10.5	12.5	μs
Switching Frequency	Minimum Switching Frequency	F_{SW_MIN}	V_{COMP}=0.6V	20	23.5	27	kHz
Soft Start Process	Soft Start Time	T_{SS}	(Note 5)		3.2		ms

Auto-Recovery	Auto-Recovery Time	T_{AR}	(Note 5)		2		s
Internal OTP	Thermal Shut-Down Threshold	T_{OTP}	(Note 5)	135	150	165	°C
	Hysteresis to Resume Operation`	T_{HYS}	(Note 5)		60		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Chip mounted on low effective single layer PCB.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \approx T_J = 25°C$. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

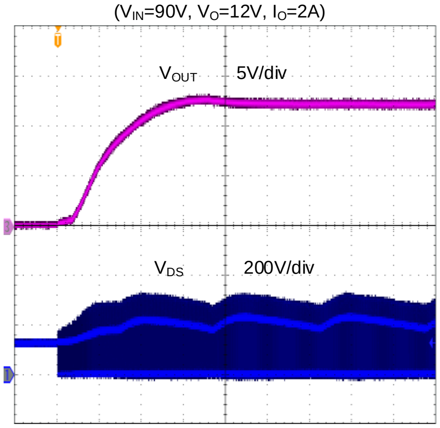
Note 5: Guaranteed by design or statistical correlation and not production tested.

Note 6: Pulse width limited by maximum junction temperature.

Typical Performance Characteristics

Vin start up

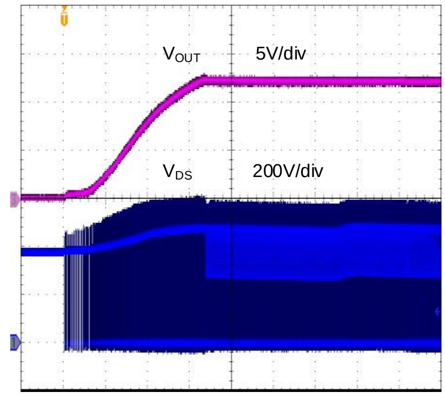
(V_{IN}=90V, V_O=12V, I_O=2A)



Time (4ms/div)

Vin start up

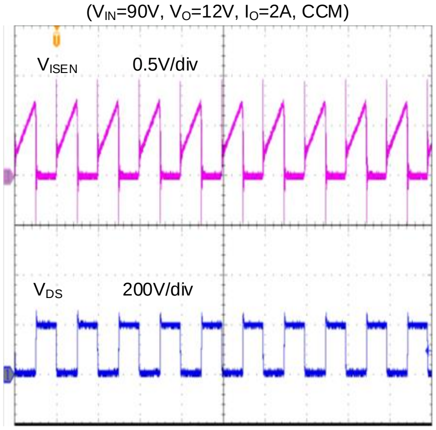
(V_{IN}=264V, V_O=12V, I_O=2A)



Time (2ms/div)

Steady

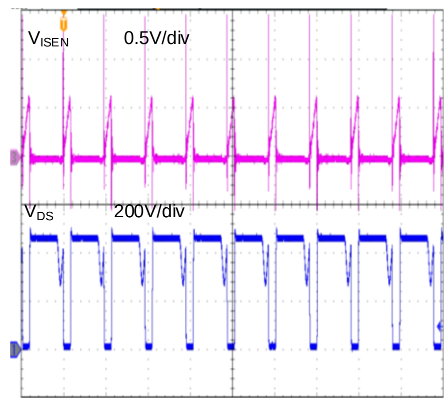
(V_{IN}=90V, V_O=12V, I_O=2A, CCM)



Time (10µs/div)

Steady

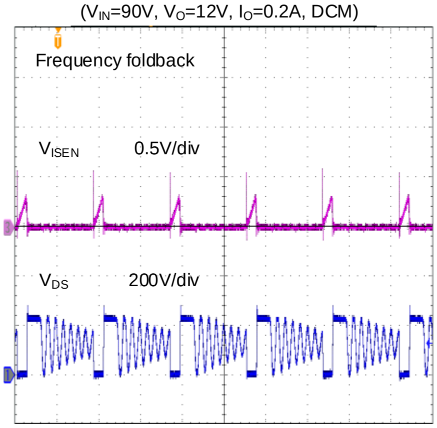
(V_{IN}=264V, V_O=12V, I_O=2A, DCM)



Time (10µs/div)

Steady

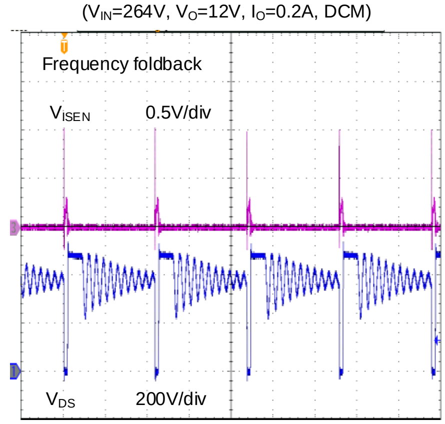
(V_{IN}=90V, V_O=12V, I_O=0.2A, DCM)



Time (10µs/div)

Steady

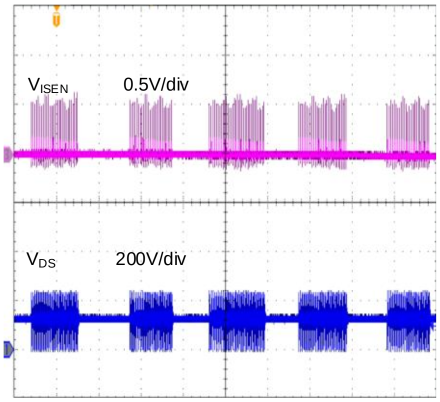
(V_{IN}=264V, V_O=12V, I_O=0.2A, DCM)



Time (10µs/div)

Steady

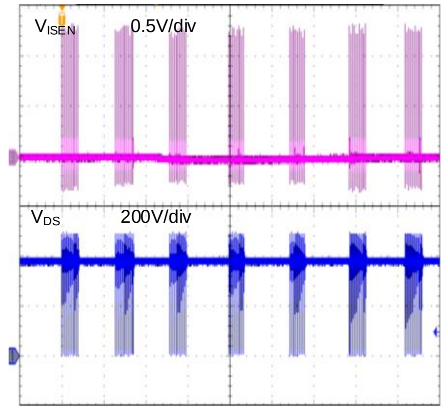
(V_{IN}=90V, V_O=12V, I_O=10mA, burst mode)



Time (1ms/div)

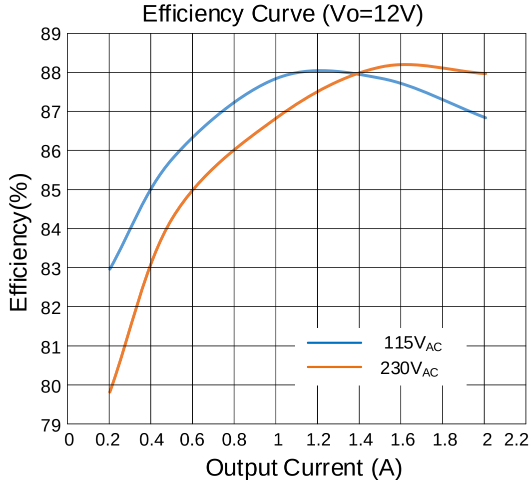
Steady

(V_{IN}=264V, V_O=12V, I_O=10mA, burst mode)



Time (1ms/div)

Efficiency Curve (Vo=12V)



Operation Principles

HV Start up

The SY50428 integrates a high voltage start-up circuit internally connected to the DRAIN pin. A current source I_{HV} is used to charge the VCC pin capacitor. When the VCC pin voltage is charged to V_{VCC_ON} threshold, the current source turns off.

Pseudo Fixed Frequency Control

The SY50428 uses a proprietary Silergy pseudo fixed frequency control to avoid sub-harmonic oscillations when the converter operates under continuous conduction mode (CCM) and a duty-cycle D >50%. Sub-harmonic oscillation is an inherent issue for peak current control architecture. Traditionally, slope compensation is used to avoid this issue. The SY50428 does not need slope compensation, simplifying the design.

Frequency Fold Back Control

The SY50428 uses frequency fold-back control to improve medium and light load efficiency. As the load decreases, the COMP pin voltage is also reduced. When the COMP pin voltage drops below 1.0V, the device begins to decrease its switching frequency. A minimum switching frequency of 23.5kHz is reached when the COMP pin voltage drops to 0.6V. The switching frequency is maintained above 20kHz to minimize audible noise. If the load decreases further, the device enters burst mode. The switching frequency control curve is shown below:

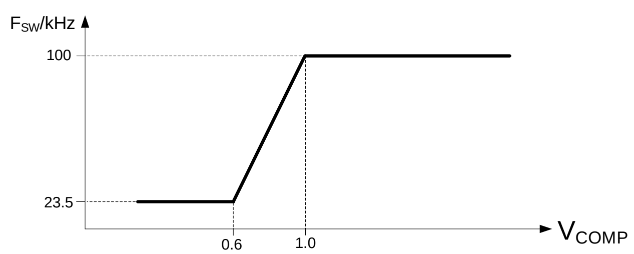


Fig.3 Switching Frequency Curve

Burst Mode

SY50428 uses burst mode control under very light load or no-load conditions. Under very low load, when the COMP pin voltage drops below V_{COMP_ENSLP} (0.4V typ.), the device enters sleep mode, where switching stops and most parts of the internal control circuitry are shut down to save energy. As there is no switching, the output voltage will gradually drop. In this state, the COMP pin voltage starts increasing until reaches the threshold V_{COMP_EXSLP} (0.5V typ.), when the device wakes up and resumes normal operation. This control architecture helps maintain high efficiency during light load mode operation. During burst mode a slightly larger output voltage ripple is expected.

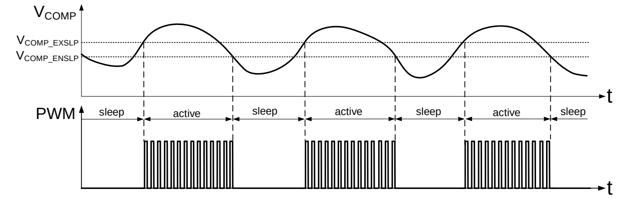


Fig.4 Timing of Burst Operating Mode

Internal Soft Start Process

The SY50428 integrates a soft start, to achieve monotonic output voltage rise, and keep the peak current of the power MOSFET within the safe operating area (SOA). The device gradually increases the peak current set point gradually using 8 distinct steps, until it reaches maximum value (0.9V typ.), and also gradually increases the switching frequency until it reaches its maximum value (100kHz typ.), as shown below:

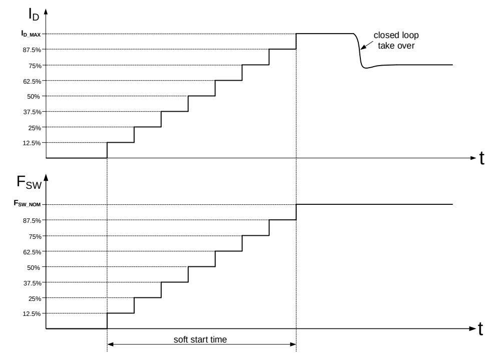


Fig.5 Timing of Soft Start Process

VCC OVP

Under abnormal conditions, such as opto-coupler open circuit or failure, the output voltage will increase along with VCC (VCC is supplied by the auxiliary winding). To avoid device damage caused by a VCC pin overvoltage condition, switching stops as soon as VCC voltage raises above the OVP threshold V_{VCC_OVP} and the device enters auto-recovery mode. Before V_{VCC} reaches V_{VCC_OVP} threshold, a 5mA current sink on the VCC pin will try to clamp VCC pin voltage. As soon as the OVP condition is detected a timer is enabled. When the auto-recovery timer elapses, the device will try to resume normal operation.

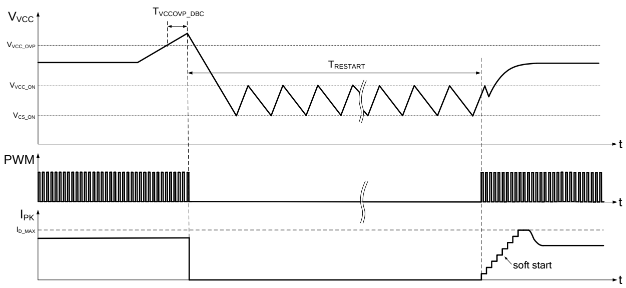


Fig.6 VCC OVP timing

OLP

During overload conditions, the COMP pin voltage will be pulled up to high level, and the peak current will reach the maximum set-point (0.9V typ.). When the COMP pin voltage rises above the OLP threshold, a timer is enabled, and if the COMP pin voltage is continuously higher than the OLP threshold until the timer elapses, the OLP will is triggered, the device stops switching and enters auto-recovery mode by initiating a soft-start sequence. The device stays in auto-recovery mode until the overload condition disappears. When the overload disappears, the converter resumes normal operation.

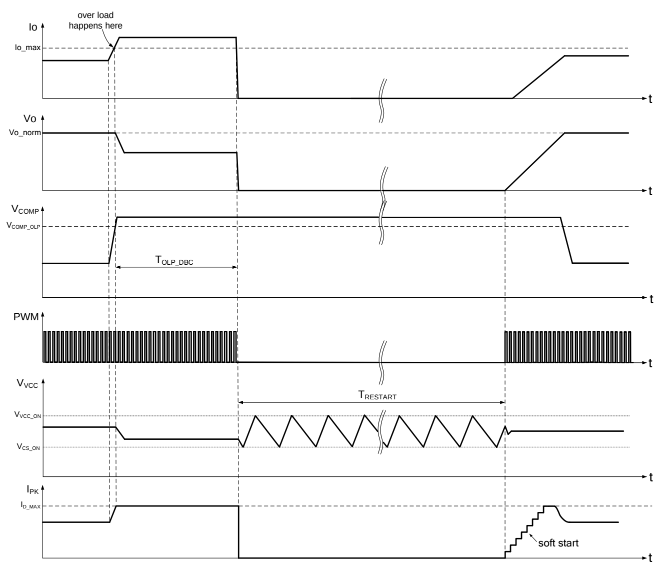


Fig.7 OLP Timing

Secondary Diode Short Circuit Protection

Under secondary side diode short circuit conditions, when the primary power MOSFET is turned on, the primary current of the flyback converter will increase at a very high di/dt rate, after the ISEN pin leading edge blanking time elapses, primary peak current sense voltage V_{ISEN} will be above 0.9V (maximum peak current limit level under normal condition). SY50428 uses a primary OCP threshold V_{ISEN_PRIOCP}, when V_{ISEN} is higher than V_{ISEN_PRIOCP}, and lasts for 4 consecutive switching cycles, secondary diode short circuit protection will be triggered, the device will stop switching and enter auto-recovery mode.

ISEN Pin Short Circuit Protection

The SY50428 will check if the ISEN pin is shorted to GND during the soft start process, when V_{IN} starts rising. When the primary side power MOSFET is turned on, a blanking time $T_{ISENSCP\_BLK}$ (3.25us typ.) is used. After this blanking time elapses, the device will compare the ISEN pin voltage with the internal threshold voltage (50mV typ.). If the ISEN pin voltage is lower than this threshold, an ISEN pin short to GND fault is detected. The device will stop switching and enter auto-recovery mode.

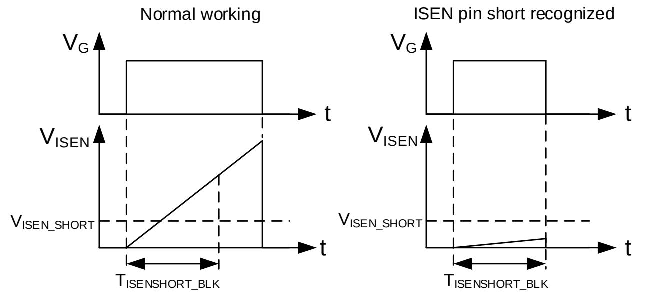


Figure.8 Timing of ISEN Pin Short Detecting

Internal OTP

The SY50428 monitors die temperature under normal operation. Once the die temperature rises above the internal OTP threshold T_{OTP}, the device will stop switching and enter auto-recovery mode. When the die temperature drops below T_{OTP}-T_{HYS}, it will resume normal operation.

Input BO/OVP through PRT Pin

Input brownout (BO) and overvoltage protection (OVP) can be implemented using the PRT pin. A resistor divider (R_1 and R_2) is used to program the threshold as shown in the following figure. During Vin start-up, when VCC rises above the V_{VCC_ON} threshold, the device will check the PRT pin voltage. Only when V_{PRT} is higher than V_{PRT_BI} will the device begin switching.

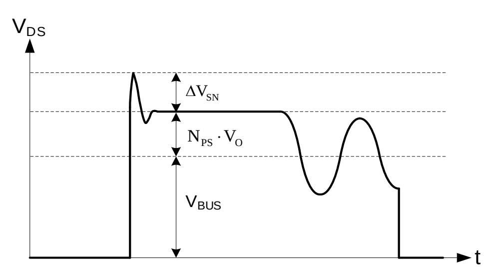


Fig.9 PRT pin configuration

The upper resistor R_1 is selected based on the acceptable power loss of the resistor divider. Assuming maximum allowed power loss of the resistor divider is P_{RD}, R_1 should be selected as shown by the formula below:

$$R_1 > \frac{2V_{IN}^2}{P_{RD}}$$

With R_1 selected, R_2 can be calculated based on R_1 value and the customer defined input BO threshold V_{IN_BO} (RMS value), as shown in the formula below:

$$R_2 = R_1\left(\frac{V_{PRT\_BO}}{\sqrt{2}V_{IN\_BO} - V_{PRT\_BO}}\right)$$

It is recommended to place capacitor C_1 between the PRT pin and GND pin for switching noise suppression. The recommended value range for C_1 is: 1nF~10nF.

The input OVP threshold is proportional to the input BO threshold. This ratio is fixed to 4.3 (typical value), as shown below:

$$V_{IN\_OVP} = 4.3V_{IN\_BO}$$

If PRT pin input BO/OVP protection is not used, it is recommended to directly short PRT pin to GND.

Power Supply Design Guard

BUS Capacitor Calculation

Generally, the bulk capacitor C_{BUS} is selected according to the following rules:

1~2uF per watt of input power

$$C_{BUS\_MIN} = (1.0 \cdot P_{IN})uF$$

$$C_{BUS\_MAX} = (2.0 \cdot P_{IN})uF$$

The BUS capacitor can be selected according to the acceptable voltage ripple $\triangle V_{BUS}$, under minimum AC input voltage and full load conditions, as shown in the figure below:

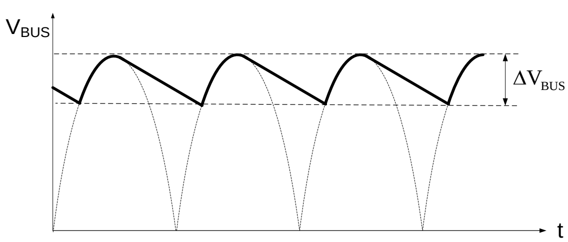


Fig.10 Illustration of Voltage Ripple on BUS Capacitor

With the voltage ripple $\triangle V_{BUS}$ selected, then the BUS capacitor value can be calculated as shown below:

$$C_{BUS} = \frac{P_O}{\eta \cdot \pi \cdot f_{AC} \cdot \Delta V_{BUS}} \cdot \frac{\arcsin\left(1 - \frac{\Delta V_{BUS}}{\sqrt{2} \cdot V_{IN\_MIN}}\right) + \frac{\pi}{2}}{2\sqrt{2} \cdot V_{IN\_MIN} - \Delta V_{BUS}}$$

Where P_O is rated output power, $\triangle V_{BUS}$ is target voltage ripple on the BUS capacitor, η is converter efficiency, f_{AC} is frequency of AC input voltage and V_{IN_MIN} is the minimum AC input voltage.

Transformer Parameter Calculation

(1) Primary/Secondary Turns Ratio: N_{PS}

The maximum allowed N_{PS} is limited by the allowed voltage across the primary power MOSFET:

$$N_{PS} \le \frac{V_{MOS\_BR} \cdot K_{DR} - \sqrt{2} \cdot V_{IN\_MAX} - \Delta V_{SN}}{V_O}$$

Where V_{MOS_BR} is the breakdown voltage of the primary MOSFET, K_{DR} is V_{DS} de-rating factor of the MOSFET, ΔV_{SN} is peak voltage generated when the primary MOSFET is turned off, and V_O is the output voltage.

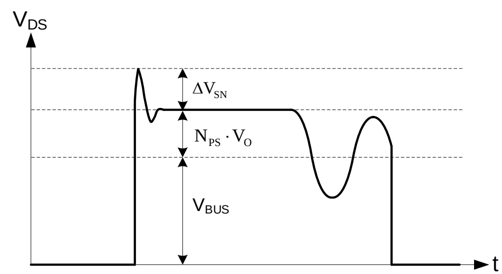


Fig.11 DRAIN Waveform of Primary MOS

Primary Inductance: L_M

The primary inductance of the transformer is related to the primary current ripple. Generally, the primary side current ripple is defined as shown in the figure below, and current ripple factor is defined using the following equation:

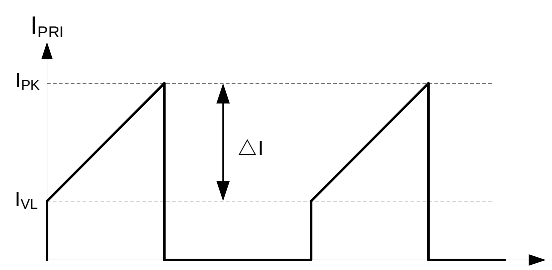


Fig.12 Illustration of Primary Current Ripple under CCM

$$K_{RP} = \frac{0.5 \cdot \Delta I}{I_{PK} - 0.5 \cdot \Delta I}$$

K_{RP}<1: CCM

K_{RP}=1: BCM

Generally, to achieve optimized transformer size and efficiency for universal input voltage applications, under low input and full load conditions, CCM operation is selected, and under high input condition and full load condition, DCM mode is selected.

Under the lowest input and full load conditions, it is recommended to choose K_{RP} between 0.3~0.6 for optimized performance. With K_{RP} selected, primary inductance of transformer is calculated as shown below:

$$L_M = \frac{V_{BUS\_MIN}^2 \cdot D_{MAX}^2 \cdot \eta}{2 \cdot P_O \cdot f_{SW} \cdot K_{RP}}$$

Where f_{SW} is rated switching frequency, P_O is rated output power, η is converter efficiency. D_{MAX} is maximum duty cycle at V_{BUS_MIN} and rated output power, and D_{MAX} is calculated as follows:

$$D_{MAX} = \frac{N_{PS} \cdot V_O}{V_{BUS\_MIN} + N_{PS} \cdot V_O}$$

(2) Turns of Primary Winding

(a) Select the magnetic core type, identify the effective cross-sectional area A_E

(b) Preset the maximum magnetic flux density B_{MAX} at minimum BUS voltage and full load condition:

$$B_{MAX}=0.2T\sim0.3T$$

(c) Calculate maximum primary peak current I_{PK} at rated output power:

$$I_{PK} = \frac{V_O \cdot I_O \cdot (1+K_{RP})}{V_{BUS\_MIN} \cdot D_{MAX} \cdot \eta}$$

(d) Calculate primary turns: N_P

$$N_P = \frac{L_M \cdot I_{PK}}{B_{MAX} \cdot A_E}$$

Where A_E is effective cross-sectional area of core

(3) Turns of Secondary Winding: N_S

$$N_S = \frac{N_P}{N_{PS}}$$

(4) Turns of auxiliary winding: N_A

Before calculating auxiliary turns, the VCC pin voltage supplied by auxiliary winding should be predefined first. Generally, VCC pin voltage under heavy load condition should be pre-set to 12V~15V, then auxiliary turns are calculated as:

$$N_A = \frac{V_{CC\_MIN} \cdot N_S}{V_O}$$

The worst case for the VCC pin voltage is under zero load conditions. Auxiliary winding turns should be fine-tuned according to the actual VCC pin voltage under these conditions.

Peak Current Sense Resistor Calculation

Under minimum AC input voltage conditions, when the BUS voltage is at its peak value and primary peak current reaches the ISEN pin maximum set-point, the maximum output current is reached (overcurrent protection threshold). For the OCP threshold, primary peak current is calculated as shown:

$$D_{OCP} = \frac{N_{PS} \cdot V_O}{\sqrt{2} \cdot V_{IN\_MIN} + N_{PS} \cdot V_O}$$

$$I_{PK\_MAX} = \frac{P_O \cdot K_{OCP}}{\sqrt{2} \cdot V_{IN\_MIN} \cdot D_{OCP} \cdot \eta} + \frac{\sqrt{2} \cdot V_{IN\_MIN} \cdot D_{OCP}}{2 \cdot L_M \cdot f_{SW}}$$

Where K_{OCP} is OCP safety coefficient, generally set to 120%~150%.

$$K_{OCP} = \frac{I_{O\_OCP}}{I_O}$$

After the maximum primary peak current has been calculated, the sense resistor R_{ISEN} can be easily derived using the equation below:

$$R_{ISEN} = \frac{V_{ISEN\_MAX}}{I_{PK\_MAX}}$$

Where V_{ISEN_MAX} is ISEN pin current sense voltage threshold (typical=0.9V).

Note: The current sense resistor needs to be fine tuned according to the converter's measured OCP point. If the OCP point is higher than the target, R_{ISEN} should be increased, if the OCP point is lower than target level, R_{ISEN} should be decreased.

Secondary Rectification Diode Selection

Under the conditions of the maximum BUS voltage and maximum output voltage, the reverse voltage of the secondary rectification diode will reach maximum level. The maximum value of diode reverse voltage is calculated as shown below:

$$V_{DS(SR)\_MAX} = \frac{\sqrt{2} \cdot V_{IN\_MAX}}{N_{PS}} + V_{O\_MAX} + V_{SPIKE}$$

Where V_{IN_MAX} is maximum AC input voltage, N_{PS} is the primary/secondary turns ratio of the transformer, V_{O_MAX} is maximum output voltage and V_{SPIKE} is the voltage peak generated when the primary MOSFET is turned on.

Maximum peak current of SR MOSFET is calculated as shown below:

$$I_{D(SR)\_MAX} = I_{PK\_MAX} \cdot N_{PS}$$

Where I_{PK_MAX} is the maximum primary peak current at V_{BUS_MIN} and OCP point.

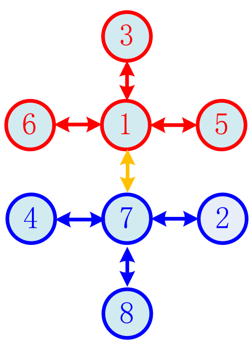
Layout Considerations

A proper PCB design must adhere to the following guidelines:

(a) To achieve good EMI performance and reduce the line frequency voltage ripple, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

(b) The circuit loop of all switching circuits should be kept as small as possible: primary power loop, secondary loop and auxiliary power loop.

(c) The connection of primary ground is recommended as shown:



Ground ①: Ground of BUS capacitor

Ground ②: Ground of VCC pin capacitor

Ground ③: Ground node of auxiliary winding

Ground ④: Ground node of PRT pin resistor divider

Ground ⑤: Ground of primary side Y capacitor

Ground ⑥: Ground of current sense resistor

Ground ⑦: Ground pin of SY50428

Ground ⑧: Ground of opto-coupler receiver

(d) Bias supply trace should be connected to the bias supply capacitor first and then to the GND pin. The bias supply capacitor should be placed near the device.

(e) The switching loop formed by ISEN pin – current sense resistor – GND pin should be kept as small as possible.

(f) The resistor divider connected to the PRT pin is recommended to be placed close to the device.

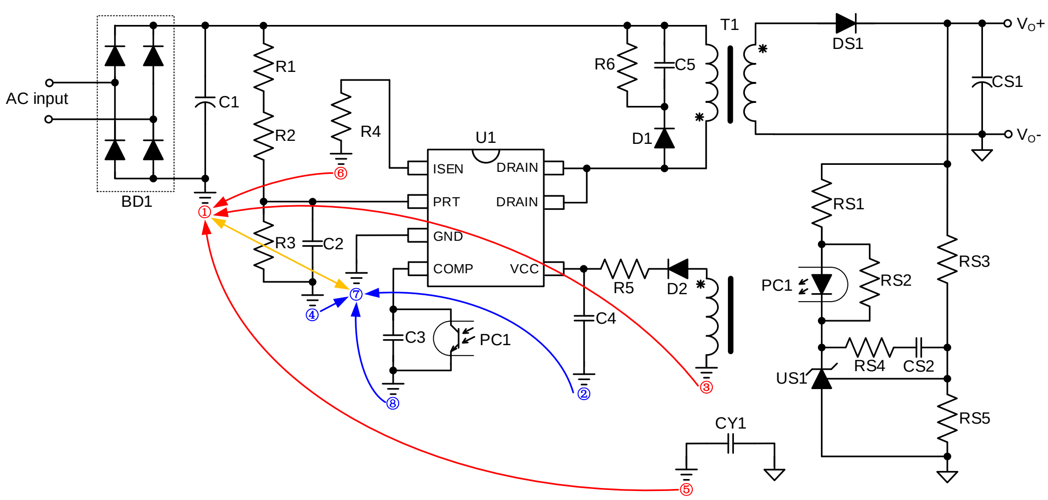


Figure 13. PCB Layout Suggestion

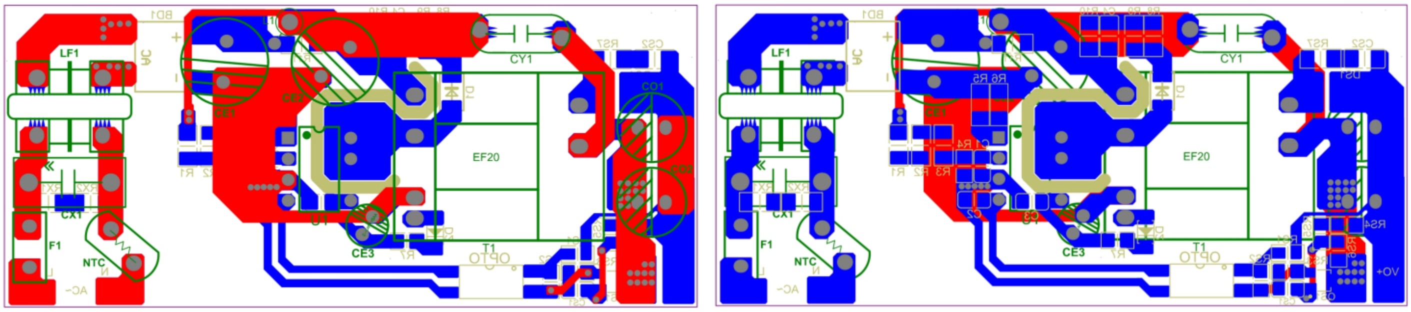


Figure 14. PCB Layout Suggestion

Typical Application Schematic

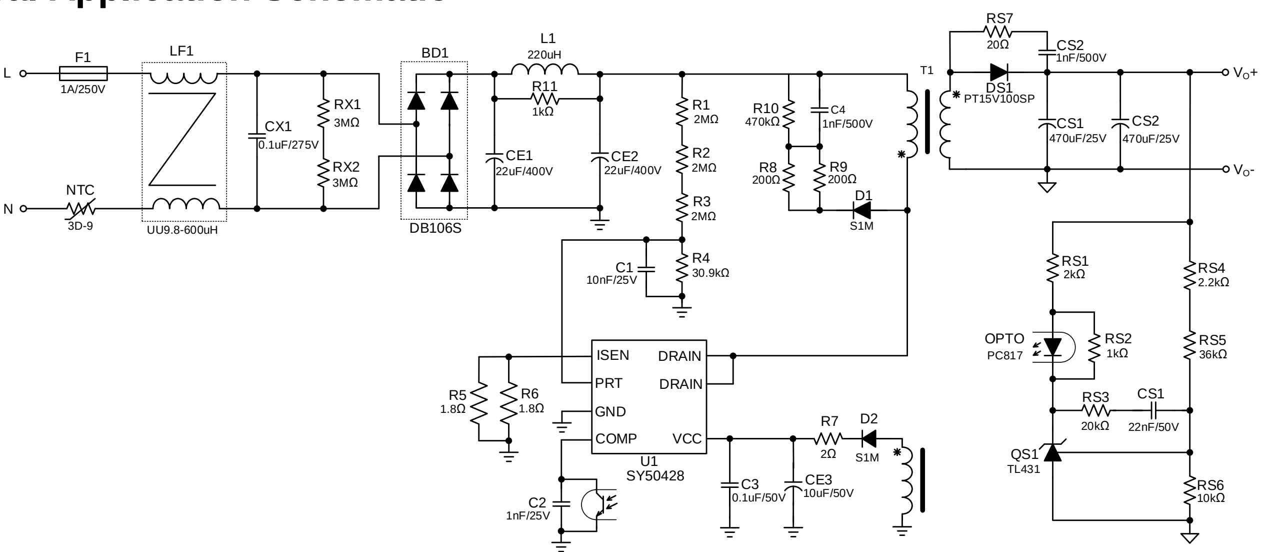


Figure 15. 24W Auxiliary Power Supply Application Circuit

Recommended BOM List

Designator	Description	Part Number	Manufacturer
F1	Fuse, 1A/250V	T1A 250V	jdtfuse
NTC	Thermistor	3D-9	/
CX1	X cap	0.1uF/275Vac	TENTA
RX1,RX2	X cap discharge resistor, 3MΩ, 1206	1206W4J0305T5E	UNI-ROYAL
LF1	Common mode choke	UU9.8-600uH	/
BD1	Full bridge rectifier	DB107S	GOODWORK
L1	Inductor, 220uH, 0510, 1W	220uH	/
CE1, CE2	Electrolytic capacitor, 22μF/400V	22uF400V87EC0267	AiSHi
CE3	Electrolytic capacitor, 10μF/50V	10uF50V87EC0267	AiSHi
R1,R2,R3	SMD resistor, 2MΩ, 1206	1206W4J0205T5E	UNI-ROYAL
R4	SMD resistor, 30.9kΩ, 0805	0805W8J03092T5E	UNI-ROYAL
R5,R6	SMD resistor, 1.8Ω, 1206	1206W4J0201T5E	UNI-ROYAL
R7	SMD resistor, 2Ω, 0805	1206W4J0751T5E	UNI-ROYAL
R8,R9	SMD resistor, 200Ω, 1206	1206W4J0201T5E	UNI-ROYAL

R10	SMD resistor, 470kΩ, 1206	1206W4J0474T5E	UNI-ROYAL
R11	SMD resistor, 1kΩ, 1206	1206W4J0102T5E	UNI-ROYAL
C1	SMD capacitor, 10nF/25V, 0805	0805B103K500NT	FH
C2	SMD capacitor, 1nF/25V, 0805	0805B102K500NT	FH
C3	SMD capacitor, 0.1uF/50V, 0805	0805B105K500NT	FH
C4	SMD capacitor, 1nF/500V, 1206	CC1206KRX5R8BB102	YAGEO
D1	Diode, 1A/1000V, SMA	S1M	DIODES
D2	Diode, 1A/1000V, SOD-123F	S1M	DIODES
U1	FLYBACK switcher, DIP7	SY50428FIB	Silergy
T1	Transformer	EF20, Lm=800uH	/
OPTO	Opto-coupler	PC817	Sharp
CY1	Y cap, 100pF/Y1/400V	CY1101KE1IEB45W2A2	Dersonic
RS1	SMD resistor, 2kΩ, 0805	0805W8J0202T5E	UNI-ROYAL
RS2	SMD resistor, 1kΩ, 0805	0805W8J0102T5E	UNI-ROYAL
RS3	SMD resistor, 20kΩ, 0805	0805W8J0203T5E	UNI-ROYAL
RS4	SMD resistor, 2.2kΩ, 0805	0805W8J0222T5E	UNI-ROYAL
RS5	SMD resistor, 36kΩ, 0805	0805W8J0363T5E	UNI-ROYAL
RS6	SMD resistor, 10kΩ, 0805	0805W8J0103T5E	UNI-ROYAL
RS7	SMD resistor, 20Ω, 1206	1206W4J0200T5E	UNI-ROYAL
CS1	SMD capacitor, 22nF/25V, 0805	0805B223K500NT	FH
CS2	SMD capacitor, 1nF/500V, 1206	CC1206KRX7RBBB102	FH
CO1,CO2	Electrolytic capacitor, 470uF/25V	470uF25V87EC0267	AiSHi
DS1	Diode, 15A/100V	PT15V100SP	PFC
US1	Shunt voltage reference	TL431	HKT

Design Example of 24W Power Supply (SY50428)

A design example of typical application is shown step by step below.

Input/Output Specifications

Parameter	Symbol	Value
Input Voltage Range	V_{IN}	90~264Vac
AC Input Frequency	f_{AC}	50Hz
Rated Output Power	P_O	24W
Rated Output Voltage	V_O	12V
Rated Output Current	I_O	2A
OCP Proportion	K_{OCP}	130%

Preset Parameters

Parameters	Symbol	Value
Break-down Voltage of Power MOSFET	V_{MOS_BR}	800V
V_{DS} De-rating Factor of Power MOSFET	K_{DR}	85%
Spike on V_{DS} During Power MOSFET Turn Off	ΔV_{SN}	120V
Converter Efficiency	η	87%
Primary CCM Current Ripple Factor at 90Vac and Full Load	K_{RP}	0.45
Voltage Ripple on BUS Capacitor	ΔV_{BUS}	45
Transformer Effective Cross-Sectional Area (EF20)	A_E	33.5mm^2
Peak Voltage on the Secondary Rectifying Diode	V_{SPIKE}	10V
Power Loss of PRT Pin Resistor Divider	P_{RD}	25mW
Input BO Threshold	V_{IN_BO}	70Vac

1) BUS Capacitor Selection

Voltage ripple on BUS capacitor is set to: ΔV_{BUS}=45V

$$C_{BUS}=\frac{P_O}{\eta\cdot\pi\cdot f_{AC}\cdot\Delta V_{BUS}}\cdot\frac{\arcsin(1-\frac{\Delta V_{BUS}}{\sqrt{2}\cdot V_{IN\_MIN}})+\frac{\pi}{2}}{2\sqrt{2}\cdot V_{IN\_MIN}-\Delta V_{BUS}}=\frac{24}{87\%\times3.14\times50\times45}\cdot\frac{\arcsin(1-\frac{45}{\sqrt{2}\times90})+\frac{\pi}{2}}{2\sqrt{2}\times90-45}=42.3\text{uF}$$

Select BUS capacitor: $C_{BUS}=44\text{uF}$

Minimum BUS voltage:

$$V_{BUS\_MIN}=\sqrt{2}\cdot V_{IN\_MIN}-\Delta V_{BUS}=\sqrt{2}\times90-45=82.3\text{V}$$

2) Transformer Design

(a)Calculate primary/secondary turns ratio: N_{PS}

$$N_{PS}\le\frac{V_{MOS\_BR}\cdot K_{DR}-\sqrt{2}V_{IN\_MAX}-\Delta V_{SN}}{V_O}=\frac{800\times0.85-\sqrt{2}\cdot264-120}{12}=15.58$$

N_{PS} is selected to: $N_{PS}=8$

(b) Calculate maximum duty cycle D_{MAX} at minimum BUS voltage and rated output power condition

$$D_{MAX}=\frac{N_{PS}\cdot V_O}{V_{BUS\_MIN}+N_{PS}\cdot V_O}=\frac{8\times12}{82.3+8\times12}=53.8\%$$

(c) Calculate primary inductance: L_M

$$L_M = \frac{V_{BUS\_MIN}{}^2 \cdot D_{MAX}{}^2 \cdot \eta}{2 \cdot P_O \cdot f_{SW} \cdot K_{RP}} = \frac{82.3^2 \times 53.8\%^2 \times 87\%}{2 \times 24 \times 100k \times 0.45} = 791uH$$

Select $L_M = 800uH$

(d)Calculate primary peak current at minimum BUS voltage and rated output power condition:

$$I_{PK} = \frac{P_O}{V_{BUS\_MIN} \cdot D_{MAX} \cdot \eta} + \frac{V_{BUS\_MIN} \cdot D_{MAX}}{2 \cdot L_M \cdot f_{SW}} = \frac{24}{82.3 \times 53.8\% \times 87\%} + \frac{82.3 \times 53.8\%}{2 \times 800u \times 100k} = 0.9A$$

(e)Calculate primary winding turns: N_P

Transformer core effective cross-sectional area: $A_E = 33.5 \cdot 10^{-6} m^2$

Maximum allowed flux density at rated output power: $B_{MAX} = 0.26T$

$$N_P = \frac{L_M \cdot I_{PK}}{B_{MAX} \cdot A_E} = \frac{800u \times 0.9}{0.26 \times 33.5 \times 10^{-6}} = 82.6$$

Select primary winding turns: N_P=80

(f) Calculate secondary winding turns: N_S

$$N_S = \frac{N_P}{N_{PS}} = \frac{80}{8} = 10$$

Select secondary turns: N_S=10

(g) Calculate auxiliary winding turns: N_A

VCC supply voltage from auxiliary winding is set to: $V_{CC(AUX)}$=12V

$$N_A = \frac{V_{CC\_AUX} \cdot N_S}{V_O} = \frac{14 \times 10}{12} = 12$$

Select auxiliary winding turns: N_A=12

Note: Auxiliary winding turns should be fine-tuned according to actual VCC pin voltage under minimum output voltage and no-load condition)

(h) If other transformer core type is selected, then re-calculate (e)~(g).

3) Peak current sense resistor calculation:

(a)Calculate duty cycle under minimum input voltage (maximum BUS voltage): D_{OCP}

$$D_{OCP} = \frac{N_{PS} \cdot V_O}{\sqrt{2} \cdot V_{IN\_MIN} + N_{PS} \cdot V_O} = \frac{8 \times 12}{\sqrt{2} \times 90 + 8 \times 12} = 43\%$$

(b)Calculate primary side peak current at OCP point: I_{PK_MAX}

$$I_{PK\_MAX} = \frac{P_O \cdot K_{OCP}}{\sqrt{2} \cdot V_{IN\_MIN} \cdot D_{OCP} \cdot \eta} + \frac{\sqrt{2} \cdot V_{IN\_MIN} \cdot D_{OCP}}{2 \cdot L_M \cdot f_{SW}} = \frac{24 \times 130\%}{\sqrt{2} \times 90 \times 43\% \times 87\%} + \frac{\sqrt{2} \times 90 \times 43\%}{2 \times 800u \times 100k} = 1.0A$$

(c)Calculate current sense resistor: R_{ISEN}

$$R_{ISEN} = \frac{V_{ISEN\_MAX}}{I_{PK\_MAX}} = \frac{0.9}{1.0} = 0.9\Omega$$

Note: ISEN pin current sense resistor R_{ISEN} should be fine-tuned according to the actual OCP point.

4) Secondary rectifying diode selection

(a)Maximum reverse voltage calculation:

$$V_{DS(SR)\_MAX} = \frac{\sqrt{2} \cdot V_{IN\_MAX}}{N_{PS}} + V_O + V_{SPIKE} = \frac{\sqrt{2} \times 264}{8} + 12 + 10 = 84.2V$$

Considering voltage de-rating, rectify diode with 100V rating is recommended.

(b)Maximum instantaneous rectifying diode current:

$$I_{D(SR)\_MAX} = N_{PS} \cdot I_{PK\_MAX} = 8 \times 1.0 = 8.0A$$

5) Calculate PRT pin resistor divider

(a) Calculate PRT pin upper resistor: R_H

$$R_{H(MIN)} = \frac{2 \cdot V_{IN\_MAX}{}^2}{P_{RD}} = \frac{2 \times 264^2}{25m} = 5.6M\Omega$$

Select R_H=6M Ω

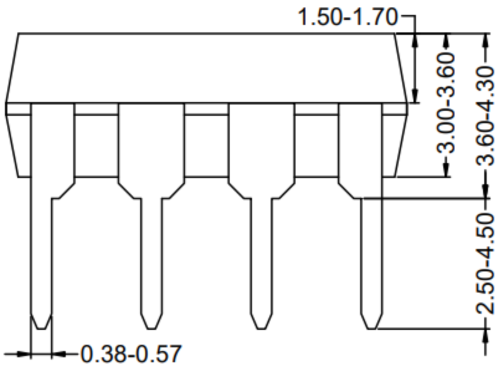
(b) After R_H is determined, calculate lower resistor R_L:

$$R_L = R_H \cdot \frac{V_{PRT\_BO}}{\sqrt{2} \cdot V_{IN\_BO} - V_{PRT\_BO}} = \frac{0.5}{\sqrt{2} \times 70 - 0.5} \cdot 6M = 30.5k\Omega$$

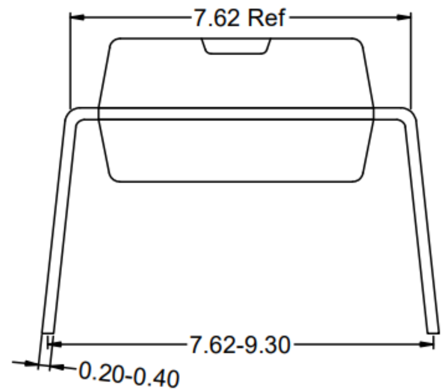
Select R_L=30.9k Ω

DIP7 Package Outline

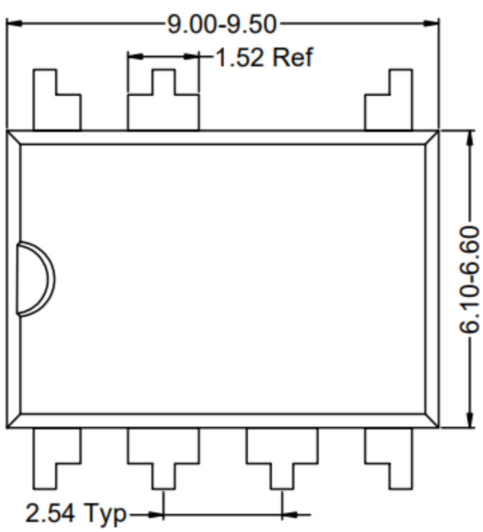
Side View A



Side View B



Top View

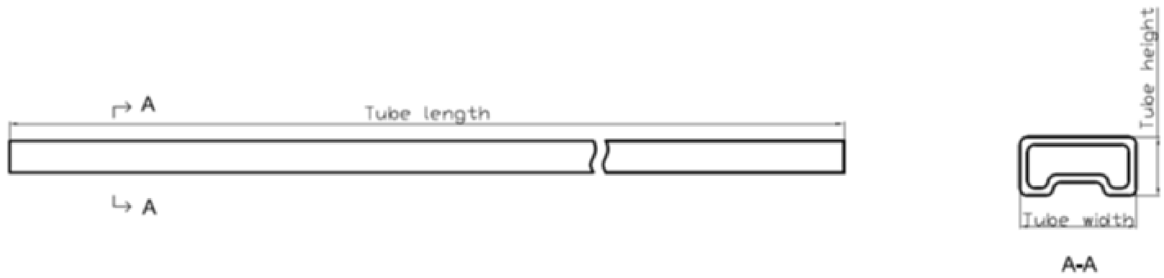


Notes: All dimensions in millimeters and exclude mold flash & metal burr.

Packaging Specification

Tube dimensions:

DIP7



Package Type	Tube Length(mm)	Tube Width(mm)	Tube Height(mm)	Qty per Tube (pcs)	Qty per Box
DIP7	520+/-10	11.7+/-2	10.7+/-0.5	50	2000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
December 19,2025	Revision 1.0	Initial Release