

General Description

The SY5023C is a high frequency flyback controller operating in quasi-resonant (QR) mode. It integrates high voltage (HV) start up block for smaller no load loss. It can drive enhancement-mode (E-mode) GaN FET directly. The device is designed for power delivery (PD) capable adapters and quick chargers. Its maximum operating frequency of up to 500kHz allows for reduced transformer, PCB, and capacitor sizes.

The SY5023C operates using peak current control. At heavy load the device enables QR mode. In this mode, the GaN FET turns on at the valley point to minimize switching losses. As the load decreases, the SY5023C enters DCM mode to lower the switching frequency and improve efficiency. Under very light load conditions, the device enters burst mode to further reduce power loss.

The SY5023C integrates comprehensive protection features to ensure reliable operation, including HV startup, brown-out protection, output and VCC overvoltage protection (OVP), output undervoltage protection (UVP), internal and external overtemperature protection (OTP), and open-loop protection (OLP).

It is recommended to use the SY5236 or SY5236A as a secondary-side synchronous rectifier (SR) controller in conjunction with the SY5023C to enable zero voltage switching (ZVS) at high input voltage for efficiency.

The SY5023C is available in a compact SSOP9 package.

Features

- Integrated E-Mode GaN Drive.
- QR/DCM Operating Modes
- Soft GaN Gate Drive for Optimized EMI Performance
- Wide VCC Operating Range: 7-85V
- Switching Frequency Range: 25kHz–500kHz
- Frequency Modulation to Reduce EMI Noise
- Integrated 700V HV Startup Circuitry
- Programmable Output OVP and UVP
- Programmable Brown-In/Out Protection
- Programmable AC input OVP
- Current Sense Resistor Short-Circuit Protection
- Winding or SR Short-Circuit Protection
- Internal and External OTP
- Compact Package: SSOP9

Applications

- AC/DC Adapters
- PD Adapters
- Quick Chargers

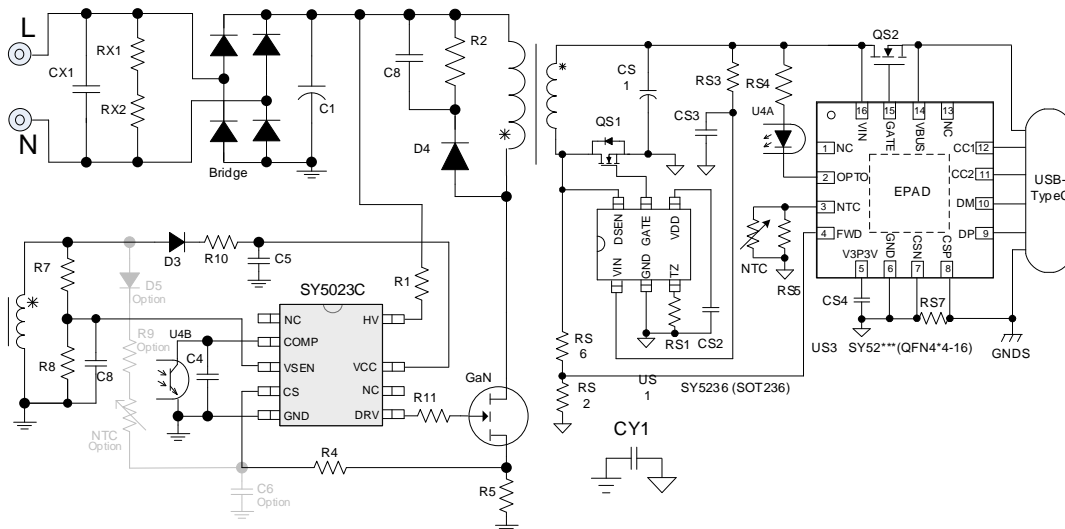


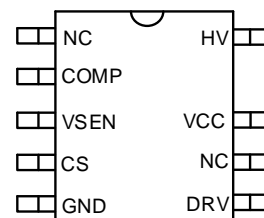
Figure 1. Typical Application Using Synchronous Rectification (SR)

Ordering Information

Ordering Part Number	Package type	Top Mark
SY5023CFVP	SSOP9 RoHS-Compliant and Halogen-Free	ABCRxyz

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	NC	Not connect.
2	COMP	Secondary side compensation voltage, connected to an optocoupler.
3	VSEN	Output voltage, input voltage, and QR valley detection pin.
4	CS	Current sensing pin, external OTP pin.
5	GND	Ground pin.
6	DRV	Drive of E-mode GaN.
7	NC	Not connect.
8	VCC	Power supply of Internal circuit.
9	HV	HV startup.

Block Diagram

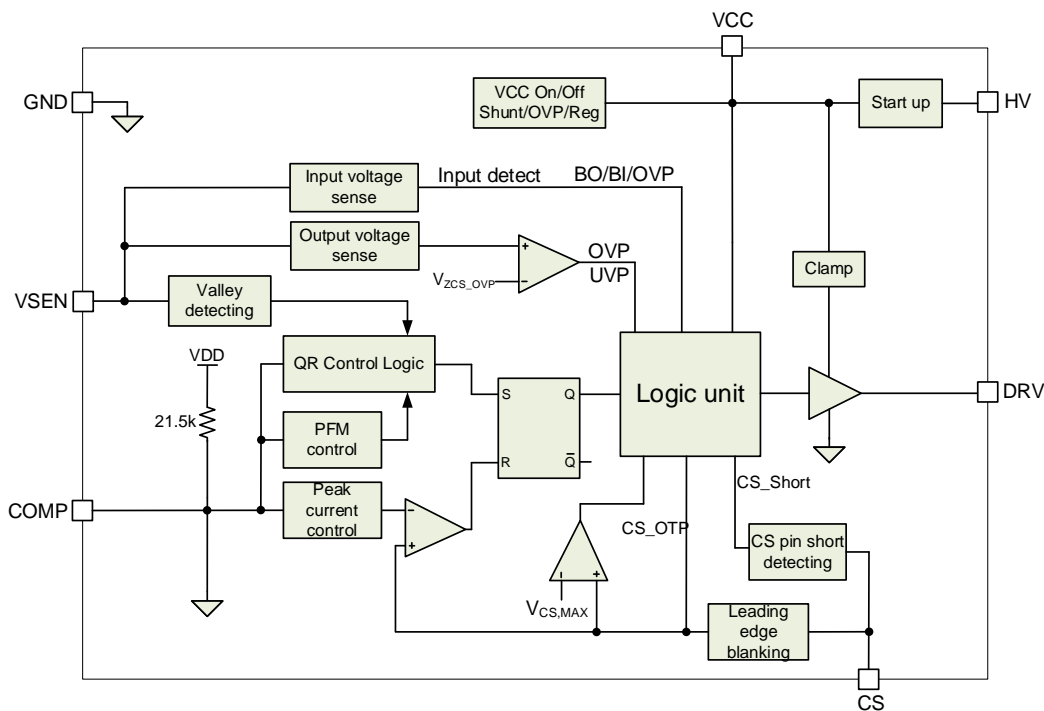


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
HV	-0.3	700	V
VCC	-0.3	100	
DRV	-0.3	8	
CS, COMP	-0.3	4	
VSEN	-1 (Note 1)	7	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature Range	-60	150	
Dynamic VSEN Negative Voltage in 50μs Duration (Note 1)		-1	V
Dynamic VSEN Negative Current in 50μs Duration (Note 1)		-2	mA
Human Body Model ESD (HV Pin and VCC Pin) per ESDA/JEDEC JS-001-2017 (Note 6)		±1	kV
Human Body Model ESD (All Pins Except HV Pin and VCC Pin) per ESDA/JEDEC JS-001-2017 (Note 6)		±2	kV
Charged Device Model ESD per JS-002-2018 (Note 6)		±500	V
Latch-Up Test per JEDEC78E (Note 6)		±100	mA
MSL Rating		3	

Thermal Information

Parameter (Note 2)	Min	Max	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance		158	°C/W
θ_{JC} Junction-to-Case Thermal Resistance		30	
PD Power Dissipation $T_A = 25^\circ\text{C}$		0.79	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
HV	-0.3	700	V
VCC	7	85	
DRV	-0.3	7	
CS	-0.3	0.6	
VSEN	-0.3	3.0	
COMP	-0.3	3.0	
Junction Temperature Range	-40	125	°C
Case Temperature Range	-40	105	°C

Electrical Characteristics

(V_{VCC} = 13V (Note 7), T_J = 25°C unless otherwise specified (Note 4))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
HV	HV Voltage	V _{HV_MAX}		700			V
	Leakage Current	I _{HV_LK}	V _{HV} = 700V _{DC}			15	μA
	HV Charge VCC	I _{HV_CHARGE}	V _{HV} = 100V _{DC}	1.60	2.15	2.70	mA
VCC	Start-up Current	I _{CC_START}	V _{CC} = V _{CC_ON} - 0.5V	30	42	55	μA
	Turn-On Threshold	V _{CC_ON}	V _{CC} rising up	16.0	17.5	19.0	V
	Turn-Off Threshold	V _{CC_OFF}	V _{CC} falling down	5.3	5.8	6.3	V
	Regulation Threshold	V _{CC_REG}	In error mode	5.7	6.1	6.5	V
	OVP Threshold	V _{CC_OVP}		86	92	98	V
	OVP Debounce Cycles	N _{VCCOVP_DBC}	(Note 8)		4		cycles
	Current Sink at OVP	I _{CC_SHUNT}	V _{CC} = V _{CC_OVP} + 1V	2.4	3.0	3.6	mA
	Operating Current	I _{CC_OPERATING}			0.6		mA
	VCC Current in Burst	I _{CC_BURST}	V _{COMP} < 0.27V	130	160	190	μA
CS	Maximum Peak Current	V _{CS_MAX}		550	600	650	mV
	Leading Edge Blanking Time for V _{CS_MAX}	t _{CS_LEB1}			100		ns
	Debounce of V _{CS_MAX}	N _{VCSMAX_DBC}	(Note 8)		4		cycles
	Vcs Limitation	V _{CS_LIMIT}		373	395	417	mV
	Leading Edge Blanking Time for V _{CS_LIMIT}	t _{CS_LEB3}		195	280	365	ns
	Current Mirror in ton	K _{VSEN-CS}	I _{VSEN} / I _{CS}		20:1		/
	Detection of CS short	t _{CS_SHORT}	Only in soft-start	4.0	5.8	7.6	μs
	Threshold for CS short	V _{CS_SHORT}		45	65	85	mV
	Vcs Modulation	K _{VCS_MOD}	(Note 8)		±5%		/
	Frequency Modulation.	F _{MODULATION}			4		kHz
	Debounce of CS_OTP	N _{CSOTP}	(Note 8)		4		cycles
	Vcs at V _{CC} < V _{CC_REG}	V _{CS_VCCREG}	In burst mode.		200		mV
	Soft Start Time	t _{SS}	(Note 8)		7		ms
VSEN	Output OVP Threshold	V _{VSEN_OVP}		2.03	2.14	2.25	V
	Blanking Time	t _{VSEN_BLK}		0.9	1.2	1.5	μs
	Debounce of OVP	N _{VSEN_OVP}	(Note 8)		4		cycles
	Output UVP Threshold	V _{VSEN_UVP}	After soft-start. Only in QR mode.	125	150	175	mV
	Debounce of UVP	N _{VSEN_UVP}			4		cycles
	BO Threshold Current	I _{VSEN_BO}		90	100	110	μA
	BO Debounce Time	t _{BO_DBC}			150		ms
	Restart Time 1	t _{ERROR_SHORT}	Short error mode		0.3		s
	Restart Time 2	t _{ERROR}	Error mode		2.0		s
	BI Threshold Current	I _{VSEN_BI}		104	118	132	μA
	AC high Line Threshold	I _{VSEN_ACHIGH}		205	225	245	μA
	Back to AC Low Line	t _{ACLOW_DBC}	Debounce time		60		ms
	AC input OVP Threshold	I _{VSEN_ACOVP}			530		μA
Debounce of AC input OVP	N _{VSEN_ACOVP}			4		cycles	

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
	Timeout when Valley Cannot be Detected	t _{TIMEOUT}			10		μs
	Valley Point Threshold	V _{VSEN_VALLEY}			0		mV
	Turn on Delay in QR	t _{VSEN_DELAY}			200		ns
COMP	Internal Pull up Voltage	V _{COMP_UP}		2.3	2.8	3.3	V
	Internal Pull up Resistor	R _{COMP_PU}		16.0	21.5	27.0	kΩ
	OLP Threshold	V _{COMP_OLP}	V _{COMP} > V _{COMP_OLP}	2.2	2.5	2.8	V
	OLP Debounce Time	t _{OLP_DBC}		100	150	200	ms
	DCM to QR Threshold	V _{COMP_DCMQR}			0.935		V
	QR to DCM Threshold	V _{COMP_QRDCM}			0.915		V
	Sleep in Threshold	V _{COMP_SLEEPIN}	V _{COMP} fall down	0.24	0.27	0.30	V
	Sleep out Threshold	V _{COMP_SLEEPOUT}	V _{COMP} rising up	0.29	0.325	0.36	V
DRV	Drive voltage	V _{DRV}		5.9	6.2	6.5	V
	Drive source current	I _{DRV_SOURCE}			3.5		mA
	Drive sink current	I _{DRV_SINK}			100		mA
	DRV internal resistor to GND	R _{DRV_GND}			200		kΩ
Switching Frequency	Maximum Fsw in DCM	F _{SW_MAXDCM}			50		kHz
	Minimum Fsw in DCM	F _{SW_MINDCM}	V _{COMP} =0.25V	20	24	28	kHz
	Maximum ON Time	t _{ON_MAX}		14	20	26	μs
	Maximum Off Time	t _{OFF_MAX}		100	140	180	μs
Internal OTP	OTP Threshold	T _{OTP_SHUTDOWN}	(Note 5)		150		°C
	Recovery Threshold	T _{OTP_RECOVERY}	(Note 5)		130		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured with natural convection at $T_A = 25^\circ\text{C}$ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standards. Test conditions: Device mounted on “2 x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal via to bottom layer ground plane.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J = 25^\circ\text{C}$. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

Note 6: Meets ESDA/JEDEC JS-001-2017 and JEDEC78E.

Note 7: Increase VCC pin voltage gradually higher than the V_{CC_ON} voltage, then reduce it to 13V.

Note 8: Application test result.

Detailed Description

HV Startup and Power Supply

At power-on, the HV charges the VCC capacitor. When VCC voltage rises above the startup threshold, the HV circuitry will be turned off to reduce power loss.

If the device enters protection mode, PWM operation is suspended for a fixed error timeout period (t_{ERROR}). During this time, internal power consumption causes the VCC voltage to drop. When VCC falls below the regulation threshold (V_{CC_REG}) the HV circuitry is reenabled to recharge VCC until $V_{CC} > V_{CC_ON}$. After t_{ERROR} , the internal logic will be reset, and a restart sequence is initiated.

Input Voltage Detection

The SY5023C monitors the input voltage through the VSEN pin during the t_{ON} period (when the GaN FET is on). During t_{ON} , the VSEN pin is clamped to approximately 0V. If the current at the VSEN pin is higher than I_{VSEN_ACHIGH} , an AC high condition is immediately assumed. If the current remains below I_{VSEN_ACHIGH} for a duration longer than t_{ACLOW_DBC} , an AC low condition is assumed.

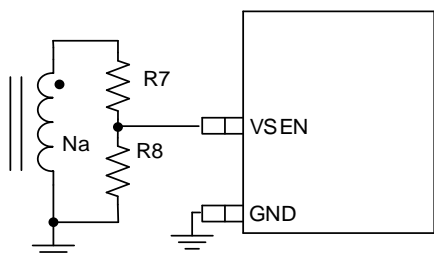


Figure 3. Input Voltage Detection

During the t_{ON} period, a current flows from the VSEN pin to Na through resistor R7. The AC high threshold can be calculated as follows:

$$V_{BUS_ACHIGH} = I_{VSEN_ACHIGH} \times R7 \times \frac{N_p}{N_a}$$

(N_a is auxiliary winding. N_p is primary winding.)

Valley Detection

The following waveform illustration shows the valley detection method. When the falling edge of the zero-crossing voltage is detected at the VSEN pin, the SY5023C will turn on the GaN FET after a fixed delay.

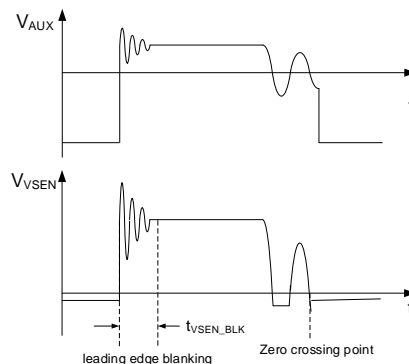


Figure 4. Valley Detection

Noise is present at the VSEN pin when the GaN FET turns off, which may affect valley detection. The SY5023C uses a t_{VSEN_BLK} time to avoid noise interference.

QR Mode

When V_{COMP} is higher than V_{COMP_DCMQR} , QR mode is enabled. In QR mode, when the load is very heavy, the PWM turns on at the 1st valley point of the GaN FET drain voltage. EMI is better and efficiency is higher. The peak current (V_{CSPK}) is controlled by the V_{COMP} voltage. As the load decreases, the valley number increases in one-step increments until it reaches the 6th valley

DCM Mode

When V_{COMP} is lower than V_{COMP_QRDCM} , DCM mode is enabled. In DCM mode, V_{CSPK} and the switching frequency are controlled by V_{COMP} . PWM turns on instantly at the F_{SW} clock and does not wait for the valley point. As the load decreases, frequency and V_{CSPK} decrease to keep a constant output voltage.

Burst Mode

When both the switching frequency and V_{CSPK} have decreased to the minimum values, if the output load continues decreasing, V_{COMP} will be lower than $V_{COMP_SLEEPIN}$. At this point, PWM will stop. PWM resumes only when V_{COMP} rises above the $V_{COMP_SLEEPOUT}$ threshold. In this condition, the device operates in burst mode.

Soft-Start

At startup, when V_{COMP} rises above the $V_{COMP_SLEEPOUT}$ threshold, PWM operation begins, and the current sense threshold (V_{CS}) increases step by step from the minimum value across seven steps. Under heavy load or V_{OUT} short conditions, the soft-start period terminates after t_{SS} . Under light load or no-load conditions, if the V_{CS} value determined by V_{COMP} is lower than the value determined by soft-start, the soft-start sequence will terminate and V_{COMP} takes control of V_{CS} .

V_{CS_LIMIT}

After t_{CS_LEB3} in each switching cycle, if V_{CS} is higher than the V_{CS_LIMIT}, PWM turns off immediately. This decision is made on a cycle-by-cycle basis and does not affect the PWM operation of the subsequent cycle.

V_{CS_MAX} during Transformer Winding Short Circuit

Under normal operating conditions, V_{CS_LIMIT} restricts the GaN peak current to ensure sufficient protection. However, in the event of a transformer winding or secondary diode short circuit, the current slope becomes extremely steep, causing the transformer to enter saturation state. As a result, the current can rise to a much higher level during t_{CS_LEB3}.

To address this, the SY5023C monitors V_{CS} after t_{CS_LEB1}, which is shorter than t_{CS_LEB3}. If V_{CS} is higher than V_{CS_MAX} for four consecutive cycles, PWM operation stops and the timer starts. After the t_{ERROR} period, the internal logic resets, and a restart is triggered, with the HV circuitry recharging V_{CC} to the V_{CC_ON} threshold.

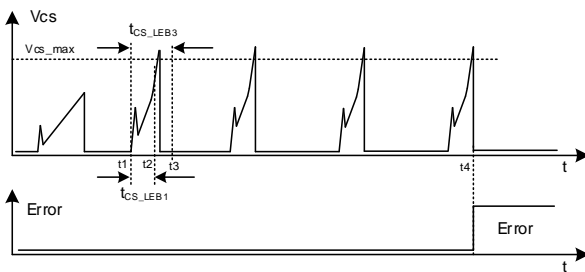


Figure 5. V_{CS_MAX} Process

Brown-In and Brown-Out

When the input voltage falls below 90VAC, the current and heat dissipation in the transformer and primary GaN FET increase significantly. To protect the power supply, the SY5023C provides brown-in (BI) and brown-out (BO) protections using the VSEN pin.

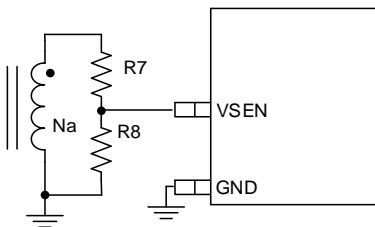


Figure 6. Brown out Detection

During the t_{ON} period, the VSEN pin is clamped to approximately 0V. A current flows from the VSEN pin to Na through resistor R7. Brown-in and brown-out are defined as follows:

- Brown-In (BI): During t_{ON}, if the VSEN current is higher than I_{VSEN_BI} a brown-in condition is confirmed.

- Brown-Out (BO): During t_{ON}, if the VSEN current is lower than I_{VSEN_BO} for a duration longer than t_{BO_DBC} a brown-out condition is triggered.

The BO threshold is determined by R7, with the bus voltage at brown-out calculated as:

$$V_{BUS_BO} = I_{VSEN_BO} \times R7 \times \frac{Np}{Na}$$

(Na is auxiliary winding. Np is primary winding.)

Following a BO event, PWM operation stops. After a t_{ERROR_SHORT} delay, the internal logic resets and a startup sequence is initiated, with the HV input recharging V_{CC} to the V_{CC_ON} threshold. After restart, one PWM pulse is generated, and the VSEN pin current will be detected. If the BI condition is met, PWM operation continues and the SY5023C will recover to normal operating state.

AC Input OVP

When the input voltage rises up to 300VAC, the switching loss and heat dissipation in primary GaN FET will increase significantly. To protect the power supply, the SY5023C provides AC input OVP.

During the t_{ON} period, VSEN pin is clamped to approximately 0V. A current flows from VSEN pin to Na through resistor R7. If the VSEN current is higher than I_{VSEN_ACOVP} in four continuous cycles, a AC input OVP is confirmed. Then PWM operation stops. After a t_{ERROR} delay, the internal logic resets and a startup sequence is initiated, with the HV input recharging V_{CC} to the V_{CC_ON}.

Output OVP and UVP

The SY5023C detects the output voltage through the VSEN pin and provides output overvoltage protection (OVP) and undervoltage protection (UVP).

When VSEN voltage is higher than V_{VSEN_OVP} for N_{VSEN_OVP} cycles, V_{VSEN_OVP} is triggered and PWM stops. After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV circuitry charging V_{CC} to V_{CC_ON}.

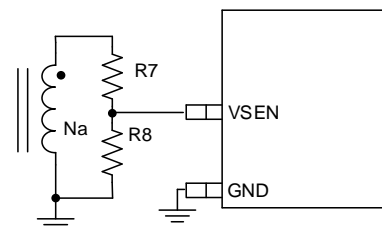


Figure 7. VSEN OVP and UVP Setting

The output OVP threshold is calculated as follows:

$$V_{OUT_OVP} = V_{VSEN_OVP} \times \frac{R7 + R8}{R8} \times \frac{Ns}{Na}$$

(Na is auxiliary winding. Ns is secondary winding.)

After the soft-start time, when VSEN voltage is lower than V_{SEN_UVP} continuously for N_{VSEN_UVP} cycles, V_{SEN_UVP} is triggered and PWM stops. After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV circuitry charging VCC to V_{CC_ON} . Vsen UVP function is only enabled in QR mode.

R7 is determined by the brown-out threshold. R8 is determined by the output OVP threshold. UVP is used to avoid continuous operation under V_{OUT} short circuit conditions and is not mandatory for the design.

VCC OVP

The SY5023C provides VCC overvoltage protection (OVP) to protect the device from abnormal high voltage caused by an open feedback loop or improper N_A winding turns. When VCC rises to V_{CC_OVP} and external power current capability is higher than the shunt ability, VCC can continue rising.

VCC is continuously monitored. If VCC is higher than V_{CC_OVP} for N_{VCCOVP_DBC} cycles, V_{CC_OVP} is triggered and PWM stops. After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV circuitry charging VCC to V_{CC_ON} .

Open-Loop Protection

If the output is short-circuited or the load increases excessively, the optocoupler circuitry opens and V_{COMP} increases. When V_{COMP} exceeds V_{COMP_OLP} and remains above this threshold for t_{OLP_DBC} , open-loop protection (OLP) is triggered and PWM stops. After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV circuitry charging VCC to V_{CC_ON} .

CS Pin Short Circuitry

During soft-start, V_{CS} is sampled at t_{CS_SHORT} during the t_{ON} period of every PWM cycle and compared with V_{CS_SHORT} . If $V_{CS} < V_{CS_SHORT}$ continuously for 2 cycles, short-circuit protection is triggered and PWM stops. After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV circuitry charging VCC to V_{CC_ON} .

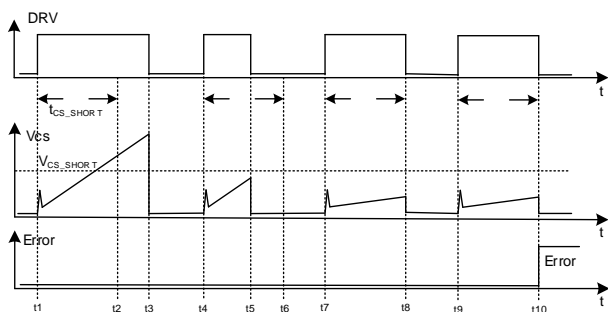


Figure 8. CS Short Protection

Figure 8 shows the short protection logic:

- At t_2 , V_{CS} is higher than V_{CS_SHORT} . No protection.

- At t_5 , the t_{CS_SHORT} timer has not expired. No comparison is needed. No protection.
- At t_8 , V_{CS} is lower than V_{CS_SHORT} at t_{CS_SHORT} mark. This is the first cycle.
- At t_{10} , V_{CS} short circuitry has been detected in 2 consecutive cycles, protection is triggered.

Internal OTP

The SY5023C continuously monitors the die temperature during normal operation. When the die temperature rises above $T_{OTP_SHUTDOWN}$, PWM operation stops. After a t_{ERROR} delay, the logic resets, and a startup sequence is initiated, with the HV circuitry charging VCC to V_{CC_ON} . After restart, PWM resumes normal operation once the temperature falls down below $T_{OTP_RECOVERY}$.

Design Guide

BUS Capacitor Selection

The bulk capacitor C_{BUS} is generally selected according to the following guidelines (PFC refers to Power Factor Correction):

- Without PFC: 1.5–1.8 μ F per watt of output power.
- With PFC: 0.5–0.8 μ F per watt of output power.

Minimum BUS Voltage

The minimum BUS voltage occurs when the input voltage V_{AC} is at its lowest and the output current reaches its maximum rated value. Calculating the required BUS capacitance involves assumptions and estimated parameters, which often lead to inaccurate results, which often lead to inaccurate results. Additionally, the actual capacitance of aluminum capacitors is only 85-90% of the nominal value, further reducing calculation accuracy. Therefore, precise results are difficult to obtain through calculation alone.

The following examples are helpful for fast selection and can be used as a reference.

For a 30~45W solution without PFC (Power Factor Correction) circuitry, a bus capacitor configuration of 27 μ F + 27 μ F is recommended. The corresponding V_{BUS_MIN} is as follows:

Output Power	30W	35W	40W	45W
AC90V 50Hz	86V	80V	75V	68V
AC90V 60Hz	93V	87V	83V	78V

For a 66W solution without PFC circuitry, operating under full load conditions (20V, 3.3A) the corresponding V_{BUS_MIN} is as follows:

Bus Nominal Capacitance	82+22 μ F	82+10 μ F	82 μ F	68 μ F
AC90V 50Hz	82V	78V	72V	60V

For a 140W solution using a boost PFC plus flyback topology, the output is 28V at 5A. The bus nominal capacitance is 39 μF + 39 μF .

- At AC 90V, 50Hz, the boost PFC outputs DC 240V. V_{BUS} ranges from 222V (min) to 253V (max), resulting in a ripple of 31V.

- At AC 176V, 50Hz, boost PFC outputs DC 350V. V_{BUS} ranges from 338V (min) to 362V (max), resulting in a ripple of 24V.

For optimal performance, $V_{\text{BUS_MIN}}$ should be higher than DC 60V.

Transformer Calculation

(1) Primary/secondary turns ratio: N_{PS}

N_{PS} can be calculated by the following formula:

$$V_{\text{OR}} = N_{\text{PS}} \times (V_{\text{O}} + V_{\text{D_F}})$$

V_{OR} is the reflected voltage on the primary winding. A typical value ranges from 80~130V. V_{O} is the output voltage. $V_{\text{D_F}}$ is the forward voltage of the secondary rectification diode. If a synchronous rectified (SR) is used on the secondary side, set $V_{\text{D_F}} = 0$.

(2) Select transformer (A_{e} and Bobbin)

The transformer should be selected based on output power, enclosure size, and BOM cost. The following examples provide useful references for quick selection:

- 65W, ATQ18, $A_{\text{e}} = 62\text{mm}^2$, winding width (w) = 6.0mm
- 80W, PQ22.5, $A_{\text{e}} = 73\text{mm}^2$, winding width (w) = 9.5mm
- 100W, ATQ24, $A_{\text{e}} = 90\text{mm}^2$, winding width (w) = 8.0mm
- 140W, RM10, $A_{\text{e}} = 98\text{mm}^2$, winding width = 10.3mm

The winding width of the bobbin is a critical parameter. A wider winding area reduces leakage inductance and allows for thicker winding wires, which improves efficiency.

(3) Select N_{S} wire diameter and turns

To meet safety standards, the secondary (N_{S}) winding should use triple-insulated wire. The diameter of the triple-insulated wire is determined by the output current. The following examples are helpful for quick selection:

- 20V 3.3A, ATQ18, $w=6.0\text{mm}$, $0.10 \times 80\text{mm} \times 1$, $N_{\text{S}}=4\text{ts}$.
- 11V 7.3A, PQ22.5, $w=9.5\text{mm}$, $0.10 \times 60\text{mm} \times 2$, $N_{\text{S}}=4\text{ts}$.
- 20V 5A, ATQ24, $w=8.0\text{mm}$, $0.10 \times 100\text{mm} \times 1$, $N_{\text{S}}=5\text{ts}$.
- 28V 5A, RM10, $w=10.3\text{mm}$, $0.10 \times 120\text{mm} \times 1$, $N_{\text{S}}=6\text{ts}$.

(4) Calculate transformer (N_{P}):

$$N_{\text{P}} = N_{\text{PS}} * N_{\text{S}}$$

(5) Calculate primary inductance (L_{P}):

$$L_{\text{P}} = \frac{B_{\text{MAX}} * A_{\text{E}} * N_{\text{PS}} * N_{\text{P}} * V_{\text{BUS_MIN}}}{2 * I_{\text{OUT_OLP}} * (V_{\text{OR}} + V_{\text{BUS_MIN}})}$$

Where:

- $I_{\text{OUT_OLP}}$ is the output overload protection threshold (unit: A).
- B_{MAX} is B of the transformer (typically 0.35~0.37T; unit: T).

(6) Calculate current sense resistor (R_{CS}):

$$R_{\text{CS}} = \frac{L_{\text{P}} * V_{\text{CS_LIMIT}}}{B_{\text{MAX}} * A_{\text{E}} * N_{\text{P}}}$$

Where:

- $V_{\text{CS_LIMIT}}$ is the V_{CS} limitation value as specified in the EC table.

In the L_{P} calculation, N_{S} and N_{P} are determined first. This method eliminates the need for iterative adjustments and consistently results in a satisfactory design, achieving efficiency that is close to optimal for a given transformer.

Turns of auxiliary winding: N_{A}

At $V_{\text{OUT_MIN}}$, AUX winding should supply V_{CC} . Turns of AUX winding N_{A} can be calculated as follows:

- $8.5\text{V} < \frac{V_{\text{OUT_MIN}}}{N_{\text{S}}} \times N_{\text{A}} < 12\text{V}$

Secondary Rectifier MOSFET Selection

Under the conditions of $V_{\text{BUS_MAX}}$ and $V_{\text{OUT_OVP}}$, the reverse voltage of the secondary rectification MOSFET will reach its maximum level. The maximum voltage (ignoring the voltage spike) is calculated as follows:

$$V_{\text{D_R_MAX}} = \frac{\sqrt{2} V_{\text{IN_MAX}}}{N_{\text{PS}}} + V_{\text{O_OVP}}$$

Current and $R_{\text{DS(ON)}}$ parameters can refer to the following examples:

- For a 20V, 3.3A solution, the BSC098N10NS5 is recommended, which is 100V 8.2m Ω_{typ} .
- For a 20V, 4.5A solution, the BSC0805LS is recommended, which is 100V 6.0m Ω_{typ} .
- For a 28V, 5.0A solution, two MOSFETs in parallel are recommended for heat dissipation. For example, two BSC160N15NS5 devices (100V, 13.7m Ω_{typ}) can be used.

Ensure that the selected MOSFETs can handle the power dissipation under full-load conditions.

Layout Considerations

Follow these PCB layout guidelines for optimal performance and EMI considerations.

Signals are grouped into two categories:

- Switching nodes:

Primary side: Drain, AUX, Core

Secondary side: Drain, AUX, Core

- Sensitive signal nodes (easily affected by interference):

Primary side: V_{CS} , Comp, VSEN, etc.

Secondary side: REG or TZ (for SY5236), Feedback.

To ensure proper operation, sensitive signal nodes should be routed away from switching nodes. If PCB constraints make this difficult, use static nodes such as V_{BUS} , GND, VCC, V_{OUT} , SGND, etc as shielding between switching and signal paths.

To optimize EMI performance:

- Keep switching node areas on the PCB as small as possible. Avoid using switching nodes (e.g., GaN drain) for heat dissipation.
- Minimize the area of the main current loop.

Key current loops:

- Current path during t_{ON} : Bus capacitor \rightarrow Transformer \rightarrow GaN \rightarrow R_{CS} \rightarrow GND \rightarrow Bus capacitor
- Current path during t_{OFF} time: Transformer \rightarrow SR_MOS \rightarrow C_{OUT} \rightarrow GND \rightarrow Transformer.

- Leakage inductance and snubber circuit current loop
- Gate drive loops for primary and secondary GaN or MOSFETs

Component placement guidelines:

- Place the following components close to the SY5023C:
- COMP capacitor
- CS resistor (in series)
- VCC capacitor
- Place the VSEN pull-up resistor near the transformer's AUX pin, and the pull-down resistor near the VSEN pin.
- Place the following components near the SR controller:
- REG or TZ resistors
- V_{DD} and V_{IN} capacitors

GND routing:

- Connect the GND pin of the SY5023C directly to RCS_GND to ensure an accurate V_{CS} signal and minimize the drive loop area.

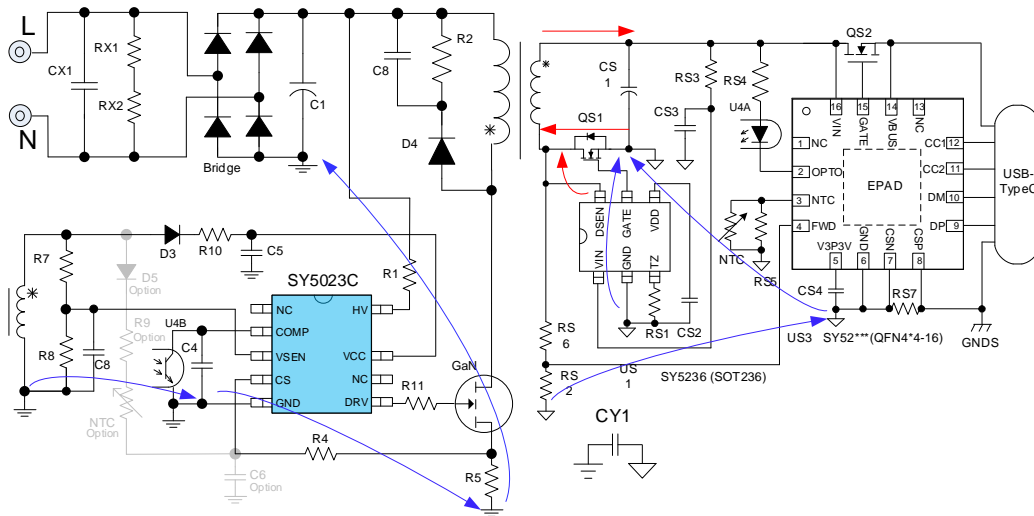


Figure 9. Recommended PCB Layout

Design Example

A step-by-step design example of a typical application is shown below.

Input/output specifications:

Parameter	Symbol	Value
Input voltage range	V_{IN}	AC90V–264V
Rated output voltage	V_O	5V–20V
Output OVP level	V_{O_OVP}	24V
Rated output current	I_O	3.3A
OLP	I_{OUT_OLP}	4.0A
Efficiency	η	93%

Preset parameters:

Parameter	Symbol	Value
The breakdown voltage of power MOS	V_{MOS_BR}	700V
Secondary diode forward voltage drop	V_{D_R}	0V (SR)
Transformer effective A_e (ATQ18)	A_E	62 mm ²

1. BUS capacitor selection

Selected BUS capacitor: $C_{BUS} = 99\mu\text{F}$ (1.5 $\mu\text{F/W}$)

2. Minimum BUS voltage calculation

Estimate $V_{BUS_MIN} = 80\text{V}$

3. Transformer design

(1) Primary-to-secondary turns ratio: $V_{OR}=140\text{V}$, $V_O=20\text{V}$, $N_{PS}=7$. $V_{OR} = N_{PS} \times V_O$

(2) Select transformer (Ae and Bobbin): ATQ18, $A_e=62\text{mm}^2$, Winding width=6.0mm.

(3) Select N_s wire diameter and turns: 20V 3.3A, ATQ18, Width=6.0mm, 0.10*80mm*1, $N_s=4\text{ts}$.

(4) Calculate transformer N_p : $N_p=7*4\text{ts}=28\text{ts}$.

(5) Calculate Primary Inductance: $L_p=199\mu\text{H}$ (QR)

$$L_p = \frac{B_{MAX} * A_E * N_{PS} * N_p * V_{BUSMIN}}{2 * I_{OUTOLP} * (V_{OR} + V_{BUSMIN})}$$

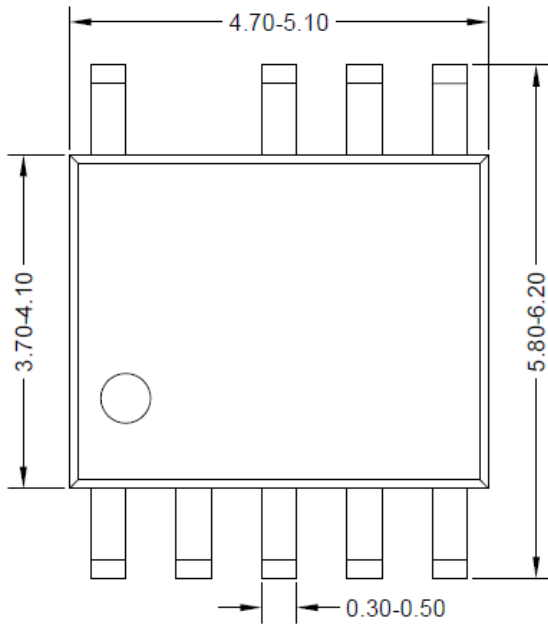
$$L_p = \frac{0.36T * 62\text{mm}^2 * 7 * 28 * 80V}{2 * 4.0A * (140V + 80V)} = 199\mu\text{H}$$

(6) Calculate current sense resistor: R_{cs}

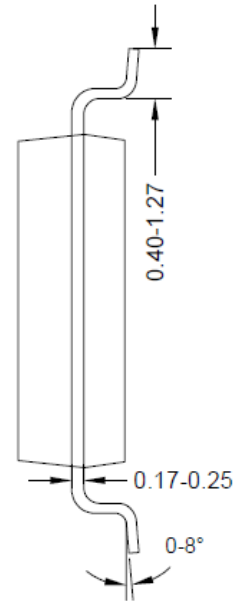
$$R_{CS} = \frac{L_p * V_{CS_LIMIT}}{B_{MAX} * A_E * N_p} = \frac{199\mu\text{H} * 0.395V}{0.36T * 62\text{mm}^2 * 28\text{ts}} = 0.126\Omega$$

(7) Calculate auxiliary winding turns: $V_{OUT_MIN} = 5\text{V}$, $N_A = 7\text{ts}$. $8.5\text{V} < \frac{V_{OUT_MIN}}{N_s} \times N_A < 12\text{V}$.

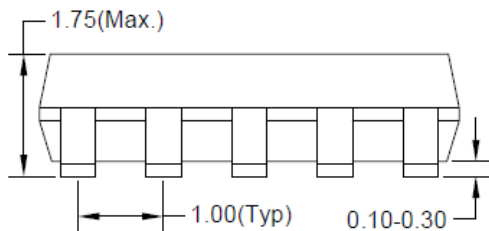
SSOP9 Package Outline Drawing



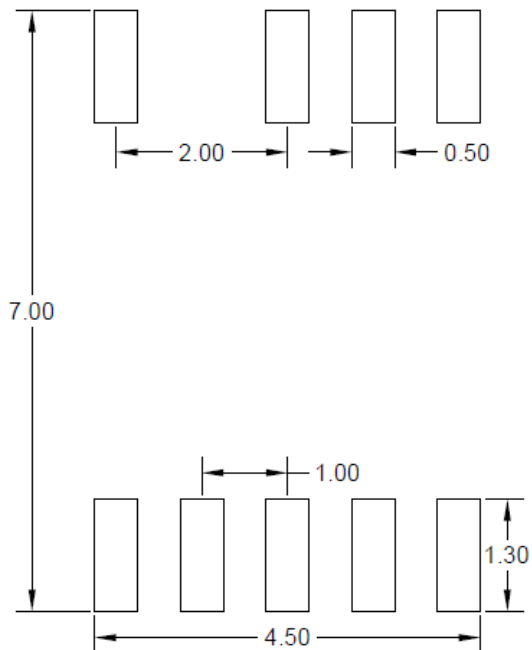
Top View



Side View



Front View

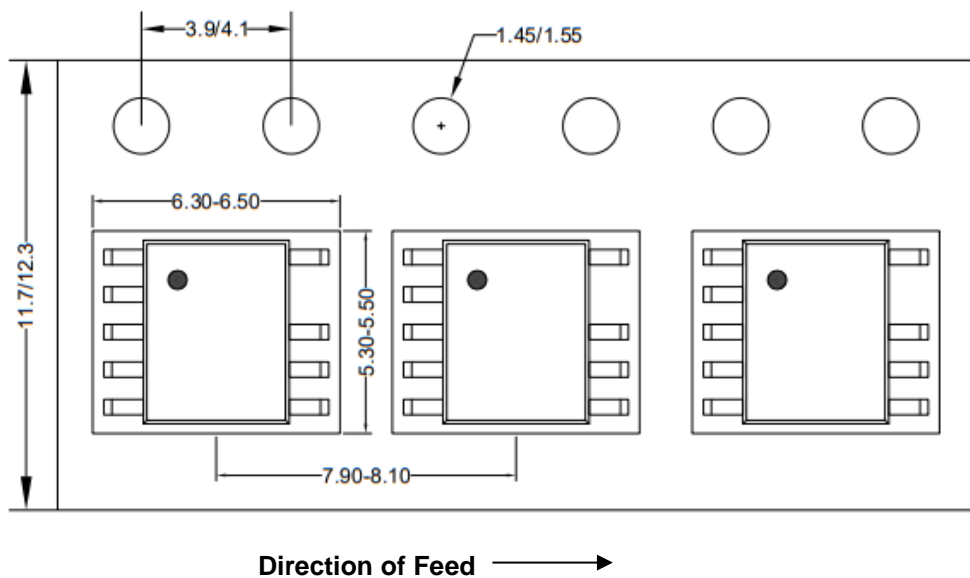


**Recommended PCB Layout
(Reference Only)**

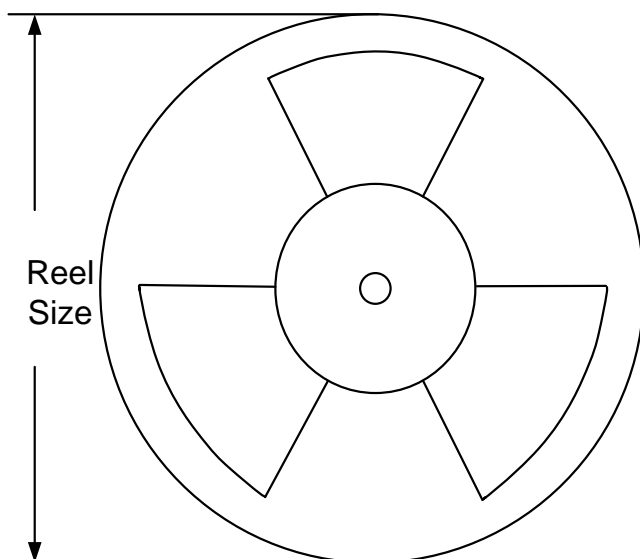
Note: All dimensions are in millimeters and exclude mold flash and metal burr.

Tape and Reel Specification

Tape Dimensions and Pin 1 Orientation



Reel Dimensions



Package types	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Trailer * length (mm)	Leader * length (mm)	Qty per reel (pcs)
SSOP9	12	8	13"	400	400	4000



Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
December 26, 2025	Revision 1.0	Initial Release

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