# SY70201

## High Efficiency High Integration PMIC

## General Description

The SY70201 is a Multi-channel PMIC which is composed of 4 synchronous Buck regulators, 1 LSW and 1 synchronous Boost regulator, 1 reset output and 1 reset enable output.

All channels of regulators support PFM mode for light load efficiency. Each channel provides DVS (Dynamic Voltage Scaling), forced discharge, power good indicator, as well as power off mode by $I^2C$ interface. The PMIC are designed to use very small size inductors and support to control the special power-up sequence with soft-start and delay time.

The SY70201 is available in a compact QFN5×5-36 package.

## Features

- Input Range: 2.6V to 5.5V
- 5 Independent Synchronous Bucks and 1 Independent 400mA Synchronous Boost, 1 Voltage Detector
  - Buck1: Max. Current 3.5A (0.725 V to 1.825V, 6.25mV Step, Default on 1.2V)
  - Buck2: Max. Current 3.8A (0.5 V to 1.2V, 6.25mV Step, Default on 1.2V)
  - Buck3: Max. Current 3A (0.96V to 1.86 V, 7.5mV Step, Default on 1.8V)
  - Buck5: Max. Current 4A (1.5 V to 2.75 V, 12.5mV Step, Default on 2.5 V)
  - Boost6: Max. Current 0.4A (8 V to 15 V, 500mV Step, Default on 12 V)
  - LSW: Max 300mA. Max. Ron 120mhom, Input Connect to VIN Internally, ON/OFF Controlled by $I^2C$)
- $I^2C$ Interface up to 3.4MHz
- Independent PMIC Hardware Reset (Make all Channels Return to the Default Voltage)
- DVS (Dynamic Voltage Scaling) Controlled by $I^2C$ Interface
- Auto PWM/PFM Mode or Forced PWM Mode Controlled by $I^2C$ Interface
- Pull down Mode to Discharge all Channels Forcedly Controlled by $I^2C$ Interface
- Support to Adjustable Discharge Resister Controlled by $I^2C$ Interface
- Programmable the Various Function by OTP (Each Channel Start up Delay Time, RSTO Delay Time (Power On, RSTO Threshold)
- Enable Output Pin to Synchronous External Device Sequence
- Ultra-Fast Transient Response
- Support to Protection Function (Thermal Shutdown (Typ. 150˚C), Over Voltage Protection (External/Output), Over Current Protection, Over Load Protection)
- Input Voltage Monitor Function: Input Monitor bit will be Set from 0 to 1 when Input Exceeds Specific Value.
- Compact 5mm x 5mm QFN Package, 0.45mm pitch
- Green RoHS Package, Pb-Free Lead Finish, Halogen Free Mold Compound.

## Applications

- SSD Power System

## Typical Applications

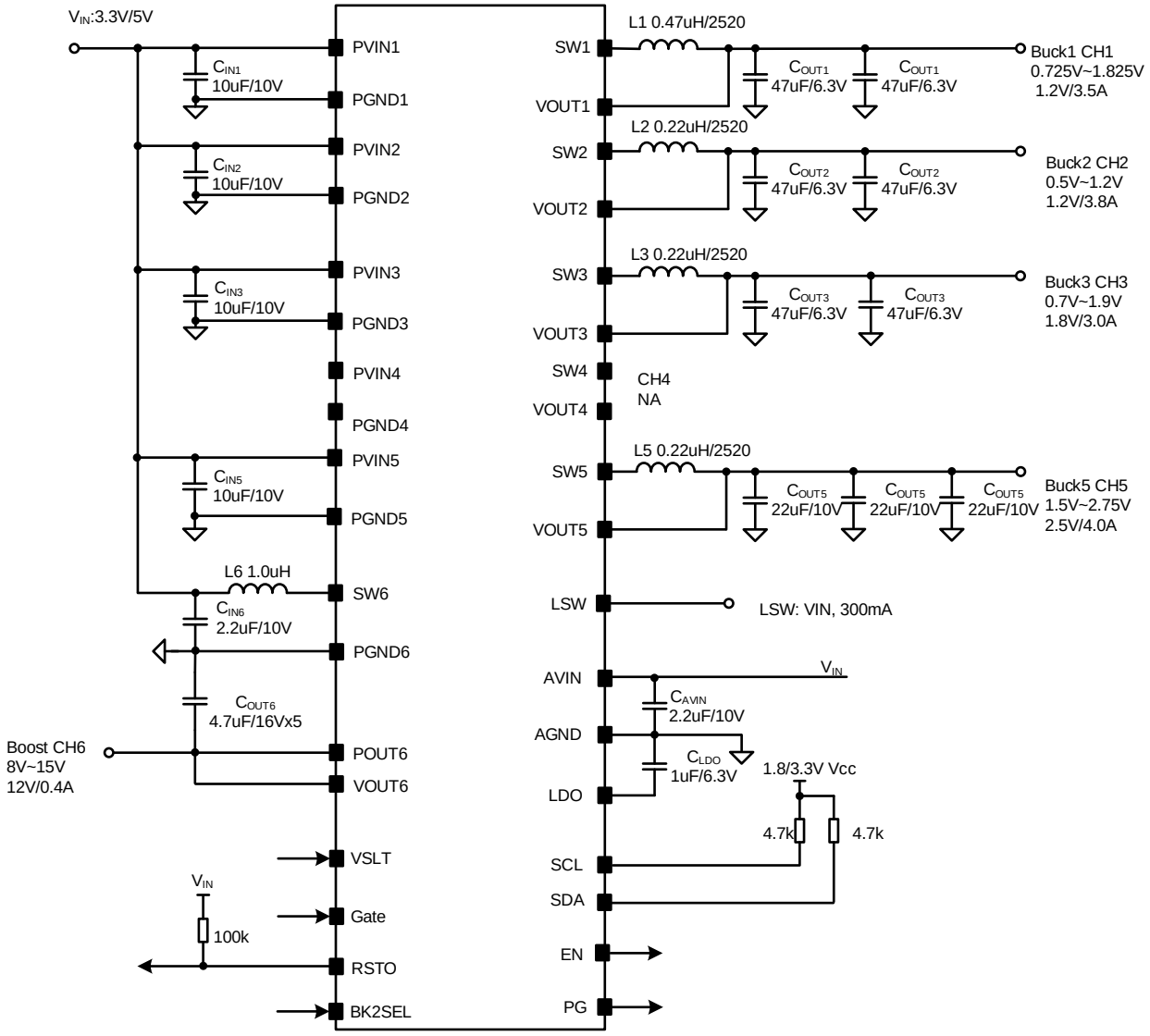


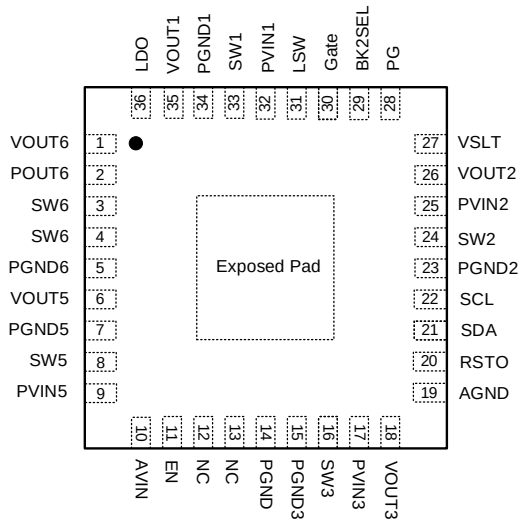

*Figure 1. Schematic Diagram*

## Ordering Information

| Ordering Part Number | Package Type | Top Mark |
|---|---|---|
| SY70201QPQ | QFN5×5-36<br>RoHS-Compliant and Halogen-Free | **EBB*xyz*** |

***x = year code, y = week code, z = lot number code***

## Pinout (top view)




(QFN5×5-36)

## Pin Description

| Pin Number | Pin Name | Pin Description |
|---|---|---|
| 1 | VOUT6 | Feedback pin for CH6. Connect this pin to CH6 output MLCC cap node to regulate the output voltage. |
| 2 | POUT6 | Power output pin for CH6. Decouple this pin to PGND6 with MLCC cap and minimize the loop area formed by POUT6, PGND6, and output MLCC cap. |
| 3,4 | SW6 | Switching node pin for CH6. Connect this pin to the switching node of inductor. |
| 5 | PGND6 | Power ground pin for CH6. |
| 6 | VOUT5 | Feedback pin for CH5. Connect this pin to CH5 output MLCC cap node to regulate the output voltage. |
| 7 | PGND5 | Power ground pin for CH5. |
| 8 | SW5 | Switching node pin for CH5. Connect this pin to the switching node of inductor. |
| 9 | PVIN5 | Power input pin of CH5. Decouple this pin to PGND5 with 10uF MLCC cap. |
| 10 | AVIN | Signal power input pin. Decouple this pin to AGND with 2.2uF MLCC cap. |
| 11 | EN | Enable output pin. It used to enable/disable other block. |
| 12 | NC | NC. |
| 13 | NC | NC. |
| 14 | PGND | Power groud pin. |
| 15 | PGND3 | Power ground pin for CH3. |
| 16 | SW3 | Switching node pin for CH3. Connect this pin to the switching node of inductor. |
| 17 | PVIN3 | Power input pin of CH3. Decouple this pin to PGND3 with 10uF MLCC cap. |
| 18 | VOUT3 | Feedback pin for CH3. Connect this pin to CH3 output MLCC cap node to regulate the output voltage. |
| 19 | AGND | Analog ground pin. |
| 20 | RSTO | Reset Output pin. It's open drain and it provides a high output after a fixed delay time when VIN exceeds the reset detection voltage. |
| 21 | SDA | Data line for the $I^2C$ interface. Open drain. |
| 22 | SCL | Clock input for the $I^2C$ interface. Open drain input. |
| 23 | PGND2 | Power ground pin for CH2. |

| | | |
|---|---|---|
| 24 | SW2 | Switching node pin for CH2. Connect this pin to the switching node of inductor. |
| 25 | PVIN2 | Power input pin of CH2. Decouple this pin to PGND2 with 10uF MLCC cap. |
| 26 | VOUT2 | Feedback pin for CH2. Connect this pin to CH2 output MLCC cap node to regulate the output voltage. |
| 27 | VSLT | POR threshold select pin.<br>Pull low to GND select 3.3Vin input.<br>Internally, a 5MΩ resistor is integrated to pull low this pin. |
| 28 | PG | NFET Drain which is controlled by Gate pin as below. (pin30) |
| 29 | BK2SEL | CH2(Buck2) default output voltage selection pin. Tie this pin to GND or VIN before power on.<br>Pull Low to GND to select 1.1V output;<br>Pull High to VIN to select 1.2V (Default) |
| 30 | Gate | PG pin NFET driver output.<br>Pull low to turn off the PG internal NFET and PG pin will be pulled high by external resister.<br>Pull high to turn on the PG internal NFET and PG pin will be pulled low by internal NFET. |
| 31 | LSW | Load Switch output pin. Decouple this pin to GND with at least 1uF MLCC cap. |
| 32 | PVIN1 | Power input pin of CH1. Decouple this pin to PGND1 with 10uF MLCC cap. |
| 33 | SW1 | Switching node pin for CH1. Connect this pin to the switching node of inductor. |
| 34 | PGND1 | Power ground pin for CH1. |
| 35 | VOUT1 | Feedback pin for CH1. Connect this pin to CH1 output MLCC cap node to regulate the output voltage. |
| 36 | LDO | Internal LDO output pin. Decouple LDO to GND with 1.0uF MLCC cap. |

## Absolute Maximum Ratings

| Parameter (Note 1) | Min | Max | Unit |
|---|---|---|---|
| SW6, VOUT6, POUT6 | -0.3 | 20 | V |
| Other PINs | -0.3 | 6 | |
| Junction Temperature Range | | 150 | °C |
| Lead Temperature (Soldering, 10 sec.) | | 260 | |
| Storage Temperature Range | -55 | 150 | |
| **ESD Susceptibility** | | | |
| HBM (Human Body Model) | ±2000 | | V |
| CDM (Charged Device Model) | ±750 | | |

## Thermal Information

| Parameter (Note 2) | Typ | Unit |
|---|---|---|
| $\theta_{JA}$ Junction-to-Ambient Thermal Resistance | 25 | °C/W |
| $\theta_{JC\_TOP}$ Junction-to-Case Top Thermal Resistance | 4 | |
| $P_D$ Power Dissipation $T_A$ = 25°C | 5 | W |

## Recommended Operating Conditions

| Parameter (Note 3) | Min | Max | Unit |
|---|---|---|---|
| Supply Input Voltage | 2.6 | 5.5 | V |
| Junction Temperature Range | -40 | 125 | °C |
| Ambient Temperature Range | -40 | 85 | |

## Block Diagram

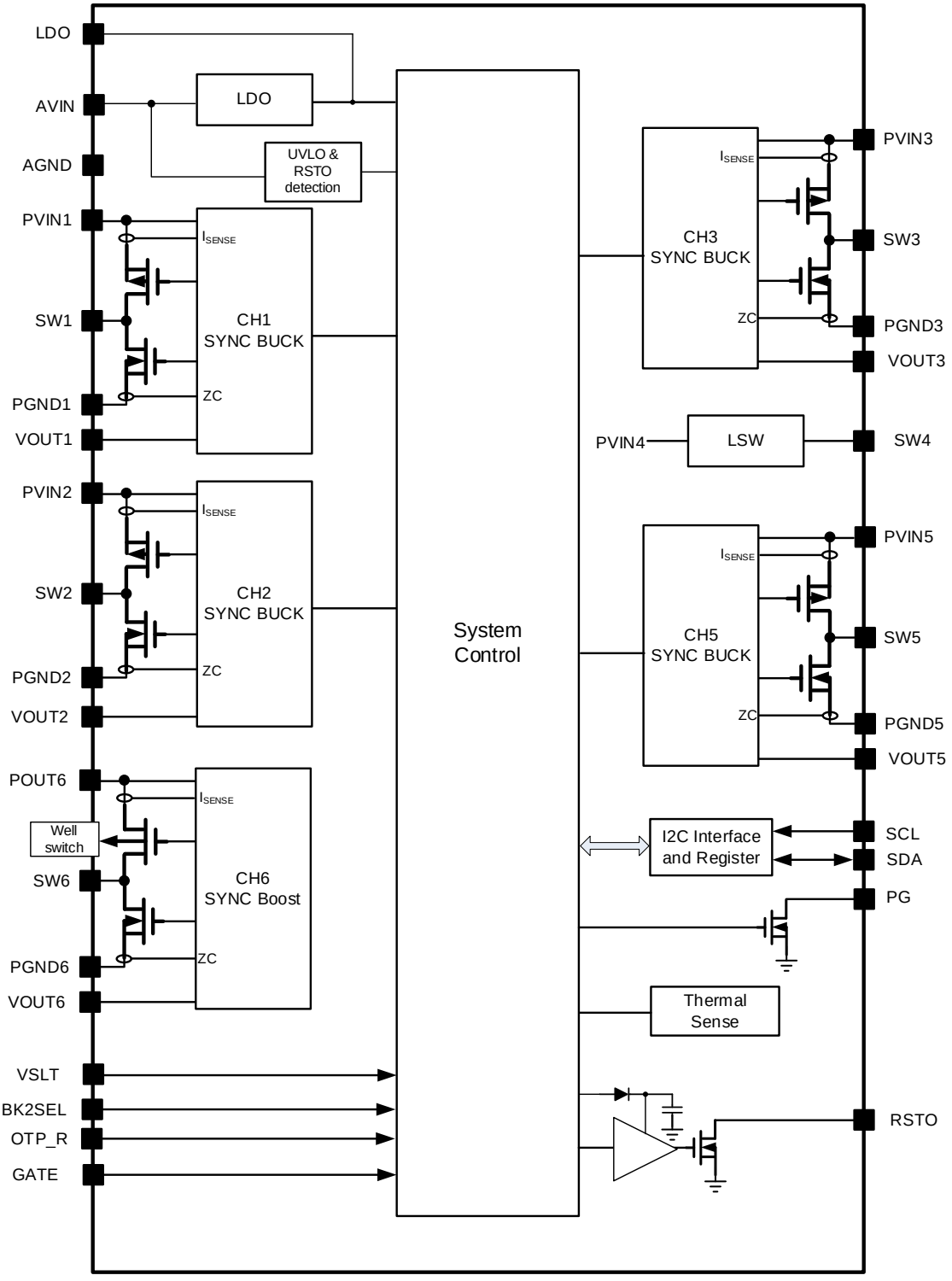



*Figure 2.Block Diagram*

## Electrical Characteristics

($V_{IN}$=3.3V/5V, $T_A$ = 25°C, $T_J$ = -40°C to +125°C, unless otherwise specified (**Note 4**))

| Parameter | | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input Supply (VIN) | Input Voltage Range | | 2.6 | - | 5.5 | V |
| | UVLO Falling Threshold | VSLT = 0 | | 2.7 | | V |
| | | VSLT = 1 | - | 3.6 | - | V |
| | UVLO Hysteresis | Vin Rising | | 100 | | mV |
| | UVLO Threshold Accuracy | | -2 | | +2 | % |
| | Quiescent Current | Vin=3.3V, all channel enabled and no load condition | - | - | 400 | uA |
| | System Delay Time (TDelay_SYS) | | 1.6 | 2 | 2.4 | ms |
| | Input OVP Threshold | | 5.66 | 5.8 | 5.94 | V |
| | Input OVP Falling Hysteresis | | | 200 | | mV |
| Gate Driver Input | Logic Level High | | 1.2 | - | - | V |
| | Logic Level Low | | - | - | 0.4 | V |
| | Gate Pin Internally Pull-down Resister | - | | 1.5 | | Mohm |
| Select Input (VSLT) (**Note 5**) | Logic Level High | | 1.2 | | | V |
| | Logic Level Low | | | | 0.4 | V |
| | VSLT Internally Pull down Resister | | | 5 | | Mohm |
| Power On Reset (RSTO)/ Under-Voltage-Lock Out(UVLO) (**Note 6**, **Note 7**) | RSTO Falling Threshold | VSLT = 0 | - | 2.7 | - | V |
| | | VSLT = 1 | - | 3.6 | - | V |
| | RSTO Hysteresis | Vin Rising | | 100 | | mV |
| | RSTO Threshold Accuracy | | -2 | | +2 | % |
| | RSTO Delay Time from POR | | | 10 | | ms |
| | RSTO Delay Time Accuracy for POR | | -10 | | +10 | % |
| | RSTO Pull Low FET $R_{ON}$ | | | 10 | 20 | ohm |
| Power Good Output (PG) | PG Output Low level Voltage(VOL) | IOL = 20mA (sinking) | - | - | 0.4 | V |
| | PG Pull Low FET $R_{ON}$ | | | 10 | 20 | ohm |
| EN Output | Output High level voltage | $V_{OH\_EN}$, connect 100k from EN to GND | 0.8x$V_{IN}$ | | $V_{IN}$ | V |
| | Output Low level voltage | $V_{OL\_EN}$, connect 100k from EN to VIN | 0 | | 0.2x$V_{IN}$ | V |
| | EN Turn High Delay Time from VIN UVLO | $T_{EN}$, after system delay time | | 2 | | ms |
| $I^2C$ Interface (SDA/SCL) | Clock Frequency | - | 0 | - | 3400 | kHz |
| | Input High Voltage (VIH) (note1) | - | 1.4 | - | | V |
| | Input Low Voltage (VIL) (note1) | - | - | - | 0.4 | V |
| | Output Low level Voltage (VOL) | IOL = 20mA (sinking) | - | - | 0.4 | V |
| | $I^2C$ Logic Delay | | | 0 | | |
| Thermal Shutdown | Thermal Shutdown Temperature | Thermal shutdown threshold | - | 150 | - | ℃ |
| | | Thermal shutdown hysteresis | - | 20 | - | ℃ |

## Power Converters

($V_{IN}$ = 3.3V/5V, $T_A$= 25 ˚C, $T_J$ = -40°C to +125°C, unless otherwise specified (**Note 4**))

| Parameter | | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Channel 1 Synchronous Buck Converter | Output Voltage Default Value | | - | 1.2 | - | V |
| | Output Voltage DVS Step | | - | 6.25 | - | mV |
| | Output Voltage DVS Range | Controlled by I2C | 0.725 | - | 1.825 | V |
| | Output Accuracy | @ PWM Mode | -1 | | 1 | % |
| | Output Line Regulation | $V_{IN}$ = 2.6V to 5.5V | - | 0.1 | - | %/V |
| | Switching Frequency | | | 2.0 | | MHz |
| | High Side FET Ron | PFET switch (VIN to SW) | - | 25 | - | mohm |
| | Low Side FET Ron | NFET switch (SW to GND) | - | 10 | - | mohm |
| | Max Output DC Load Current | | 3.5 | - | - | A |
| | High Side FET Current Limit | | 6 | | 8 | A |
| | Negative Current Limit | | 0.9 | | | A |
| | DVS Slew Rate | | | 2 | | us/step |
| | Soft Start Time | Rising Slew (10% to 90%) | | 200 | | us |
| | Soft Start Time Tolerance | - | -30 | - | 30 | % |
| | Output Load Transient | $V_{IN}$ = 3.3V<br>Each rising and falling from 1mA to 1.7A (1.0A/us Slew rate) | -3 | Target Voltage | 3 | % |
| | Output OVP Threshold | | | 2.231 | | V |
| | Start-up Default Delay Time | Power up (500us Step)<br>Programmable by OTP | 0 | 3 | 7.5 | ms |
| | Start-up Delay Tolerance | - | -30 | - | 30 | % |
| | Discharge Resistance | $I^2C$ Control (2 or 10)<br>Dis_R bit=0(default) | | 10 | | ohm |
| | | Dis_R bit=1 | | 2 | | |
| | Discharge Resistance Accuracy | $V_{IN}$=3.3V, $V_{OUT}$=default value, $T_A$=25 ˚C | -40 | | 40 | % |
| Channel 2 Synchronous Buck Converter | Output Voltage Default Value | BK2SEL=VIN | - | 1.2 | - | V |
| | | BK2SEL=GND | | 1.1 | | |
| | Output Voltage DVS Step | | - | 6.25 | - | mV |
| | Output Voltage DVS Range | Controlled by $I^2C$ | 0.5 | - | 1.2 | V |
| | Output Accuracy | @ PWM Mode | -1 | | 1 | % |
| | Output Line Regulation | $V_{IN}$ = 2.6V to 5.5V | - | 0.1 | - | %/V |
| | Switching Frequency | | | 2.0 | | MHz |
| | FET Ron | PFET switch (VIN to SW) | - | 25 | - | mohm |
| | | NFET switch (SW to GND) | - | 10 | - | mohm |
| | Max Output DC Load Current | | 3.8 | - | - | A |
| | High Side FET Current Limit | | 5.7 | | 7.5 | A |
| | Negative Current Limit | | 0.8 | | | A |
| | DVS Slew Rate | | | 2 | | us/step |
| | Soft Start Time | Rising Slew (10% to 90%) | | 200 | | us |
| | Soft Start Time Tolerance | - | -30 | - | 30 | % |
| | Output Load Transient | $V_{IN}$ = 3.3V | -3 | Target Voltage | 3 | % |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | Each rising and falling from 1mA to 1.9A (1A/us Slew rate) | | | | |
| | Output OVP Threshold | | | 1.31 | | V |
| | Start-up Default Delay Time | By Power up (500us Step) Programmable by OTP | 0 | 1 | 7.5 | ms |
| | Start-up Delay Tolerance | - | -30 | - | 30 | % |
| | Discharge Resistance | $I^2C$ Control (2 or 10) Dis_R bit=0 | - | 2 | | ohm |
| | | Dis_R bit=1(default) | | 10 | | |
| | Discharge Resistance Accuracy | $V_{IN}$=3.3V, $V_{OUT}$=default value, $T_A$=25 ˚C | -40 | | 40 | % |
| Channel 3 Synchronous Buck Converter | Output Voltage Default Value | | - | 1.8 | - | V |
| | Output Voltage DVS Step | | - | 7.5 | - | mV |
| | Output Voltage DVS Range | Controlled by $I^2C$ | 0.96 | - | 1.86 | V |
| | Output Accuracy | @ PWM Mode | -1 | | 1 | % |
| | Output Line Regulation | $V_{IN}$ = 2.6V to 5.5V | - | 0.1 | - | %/V |
| | Switching Frequency | | | 2.5 | | MHz |
| | High Side FET Ron | PFET switch (VIN to SW) | - | 30 | - | mohm |
| | Low Side FET Ron | NFET switch (SW to GND) | - | 12 | - | mohm |
| | Max Output DC Load Current | | 3.0 | - | - | A |
| | High Side FET Current Limit | | 6 | | 7.8 | A |
| | Negative current limit | | 1.4 | | | A |
| | DVS Slew Rate | | | 2 | | us/step |
| | Soft Start Time | Rising Slew (10% to 90%) | | 200 | | us |
| | Soft Start Time Tolerance | - | -30 | - | 30 | % |
| | Output Load Transient | $V_{IN}$ = 3.3V Each rising and falling from 1mA to 1.5A (1A/us Slew rate) | -3 | Target Voltage | 3 | % |
| | Output OVP Threshold | | | 2.025 | | V |
| | Start-up Default Delay Time | By Power up (500us Step) Programmable by OTP | 0 | 0 | 7.5 | ms |
| | Start-up Delay Tolerance | - | -30 | - | 30 | % |
| | Discharge Resistance | $I^2C$ Control (2 or 10) Dis_R bit=0(default) | - | 10 | | ohm |
| | | Dis_R bit=1 | | 2 | | |
| | Discharge Resistance Accuracy | $V_{IN}$=3.3V, $V_{OUT}$=default value, $T_A$=25 ˚C | -40 | | 40 | % |
| Channel 5 Synchronous Buck Converter | Output Voltage Default Value | | - | 2.5 | - | V |
| | Output Voltage DVS Step | | - | 12.5 | - | mV |
| | Output Voltage DVS Range | Controlled by $I^2C$ | 1.5 | - | 2.75 | V |
| | Output Accuracy | @ PWM Mode | -1 | | 1 | % |
| | Output Line Regulation | $V_{IN}$ = 2.6V to 5.5V | - | 0.1 | - | %/V |
| | Switching Frequency | | | 2.3 | | MHz |
| | High Side FET Ron | PFET switch (VIN to SW) | - | 20 | - | mohm |
| | Low Side FET Ron | NFET switch (SW to GND) | - | 15 | - | mohm |
| | Max Output DC Load Current | | 4 | - | - | A |
| | High Side FET Current Limit | | 7 | | 9.1 | A |
| | Negative current limit | | 2 | | | A |

| | | | | | | |
|---|---|---|---|---|---|---|
| | DVS Slew Rate | | | 4 | | us/step |
| | Soft Start Time | Rising Slew (10% to 90%) | | 200 | | us |
| | Soft Start Time Tolerance | - | -30 | - | 30 | % |
| | Output Load Transient | $V_{IN}$ = 3.3V<br>Each rising and falling from 1mA to 2.0A (1A/us Slew rate) | -3 | Target Voltage | 3 | % |
| | Output OVP Threshold | | | 3.63 | | V |
| | Start-up Default Delay Time | By Power up (500us Step)<br>Programmable by OTP | 0 | 0 | 7.5 | ms |
| | Start-up Delay Tolerance | - | -30 | - | 30 | % |
| | Discharge Resistance | $I^2C$ Control (2 or 10)<br>Dis_R bit=0 | - | 2 | | ohm |
| | | Dis_R bit=1(default) | | 10 | | |
| | Discharge Resistance Accuracy | $V_{IN}$=3.3V, $V_{OUT}$=default value, $T_A$=25 ˚C | -40 | | 40 | % |
| Channel 6 Synchronous Boost Converter | Output Voltage Default Value | | | 12 | | V |
| | Output Voltage DVS Step | | | 500 | | mV |
| | Output Voltage DVS Range | Controlled by $I^2C$ | 8 | | 15 | V |
| | Output Accuracy | @ PWM | -1 | | +1 | % |
| | Line Regulation | $V_{IN}$ = 2.6V to 5.5V | | 0.1 | | %/V |
| | Switching Frequency | | | 1.8 | | MHz |
| | High Side FET Ron | PFET switch (VIN to SW) | | 120 | | mohm |
| | Low Side FET Ron | NFET switch (SW to GND) | | 70 | | mohm |
| | Max Output DC Load Current | $V_{IN}$=3V Min. | 0.4 | | | A |
| | NFET Current Limit | $V_{IN}$=3V Min. | 3.1 | | 4.5 | A |
| | Negative current limit | | 1.3 | | | A |
| | DVS Slew Rate | | | 32 | | us/step |
| | Soft Start Time | Rising Slew (10% to 90%) | | 1.5 | | ms |
| | Soft Start Time Tolerance | - | -30 | - | 30 | % |
| | Output Load Transient | $V_{IN}$ = 3.3V<br>Each rising and falling from 1mA to 0.35A ( 30us Slew) | -3 | | +3 | % |
| | Output OVP Threshold | | | 14.25 | | V |
| | Start-up Default Delay Time | By Power up (500us Step)<br>Programmable by OTP | 0 | 4 | 7.5 | ms |
| | Start-up Delay Tolerance | - | -30 | - | 30 | % |
| | Discharge Resistance | $I^2C$ Control (100 or 300)<br>Dis_R bit=0 | - | 300 | | ohm |
| | | Dis_R bit=1(default) | | 100 | | |
| | Discharge Resistance Accuracy | $V_{IN}$=3.3V, $V_{OUT}$=12V, $T_A$=25deg | -20 | | 20 | % |
| Load Switch | Output Voltage | | | VIN | - | V |
| | LSW Ron | | - | 100 | 130 | mohm |
| | Maximum DC Output Current | | 250 | | | mA |
| | Current Limit | | 260 | | 600 | mA |
| | SCP Threshold | | | 2 | | V |
| | SCP Deglitch Time | | | 150 | | us |
| | Soft Start Time | $V_{IN}$=3.3V, Rising Slew (10% to 90%) | | 200 | | us |

| | | | | | | |
|---|---|---|---|---|---|---|
| | Soft Start Time Tolerance | - | -30 | - | 30 | % |
| | Start-up Default Delay Time | By Power up (500us Step) Programmable by OTP | 0 | 0 | 7.5 | ms |
| | Start-up Delay Tolerance | - | -30 | - | 30 | % |
| | Discharge Resistance | | | 100 | | ohm |

**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:** $\theta_{JA}$ is measured in the natural convection at $T_A$ = 25°C on a four-layer Silergy Evaluation Board.

**Note 3:** The device is not guaranteed to function outside its operating conditions.

**Note 4:** It is guaranteed to satisfy ELECTRICAL SPECIFICATIONS under temperature condition. (-40˚C ~85˚C)

**Note 5:** The VSLT pin is connected to GND at 3.3V Input, VSLT pin is connected to VIN at 5.0Vin input.

**Note 6:** RSTO pin should be low immediately after the VIN voltage is below RSTO Threshold.

Rising Threshold = RSTO Threshold + RSTO Hysteresis(100mV)

Falling Threshold = RSTO Threshold

**Note 7:** Power on Reset(RSTO) should be high after Start up Delay Time which should be programmable by OTP when VIN voltage is above RSTO threshold voltage with RSTO Hysteresis (100mV).

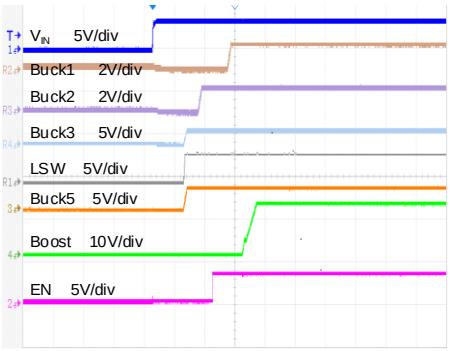
Even if the Input Voltage doesn’t fall on UVLO under, it has to operate identically.

## Typical Performance Characteristics

($T_A$=25℃)

Power On Sequence

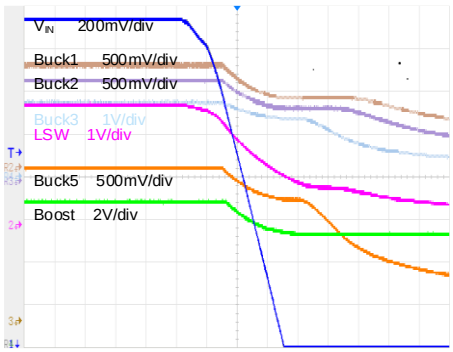
($V_{IN}$=3.3V, Buck1=1.2V, Buck2=1.2V, Buck3=1.8V, Buck5=2.5V, LSW=3.3V, Boost=12V, $I_{OUT}$=0A)




Time (2ms/div)

Power Off Sequence

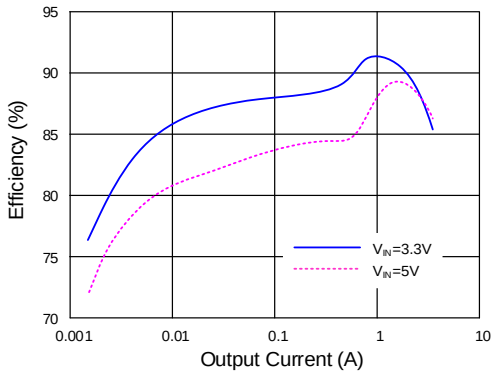
($V_{IN}$=3.3V, Buck1=1.2V, Buck2=1.2V, Buck3=1.8V, Buck5=2.5V, LSW=3.3V, Boost=12V, $I_{OUT}$=0A)




Time (50μs/div)

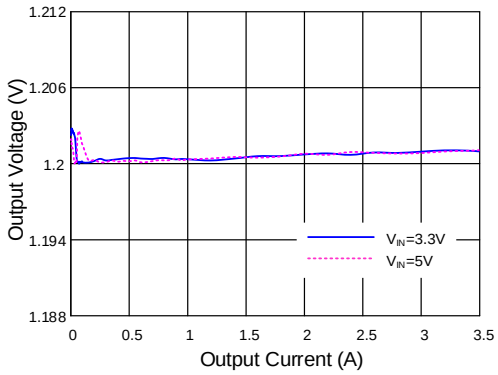
Buck1 Efficiency

($V_{IN}$=3.3/5V, $V_{OUT}$=1.2V, L=0.47μH, $C_{OUT}$=94μF, $I_{OUT}$=0-3.5A,PFM)



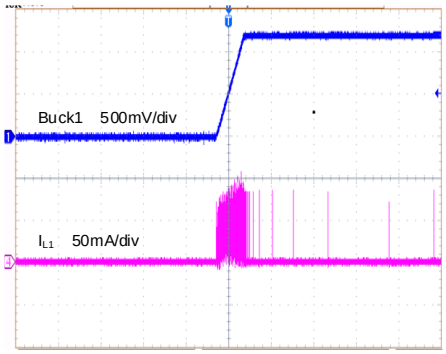

Buck1 Load Regulation

($V_{IN}$=3.3/5V, $V_{OUT}$=1.2V, L=0.47μH, $C_{OUT}$=94μF, $I_{OUT}$=0-3.5A,PFM)




Buck1 Power On

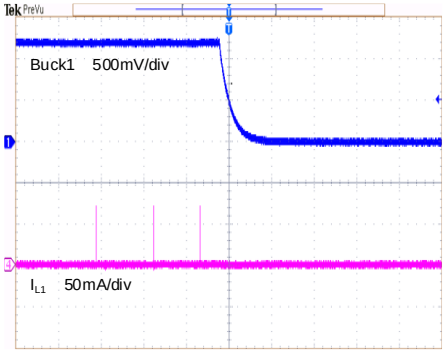
($V_{IN}$=3.3V, $V_{OUT}$=1.2V, L=0.47μH, $C_{OUT}$=94μF, $I_{OUT}$=0A)




Time (400μs/div)

Buck1 Power Off

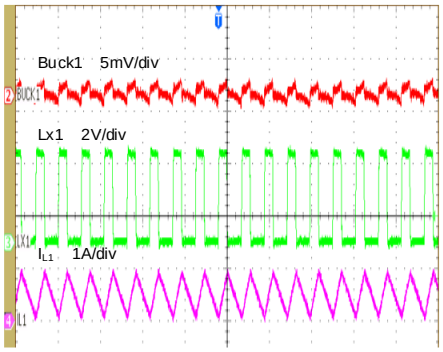
($V_{IN}$=3.3V, $V_{OUT}$=1.2V, L=0.47μH, $C_{OUT}$=94μF, $I_{OUT}$=0A)




Time (2ms/div)

Buck1 Ripple

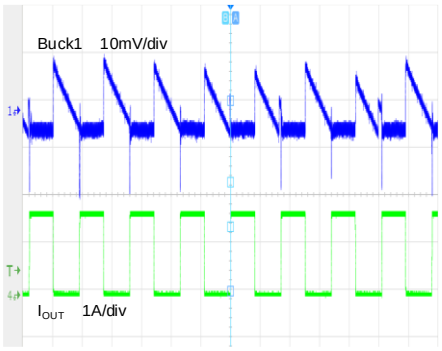
($V_{IN}$=3.3V, $V_{OUT}$=1.2V, L=0.47μH, $C_{OUT}$=94μF, $I_{OUT}$=0.5A)




Time (1μs/div)

Buck1 Transient

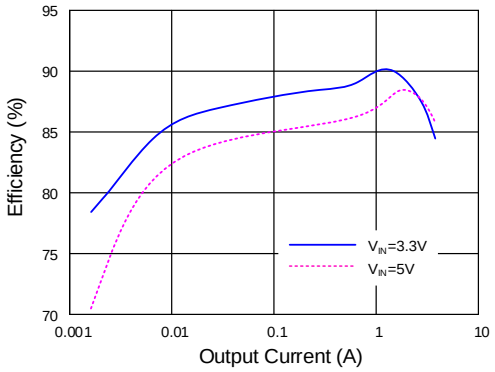
($V_{IN}$=3.3V, $V_{OUT}$=1.2V, L=0.47μH, $C_{OUT}$=94μF,
$I_{OUT}$=0.001~1.7A(1.72μs), FCCM)




Time (5μs/div)

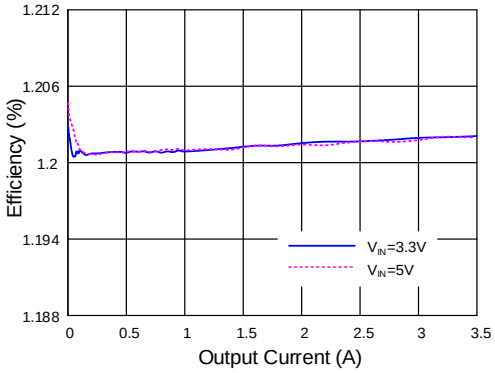
Buck2 Efficiency

($V_{IN}$=3.3/5V, $V_{OUT}$=1.2V, L=0.22μH, $C_{OUT}$=94μF, $I_{OUT}$=0-3.8A,PFM)



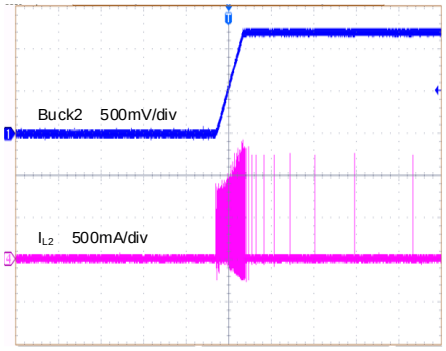

Buck2 Load Regulation

($V_{IN}$=3.3/5V, $V_{OUT}$=1.2V, L=0.22μH, $C_{OUT}$=94μF, $I_{OUT}$=0-3.8A,PFM)




Buck2 Power On

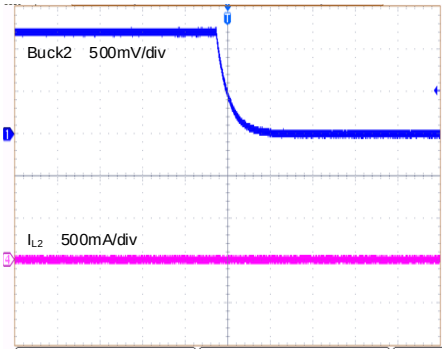
($V_{IN}$=3.3V, $V_{OUT}$=1.2V, L=0.22μH, $C_{OUT}$=94μF, $I_{OUT}$=0A)




Time (400μs/div)

Buck2 Power Off

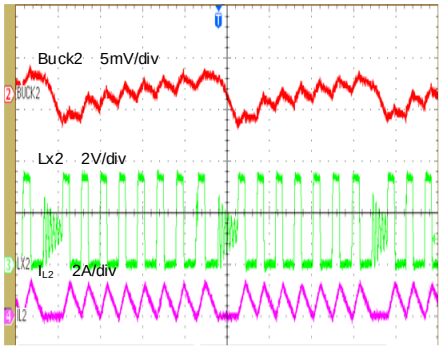
($V_{IN}$=3.3V, $V_{OUT}$=1.2V, L=0.22μH, $C_{OUT}$=94μF, $I_{OUT}$=0A)




Time (2ms/div)

Buck2 Ripple

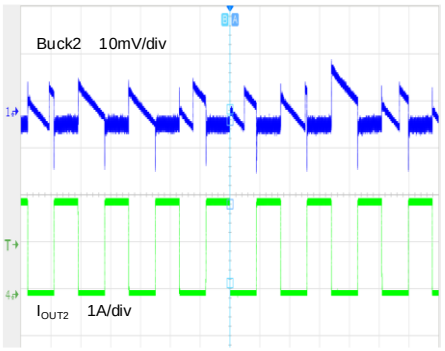
($V_{IN}$=3.3V, $V_{OUT}$=1.2V, L=0.22µH, $C_{OUT}$=94µF, $I_{OUT}$=0.5A)




Time (1µs/div)

Buck2 Transient

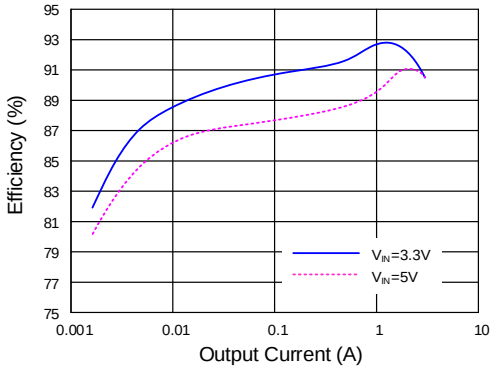
($V_{IN}$=3.3V, $V_{OUT}$=1.2V, L=0.22µH, $C_{OUT}$=94µF, $I_{OUT}$=0.001~1.9A)




Time (2ms/div)

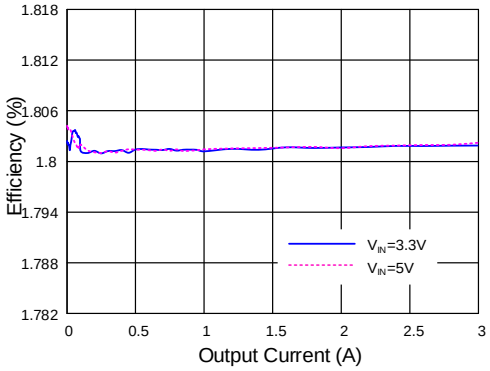
Buck3 Efficiency

($V_{IN}$=3.3/5V, $V_{OUT}$=1.8V, L=0.22µH, $C_{OUT}$=94µF, $I_{OUT}$=0-3A,PFM)



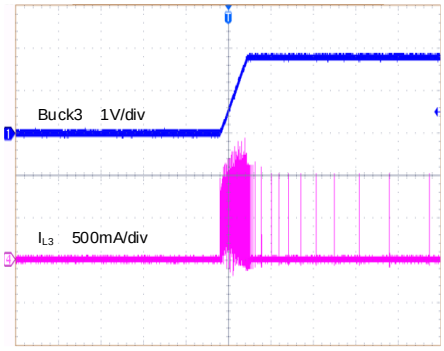

Buck3 Load Regulation

($V_{IN}$=3.3/5V, $V_{OUT}$=1.8V, L=0.22µH, $C_{OUT}$=94µF, $I_{OUT}$=0-3A,PFM)




Buck3 Power On

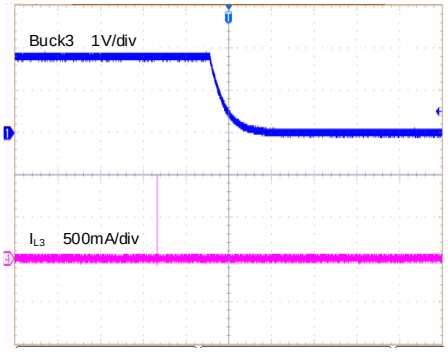
($V_{IN}$=3.3V, $V_{OUT}$=1.8V, L=0.22µH, $C_{OUT}$=94µF, $I_{OUT}$=0A)




Time (400µs/div)

Buck3 Power Off

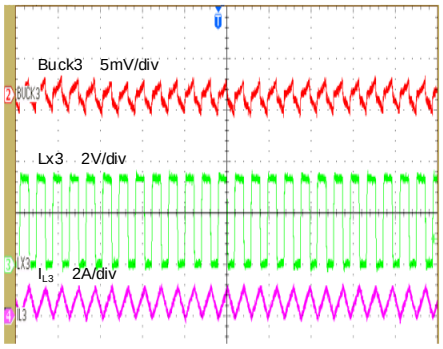
($V_{IN}$=3.3V, $V_{OUT}$=1.8V, L=0.22µH, $C_{OUT}$=94µF, $I_{OUT}$=0A)




Time (2ms/div)

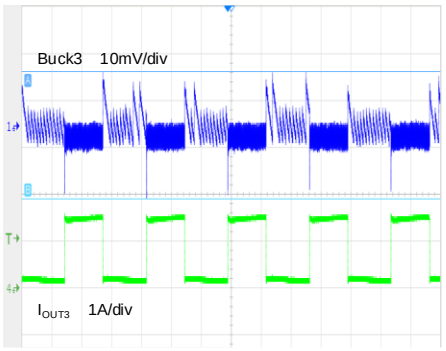
Buck3 Ripple

($V_{IN}$=3.3V, $V_{OUT}$=1.8V, L=0.22µH, $C_{OUT}$=94µF, $I_{OUT}$=0.5A)



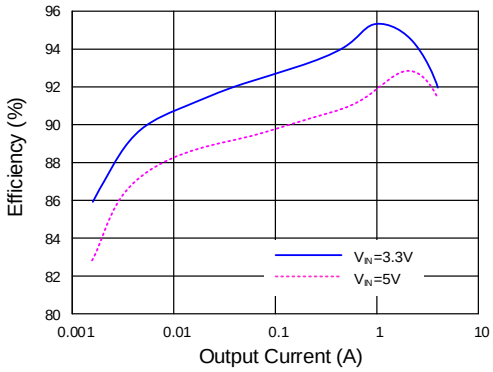

Buck3 Transient

($V_{IN}$=3.3V, $V_{OUT}$=1.8V, L=0.22µH, $C_{OUT}$=94µF, $I_{OUT}$=0.001~1.5A)



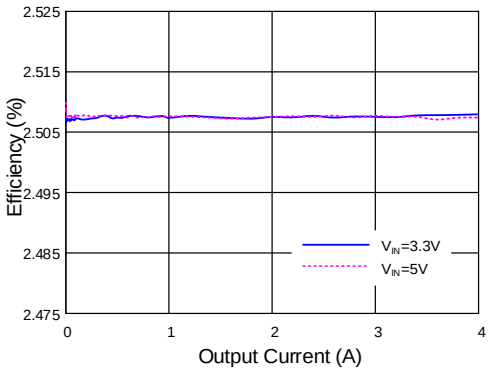

Buck5 Efficiency

($V_{IN}$=3.3/5V, $V_{OUT}$=2.5V, L=0.22µH, $C_{OUT}$=66µF, $I_{OUT}$=0-4A,PFM)



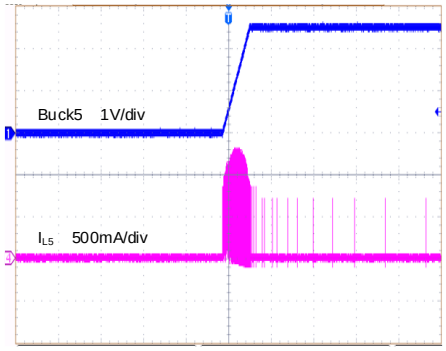

Buck5 Load Regulation

($V_{IN}$=3.3/5V, $V_{OUT}$=2.5V, L=0.22µH, $C_{OUT}$=66µF, $I_{OUT}$=0-4A,PFM)



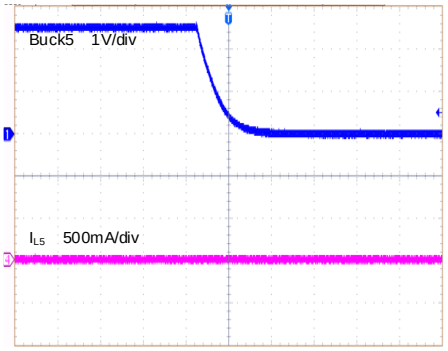

Buck5 Power On

($V_{IN}$=3.3V, $V_{OUT}$=2.5V, L=0.22µH, $C_{OUT}$=66µF, $I_{OUT}$=0A)



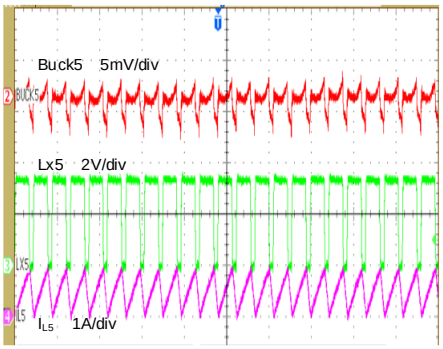

Buck5 Power Off

($V_{IN}$=3.3V, $V_{OUT}$=2.5V, L=0.22µH, $C_{OUT}$=66µF, $I_{OUT}$=0A)



Buck5 Ripple

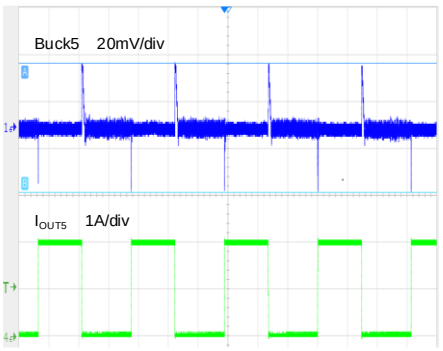
($V_{IN}$=3.3V, $V_{OUT}$=2.5V, L=0.22µH, $C_{OUT}$=66µF, $I_{OUT}$=0.5A)




Time (1µs/div)

Buck5 Transient

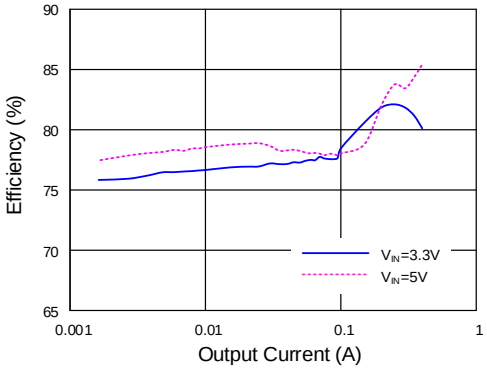
($V_{IN}$=3.3V, $V_{OUT}$=2.5V, L=0.22µH, $C_{OUT}$=66µF, $I_{OUT}$=0.001~2A)




Time (2ms/div)

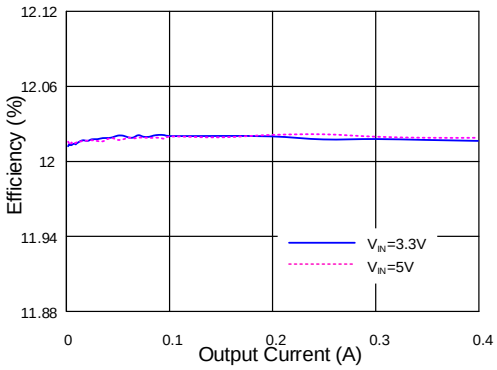
Boost Efficiency

($V_{IN}$=3.3/5V, $V_{OUT}$=12V, L=1.00µH, $C_{OUT}$=23.5µF, $I_{OUT}$=0-0.4A, PFM)



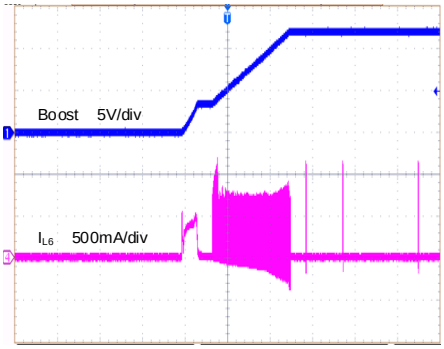

Boost Load Regulation

($V_{IN}$=3.3/5V, $V_{OUT}$=12V, L=1.00µH, $C_{OUT}$=23.5µF, $I_{OUT}$=0-0.4A,PFM)




Boost Power On

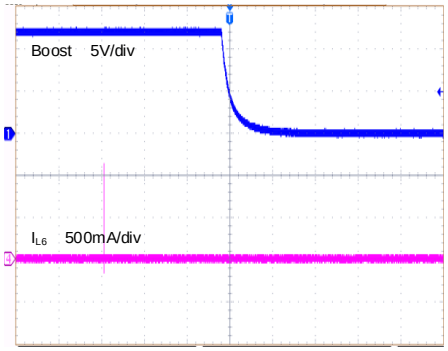
($V_{IN}$=3.3V, $V_{OUT}$=12V, L=1.00µH, $C_{OUT}$=23.5µF, $I_{OUT}$=0A)




Time (400µs/div)

Boost Power Off

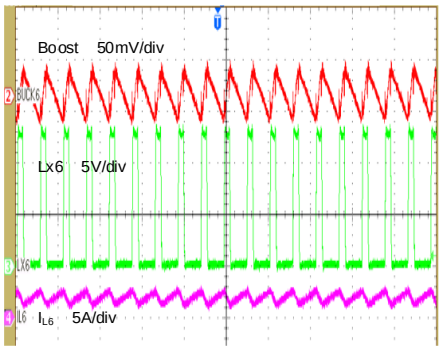
($V_{IN}$=3.3V, $V_{OUT}$=12V, L=1.00µH, $C_{OUT}$=23.5µF, $I_{OUT}$=0A)




Time (2ms/div)

Boost Ripple

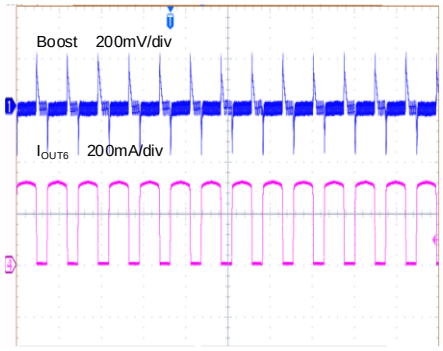
($V_{IN}$=3.3V, $V_{OUT}$=12V, L=1.00µH, $C_{OUT}$=23.5µF, $I_{OUT}$=0.4A)




Time (2ms/div)

Boost Transient

($V_{IN}$=3.3V, $V_{OUT}$=12V, L=1.00µH, $C_{OUT}$=23.5µF, $I_{OUT}$=0.001~0.35A)




Time (2ms/div)

# Functional Description

## Power On/Off Sequence

Power sequence start after input voltage $V_{IN}$ exceeds UVLO/RSTO rising threshold and there is a system delay time ($T_{Delay\_sys}$) which is about 2ms. Each channel output discharge will turn on forcedly during the 2ms $T_{Delay\_sys}$ and each channel turn on delay time Tch[n].on. After system delay time and each channel turn on delay time, each channel output voltage will ramp up to the target value with softstart time.

If VIN goes down under UVLO level, each channel will turne off after delay time. The channel discharge function will keep on or keep off according to related I²C setting register. .

UVLO/RSTO threshold (Rising) is high priority. When UVLO/RSTO threshold (Rising) is detected, all channels will be reset.

EN pin is independent output pin, it will go high after fixed delay time at $V_{IN}$ power up and go low with power off delay when VIN UVLO OFF.

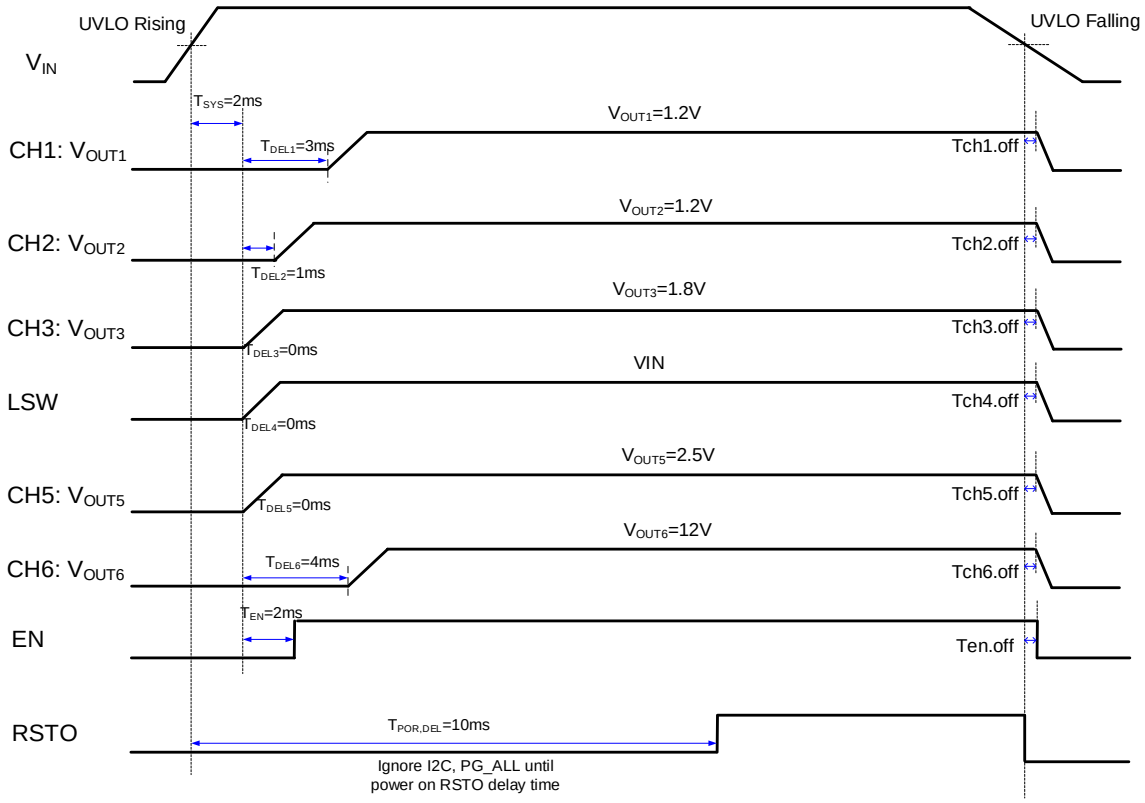



*Figure 3. Power On/Off Sequence*

*Table 1. Power On Sequence*

| Channel | Default Voltage | Start-up Delay Time | | OTP Program Range | OTP Program Step |
|---|---|---|---|---|---|
| | | Name | Default | | |
| CH1 | 1.2V | Tch1.on | 3ms | 0~7.5ms | 0.5ms |
| CH2 | 1.2V | Tch2.on | 1ms | 0~7.5ms | 0.5ms |
| CH3 | 1.8V | Tch3.on | 0ms | 0~7.5ms | 0.5ms |
| LSW | VIN | $T_{LS}$.on | 0ms | 0~7.5ms | 0.5ms |
| CH5 | 2.5V | Tch5.on | 0ms | 0~7.5ms | 0.5ms |
| CH6 | 12V | Tch6.on | 4ms | 0~7.5ms | 0.5ms |
| EN | VIN | $T_{EN}$ | 2ms | 0~7.5ms | 0.5ms |
| RSTO | POR_VRSTO_DELAY | | 10ms | 7ms~14ms | 1ms |

**Power on stage:** When $V_{IN}$ exceeds the threshold voltage, RSTO will provide a high-level output signal after a fixed delay time TPOR,DEL. The start-up delay time can be programmed by internal OTP.

*Table 2. Power off Sequence*

| Channel | Default Voltage | Off Delay Time | | OTP Program Range | OTP Program Step |
|---|---|---|---|---|---|
| | | Name | Default | | |
| CH1 | 1.2V | Tch1.off | 25us | 25~175us | 50us |
| CH2 | 1.2V | Tch2.off | 25us | 25~175us | 50us |
| CH3 | 1.8V | Tch3.off | 25us | 25~175us | 50us |
| CH4 | VIN | Tch4.off | 25us | 25~175us | 50us |
| CH5 | 2.5V | Tch5.off | 25us | 25~175us | 50us |
| CH6 | 12V | Tch6.off | 25us | 25~175us | 50us |
| EN | VIN | Ten.off | 25us | 25~175us | 50us |

**Power off stage:** When $V_{IN}$ is below UVLO falling threshold voltage, each channel will be turn off after off delay time. The Off-delay time can be programmed by internal OTP.

## RSTO (Power on Reset)

When $V_{IN}$ reaches the target threshold voltage, RSTO (Power on Reset) will be high after TRSTO_DELAY time (the default 10ms), $I^2C$ is only enable after RSTO 10ms delay is finished.

When $V_{IN}$ drops below the RSTO Threshold Voltage selected by VSLT state, RSTO (Power On Reset) will be low and when RSTO threshold (@Falling) is detected, $I^2C$ will be disable.

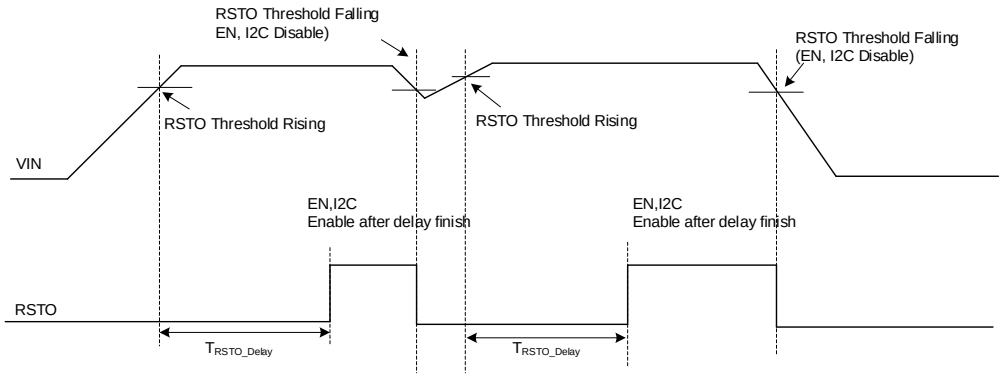



*Figure 4. RSTO Operation*

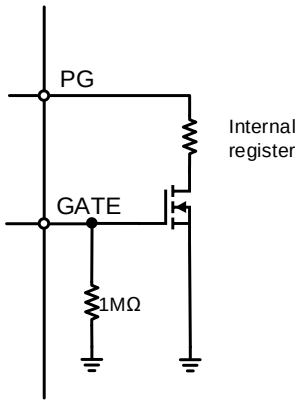
## Gate and PG Pin Function Description

The internal structure of PG pin and Gate pin is shown as below.

PG pin is connected to internal NFET driver output, which is controlled by Gate pin.

Pull Low Gate pin to turn off the PG internal NFET, PG pin will be pulled high by external resister.

Pull High Gate pin to turn on the PG internal NFET, PG pin will be pulled low by internal NFET.




## OVP Function Description

When the regulators output voltage or $V_{IN}$ exceed the over voltage protection (OVP) threshold, the OVP is activated and if this continues for min 2us, all channels will be turned off. To restart the channels, the input voltage should be recovered after the fault condition is removed.

**Case1. Each channels Output Voltage OVP Range (Accuracy ±2.5%)**

If output voltage exceeds below OVP threshold, all channels will be turned off at the same time and latched.

*Table 3. Output OVP Threshold Range*

| Channel | $V_{OUT}$ | OVP Threshold |
|---|---|---|
| CH1 | 1.2V | 2.231V |
| Ch2 | 1.2V | 1.31V |
| CH3 | 1.8V | 2.025V |
| CH4 | NA | NA |
| CH5 | 2.5V | 3.63V |
| CH6 | 12V | 14.25V |

**Case2. External Input Voltage OVP (Accuracy ±2.5%)**

If Input voltage exceed 5.8V, all channels will be turned off at the same time.

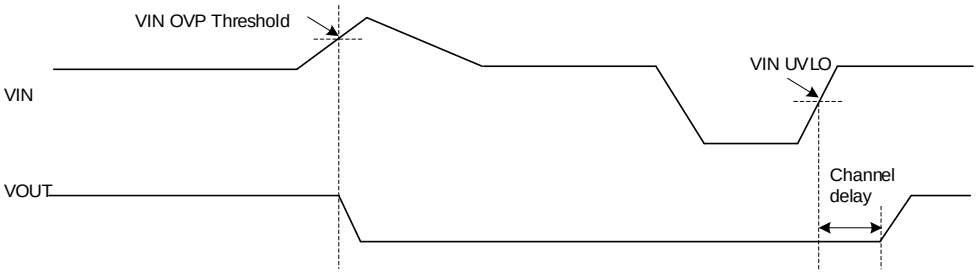



*Figure 5. External VIN OVP Operation*

## STO (Power on Reset) Sequence

When $V_{IN}$ reaches the target threshold voltage, RSTO should be high after VRSTO_DELAY. VRSTO_DELAY has the default 10ms and should be programmable by OTP from 7ms to 14ms with 1ms step. RSTO is open drain type and should be connected to VIN or VOUT regulated by a voltage regulator with a resistor(500ohm ~100Kohm) . When $V_{IN}$ drops below the RSTO threshold voltage or RSTO is set to 0 by 0x09 register, RSTO is immediately pulled low without delay.

## Thermal Shutdown (TSD)

All channels should be shut down when the IC temperature exceeds the whole converter at a die temperature of 150 degree and turned on with a down hysteresis of 20 degree.

## Over Load Protection (OLP)

If the output voltages of the regulators are below about 80% of the target output voltage and keep longer than 150us, then the over load protection (OLP) is activated, this channel will be turned off. And it is fault latch. To reactivate the channel, the input voltage should be recovered after the fault condition is removed.

## Over Current Protection (OCP)

The output over current protection (OCP) is implemented using a cycle-by-cycle peak detect control circuit. The switch current is monitored by measuring the high-side MOSFET switch voltage between the SW pin and VIN. This voltage is proportional to the switch. When the sensing voltage reflected by high-side current is above the proportional voltage to the current limit, Buck converter will turn off the high-side MOSFET.

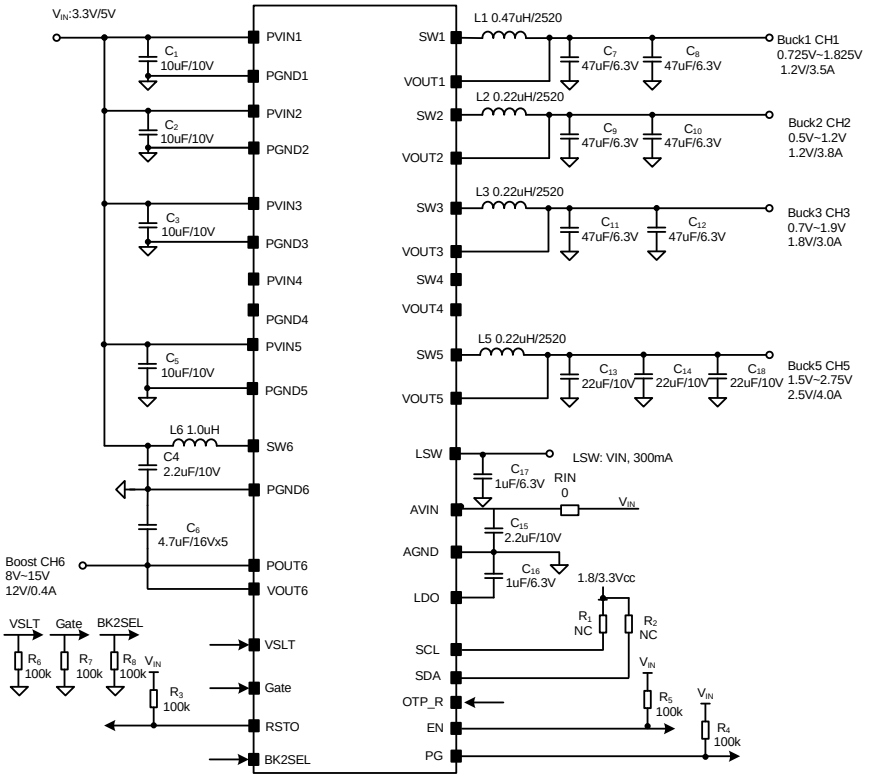
For Boost converter, the current limit circuit turns off the low-side MOSFET in the same way.

## Under Voltage Lock Out (UVLO)

The UVLO circuit for the PMIC prevents the device from malfunctioning at low-input voltage.

1) The output of each channel should be enabled in sequence after the input voltage reaches UVLO Threshold.
2) The output of each channel should be disabled at the same time without regard to output voltage level after the input voltage is below UVLO threshold and turn on discharge function.

## Application Schematic




## BOM List

| Reference Designator | Description | Part Number | Manufacturer |
|---|---|---|---|
| $U_1$ | PMIC | SY70201QPQ | Silergy |
| $C_1$, $C_2$, $C_3$, $C_5$ | 10uF/10V,0603,X5R | CL05A106MP5NUNZ | SEC, Murata |
| $C_{16}$,$C_{17}$ | 1uF/6.3V, 0603, X6S | GRM033C80G105MEA2D | Murata |
| $C_4$,$C_{15}$ | 2.2uF/10V, 0603, X5R | CL03A225KP3CRNC | SEC |
| $C_6$ | 4.7uF/16V, 0603, X5R | CL10A476MQ8QRNC | SEC |
| $C_7$,$C_8$,$C_9$,$C_{10}$,$C_{11}$,$C_{12}$ | 47uF/6.3V, 1608, X5R | CL10A476MQ8QRNC | SEC |
| $C_{13}$,$C_{14}$,$C_{18}$ | 22uF/10V, 1608, X5R | CL10A226MP8NUNE | SEC |
| $L_1$ | 0.47uH, 25mohm, 4.3A 2012 | CIGT201210EHR47MRE | SEC |
| $L_2$, $L_3$ ,$L_5$ | 0.22uH 13mohm 2520 | CIG252010EHR22MRE | SEC |
| $L_6$ | 1uH 43mohm 2016 | CIGT201610EH1R0MRE | SEC |
| RIN | 0ohm, 0603 | | |
| $R_1$,$R_2$ | NC | | |
| $R_3$,$R_4$,$R_5$,$R_6$,$R_7$,$R_8$ | 100k, 0603 | | |

## Layout Design

To achieve a higher efficiency and better noise immunity, following components should be placed close to the IC: C, L.

- It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. Reasonable vias are suggested to be placed underneath the ground pad to enhance the soldering quality and thermal performance.
- The decoupling capacitor of PVIN1 must be placed close enough to the PVIN1 pin and PGND1 pins. The loop area formed by the input capacitors, input pins and PGND pins must be minimized. The principle of decoupling capacitor placement for the rest of the Buck and LDO are the same above.
- Inductor need to be placed as close as possible to the chip keeping the switch node small. The PCB copper area associated with LX pin must be minimized to improve the noise immunity, and reduce parasitic inductance and parasitic resistance.
- Avoid the feedback lines ($V_{OUT}$) close to LX(s) or other high-frequency signal lines(SCL/SDA) as much as possible, otherwise the output will be affected by noise.

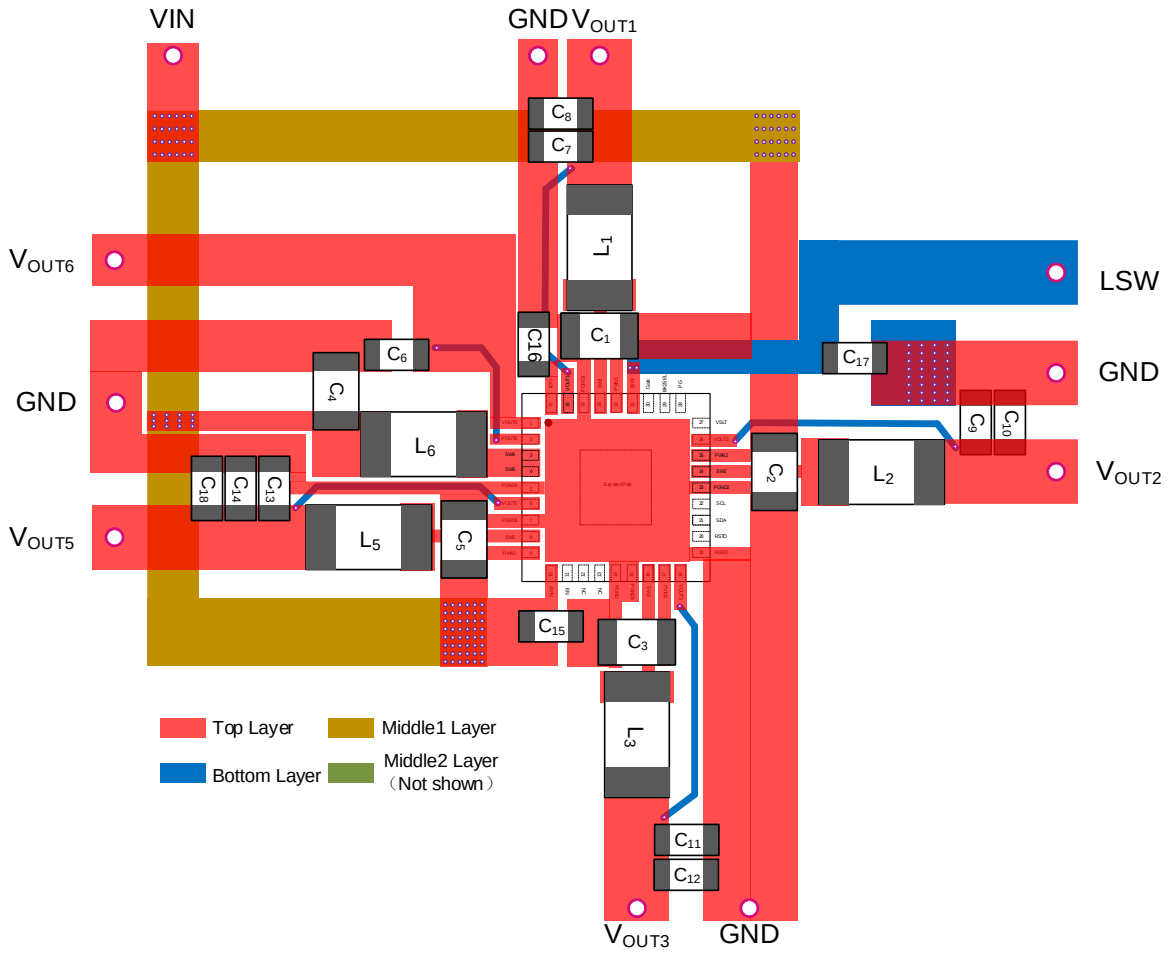



*Figure 7. Suggested PCB Layout*

# Digital Interface (I²C)

## I²C Compatible Interface

The SY70201 support I²C interface that allows the host to control the output voltage level of all channels using DVS function. I²C interface should support clock speeds up to 3.4MHz and use standard I²C commands. High speed mode at 3.4MHz is entered from the master by issuing a special one byte address, bit pattern 00001xxxx(where x is 'don't care).

All transactions start with a control byte sent from the I²C master device. The control byte begins with a START condition, followed by 7-bits of slave address which is 0110000x.

The Electrical Specifications, timing for I/O and bus lines are based on the document of I²C-bus specification and user manual revised on 13 February 2012.

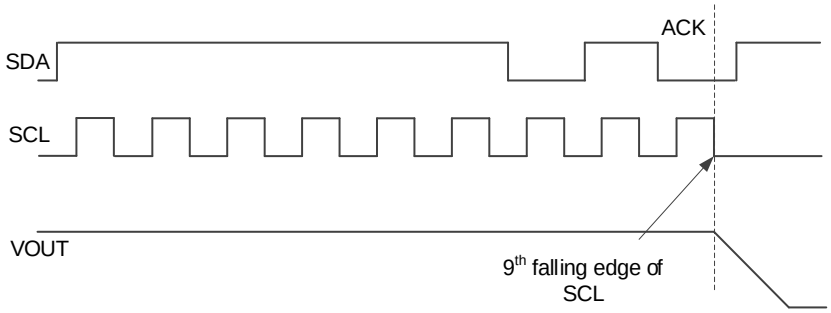
## Slave Address

Slave address is used to select the PMIC on the I²C bus. This address consists of 8-bit data. The LSB 1-bit determines the read or write mode. If the LSB 1-bit is low, the write mode is selected

| Slave Address | Access Mode |
|---|---|
| 0110 0000 (0x60) | Write |
| 0110 0001 (0X61) | Read |

## I²C Data to PMIC Response

IC response at SCL 9th clock falling edge of ACK period, and there is no delay between SCL falling edge and response time.



# Register Map

## Register Map Summary

*Table 4. I²C Control Registers*

| Register Address | Register Name | Defaults Description | Defaults (HEX) | Register Description |
|---|---|---|---|---|
| 0x00 | OUT1_REG | - | 0x64 | Voltage setting for Buck Channel 1 |
| 0x01 | OUT2_REG | - | 0x00 | Voltage setting for Buck Channel 2 |
| 0x02 | Reserved | - | - | Reserved |
| 0x03 | OUT3_REG | - | 0x08 | Voltage setting for Buck Channel 3 |
| 0x04 | OUT4_REG | - | | Reserved |
| 0x05 | OUT5_REG | - | 0x14 | Voltage setting for Buck Channel 5 |
| 0x06 | Reserved | - | - | Reserved |
| 0x07 | OUT6_REG | - | 0x06 | Voltage setting for Booster Channel 6 |
| 0x08 | Power Enable_REG | - | 0xFF | Each power channel enable/disable |
| 0x09 | Etc_Enable_REG | - | 0xFE | Etc Block enable/disable |
| 0x0A | Discharge_Enable_REG | - | 0x39 | Each power channel Discharge enable/disable |
| 0x0B | Discharge_R_REG | | 0xF6 | Discharge resistance of each power channel select |
| 0x0C | Mode_CTRL | - | 0xFF | Auto PWM/PFM Mode or forced PWM mode |
| 0X0D | PG_CHx | - | 0x00 | PG Monitor/CTRL Register |
| 0X0E | OVP_CHx | - | - | Each power channel OVP monitor |
| 0X11 | OCP_CHx | - | - | Each power channel OCP monitor |
| 0X12 | Inform_REG | - | - | Manufacturer, Version, etc |

## Register Settings

### Regulator Output Voltage Setting Mode

These registers control output voltage of each DC/DC regulators and the default data of each Register(0x00~0x07) is interlocked with the Default voltage setting Power on.

*Table 5. Regulator 1 Output Voltage Setting Mode (0X00)*

| Register Name | OUT1_REG | | DVS Registers for Regulator1 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Address | 0x00 | | Output Voltage setting of OUT1<br>DVS from 1.825V to 0.725V in 6.25mV steps | | | | | | | |
| | R/W | Default | Hex | Voltage [V] | Hex | Voltage [V] | Hex | Voltage [V] | Hex | Voltage [V] |
| VOUT1_SET | R/W | 0x64 | 0x00 | 1.825 | 0x2C | 1.55 | 0x58 | 1.275 | 0x84 | 1 |
| | | | 0x01 | 1.81875 | 0x2D | 1.54375 | 0x59 | 1.26875 | 0x85 | 0.99375 |
| | | | 0x02 | 1.8125 | 0x2E | 1.5375 | 0x5A | 1.2625 | 0x86 | 0.9875 |
| | | | 0x03 | 1.80625 | 0x2F | 1.53125 | 0x5B | 1.25625 | 0x87 | 0.98125 |
| | | | 0x04 | 1.8 | 0x30 | 1.525 | 0x5C | 1.25 | 0x88 | 0.975 |
| | | | 0x05 | 1.79375 | 0x31 | 1.51875 | 0x5D | 1.24375 | 0x89 | 0.96875 |
| | | | 0x06 | 1.7875 | 0x32 | 1.5125 | 0x5E | 1.2375 | 0x8A | 0.9625 |
| | | | 0x07 | 1.78125 | 0x33 | 1.50625 | 0x5F | 1.23125 | 0x8B | 0.95625 |
| | | | 0x08 | 1.775 | 0x34 | 1.5 | 0x60 | 1.225 | 0x8C | 0.95 |
| | | | 0x09 | 1.76875 | 0x35 | 1.49375 | 0x61 | 1.21875 | 0x8D | 0.94375 |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0x0A | 1.7625 | 0x36 | 1.4875 | 0x62 | 1.2125 | 0x8E | 0.9375 |
| | | | 0x0B | 1.75625 | 0x37 | 1.48125 | 0x63 | 1.20625 | 0x8F | 0.93125 |
| | | | 0x0C | 1.75 | 0x38 | 1.475 | 0x64 | 1.2 | 0x90 | 0.925 |
| | | | 0x0D | 1.74375 | 0x39 | 1.46875 | 0x65 | 1.19375 | 0x91 | 0.91875 |
| | | | 0x0E | 1.7375 | 0x3A | 1.4625 | 0x66 | 1.1875 | 0x92 | 0.9125 |
| | | | 0x0F | 1.73125 | 0x3B | 1.45625 | 0x67 | 1.18125 | 0x93 | 0.90625 |
| | | | 0x10 | 1.725 | 0x3C | 1.45 | 0x68 | 1.175 | 0x94 | 0.9 |
| | | | 0x11 | 1.71875 | 0x3D | 1.44375 | 0x69 | 1.16875 | 0x95 | 0.89375 |
| | | | 0x12 | 1.7125 | 0x3E | 1.4375 | 0x6A | 1.1625 | 0x96 | 0.8875 |
| | | | 0x13 | 1.70625 | 0x3F | 1.43125 | 0x6B | 1.15625 | 0x97 | 0.88125 |
| | | | 0x14 | 1.7 | 0x40 | 1.425 | 0x6C | 1.15 | 0x98 | 0.875 |
| | | | 0x15 | 1.69375 | 0x41 | 1.41875 | 0x6D | 1.14375 | 0x99 | 0.86875 |
| | | | 0x16 | 1.6875 | 0x42 | 1.4125 | 0x6E | 1.1375 | 0x9A | 0.8625 |
| | | | 0x17 | 1.68125 | 0x43 | 1.40625 | 0x6F | 1.13125 | 0x9B | 0.85625 |
| | | | 0x18 | 1.675 | 0x44 | 1.4 | 0x70 | 1.125 | 0x9C | 0.85 |
| | | | 0x19 | 1.66875 | 0x45 | 1.39375 | 0x71 | 1.11875 | 0x9D | 0.84375 |
| | | | 0x1A | 1.6625 | 0x46 | 1.3875 | 0x72 | 1.1125 | 0x9E | 0.8375 |
| | | | 0x1B | 1.65625 | 0x47 | 1.38125 | 0x73 | 1.10625 | 0x9F | 0.83125 |
| | | | 0x1C | 1.65 | 0x48 | 1.375 | 0x74 | 1.1 | 0xA0 | 0.825 |
| | | | 0x1D | 1.64375 | 0x49 | 1.36875 | 0x75 | 1.09375 | 0xA1 | 0.81875 |
| | | | 0x1E | 1.6375 | 0x4A | 1.3625 | 0x76 | 1.0875 | 0xA2 | 0.8125 |
| | | | 0x1F | 1.63125 | 0x4B | 1.35625 | 0x77 | 1.08125 | 0xA3 | 0.80625 |
| | | | 0x20 | 1.625 | 0x4C | 1.35 | 0x78 | 1.075 | 0xA4 | 0.8 |
| | | | 0x21 | 1.61875 | 0x4D | 1.34375 | 0x79 | 1.06875 | 0xA5 | 0.79375 |
| | | | 0x22 | 1.6125 | 0x4E | 1.3375 | 0x7A | 1.0625 | 0xA6 | 0.7875 |
| | | | 0x23 | 1.60625 | 0x4F | 1.33125 | 0x7B | 1.05625 | 0xA7 | 0.78125 |
| | | | 0x24 | 1.6 | 0x50 | 1.325 | 0x7C | 1.05 | 0xA8 | 0.775 |
| | | | 0x25 | 1.59375 | 0x51 | 1.31875 | 0x7D | 1.04375 | 0xA9 | 0.76875 |
| | | | 0x26 | 1.5875 | 0x52 | 1.3125 | 0x7E | 1.0375 | 0xAA | 0.7625 |
| | | | 0x27 | 1.58125 | 0x53 | 1.30625 | 0x7F | 1.03125 | 0xAB | 0.75625 |
| | | | 0x28 | 1.575 | 0x54 | 1.3 | 0x80 | 1.025 | 0xAC | 0.75 |
| | | | 0x29 | 1.56875 | 0x55 | 1.29375 | 0x81 | 1.01875 | 0xAD | 0.74375 |
| | | | 0x2A | 1.5625 | 0x56 | 1.2875 | 0x82 | 1.0125 | 0xAE | 0.7375 |
| | | | 0x2B | 1.55625 | 0x57 | 1.28125 | 0x83 | 1.00625 | 0xAF | 0.73125 |
| | | | - | | - | | - | | 0xB0 | 0.725 |

*Table 6. Regulator Output Voltage Setting Mode (0x01)*

| **Register Name** | **OUT2_REG** | | **DVS Registers for Regulator2** | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Address | 0x01 | | Output Voltage setting of OUT2<br>DVS from 0.5V to 1.2V in 6.25mV steps | | | | | | | |
| | R/W | Default | Hex | Voltage [V] | Hex | Voltage [V] | Hex | Voltage [V] | Hex | Voltage [V] |
| VOUT2_SET | R/W | 0x00 | 0x00 | 1.2 | 0x2C | 0.925 | 0x58 | 0.65 | 0x84 | - |
| | | | 0x01 | 1.19375 | 0x2D | 0.91875 | 0x59 | 0.64375 | 0x85 | - |
| | | | 0x02 | 1.1875 | 0x2E | 0.9125 | 0x5A | 0.6375 | 0x86 | - |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0x03 | 1.18125 | 0x2F | 0.90625 | 0x5B | 0.63125 | 0x87 | - |
| | | | 0x04 | 1.175 | 0x30 | 0.9 | 0x5C | 0.625 | 0x88 | - |
| | | | 0x05 | 1.16875 | 0x31 | 0.89375 | 0x5D | 0.61875 | 0x89 | - |
| | | | 0x06 | 1.1625 | 0x32 | 0.8875 | 0x5E | 0.6125 | 0x8A | - |
| | | | 0x07 | 1.15625 | 0x33 | 0.88125 | 0x5F | 0.60625 | 0x8B | - |
| | | | 0x08 | 1.15 | 0x34 | 0.875 | 0x60 | 0.6 | 0x8C | - |
| | | | 0x09 | 1.14375 | 0x35 | 0.86875 | 0x61 | 0.59375 | 0x8D | - |
| | | | 0x0A | 1.1375 | 0x36 | 0.8625 | 0x62 | 0.5875 | 0x8E | - |
| | | | 0x0B | 1.13125 | 0x37 | 0.85625 | 0x63 | 0.58125 | 0x8F | - |
| | | | 0x0C | 1.125 | 0x38 | 0.85 | 0x64 | 0.575 | 0x90 | - |
| | | | 0x0D | 1.11875 | 0x39 | 0.84375 | 0x65 | 0.56875 | 0x91 | - |
| | | | 0x0E | 1.1125 | 0x3A | 0.8375 | 0x66 | 0.5625 | 0x92 | - |
| | | | 0x0F | 1.10625 | 0x3B | 0.83125 | 0x67 | 0.55625 | 0x93 | - |
| | | | 0x10 | 1.1 | 0x3C | 0.825 | 0x68 | 0.55 | 0x94 | - |
| | | | 0x11 | 1.09375 | 0x3D | 0.81875 | 0x69 | 0.54375 | 0x95 | - |
| | | | 0x12 | 1.0875 | 0x3E | 0.8125 | 0x6A | 0.5375 | 0x96 | - |
| | | | 0x13 | 1.08125 | 0x3F | 0.80625 | 0x6B | 0.53125 | 0x97 | - |
| | | | 0x14 | 1.075 | 0x40 | 0.8 | 0x6C | 0.525 | 0x98 | - |
| | | | 0x15 | 1.06875 | 0x41 | 0.79375 | 0x6D | 0.51875 | 0x99 | - |
| | | | 0x16 | 1.0625 | 0x42 | 0.7875 | 0x6E | 0.5125 | 0x9A | - |
| | | | 0x17 | 1.05625 | 0x43 | 0.78125 | 0x6F | 0.50625 | 0x9B | - |
| | | | 0x18 | 1.05 | 0x44 | 0.775 | 0x70 | 0.5 | 0x9C | - |
| | | | 0x19 | 1.04375 | 0x45 | 0.76875 | 0x71 | - | 0x9D | - |
| | | | 0x1A | 1.0375 | 0x46 | 0.7625 | 0x72 | - | 0x9E | - |
| | | | 0x1B | 1.03125 | 0x47 | 0.75625 | 0x73 | - | 0x9F | - |
| | | | 0x1C | 1.025 | 0x48 | 0.75 | 0x74 | - | 0xA0 | - |
| | | | 0x1D | 1.01875 | 0x49 | 0.74375 | 0x75 | - | 0xA1 | - |
| | | | 0x1E | 1.0125 | 0x4A | 0.7375 | 0x76 | - | 0xA2 | - |
| | | | 0x1F | 1.00625 | 0x4B | 0.73125 | 0x77 | - | 0xA3 | - |
| | | | 0x20 | 1 | 0x4C | 0.725 | 0x78 | - | 0xA4 | - |
| | | | 0x21 | 0.99375 | 0x4D | 0.71875 | 0x79 | - | 0xA5 | - |
| | | | 0x22 | 0.9875 | 0x4E | 0.7125 | 0x7A | - | 0xA6 | - |
| | | | 0x23 | 0.98125 | 0x4F | 0.70625 | 0x7B | - | 0xA7 | - |
| | | | 0x24 | 0.975 | 0x50 | 0.7 | 0x7C | - | 0xA8 | - |
| | | | 0x25 | 0.96875 | 0x51 | 0.69375 | 0x7D | - | 0xA9 | - |
| | | | 0x26 | 0.9625 | 0x52 | 0.6875 | 0x7E | - | 0xAA | - |
| | | | 0x27 | 0.95625 | 0x53 | 0.68125 | 0x7F | - | 0xAB | - |
| | | | 0x28 | 0.95 | 0x54 | 0.675 | 0x80 | - | 0xAC | - |
| | | | 0x29 | 0.94375 | 0x55 | 0.66875 | 0x81 | - | 0xAD | - |
| | | | 0x2A | 0.9375 | 0x56 | 0.6625 | 0x82 | - | 0xAE | - |
| | | | 0x2B | 0.93125 | 0x57 | 0.65625 | 0x83 | - | 0xAF | - |
| | | | - | | - | | - | | 0xB0 | - |

*Table 7. Register 0x02*

| Register Name | Reserved | Description |
|---|---|---|
| Address | 0x02 | Reserved |

*Table 8. Regulator Output Voltage Setting Mode (0x03)*

| Register Name | OUT3_REG | | DVS Registers for Regulator3 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Address | 0x03 | | Output Voltage setting of OUT3<br>DVS from 0.86V to 1.86V in 7.5mV steps | | | | | | | |
| | R/W | Default | Hex | Voltage [V] | Hex | Voltage [V] | Hex | Voltage [V] | Hex | Voltage [V] |
| VOUT3_SET | R/W | 0x0A | 0x00 | 1.8594 | 0x2C | 1.5294 | 0x58 | 1.1994 | 0x84 | - |
| | | | 0x01 | 1.8519 | 0x2D | 1.5219 | 0x59 | 1.1919 | 0x85 | - |
| | | | 0x02 | 1.8444 | 0x2E | 1.5144 | 0x5A | 1.1844 | 0x86 | - |
| | | | 0x03 | 1.8369 | 0x2F | 1.5069 | 0x5B | 1.1769 | 0x87 | - |
| | | | 0x04 | 1.8294 | 0x30 | 1.4994 | 0x5C | 1.1694 | 0x88 | - |
| | | | 0x05 | 1.8219 | 0x31 | 1.4919 | 0x5D | 1.1619 | 0x89 | - |
| | | | 0x06 | 1.8144 | 0x32 | 1.4844 | 0x5E | 1.1544 | 0x8A | - |
| | | | 0x07 | 1.8069 | 0x33 | 1.4769 | 0x5F | 1.1469 | 0x8B | - |
| | | | 0x08 | 1.7994 | 0x34 | 1.4694 | 0x60 | 1.1394 | 0x8C | - |
| | | | 0x09 | 1.7919 | 0x35 | 1.4619 | 0x61 | 1.1319 | 0x8D | - |
| | | | 0x0A | 1.7844 | 0x36 | 1.4544 | 0x62 | 1.1244 | 0x8E | - |
| | | | 0x0B | 1.7769 | 0x37 | 1.4469 | 0x63 | 1.1169 | 0x8F | - |
| | | | 0x0C | 1.7694 | 0x38 | 1.4394 | 0x64 | 1.1094 | 0x90 | - |
| | | | 0x0D | 1.7619 | 0x39 | 1.4319 | 0x65 | 1.1019 | 0x91 | - |
| | | | 0x0E | 1.7544 | 0x3A | 1.4244 | 0x66 | 1.0944 | 0x92 | - |
| | | | 0x0F | 1.7469 | 0x3B | 1.4169 | 0x67 | 1.0869 | 0x93 | - |
| | | | 0x10 | 1.7394 | 0x3C | 1.4094 | 0x68 | 1.0794 | 0x94 | - |
| | | | 0x11 | 1.7319 | 0x3D | 1.4019 | 0x69 | 1.0719 | 0x95 | - |
| | | | 0x12 | 1.7244 | 0x3E | 1.3944 | 0x6A | 1.0644 | 0x96 | - |
| | | | 0x13 | 1.7169 | 0x3F | 1.3869 | 0x6B | 1.0569 | 0x97 | - |
| | | | 0x14 | 1.7094 | 0x40 | 1.3794 | 0x6C | 1.0494 | 0x98 | - |
| | | | 0x15 | 1.7019 | 0x41 | 1.3719 | 0x6D | 1.0419 | 0x99 | - |
| | | | 0x16 | 1.6944 | 0x42 | 1.3644 | 0x6E | 1.0344 | 0x9A | - |
| | | | 0x17 | 1.6869 | 0x43 | 1.3569 | 0x6F | 1.0269 | 0x9B | - |
| | | | 0x18 | 1.6794 | 0x44 | 1.3494 | 0x70 | 1.0194 | 0x9C | - |
| | | | 0x19 | 1.6719 | 0x45 | 1.3419 | 0x71 | 1.0119 | 0x9D | - |
| | | | 0x1A | 1.6644 | 0x46 | 1.3344 | 0x72 | 1.0044 | 0x9E | - |
| | | | 0x1B | 1.6569 | 0x47 | 1.3269 | 0x73 | 0.9969 | 0x9F | - |
| | | | 0x1C | 1.6494 | 0x48 | 1.3194 | 0x74 | 0.9894 | 0xA0 | - |
| | | | 0x1D | 1.6419 | 0x49 | 1.3119 | 0x75 | 0.9819 | 0xA1 | - |
| | | | 0x1E | 1.6344 | 0x4A | 1.3044 | 0x76 | 0.9744 | 0xA2 | - |
| | | | 0x1F | 1.6269 | 0x4B | 1.2969 | 0x77 | 0.9669 | 0xA3 | - |
| | | | 0x20 | 1.6194 | 0x4C | 1.2894 | 0x78 | 0.9594 | 0xA4 | - |
| | | | 0x21 | 1.6119 | 0x4D | 1.2819 | 0x79 | - | 0xA5 | - |
| | | | 0x22 | 1.6044 | 0x4E | 1.2744 | 0x7A | - | 0xA6 | - |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0x23 | 1.5969 | 0x4F | 1.2669 | 0x7B | - | 0xA7 | - |
| | | | 0x24 | 1.5894 | 0x50 | 1.2594 | 0x7C | - | 0xA8 | - |
| | | | 0x25 | 1.5819 | 0x51 | 1.2519 | 0x7D | - | 0xA9 | - |
| | | | 0x26 | 1.5744 | 0x52 | 1.2444 | 0x7E | - | 0xAA | - |
| | | | 0x27 | 1.5669 | 0x53 | 1.2369 | 0x7F | - | 0xAB | - |
| | | | 0x28 | 1.5594 | 0x54 | 1.2294 | 0x80 | - | 0xAC | - |
| | | | 0x29 | 1.5519 | 0x55 | 1.2219 | 0x81 | - | 0xAD | - |
| | | | 0x2A | 1.5444 | 0x56 | 1.2144 | 0x82 | - | 0xAE | - |
| | | | 0x2B | 1.5369 | 0x57 | 1.2069 | 0x83 | - | 0xAF | - |
| | | | - | | - | | - | | 0xB0 | - |

*Table 9. Regulator Output Voltage Setting Mode (0x04)*

| Register Name | Reserved | Description |
|---|---|---|
| Address | 0x04 | Reserved |

*Table 10. Regulator Output Voltage Setting Mode (0x05)*

| Register Name | OUT5_REG | | DVS Registers for Regulator5 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Address | 0x05 | | Output Voltage setting of OUT5<br>DVS from 1.5V to 2.75V in 12.5mV steps | | | | | | | |
| | R/W | Default | Hex | Voltage [V] | Hex | Voltage [V] | Hex | Voltage [V] | Hex | Voltage [V] |
| VOUT5_SET | R/W | 0x14 | 0x00 | 2.75 | 0x2C | 2.2 | 0x58 | 1.65 | 0x84 | - |
| | | | 0x01 | 2.7375 | 0x2D | 2.1875 | 0x59 | 1.6375 | 0x85 | - |
| | | | 0x02 | 2.725 | 0x2E | 2.175 | 0x5A | 1.625 | 0x86 | - |
| | | | 0x03 | 2.7125 | 0x2F | 2.1625 | 0x5B | 1.6125 | 0x87 | - |
| | | | 0x04 | 2.7 | 0x30 | 2.15 | 0x5C | 1.6 | 0x88 | - |
| | | | 0x05 | 2.6875 | 0x31 | 2.1375 | 0x5D | 1.5875 | 0x89 | - |
| | | | 0x06 | 2.675 | 0x32 | 2.125 | 0x5E | 1.575 | 0x8A | - |
| | | | 0x07 | 2.6625 | 0x33 | 2.1125 | 0x5F | 1.5625 | 0x8B | - |
| | | | 0x08 | 2.65 | 0x34 | 2.1 | 0x60 | 1.55 | 0x8C | - |
| | | | 0x09 | 2.6375 | 0x35 | 2.0875 | 0x61 | 1.5375 | 0x8D | - |
| | | | 0x0A | 2.625 | 0x36 | 2.075 | 0x62 | 1.525 | 0x8E | - |
| | | | 0x0B | 2.6125 | 0x37 | 2.0625 | 0x63 | 1.5125 | 0x8F | - |
| | | | 0x0C | 2.6 | 0x38 | 2.05 | 0x64 | 1.5 | 0x90 | - |
| | | | 0x0D | 2.5875 | 0x39 | 2.0375 | 0x65 | - | 0x91 | - |
| | | | 0x0E | 2.575 | 0x3A | 2.025 | 0x66 | - | 0x92 | - |
| | | | 0x0F | 2.5625 | 0x3B | 2.0125 | 0x67 | - | 0x93 | - |
| | | | 0x10 | 2.55 | 0x3C | 2 | 0x68 | - | 0x94 | - |
| | | | 0x11 | 2.5375 | 0x3D | 1.9875 | 0x69 | - | 0x95 | - |
| | | | 0x12 | 2.525 | 0x3E | 1.975 | 0x6A | - | 0x96 | - |
| | | | 0x13 | 2.5125 | 0x3F | 1.9625 | 0x6B | - | 0x97 | - |
| | | | 0x14 | 2.5 | 0x40 | 1.95 | 0x6C | - | 0x98 | - |
| | | | 0x15 | 2.4875 | 0x41 | 1.9375 | 0x6D | - | 0x99 | - |
| | | | 0x16 | 2.475 | 0x42 | 1.925 | 0x6E | - | 0x9A | - |
| | | | 0x17 | 2.4625 | 0x43 | 1.9125 | 0x6F | - | 0x9B | - |
| | | | 0x18 | 2.45 | 0x44 | 1.9 | 0x70 | - | 0x9C | - |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0x19 | 2.4375 | 0x45 | 1.8875 | 0x71 | - | 0x9D | - |
| | | | 0x1A | 2.425 | 0x46 | 1.875 | 0x72 | - | 0x9E | - |
| | | | 0x1B | 2.4125 | 0x47 | 1.8625 | 0x73 | - | 0x9F | - |
| | | | 0x1C | 2.4 | 0x48 | 1.85 | 0x74 | - | 0xA0 | - |
| | | | 0x1D | 2.3875 | 0x49 | 1.8375 | 0x75 | - | 0xA1 | - |
| | | | 0x1E | 2.375 | 0x4A | 1.825 | 0x76 | - | 0xA2 | - |
| | | | 0x1F | 2.3625 | 0x4B | 1.8125 | 0x77 | - | 0xA3 | - |
| | | | 0x20 | 2.35 | 0x4C | 1.8 | 0x78 | - | 0xA4 | - |
| | | | 0x21 | 2.3375 | 0x4D | 1.7875 | 0x79 | - | 0xA5 | - |
| | | | 0x22 | 2.325 | 0x4E | 1.775 | 0x7A | - | 0xA6 | - |
| | | | 0x23 | 2.3125 | 0x4F | 1.7625 | 0x7B | - | 0xA7 | - |
| | | | 0x24 | 2.3 | 0x50 | 1.75 | 0x7C | - | 0xA8 | - |
| | | | 0x25 | 2.2875 | 0x51 | 1.7375 | 0x7D | - | 0xA9 | - |
| | | | 0x26 | 2.275 | 0x52 | 1.725 | 0x7E | - | 0xAA | - |
| | | | 0x27 | 2.2625 | 0x53 | 1.7125 | 0x7F | - | 0xAB | - |
| | | | 0x28 | 2.25 | 0x54 | 1.7 | 0x80 | - | 0xAC | - |
| | | | 0x29 | 2.2375 | 0x55 | 1.6875 | 0x81 | - | 0xAD | - |
| | | | 0x2A | 2.225 | 0x56 | 1.675 | 0x82 | - | 0xAE | - |
| | | | 0x2B | 2.2125 | 0x57 | 1.6625 | 0x83 | - | 0xAF | - |
| | | | - | | - | | - | | 0xB0 | - |

*Table 11. Register 0x06*

| Register Name | Reserved | Description |
|---|---|---|
| Address | 0x06 | Reserved |

*Table 12. Boost Regulator Output Voltage Setting Mode (0X07)*

| Register Name | OUT6_REG | | DVS Registers for Regulator6 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Address | 0x07 | | Output Voltage setting of OUT6<br>DVS from 8V to 15V in 500mV steps | | | | | | | |
| | R/W | Default | Hex | Voltage [V] | Hex | Voltage [V] | Hex | Voltage [V] | Hex | Voltage [V] |
| VOUT6_SET | R/W | 0x06 | 0x00 | 15 | 0x04 | 13 | 0x08 | 11 | 0x0C | 9 |
| | | | 0x01 | 14.5 | 0x05 | 12.5 | 0x09 | 10.5 | 0x0D | 8.5 |
| | | | 0x02 | 14 | 0x06 | 12 | 0x0A | 10 | 0x0E | 8 |
| | | | 0x03 | 13.5 | 0x07 | 11.5 | 0x0B | 9.5 | 0x0F | - |

### Power Rail Enable/Disable Register (0x08)

This register controls the channels enabled or disabled of each DC/DC regulators. If EN(n) bit transitions from 0 to 1 then the regulator(n) should be enabled with soft-start., it will be low.

*Table 13. Power Channel Enable Register (0x08)*

| Register Name | Enable_REG | | | Enable Register | |
|---|---|---|---|---|---|
| Address | | | | 0x08 | |
| | Bit | R/W | Default | Description | |
| EN1 | 0 | R/W | 1 | Regulator 1 ON/OFF Control bit | |
| | | | | 0 = OFF | 1 = ON |
| EN2 | 1 | R/W | 1 | Regulator 2 ON/OFF Control bit | |
| | | | | 0 = OFF | 1 = ON |
| EN | 2 | R/W | 1 | External EN pin High/Low Control bit | |
| | | | | 0 = Low | 1 = High |
| EN3 | 3 | R/W | 1 | Regulator 3 ON/OFF Control bit | |
| | | | | 0 = OFF | 1 = ON |
| EN4 | 4 | R/W | 1 | Reserved | |
| EN5 | 5 | R/W | 1 | Regulator 5 ON/OFF Control bit | |
| | | | | 0 = OFF | 1 = ON |
| Reserved | 6 | R/W | 1 | Reserved | |
| EN6 | 7 | R/W | 1 | Regulator 6 ON/OFF Control bit | |
| | | | | 0 = OFF | 1 = ON |

### Etc Block Enable/Disable Register (0x09)

This register controls the etc block enabled or disabled.

After power on it will be return to setting register(0x00~0x0C) value.

If load switch(Bit2) bit transitions from 0 to 1 then load switch should be enabled with soft-start.

*Table 14. Etc Block Enable Register (0x09)*

| Register Name | Etc.enable_REG | | | Etc. Enable Register | |
|---|---|---|---|---|---|
| Address | | | | **0x09** | |
| | Bit | R/W | Default | Description | |
| Reserved | 3 | R/W | 0 | reserved | |
| RSTO | 1 | R/W | 1 | RSTO High & Low | |
| | | | | 0 = Low<br>RSTO pin output changes from high to low | 1 = High<br>RSTO pin output does not change and keeps high |
| LSW ON/OFF | 2 | R/W | 1 | Load Switch ON/OFF Control bit | |
| | | | | 0=OFF | 1=ON |
| Reserved | 3 | R/W | 1 | reserved | |
| Reserved | 4 | R/W | 1 | reserved | |
| PG_Enable | 5 | R/W | 1 | PG Comparator enable/disable bit<br>If set this bit from 1 to 0, IC will disable PG monitor function.<br>If this bit it set to 1, PG monitor function is enabled. | |
| | | | | 0 = PG Disable | 1 = PG Enable |
| OVP_Enable | 6 | R/W | 1 | All output channel OVP Function enable/disable bit<br>If set this bit from 1 to 0, All Channel will OVP function is disabled. | |
| | | | | 0 = OVP Disable | 1 = OVP Enable |
| Sensing_Enable | 7 | R/W | 1 | Input Voltage Sensing function enable/disable bit<br>If set this bit from 1 to 0, input voltage monitor function will be disabled. | |
| | | | | 0 = Monitor Disable | 1 = Monitor Enable |

### Auto Discharge Mode Register (0x0A)

This register controls Auto Discharge to discharge the capacitors, so the capacitors located on each output channels of PMIC can be discharged forcedly during system delay time and channel power on delay time.

*Table 15. Auto Discharge Mode Register (0x0A)*

| Register Name | Discharge_REG | | | Auto Discharge Mode | |
|---|---|---|---|---|---|
| Address | | | | 0x0A | |
| | Bit | R/W | Default | Auto Discharge mode | |
| AutoDis_1 | 0 | R/W | 1 | Auto Discharge mode for Channel 1 | |
| | | | | 0 = No Discharge | 1 = Discharge |
| AutoDis_2 | 1 | R/W | 0 | Auto Discharge mode for Channel 2 | |
| | | | | 0 = Discharge | 1 = No Discharge |
| Reserved | 2 | R/W | 0 | Reserved | |
| AutoDis_3 | 3 | R/W | 1 | Auto Discharge mode for Channel 3 | |
| | | | | 0 = No Discharge | 1 = Discharge |
| AutoDis_4 | 4 | R/W | 1 | Auto Discharge mode for Channel 4 | |
| | | | | 0 = No Discharge | 1 = Discharge |
| AutoDis_5 | 5 | R/W | 1 | Auto Discharge mode for Channel 5 | |
| | | | | 0 = No Discharge | 1 = Discharge |
| Reserved | 6 | R/W | 0 | Reserved | |
| AutoDis_6 | 7 | R/W | 0 | Auto Discharge mode for Channel 6 | |
| | | | | 0 = Discharge | 1 = No Discharge |

### Discharge Resistance Select Register (0x0B)

*Table 16. Discharge Resistance Select Register (0x0B)*

| Register Name | Discharge_R_REG | | | Discharge Resistance Select | |
|---|---|---|---|---|---|
| Address | | | | 0x0B | |
| | Bit | R/W | Default | Discharge resistance | |
| Dis_R_1 | 0 | R/W | 0 | Discharge resistance for Channel 1 | |
| | | | | 0 = 10ohm | 1 = 2ohm |
| Dis_R_2 | 1 | R/W | 1 | Discharge resistance for Channel 2 | |
| | | | | 0 = 2ohm | 1 = 10ohm |
| Reserved | 2 | R/W | 1 | Reserved | |
| Dis_R_3 | 3 | R/W | 0 | Discharge resistance for Channel 3 | |
| | | | | 0 = 10ohm | 1 = 2ohm |
| Dis_R_4 | 4 | R/W | 1 | Discharge resistance for Channel 4 | |
| | | | | 0 = 2ohm | 1 = 10ohm |
| Dis_R_5 | 5 | R/W | 1 | Discharge resistance for Channel 5 | |
| | | | | 0 = 2ohm | 1 = 10ohm |
| Reserved | 6 | R/W | 1 | Reserved | |
| Dis_R_6 | 7 | R/W | 1 | Discharge resistance for Channel 6 | |
| | | | | 0 = 300ohm | 1 = 100ohm |

### PWM/PFM Mode Register (0x0C)

This register controls Auto PWM/PFM mode changed to PWM at heavy load and PFM at light load automatically, or Forced PWM mode at whole load.

*Table 17. Auto PWM&PFM Mode / Forced PWM Mode (0x0C)*

| Register Name | PWM&PFM_REG | | | Auto PWM/PFM Mode / Forced PWM Mode | |
|---|---|---|---|---|---|
| Address | | | | 0x0C | |
| | Bit | R/W | Default | Auto PWM&PFM mode / Forced PWM mode | |
| PWM_EN1 | 0 | R/W | 1 | Auto PWM / PFM mode / Forced PWM mode for ch1 | |
| | | | | 0 = Forced PWM | 1 = Auto PWM/PFM |
| PWM_EN2 | 1 | R/W | 1 | Auto PWM / PFM mode / Forced PWM mode for ch2 | |
| | | | | 0 = Forced PWM | 1 = Auto PWM/PFM |
| Reserved | 2 | R/W | 1 | Reserved | |
| PWM_EN3 | 3 | R/W | 1 | Auto PWM / PFM mode / Forced PWM mode for ch3 | |
| | | | | 0 = Forced PWM | 1 = Auto PWM/PFM |
| PWM_EN4 | 4 | R/W | 1 | Reserved | |
| PWM_EN5 | 5 | R/W | 1 | Auto PWM / PFM mode / Forced PWM mode for ch5 | |
| | | | | 0 = Forced PWM | 1 = Auto PWM/PFM |
| Reserved | 6 | R/W | 1 | Reserved | |
| PWM_EN6 | 7 | R/W | 1 | Auto PWM / PFM mode / Forced PWM mode for ch6 | |
| | | | | 0 = Forced PWM | 1 = Auto PWM/PFM |

### PG Monitor Register (0x0D)

PG monitor register is used to monitor the output voltage of each channel. If one of the channels exceeds 108% of regulation voltage or lower than 92% of regulation voltage and last longer than 2us, the related channel bit will be set from 0 to 1.

The fault register will keep in 1 even if the fault condition disappears.

The register bit can be reset by setting of RESET bit from 0 to 1.

*Table 18. PG Monitor Register (0x0D)*

| Register Name | PG monitor REG | | | |
|---|---|---|---|---|
| Address | | | | 0x0D |
| | Bit | R/W | Default | PG monitor |
| PG_CH1 | 1 | R | 0 | If VOUT1>106% OR VOUT1<94% of regulation voltage, this bit will change from 0 to 1. And PG pin will be pulled low. |
| PG_CH2 | 2 | R | 0 | If VOUT2>108% OR VOUT2<92% of regulation voltage, this bit will change from 0 to 1. And PG pin will be pulled low. |
| Reserved | 3 | R | 0 | Reserved |
| PG_CH3 | 4 | R | 0 | If VOUT3>106% OR VOUT3<94% of regulation voltage, this bit will change from 0 to 1. And PG pin will be pulled low. |
| PG_CH4 | 5 | R | 0 | Reserved |
| PG_CH5 | 6 | R | 0 | If VOUT5>106% OR VOUT5<94% of regulation voltage, this bit will change from 0 to 1. And PG pin will be pulled low. |
| Reserved | 7 | R | 0 | Reserved |
| PG_CH6 | 7 | R | 0 | If VOUT6>107% OR VOUT6<93% of regulation voltage, this bit will change from 0 to 1. And PG pin will be pulled low. |

### OVP Monitor Register (0x0E)

OVP monitor register is used to monitor OVP activity of each channel. If one of the channels is detected OVP, then the related channel bit will be set from 0 to 1. Once OVP is triggered, all channels will be turn off and latched, only recycle the input voltage could reset this bit value to 0.

*Table 19. OVP Monitor Register (0x0E)*

| Register Name | OVP monitor REG | | | |
|---|---|---|---|---|
| Address | | | | 0x0E |
| | Bit | R/W | Default | OVP monitor |
| OVP_CH1 | 1 | R | 0 | If Ch1 is OVP triggered, this bit will change from 0 to 1. |
| OVP_CH2 | 2 | R | 0 | If Ch2 is OVP triggered, this bit will change from 0 to 1. |
| Reserved | 3 | R | 0 | Reserved |
| OVP_CH3 | 4 | R | 0 | If Ch3 is OVP triggered, this bit will change from 0 to 1. |
| OVP_CH4 | 5 | R | 0 | Reserved |
| OVP_CH5 | 6 | R | 0 | If Ch5 is OVP triggered, this bit will change from 0 to 1. |
| Reserved | 7 | R | 0 | Reserved |
| OVP_CH6 | 7 | R | 0 | If Ch6 is OVP triggered, this bit will change from 0 to 1. |

### OCP Monitor Register (0x11)

OCP monitor register is used to monitor OCP activity of each channel. If one of the channels is detected OCP, then the related channel bit will be set from 0 to 1. Once OCP is triggered, only recycle the input voltage could reset this bit value to 0.

*Table 20. OCP Monitor Register (0x11)*

| Register Name | OCP monitor REG | | | |
|---|---|---|---|---|
| Address | | | | 0x11 |
| | Bit | R/W | Default | OCP monitor |
| OCP_CH1 | 1 | R | 0 | If Ch1 output is OCP/OLP/SCP triggered, this bit will change from 0 to 1. |
| OCP_CH2 | 2 | R | 0 | If Ch2 output is OCP/OLP/SCP triggered, this bit will change from 0 to 1. |
| Reserved | 3 | R | 0 | Reserved |
| OCP_CH3 | 4 | R | 0 | If Ch3 output is OCP/OLP/SCP triggered, this bit will change from 0 to 1. |
| OCP_CH4 | 5 | R | 0 | If Ch4 output is OCP/OLP/SCP triggered, this bit will change from 0 to 1. |
| OCP_CH5 | 6 | R | 0 | If Ch5 output is OCP/OLP/SCP triggered, this bit will change from 0 to 1. |
| Reserved | 7 | R | 0 | Reserved |
| OCP_CH6 | 7 | R | 0 | If Ch6 output is OCP/OLP/SCP triggered, this bit will change from 0 to 1. |

### Information Register (0x12)

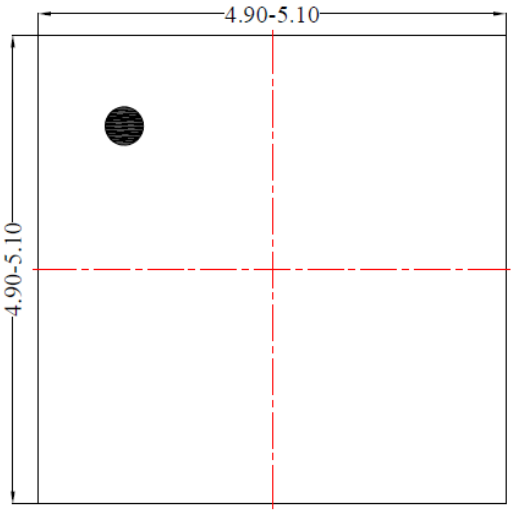
Input monitor register is used to monitor external input voltage.

If input voltage exceeds 4.0V(VSLT=0) and longer than 2us, the Input monitor bit will be set from 0 to 1. Only recycle the input voltage could reset this bit value to 0.

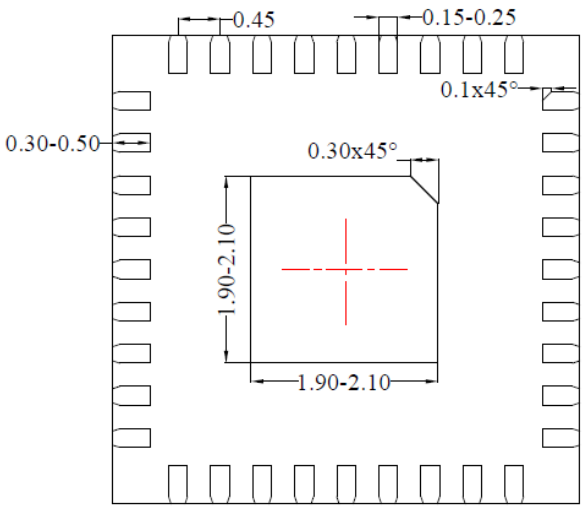
*Table 21. Function Register (0x12)*

| Register Name | Function Register | | | |
|---|---|---|---|---|
| Address | | | | 0x12 |
| | Bit | R/W | Default | Function Register |
| PG_RESET | 0 | R/W | 0 | RESET control bit.<br>If this bit is set from 0 to 1, 0x0D[bit1~bit7] will be reset to 0 if output voltage is not exceeds the PG threshold, and PG pin will be pulled high.<br>This bit value will be cleared to 0 after 1us delay time once write 1. |
| Input Monitor bit | 1 | R | 0 | If Vin<4.0V, this bit will be 0.If Vin>4.0V, this bit will be set to 1 and latched, it won't go back to 0 even Vin is below 4V again. |
| Reserve | 2 | R | 0 | 0 : Vendor for Silergy. |
| OTP write | 3 | R | 1 | 1 : OTP Write OK<br>0 : OTP Write X |
| Reserved | 4 | R | 0 | Reserved |
| Version | 5 | R | 0 | 0: Development, 1: Mass production |
| Reserved | 6 | R/W | 0 | - |
| Reserved | 7 | R/W | 0 | - |

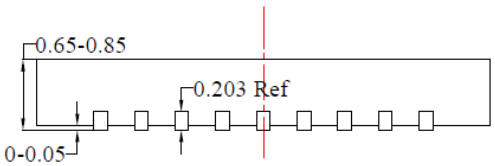
## QFN5x5-36 Package Outline Drawing



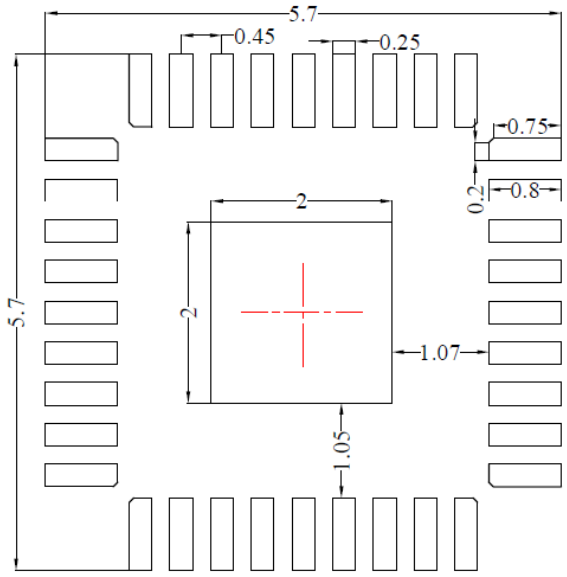

Top View




Bottom View




Front View



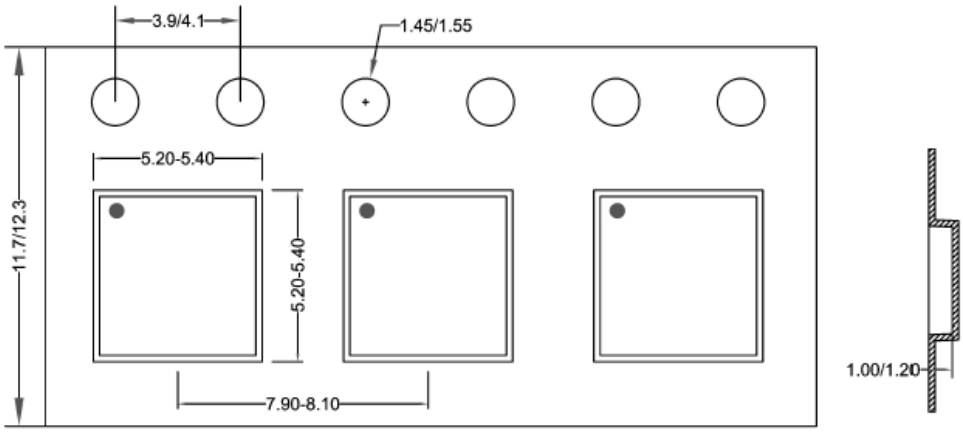

Recommended PCB layout
(Reference only)

***Notes:*** *All dimension in millimeter and exclude mold flash & metal burr.*

# Taping & Reel Specification

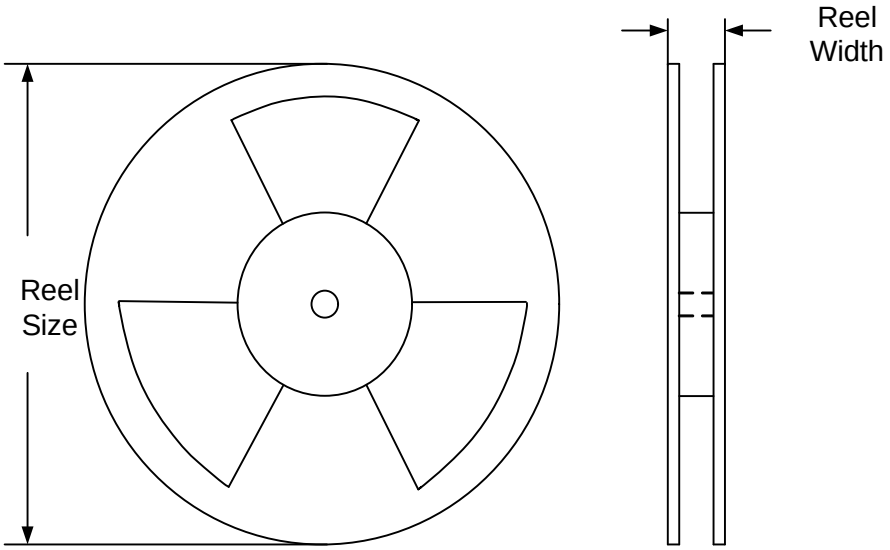
## Taping Orientation

QFN5x5




**Feeding direction** ⟶

## Carrier Tape & Reel Specification for Packages




| Package types | Tape width (mm) | Pocket pitch(mm) | Reel size (Inch) | Reel width(mm) | Trailer length(mm) | Leader length (mm) | Qty per reel |
|---|---|---|---|---|---|---|---|
| QFN5x5 | 12 | 8 | 13" | 12.4 | 400 | 400 | 5000 |

**Others: NA**

## Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

| Date | Revision | Change |
|---|---|---|
| Jan. 10, 2024 | Revision 1.0 | Initial release. |

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