SY70202S

High Efficiency High Integration PMIC for SSD System

General Description

The SY70202S is an SSD PMIC which is composed of 4 synchronous Buck regulators and 2 independent LDOs. The LDO1, and LDO2 can work on load switch mode and the Buck4 works on the LDO mode which are flexible configuration via GPIOx pins.

The configurable options also include output voltage, startup time, system level sequencing, sleep mode, deep sleep mode, and operating mode etc. Each channel provides a wide range voltage to support DVS (Dynamic Voltage Scaling) by I²C interface. The Buck converters are designed to use very small size inductors.

The SY70202S is available in a CSP 2.5 × 2.45 - 36 package.

Key Features

- Wide Input Voltage Range
  - V_{IN} = 2.8V to 3.7V
- Channel 1 Synchronous Buck:
  - 4A Maximum Output Current Capability.
  - 1.6V to 3.0V Programmable, 25mV Step.
- Channel 2 Synchronous Buck:
  - 2A Maximum Output Current Capability.
  - 0.9V to 2.0V Programmable, 10mV Step (or 0.5V to 1.6V Programmable, 10mV Step. Divided by OTP)..
- Channel 3 Synchronous Buck:
  - 4A Maximum Output Current Capability.
  - 0.5V to 1.2V Programmable, 10mV Step.
- Channel 4 Synchronous Buck:
  - 2A Maximum Output Current Capability.
  - 0.9V to 2.0V Programmable, 50mV Step.
  - Buck Mode or LDO Mode Selection.
- Channel 5 LDO1:
  - 0.4A Maximum Output Current Capability.
  - 1.0V to 2.7V Programmable, 50mV step.
  - Bypass Mode or LDO Mode Selection.
- Channel 6 LDO2:
  - 0.4A Maximum Output Current Capability.
  - 1.0V to 2.7V Programmable, 50mV Step.
  - Bypass Mode or LDO Mode Selection.
- I²C Interface up to 3.4MHz
- Auto PWM/PFM or Forced PWM Controlled by I²C Interface
- Output Voltage Level of Each Channel Controlled by I²C Interface
- Reliable Protections:
  - Input/Output Over Voltage Protection(OVP)
  - Short Circuit Protection (SCP)
  - Over Temperature Protection (OTP)
- Compact Package: CSP2.5×2.45-36
- MSL Rating: MSL1

Applications

- Solid State Drives
- Microcontroller

Simplified Typical Applications

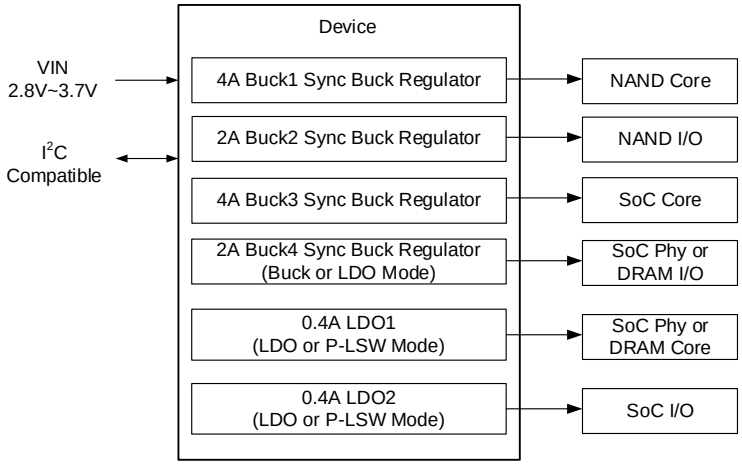
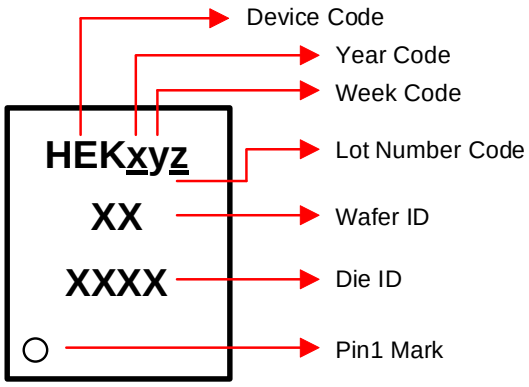


Figure 1. Simplified Application Circuit

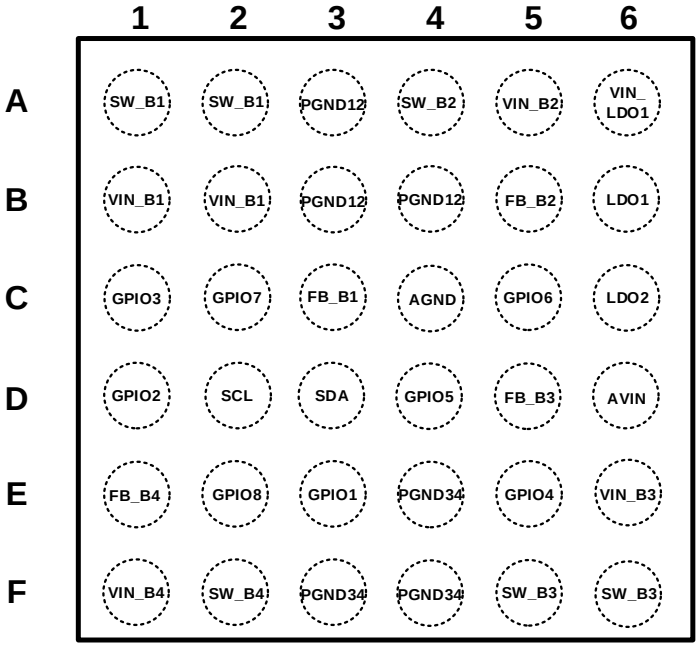
Ordering Information

Ordering Part Number	Package Type
SY70202SVTS	CSP2.5×2.45-36 RoHS-Compliant, Halogen-Free

Marking Diagram



Pinout (top view)



(CSP2.5×2.45-36)

Pin Descriptions

Pin Number	Pin Name	Pin Description
A1, A2	SW_B1	Switch Pin for Buck 1 Regulator.
A3, B3, B4	PGND12	Dedicated Power Ground for Buck1 and Buck2 Regulator.
A4	SW_B2	Switch Pin for Buck 2 Regulator.
A5	VIN_B2	Dedicated VIN power input for Buck 2 Regulator.
A6	VIN_LDO1	Dedicated VIN power input for LDO Regulator.
B1, B2	VIN_B1	Dedicated VIN power input for Buck 1 Regulator.
B5	FB_B2	Feedback for Buck 2 Regulator. Connect to the Buck 2 output capacitor.
B6	LDO1	Output for LDO1 Regulator (Leave unconnected if LDO is not used and disabled).
C1	GPIO3	General purpose input pin.
C2	GPIO7	Configurable general purpose input/open drain output.

C3	FB_B1	Feedback for Buck 1 Regulator. Connect to the Buck 1 output capacitor.
C4	AGND	Analog Ground. Kelvin connects to the other ground pins on the IC.
C5	GPIO6	General purpose input pin.
C6	LDO2	Output for LDO2 Regulator (Leave unconnected if LDO is not used and disabled).
D1	GPIO2	General purpose input pin.
D2	SCL	I^2C Clock Input.
D3	SDA	I^2C Data Input and Output.
D4	GPIO5	Configurable general purpose input/open drain output.
D5	FB_B3	Feedback for Buck 3 Regulator. Connect to the Buck 3 output capacitor.
D6	AVIN	Analog Input supply. This is also the pin that is monitored for VIN OVP.
E1	FB_B4	Feedback for Buck 4 Regulator. Connect to the Buck 4 output capacitor.
E2	GPIO8	General purpose input pin.
E3	GPIO1	General purpose open drain output pin.
E4, F3, F4	PGND34	Dedicated Power Ground for Buck3 and Buck4 Regulators
E5	GPIO4	General purpose input pin.
E6	VIN_B3	Dedicated VIN power input for Buck 3 Regulator.
F1	VIN_B4	Dedicated VIN power input for Buck 4 Regulator.
F2	SW_B4	Switch Pin for Buck 4 Regulator.
F5, F6	SW_B3	Switch Pin for Buck 3 Regulator.

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
All Pins to GND	-0.3	6	V
Junction Temperature Range		150	°C
Lead Temperature (Soldering, 10 sec.)		260	
Storage Temperature Range	-55	150	
ESD Susceptibility			
HBM (Human Body Model)	±2000		V
CDM (Charged Device Model)	±500		
Latch-up	±200		mA

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	24	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	4	
P_D Power Dissipation T_A = 25°C	4.17	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Supply Input Voltage, VIN	2.8	3.7	V
Junction Temperature Range	-40	125	°C
Ambient Temperature Range	-40	85	

Block Diagram

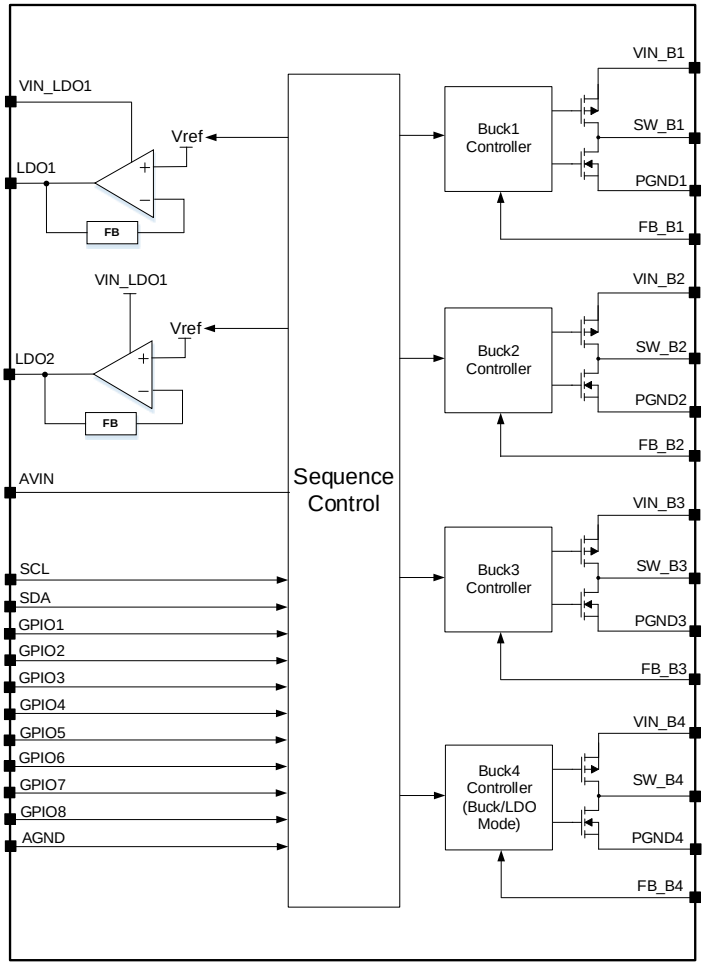


Figure 2. Block Diagram

Electrical Characteristics

(V_{IN}=3.3V, T_A = 25°C, unless otherwise specified. (Note 4))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Digital I/O	GPIOs Output Low (Open drain)	V_{OL}	I_{OL}=1mA	-	-	0.35	V
	GPIOs Input Low (GPIO2/3/4)	V_{IO_low}		-	-	0.35	V
	GPIOs Input Low (GPIO5/6/7/8)	V_{IO_low}		-	-	0.55	V
	GPIOs Input High (GPIO2/3/4/5/6/7/8)	V_{IO_high}		1.19	-	-	V
	GPIOs Input Leakage Current (GPIO 2/4/5/6/7/8)	I_{L_IN}	V_{GPIO}=3.3V Pull-up resistance=0Ω	-5		5	μA
	GPIO3 Input Leakage Current	I_{L_IN}	V_{GPIO}=3.3V Pull-up resistance=50kΩ **(Note 5)**		4.4		μA
			V_{GPIO}=3.3V Pull-up resistance=300kΩ **(Note 5)**		1.2		μA
	GPIOs Output Leakage Current	I_{L_OUT}		-5		5	μA
System Control	Supply Input Voltage	V_{IN}		2.8	-	3.7	V
	UVLO Threshold Rising	$V_{UVLO,Rising}$		2.5	2.6	2.7	V
	UVLO Hysteresis	$V_{UVLO,HYS}$	**(Note 5)**	-	100	-	mV
	Operating Supply Current		All Regulators Disabled **(Note 5)**	-	20	-	μA
	Operating Supply Current		All Regulators Enabled but no load **(Note 5)**	-	120	-	μA
	VIN OV Shutdown Threshold Rising	$V_{IN\_OVP\_R}$	**(Note 5)**	-	3.9	-	V
	VIN OV Shutdown Threshold Falling	$V_{IN\_OVP\_F}$	**(Note 5)**	-	3.6	-	V
	VIN OVP Deglitch Time		**(Note 5)**		5		μs
	Thermal Shutdown	$T_{OTP,Rising}$	Temperature rising **(Note 5)**	-	155	-	°C
	Thermal Shutdown Hysteresis	$T_{OTP,Hys}$	**(Note 5)**	-	15	-	°C
	Startup Delay after initial AVIN	$t_{sys,on}$		-	1.4	1.5	ms
	OV/UV Retry Time		Channel off time **(Note 5)**	-	10	-	ms
nIRQ(SYS WARN)	System Warning (SYSWARN) - Falling Threshold	$V_{SYSWARN}$	**(Note 5)**	-	2.9	-	V
	System Warning (SYSWARN) Accuracy	$V_{SYSWARN,ACC}$		-3.5	-	3.5	%
	System Monitor (SYSWARN) Hysteresis	$V_{SYSWARN,HYS}$	**(Note 5)**	-	50	-	mV
BUCK1	Output Voltage Range	V_{OUT1}	Controllable by I^2C interface 25mV steps.	1.6	-	3.0	V
	Output Voltage Accuracy	ΔV_{OUT1_PWM}	PWM mode operation @ T_A=25°C , V_{OUT}=Default	-1	-	1	%
			PWM mode operation @ T_j=-40°C to 125°C, V_{OUT}=Default	-2	-	2	%

		ΔV_{OUT1_PFM}	PFM mode operation, I_{out}=1mA @ T_j=-40°C to 125°C, V_{OUT}=Default	-2.0	-	2.5	%
	Supply Current, Standby	I_{VIN_B1}	Regulator Only, No Load **(Note 5)**	-	22	-	μA
			Regulator Only, No Load @ Sleep(GPIO8)=Low **(Note 5)**	-	10	-	μA
			Regulator Disable	-	0.1	1	μA
	Switching Frequency	F_{OSC1}	**(Note 5)**	-	2	-	MHz
	High Side FET Current Limit	I_{LIM1_HS}		5.6	-	-	A
	Maximum output DC load current	I_{OUT1}		4	-	-	A
	Internal Soft-Start Time	T_{SS1}	B1_SST=0. 10% to 90% of V_{NOM} **(Note 5)**	-	250	-	μs
			B1_SST=1. 10% to 90% of V_{NOM} **(Note 5)**	-	500	-	μs
	Discharge Resistor	R_{DIS1}	**(Note 5)**	-	4.4	-	Ω
	OVP Threshold	V_{OVP1}		115	120	125	%
	OVP Hysteresis	$V_{OVP1,HYS}$	**(Note 5)**	-	5	-	%
	OVP Deglitch Time	t_{OVP1}	**(Note 5)**	-	10	-	μs
	Short Circuit Protection Threshold	V_{SCP1}	**(Note 5)**	-	30	-	%
	Short Circuit Protection Deglitch Time	t_{SCP1}	**(Note 5)**	-	50	-	μs
BUCK2	Output Voltage Range	V_{OUT2}	Controllable by I^2C interface 10mV steps. (OTP change range)	0.9	-	2.0	V
				0.5		1.6	V
	Output Voltage Accuracy	ΔV_{OUT2_PWM}	PWM mode operation @ T_A=25°C, V_{OUT}=Default	-1	-	1	%
			PWM mode operation @ T_j=-40°C to 125°C, V_{OUT}=Default	-2	-	2	%
		ΔV_{OUT2_PFM}	PFM mode operation, I_{out}=1mA @ T_j=-40°C to 125°C, V_{OUT}=Default	-2.0	-	2.5	%
	Supply Current, Standby	I_{VIN_B2}	Regulator Only, No Load **(Note 5)**	-	22	-	μA
			Regulator Only, No Load @ Sleep(GPIO8)=Low **(Note 5)**	-	10	-	μA
			Regulator Disable	-	0.1	1	μA
	Switching Frequency	F_{OSC2}	**(Note 5)**	-	2	-	MHz
	High Side FET Current Limit	I_{LIM2_HS}		3.6	-	-	A
	Maximum output DC load current	I_{OUT2}		2	-	-	A
	Internal Softstart time	T_{SS2}	B2_SST=0. 10% to 90% of V_{NOM} **(Note 5)**	-	250	-	μs
			B2_SST=1. 10% to 90% of V_{NOM} **(Note 5)**	-	500	-	μs
	Discharge Resistor	R_{DIS2}	**(Note 5)**	-	9.4	-	Ω

	OVP Threshold	V_{OVP2}		115	120	125	%
	OVP Hysteresis	$V_{OVP2,HYS}$	**(Note 5)**	-	5	-	%
	OVP Deglitch Time	t_{OVP2}	**(Note 5)**	-	10	-	µs
	Short Circuit Protection Threshold	V_{SCP2}	**(Note 5)**	-	30	-	%
	Short Circuit Protection Deglitch Time	t_{SCP2}	**(Note 5)**	-	50	-	µs
BUCK3	Output Voltage Range	V_{OUT3}	Controllable by I^2C interface 10mV steps.	0.5	-	1.2	V
	Output Voltage Accuracy	ΔV_{OUT3_PWM}	PWM mode operation @ T_A=25°C, V_{OUT}=Default	-1	-	1	%
			PWM mode operation @ T_j=-40°C to 125°C, V_{OUT}=Default	-2	-	2	%
		ΔV_{OUT3_PFM}	PFM mode operation, I_{out}=1mA @ T_j=-40°C to 125°C, V_{OUT}=Default	-2.0	-	2.5	%
	Supply Current, Standby	I_{VIN_B3}	Regulator Only, No Load **(Note 5)**	-	22	-	µA
			Regulator Only, No Load @ Sleep(GPIO8)=Low **(Note 5)**	-	10	-	µA
			Regulator Disable	-	0.1	1	µA
	Switching Frequency	F_{OSC3}	**(Note 5)**	-	2	-	MHz
	High Side FET Current Limit	I_{LIM3_HS}		5.6	-	-	A
	Maximum output DC load current	I_{OUT3}		4	-	-	A
	Internal Soft-Start Time	T_{SS3}	B3_SST=0. 10% to 90% of V_{NOM} **(Note 5)**	-	250	-	µs
			B3_SST=1. 10% to 90% of V_{NOM} **(Note 5)**	-	500	-	µs
	Discharge Resistor	R_{DIS3}	**(Note 5)**		9.4	-	Ω
	OVP Threshold	V_{OVP3}		115	120	125	%
	OVP Hysteresis	$V_{OVP3,HYS}$	**(Note 5)**	-	5	-	%
	OVP Deglitch Time	t_{OVP3}	**(Note 5)**	-	10	-	µs
	Short Circuit Protection Threshold	V_{SCP3}	**(Note 5)**	-	30	-	%
	Short Circuit Protection Deglitch Time	t_{SCP3}	**(Note 5)**	-	50	-	µs
BUCK4	Output Voltage Range	V_{OUT4}	Controllable by I^2C interface 50mV steps.	0.9	-	2.0	V
	Output Voltage Increase	ΔV_{OUT4}	0x04[6]=0.**(Note 5)**	-	0	-	mV
			0x04[6]=1.**(Note 5)**	-	24	-	mV
	Output Voltage Accuracy	ΔV_{OUT4_PWM}	PWM mode operation @ T_A=25°C, V_{OUT}=Default	-1	-	1	%
			PWM mode operation @ T_j=-40°C to 125°C, V_{OUT}=Default	-2	-	2	%
			PWM mode operation @ T_j=-40°C to 125°C, V_{OUT}=1.95V	-1.5	-	1.5	%
		ΔV_{OUT4_PFM}	PFM mode operation,	-2.0	-	2.5	%

			I_{out}=1mA @ T_j=-40°C to 125°C, V_{OUT}=Default				
	Supply Current, Standby	I_{VIN_B4}	Regulator Only, No Load **(Note 5)**	-	22	-	μA
			Regulator Only, No Load @ Sleep(GPIO8)=Low **(Note 5)**	-	10	-	μA
			Regulator Disable	-	0.1	1	μA
	Switching Frequency	F_{OSC4}	**(Note 5)**	-	2	-	MHz
	High Side FET Current Limit	I_{LIM4_HS}		3.6	-	-	A
	Maximum output DC load current	I_{OUT4}		2	-	-	A
	Internal Soft-Start Time	T_{SS4}	B4_SST=0. 10% to 90% of V_{NOM} **(Note 5)**	-	250	-	μs
			B4_SST=1. 10% to 90% of V_{NOM} **(Note 5)**	-	500	-	μs
	Discharge Resistor	R_{DIS4}	**(Note 5)**	-	9.4	-	Ω
	OVP Threshold	V_{OVP4}		115	120	125	%
	OVP Hysteresis	$V_{OVP4,HYS}$	**(Note 5)**	-	5	-	%
	OVP Deglitch Time	t_{OVP4}	**(Note 5)**	-	10	-	μs
	Short Circuit Protection Threshold	V_{SCP4}	**(Note 5)**	-	30	-	%
	Short Circuit Protection Deglitch Time	t_{SCP4}	**(Note 5)**	-	50	-	μs
BUCK4@ LDO Mode	Output Voltage Range	$V_{OUT\_B4\_LDO}$	Controllable by I^2C interface, 50mV steps.	0.9	-	2.0	V
	Output Current	$I_{OUT\_B4\_LDO}$	V_{IN_B4}=2.8V to 3.7V,	0.4	-	-	A
	Output Voltage Accuracy	$\Delta V_{OUT\_B4\_LDO}$	T_A=25°C, V_{IN_B4}-$V_{OUT\_B4\_LDO}$ > 0.4V	-1	-	1	%
			T_j=-40°C to 125°C, V_{IN_B4}-$V_{OUT\_B4\_LDO}$ > 0.4V	-2	-	2	%
	Supply Current	I_{VIN_B4}	Regulator Enable, No Load **(Note 5)**	-	10	-	μA
			Regulator Disable	-	0	1	μA
	Internal Soft-Start Time	$T_{SS\_B4\_LDO}$	B4_SST=0. 10% to 90% of V_{NOM} **(Note 5)**	-	250	-	μs
			B4_SST=1. 10% to 90% of V_{NOM} **(Note 5)**	-	500	-	μs
	OVP Threshold	$V_{OVP\_B4\_LDO}$		115	120	125	%
	OVP Hysteresis	V_{OVP_HYS}	**(Note 5)**	-	5	-	%
	OVP Deglitch Time	$t_{OVP\_B4\_LDO}$	**(Note 5)**	-	10	-	μs
	Dropout Voltage	$V_{DV\_B4\_LDO}$	I_{LDO1} = 150mA, V_{IN_B4} > 2.8V,	-	-	200	mV
			I_{LDO1} = 300mA, V_{IN_B4} > 2.8V	-	-	400	mV
	Discharge Resistor	$R_{DIS\_B4\_LDO}$	**(Note 5)**	-	9.4	-	Ω
	Current Limit	$I_{LIM\_B4\_LDO}$		400	500	600	mA
	Current Shutdown Deglitch Time	$t_{LIM\_B4\_LDO}$	**(Note 5)**	-	200	-	μs
	Short Circuit Protection Threshold	$V_{SCP\_B4\_LDO}$	**(Note 5)**	-	60	-	%
	Short Circuit Protection Deglitch Time	$t_{SCP\_B4\_LDO}$	**(Note 5)**	-	50	-	μs

LDO1	LDO1 Input Voltage Range	V_{IN_LDO1}	LDO Mode	2.8	-	3.7	V
	LDO1 Output Voltage Range	V_{OUT_LDO1}	Controllable by I²C interface, 50mV steps.	1.0	-	2.7	V
	Output Current	I_{OUT_LDO1}	V_{IN_LDO1}=2.8V to 3.7V,	0.4	-	-	A
	Output Voltage Accuracy	ΔV_{OUT_LDO1}	T_A=25°C, V_{OUT}=Default V_{IN_LDO1}-V_{OUT_LDO1} > 0.4V	-1	-	1	%
			T_j=-40°C to 125°C, V_{OUT}=Default V_{IN_LDO1}-V_{OUT_LDO1} > 0.4V	-2	-	2	%
	Supply Current	I_{VIN_LDO1}	Regulator Enable, No Load **(Note 5)**	-	10	-	μA
			Regulator Disable	-	0	1	μA
	Internal Soft-Start Time	T_{SS_LDO1}	LDO1_SST=0. 10% to 90% of V_{NOM} **(Note 5)**	-	200	-	μs
			LDO1_SST=1. 10% to 90% of V_{NOM} **(Note 5)**	-	360	-	μs
	OVP Threshold	V_{OVP_LDO1}		115	120	125	%
	OVP Hysteresis	$V_{OVP\_LDO1,HYS}$		-	5	-	%
	OVP Deglitch Time	t_{OVP_LDO1}		-	10	-	μs
	Dropout Voltage	V_{DV_LDO1}	I_{LDO1} = 400mA, V_{IN_LDO1} > 2.8V,	-	-	400	mV
	Discharge Resistor	R_{DIS_LDO1}	**(Note 5)**	-	10	-	Ω
	Current Limit	I_{LIM_LDO1}		400	500	600-	mA
	Current Shutdown Deglitch Time	t_{LIM_LDO1}	**(Note 5)**	-	200	-	μs
	Short Circuit Protection Threshold	V_{SCP_LDO1}	**(Note 5)**	-	60	-	%
	Short Circuit Protection Deglitch Time	t_{SCP_LDO1}	**(Note 5)**	-	50	-	μs
LDO1 @ Load Switch	LDO1 Input Voltage Range	V_{IN_LDO1}	PLSW Mode	2.8	-	3.7	V
	Supply Current	I_{VIN_LDO1}	PLSW Mode, **(Note 5)**	-	12	-	μA
			Load Switch Disabled	-	0	1	μA
	Internal Soft-Start Time	T_{SS_LDO1}	10% to 90% of V_{NOM} **(Note 5)**	-	200	-	μs
	Load Switch Current Limit	I_{LIM_HS}	PLSW Mode	400	500	600	mA
	Load Switch Current Shutdown Deglitch Time	t_{LIM_HS}	**(Note 5)**	-	200	-	μs
	Load Switch Current Shutdown Off-time		**(Note 5)**	-	10	-	ms
	Short Circuit Protection Threshold	$V_{SCP,LDO1}$	**(Note 5)**	-	60	-	%
	Short Circuit Protection Deglitch Time	$t_{SCP,LDO1}$	**(Note 5)**	-	50	-	μs
LDO2	LDO2 Input Voltage Range	V_{IN_LDO1}	LDO Mode	2.8	-	3.7	V
	LDO2 Output Voltage Range	V_{OUT_LDO2}	Controllable by I²C interface, 50mV steps.	1.0	-	2.7	V
	Output Current	I_{OUT_LDO2}	V_{IN_LDO1}=2.8V to 3.7V,	0.4	-	-	A
	Output Voltage Accuracy	ΔV_{OUT_LDO2}	T_A=25°C, V_{OUT}=Default V_{IN_LDO1}-V_{OUT_LDO2} > 0.4V	-1	-	1	%
			T_j=-40°C to 125°C, V_{OUT}=Default V_{IN_LDO1}-V_{OUT_LDO2} > 0.4V	-2	-	2	%
	Supply Current	I_{VIN_LDO2}	Regulator Enable, No Load **(Note 5)**	-	10	-	μA

			Regulator Disable	-	0	1	μA
	Internal Soft-Start Time	T_{SS_LDO2}	LDO2_SST=0. 10% to 90% of V_{NOM} **(Note 5)**	-	200	-	μs
			LDO2_SST=1. 10% to 90% of V_{NOM} **(Note 5)**	-	360	-	μs
	OVP Threshold	V_{OVP_LDO2}		115	120	125	%
	OVP Hysteresis	$V_{OVP\_LDO2,HYS}$	**(Note 5)**	-	5	-	%
	OVP Deglitch Time	t_{OVP_LDO2}	**(Note 5)**	-	10	-	μs
	Dropout Voltage	V_{DV_LDO2}	I_{LDO2} = 400mA, V_{IN_LDO1} > 2.8V	-	-	400	mV
	Discharge Resistor	R_{DIS_LDO2}	**(Note 5)**	-	10	-	Ω
	Current Limit	I_{LIM_LDO2}		400	500	600	mA
	Current Shutdown Deglitch Time	t_{LIM_LDO2}	**(Note 5)**	-	200	-	μs
	Short Circuit Protection Threshold	V_{SCP_LDO2}	**(Note 5)**	-	60	-	%
	Short Circuit Protection Deglitch Time	t_{SCP_LDO2}	**(Note 5)**	-	50	-	μs
LDO2@ Load Switch	LDO2 Input Voltage Range	V_{IN_LDO1}	PLSW Mode	2.8	-	3.7	V
	Supply Current	I_{VIN_LDO1}	PLSW Mode, **(Note 5)**	-	12	-	μA
			Load Switch Disabled	-	0	1	μA
	Internal Soft-Start Time	T_{SS_LDO2}	10% to 90% of V_{NOM} **(Note 5)**	-	200	-	μs
	Load Switch Current Limit	I_{LIM_HS}		400	500	600	mA
	Load Switch Current Shutdown Deglitch Time	t_{LIM_HS}	**(Note 5)**	-	200	-	μs
	Load Switch Current Shutdown Off-time		**(Note 5)**	-	10	-	ms
	Short Circuit Protection Threshold	$V_{SCP,LDO2}$	**(Note 5)**	-	60	-	%
	Short Circuit Protection Deglitch Time	$t_{SCP,LDO2}$	**(Note 5)**	-	50	-	μs

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on Silergy EVB.

Note 3: The device is not guaranteed to function outside its operating conditions.

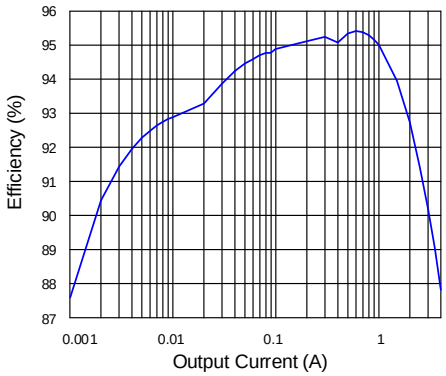
Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

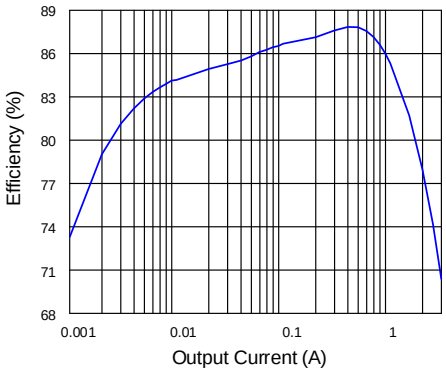
Typical Performance Characteristics

(T_A=25°C)

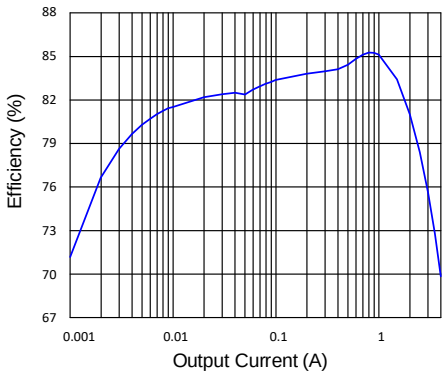
Efficiency vs Output Current
(V_{IN}=3.3V, Buck1=2.5V, L=0.47μH/DFE201612E-R47M=P2)



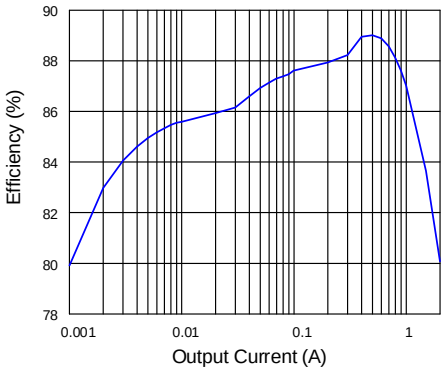
Efficiency vs Output Current
(V_{IN}=3.3V, Buck2=0.91V, L=0.47μH/DFE201612E-R47M=P2)



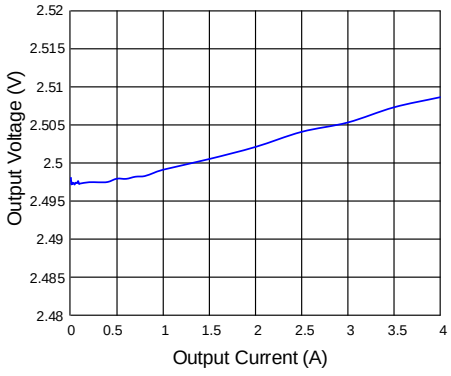
Efficiency vs Output Current
(V_{IN}=3.3V, Buck3=0.78V, L=0.47μH/DFE201612E-R47M=P2)



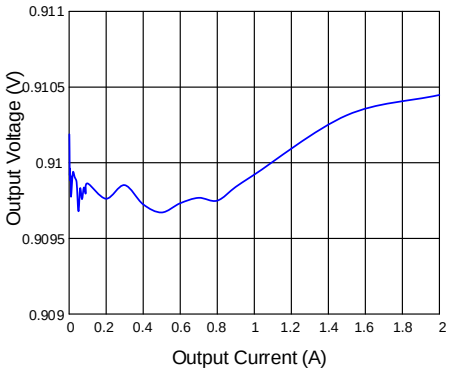
Efficiency vs Output Current
(V_{IN}=3.3V, Buck4=1.2V, L=0.47μH/DFE201612E-R47M=P2)



Output Voltage vs Load Current
(V_{IN}=3.3V, Buck1=2.5V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0~4A)

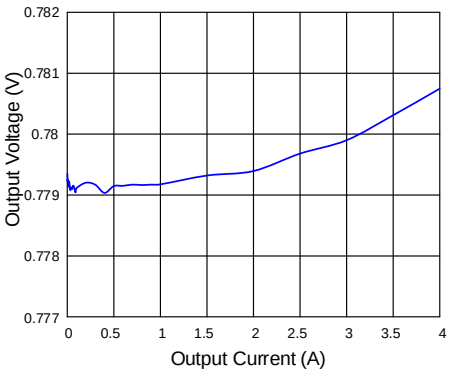


Output Voltage vs Load Current
(V_{IN}=3.3V, Buck2=0.91V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0~2A)



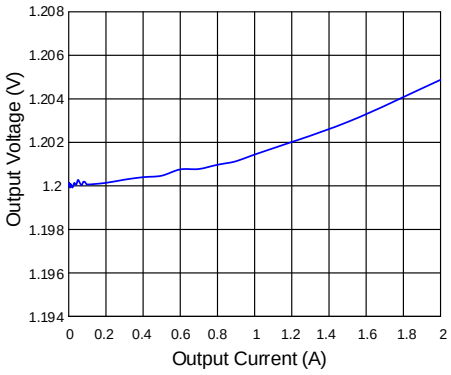
Output Voltage vs Load Current

(V_{IN}=3.3V, Buck3=0.78V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0~4A)



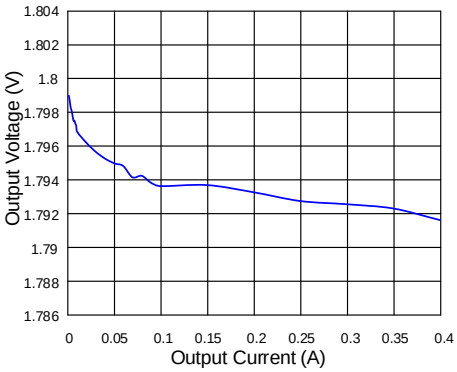
Output Voltage vs Load Current

(V_{IN}=3.3V, Buck4=1.2V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0~2A)



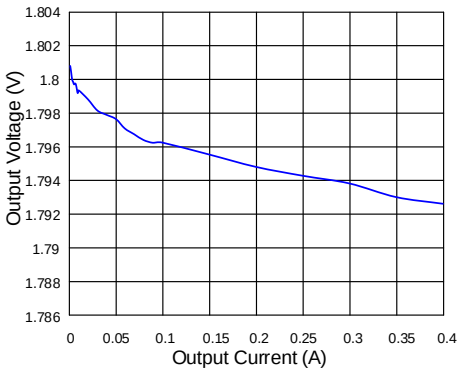
Output Voltage vs Load Current

(V_{IN}=3.3V, LDO1=1.8V, C_{OUT}=1μF, I_{OUT}=0~0.4A)



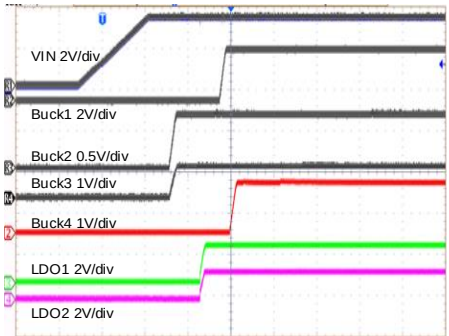
Output Voltage vs Load Current

(V_{IN}=3.3V, LDO2=1.8V, C_{OUT}=1μF, I_{OUT}=0~0.4A)



Power On Sequence

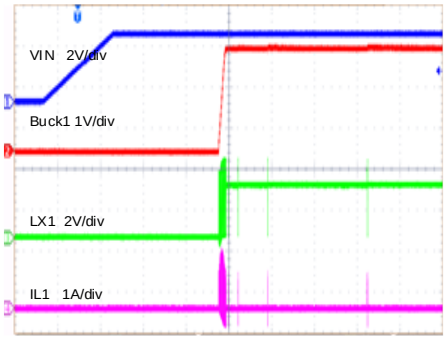
(V_{IN}=3.3V, V_{OUT1}=2.5V, V_{OUT2}=0.91V, V_{OUT3}=0.78V, V_{OUT4}=1.2V, LDO1=1.8V, LDO2=1.8V)



Time (2ms/div)

Buck1 Power On

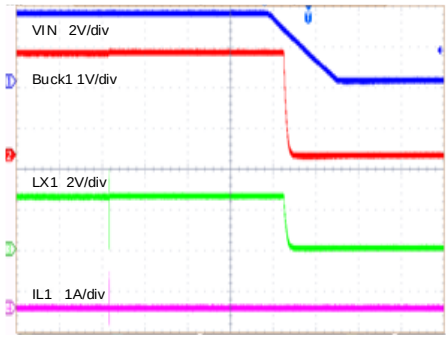
(V_{IN}=3.3V, V_{OUT1}=2.5V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A)



Time (2ms/div)

Buck1 Power Off

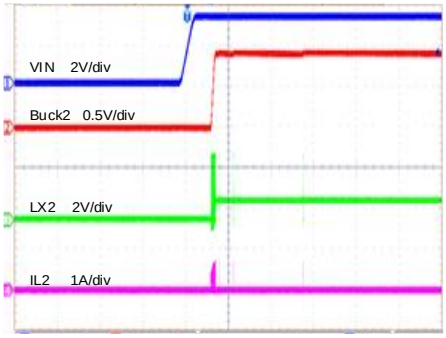
(V_{IN}=3.3V, V_{OUT1}=2.5V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A)



Time (4ms/div)

Buck2 Power On

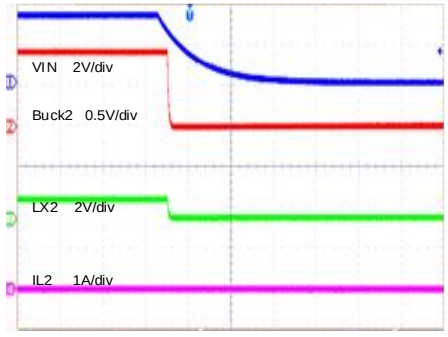
(V_{IN}=3.3V, V_{OUT2}=0.91V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A)



Time (4ms/div)

Buck2 Power Off

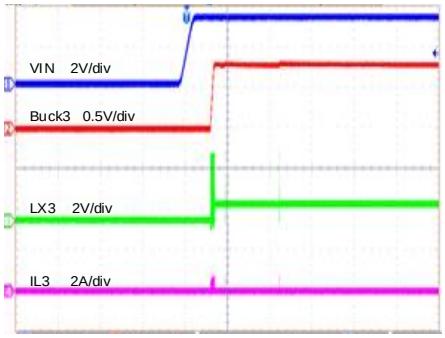
(V_{IN}=3.3V, V_{OUT2}=0.91V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A)



Time (4ms/div)

Buck3 Power On

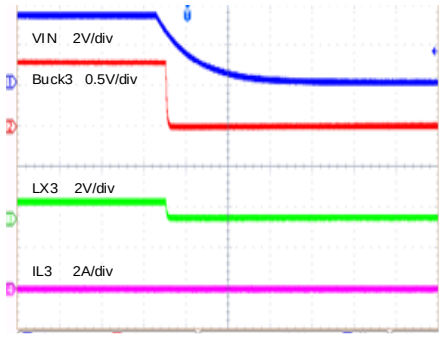
(V_{IN}=3.3V, V_{OUT3}=0.78V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A)



Time (4ms/div)

Buck3 Power Off

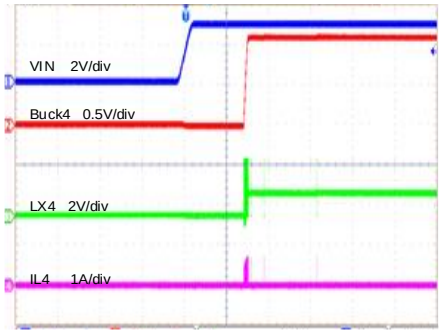
(V_{IN}=3.3V, V_{OUT3}=0.78V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A)



Time (4ms/div)

Buck4 Power On

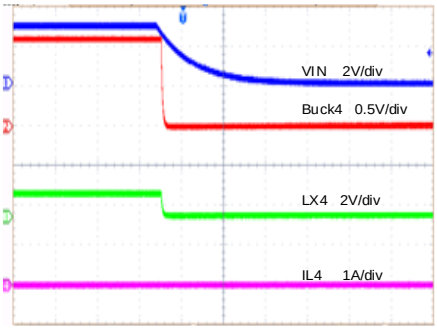
(V_{IN}=3.3V, V_{OUT4}=1.1V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A)



Time (4ms/div)

Buck4 Power Off

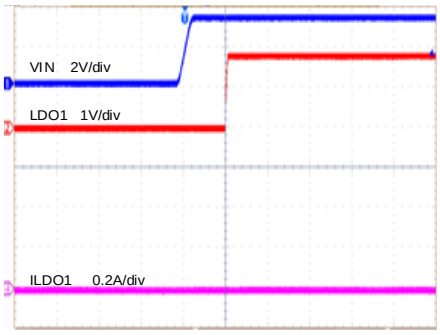
(V_{IN}=3.3V, V_{OUT4}=1.1V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A)



Time (4ms/div)

LDO1 Power On

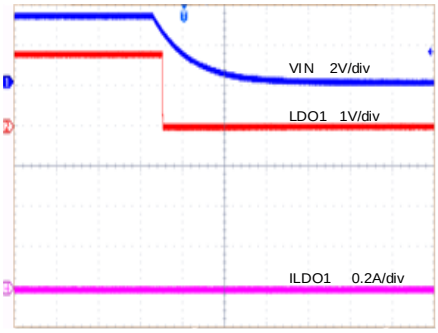
(V_{IN}=3.3V, V_{OUT4}=1.8V, C_{OUT}=1μF, I_{OUT}=0A)



Time (4ms/div)

LDO1 Power Off

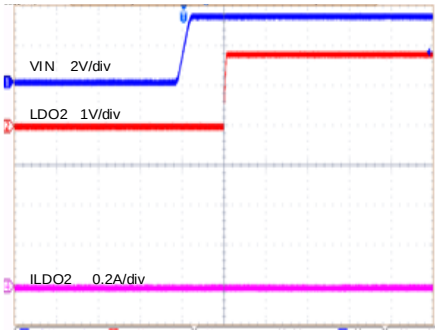
(V_{IN}=3.3V, V_{OUT4}=1.8V, C_{OUT}=1μF, I_{OUT}=0A)



Time (4ms/div)

LDO2 Power On

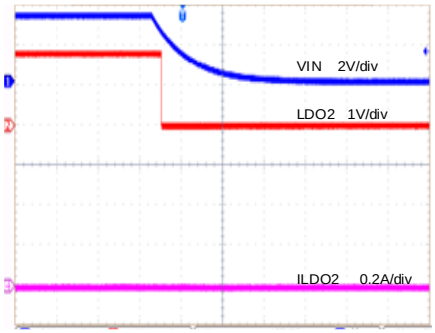
(V_{IN}=3.3V, V_{OUT4}=1.8V, C_{OUT}=1μF, I_{OUT}=0A)



Time (4ms/div)

LDO2 Power Off

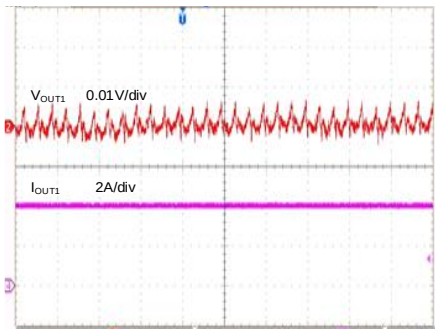
(V_{IN}=3.3V, V_{OUT4}=1.8V, C_{OUT}=1μF, I_{OUT}=0A)



Time (4ms/div)

Buck1 Waveforms

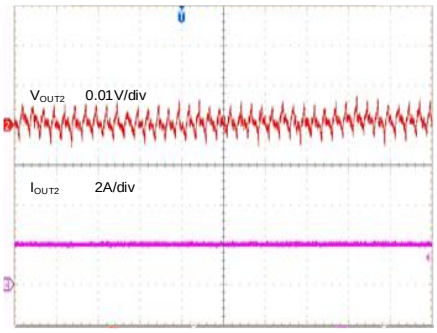
(FCCM Mode, V_{IN}=3.3V, V_{OUT1}=2.5V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=4A)



Time (1μs/div)

Buck2 Waveforms

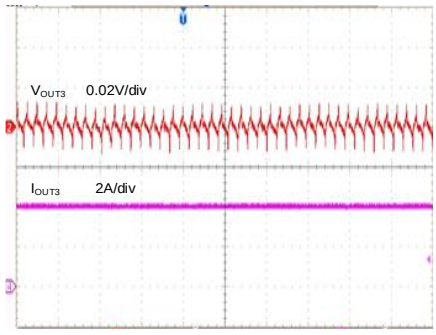
(FCCM Mode, V_{IN}=3.3V, V_{OUT2}=0.91V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=2A)



Time (1μs/div)

Buck3 Waveforms

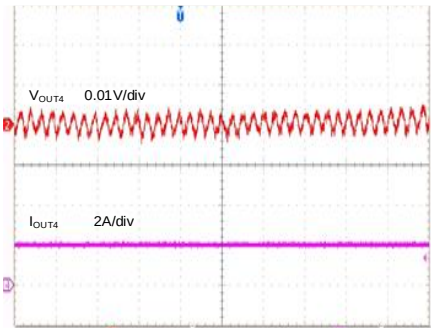
(FCCM Mode, V_{IN}=3.3V, V_{OUT3}=0.78V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=4A)



Time (1μs/div)

Buck4 Waveforms

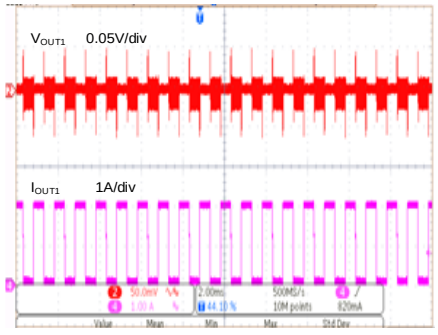
(FCCM Mode, V_{IN}=3.3V, V_{OUT4}=1.2V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=2A)



Time (1μs/div)

Buck1 Load Transient

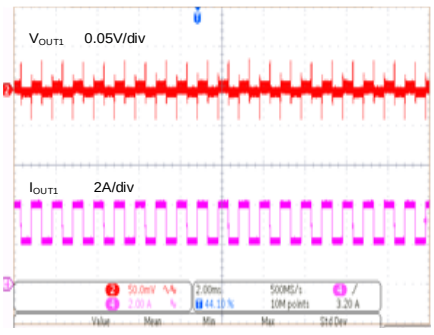
(V_{IN}=3.3V, V_{OUT1}=2.5V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0.05A~2A(0.2A/μs))



Time (2ms/div)

Buck1 Load Transient

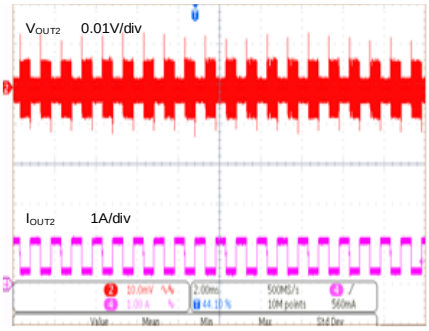
(V_{IN}=3.3V, V_{OUT1}=2.5V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=2A~4A(0.2A/μs))



Time (2ms/div)

Buck2 Load Transient

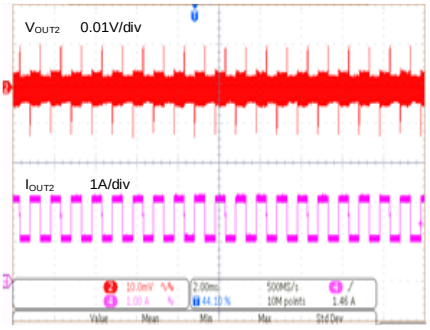
(V_{IN}=3.3V, V_{OUT2}=0.91V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0.05A~1A(0.2A/μs))



Time (2ms/div)

Buck2 Load Transient

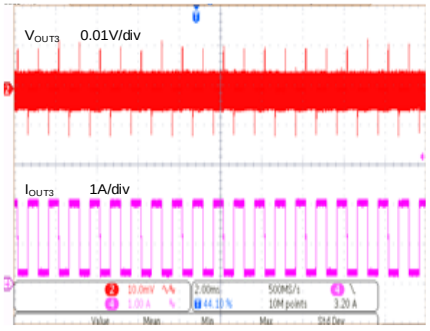
(V_{IN}=3.3V, V_{OUT2}=0.91V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=1A~2A(0.2A/μs))



Time (2ms/div)

Buck3 Load Transient

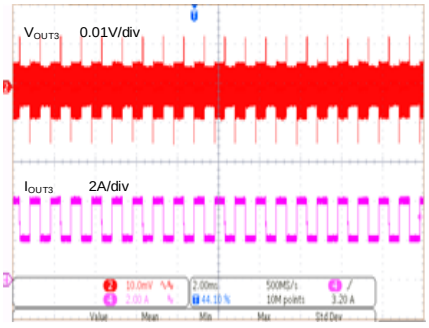
(V_{IN}=3.3V, V_{OUT3}=0.78V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0.05A~2A(0.2A/μs))



Time (2ms/div)

Buck3 Load Transient

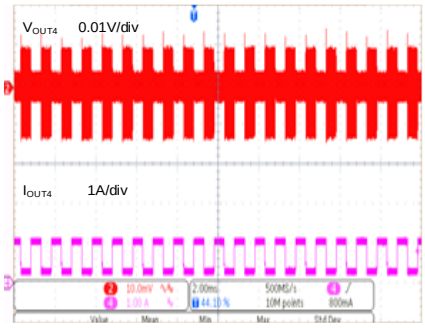
(V_{IN}=3.3V, V_{OUT3}=0.78V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=2A~4A(0.2A/μs))



Time (2ms/div)

Buck4 Load Transient

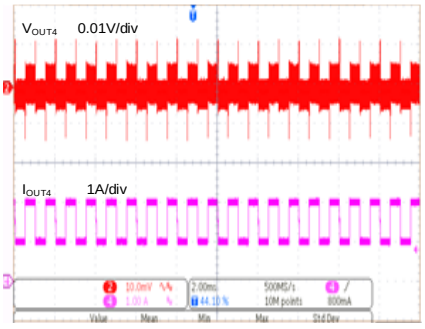
(V_{IN}=3.3V, V_{OUT4}=1.2V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0.05A~1A(0.2A/μs))



Time (2ms/div)

Buck4 Load Transient

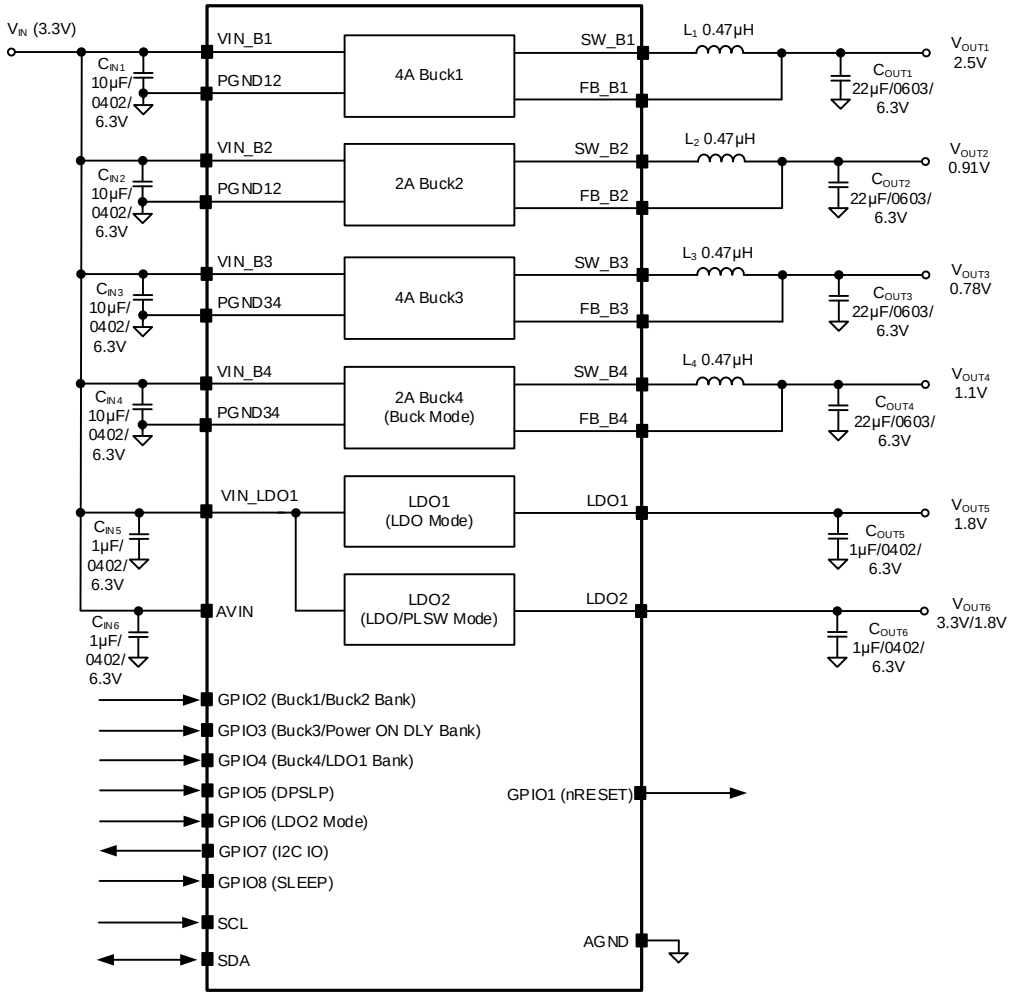
(V_{IN}=3.3V, V_{OUT4}=1.2V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=1A~2A(0.2A/μs))



Time (2ms/div)

Typical Application

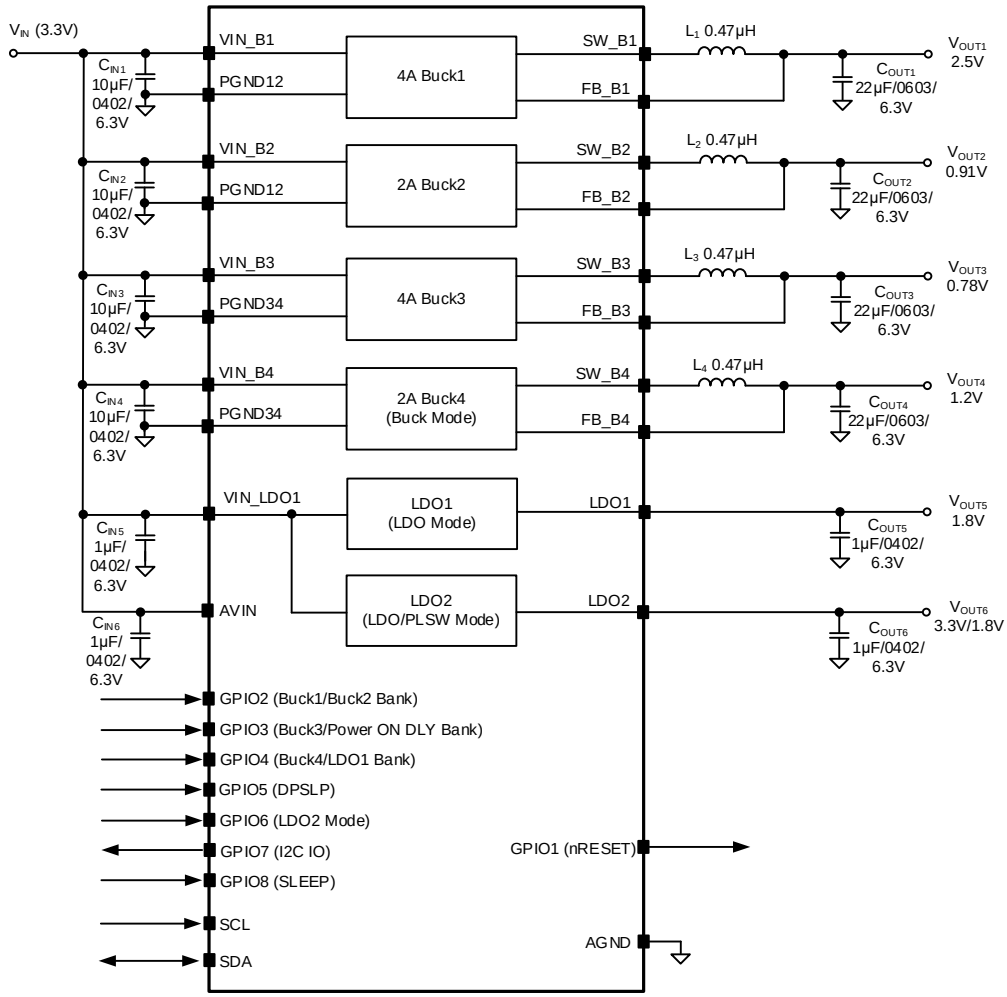
GPIO2=Floating, GPIO3=High, GPIO4=High.



Note: Buck1 I_{OUT} > 2.5A, C_{OUT}=22uF/0603/6.3V x2.

(a)

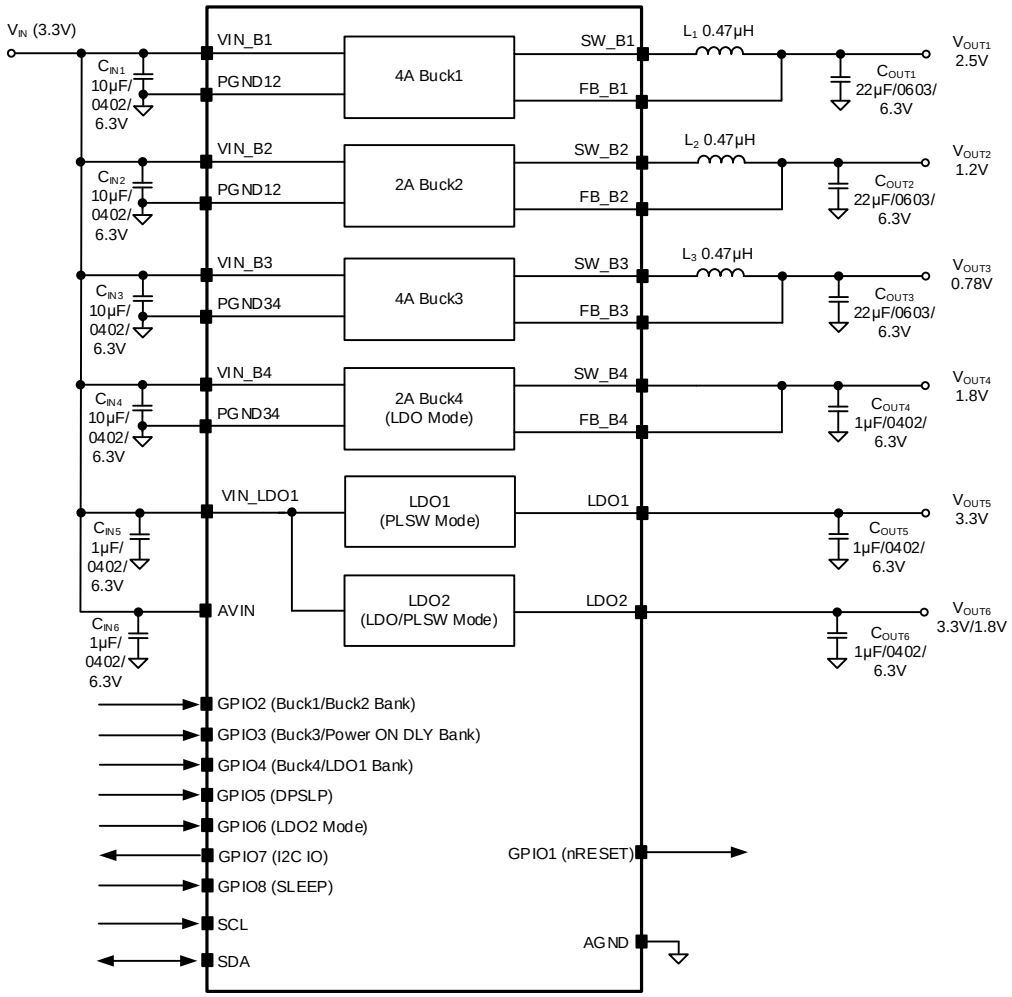
GPIO2=Floating, GPIO3=Floating, GPIO4=Floating.



Note: Buck1 I_{OUT} > 2.5A, C_{OUT}=22uF/0603/6.3V x2.

(b)

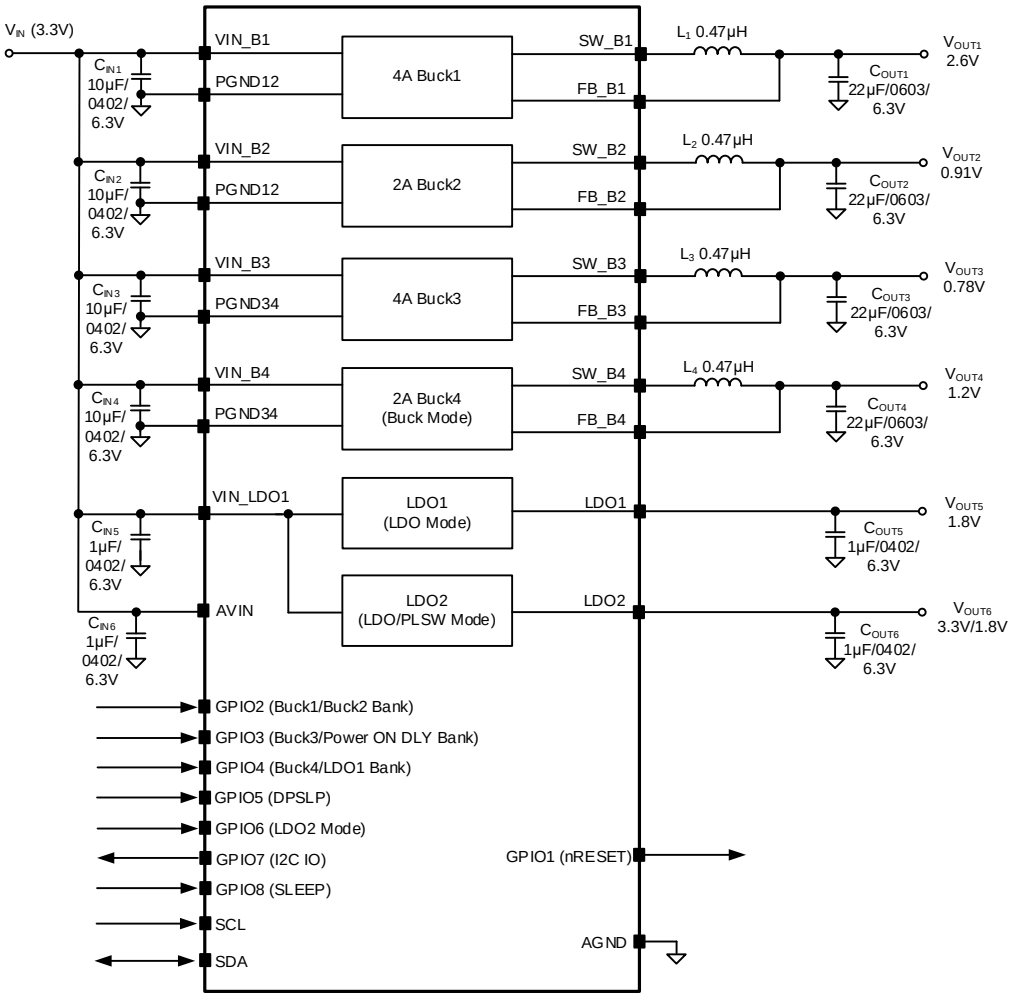
GPIO2=Floating, GPIO3=Low, GPIO4=Low.



Note: Buck1 I_{OUT} > 2.5A, C_{OUT}=22uF/0603/6.3V x2.

(c)

GPIO2=High, GPIO3=Floating, GPIO4=Floating.



Note: Buck1 I_{OUT} > 2.5A, C_{OUT}=22uF/0603/6.3V x2.

(d)

Figure 3. Application Circuit for (a) Application A, (b) Application B, (c) Application C, (d) Application D

Power On/Off Sequence

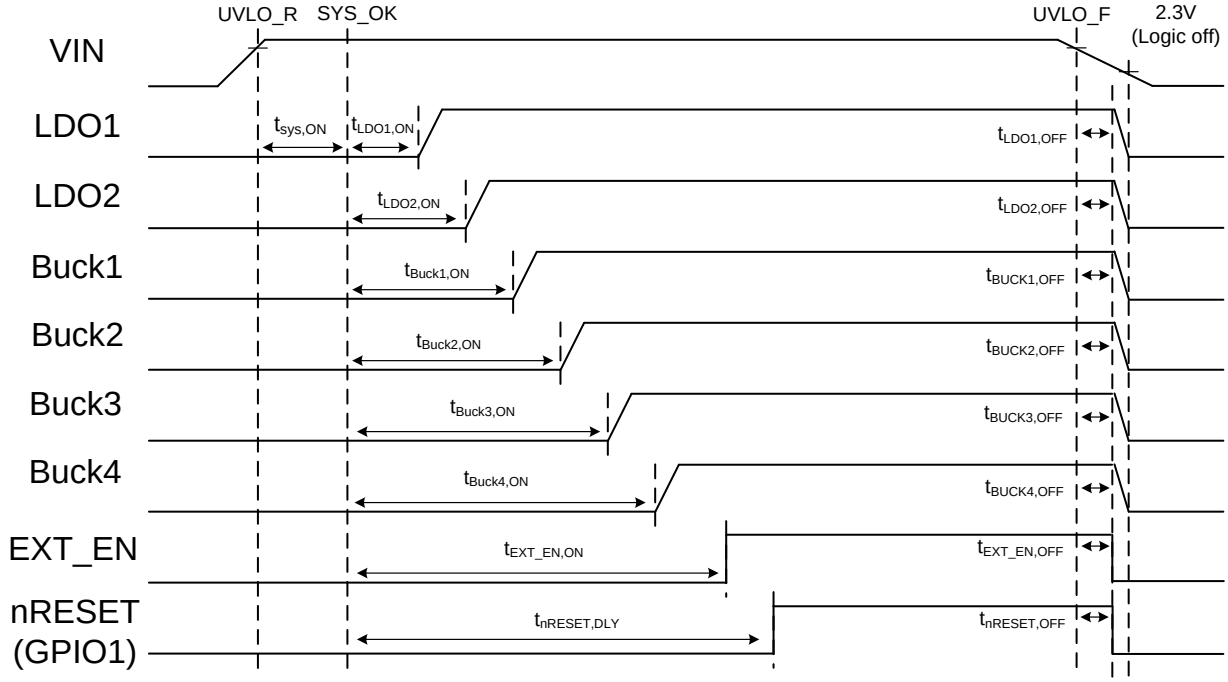


Figure 4. Power On/Off Sequence

- Power-on delay time:

$t_{LDO1,ON}$/ $t_{LDO2,ON}$/ $t_{Buck1,ON}$/ $t_{Buck2,ON}$/ $t_{Buck3,ON}$/$t_{Buck4,ON}$/$t_{EXT\_EN,ON}$ =0~7.5ms, 0.5ms/step.

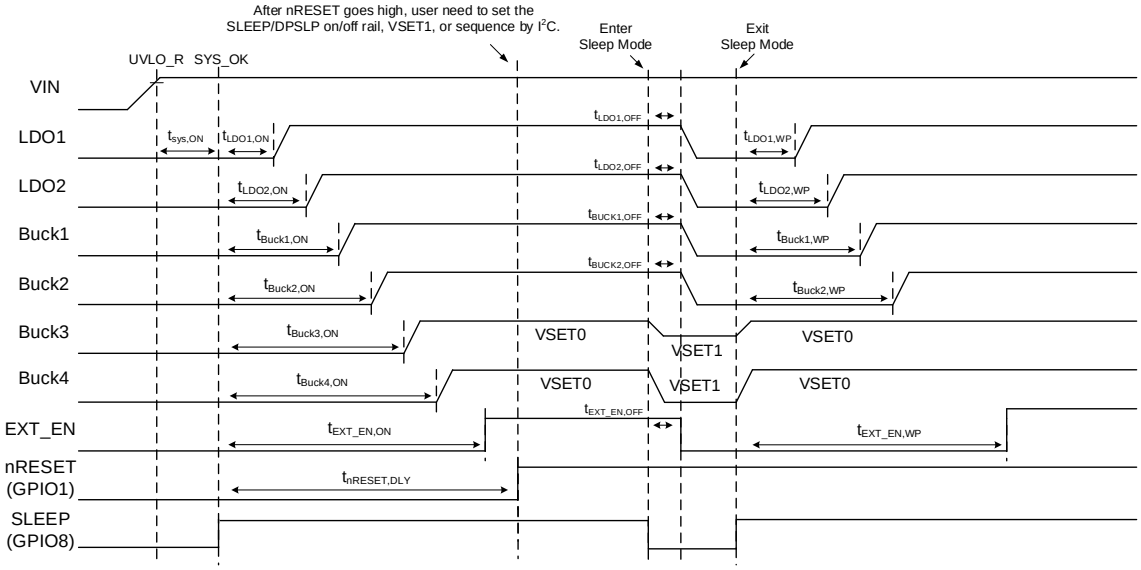
- Power-off delay time:

$t_{LDO1,OFF}$/ $t_{LDO2,OFF}$/ $t_{Buck1,OFF}$/ $t_{Buck2,OFF}$/ $t_{Buck3,OFF}$/$t_{Buck4,OFF}$/$t_{EXT\_EN,OFF}$/$t_{nRESET,OFF}$=0ms, 0.25ms, 0.5ms, or 1ms.

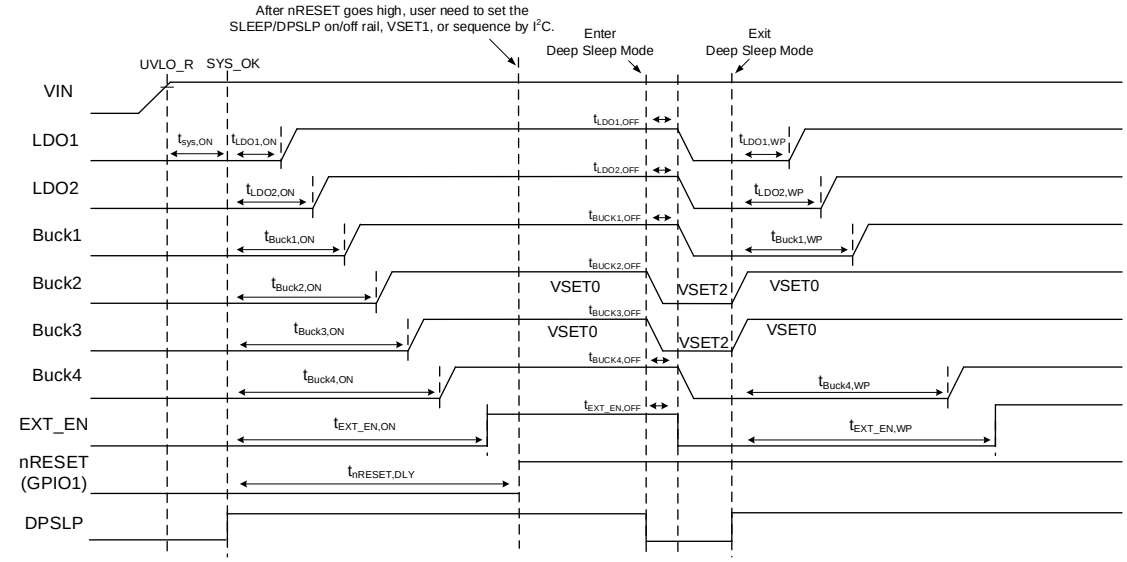
- nRESET delay time:

$t_{nRESET,DLY}$ =0.5ms, 1ms, 2ms, 4ms, 8ms, or 16ms.

SLEEP and DPSLE Sequence



(a)



(b)

Figure 5. Power on/Off Sequence
(a) Enter/Exist Sleep Mode and (b) Enter/Exist Deep Sleep Mode

- Wake up delay time:

$t_{LDO1,WP}$/ $t_{LDO2,WP}$/ $t_{Buck1,WP}$/ $t_{Buck2,WP}$/ $t_{Buck3,WP}$/$t_{Buck4,WP}$/$t_{EXT\_EN,WP}$ =0~1.5ms, 0.5ms/step.

Detailed Description

Overview

	Output Program Range	Output Program Step	Mode	I_{OUT} MAX	HS Current Limit	Discharge Resistor	Soft Start Time
BUCK1	1.6-3.0V	25mV	Buck	4.0A	5.6A	4.4Ω	250/500μs
BUCK2 RANG1	0.9-2.0V	10mV	Buck	2.0A	3.6A	9.4Ω	250/500μs
BUCK2 RANG2	0.5-1.6V	10mV	Buck	2.0A	3.6A	9.4Ω	250/500μs
BUCK3	0.5-1.2V	10mV	Buck	4.0A	5.6A	9.4Ω	250/500μs
BUCK4	0.9-2.0V	50mV	Buck or LDO	2.0A	3.6A	9.4Ω	250/500μs
LDO1	1.0-2.7V	50mV	LDO or PLSW	0.4A	LDO, PLSW: 0.5A	10Ω	200/360μs
LDO2	1.0-2.7V	50mV	LDO or PLSW	0.4A	LDO, PLSW: 0.5A	10Ω	200/360μs

Power Sequence

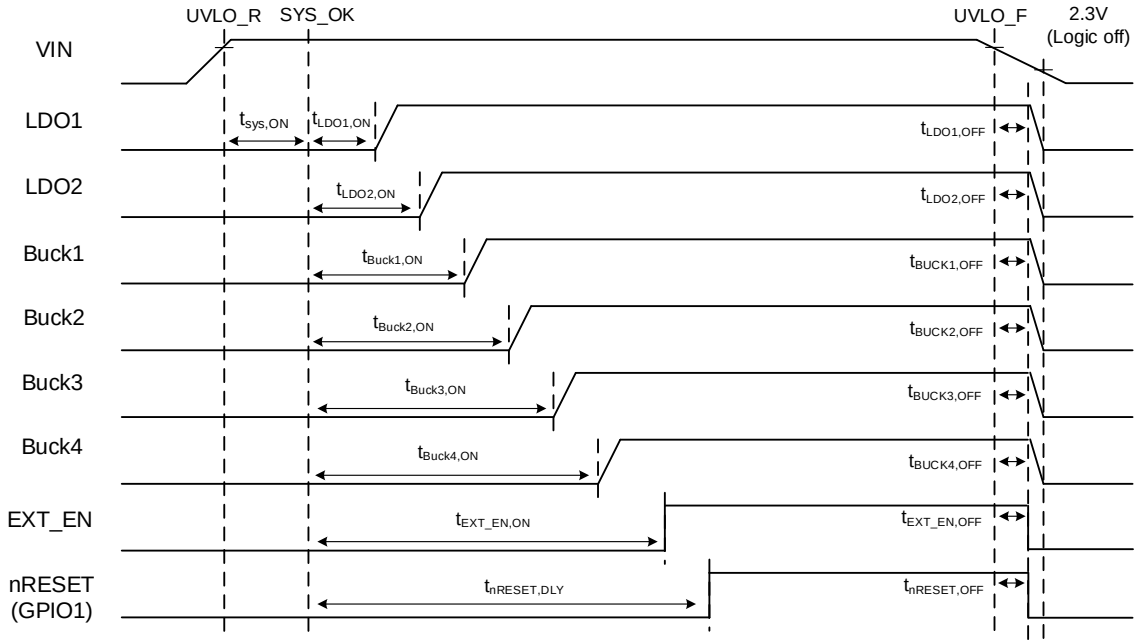


Figure 6. VIN Power On/Off Sequence

(1) When V_{IN} exceeds UVLO rising threshold, each channel will start up after the system delay $t_{sys,on}$(typ=1.4ms). During the system delay, the device will judge the GPIO2/3/4 status to define each channel default setting such as operating mode, output voltage and power on delay. The power-on delay time can be set from 0ms to 7.5ms (0.5ms/Step) to provide different power sequence for customer. If V_{IN} is smaller than UVLO falling threshold, all channels will be turned off after the delay time, the power-off delay time also can be set as 0ms, 0.25ms, 0.5ms or 1ms..

(2) nRESET and EXT_EN are open drain outputs. It is high impedance after the delay time when V_{IN} exceeds UVLO rising threshold. The delay time of nRESET can be set from 0.5ms to 16ms and the delay time of EXT_EN can be set from 0ms to 7.5ms (0.5ms/Step). The nRESET and EXT_EN will be pulled low immediately when any output is out of regulation and V_{IN} is lower than UVLO falling threshold. And, the nRESET stays high in sleep and deep sleep mode.

.Under-Voltage Lockout (UVLO)

The UVLO is achieved by detecting VIN voltage. If the voltage of AVIN pin exceeds $V_{IN,RISING}$ voltage(typ.=2.6V), all rails will start up after delay time. When AVIN pin voltage is lower than $V_{IN,FALLING}$ voltage(typ.=2.5V), all rails are shut down after delay time. The UVLO hysteresis (typ.=0.1V) is designed to prevent shutdown caused by supply transients.

.External Enable (EXT_EN)

The SY70202S provides an external power supply enable function, EXT_EN which is used to control an external regulator. If the voltage of AVIN pin exceeds $V_{IN,RISING}$ voltage(typ.=2.6V), the EXT_EN will become high impedance after fixed delay. When AVIN pin voltage is lower than $V_{IN,FALLING}$ voltage(typ.=2.5V) or fault occurs, the EXT_EN will goes low after the delay time. And, the EXT_EN can be set enable or disable on sleep or deep sleep mode by bit [6] at register 0x08h and 0x09h, respectively.

GPIOx Setting

The SY70202S has eight GPIO pins. Each GPIO can be programmed for a specific function for different applications. The GPIO2, GPIO3, and GPIO4 are the 3-level GPIOs that can be configured to set the output voltage of the power rail and the power on delay.

GPIO1:

Open drain output, as an nRESET function. nRESET acts a power good indicator, which is an open drain output. This pin will become high impedance after fixed delay. It will be pulled low immediately when any output goes out of regulation or AVIN pin voltage is lower than $V_{IN,FALLING}$. The input trigger of nRESET can be set SYS_OK or Buck2_PG by bit [7] at register 0x14h.

Note: If nRESET input trigger set as Buck2_PG, the power on delay time of Buck2 must be longer than other power rails.

After power on, after all channels turn on with sequence and then nRESET turn high with specific delay time.

If V_{IN} drop below UVLO falling threshold and recover above UVLO rising threshold again, PMIC will reset and restart with default power on sequence as first time power on.

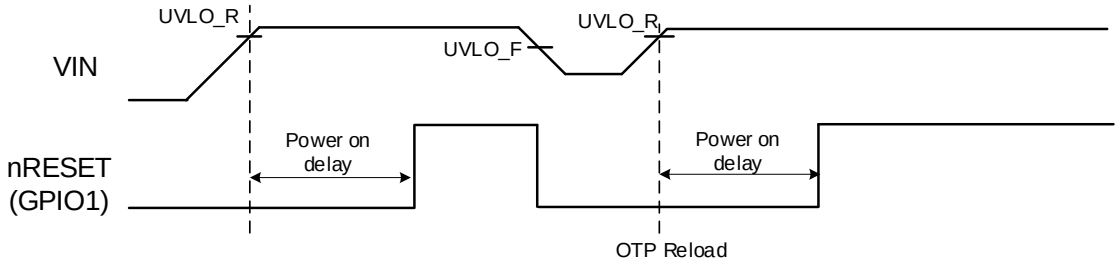


Figure 7. nRESET Logic When V_{IN} Drop below 2.3V

GPIO2:

Input pin, as a Buck1 and Buck2 output voltage select pin. The Buck1 output voltage can be set by B1_VSET, and the Buck2 output voltage can be set by B2_VSET. Buck1 and Buck2 have three options for user to select the different default configuration. The GPIO2 status must be set before UVLO and cannot be changed while the converter is running. After the converter is running, the setting of the Buck operating mode and output voltage can be changed by I²C.

Table 1. GPIO2 Function Selection

GPIO2	Buck1 Output Voltage	Buck2 Output Voltage
High	B1_VSET=2.6V	B2_VSET0=0.91V B2_VSET1=0.91V B2_VSET2=0.91V
Floating	B1_VSET=2.5V	B2_VSET0=0.91V B2_VSET1=0.91V B2_VSET2=0.91V
Low	B1_VSET=2.5V	B2_VSET0=1.2V B2_VSET1=1.2V B2_VSET2=1.2V

GPIO3:

Input pin, as a Buck3 output voltage and power on delay option select pin. The output voltage of Buck3 and the power on delay of each rail can be configured by GPIO3. There have three options for user to select the different default configurations. The GPIO3 status must be set before UVLO and cannot be changed while the converter is running. After the converter is running, the setting of the Buck operating mode and output voltage can be changed by I²C.

Table 2. GPIO3 Function Selection

GPIO3	Buck3 Output Voltage	Power on Delay
High	B3_VSET0=0.78V B3_VSET1=0.78V B3_VSET2=0.78V	Sequence A
Floating	B3_VSET0=0.78V B3_VSET1=0.78V B3_VSET2=0.78V	Sequence B
Low	B3_VSET0=0.78V B3_VSET1=0.78V B3_VSET2=0.78V	Sequence C

Table 3. Power-on Sequence

Rail	GPIO3=High Sequence A	GPIO3=Floating Sequence B	GPIO3=Low Sequence C
Buck1	3.50ms	3.00ms	3.00ms
Buck2	0.50ms	0.50ms	0.50ms
Buck3	0.50ms	0.50ms	0.00ms
Buck4	3.00ms	3.50ms	1.50ms
LDO1	2.00ms	2.00ms	2.00ms
LDO2	2.00ms	2.00ms	2.00ms
nRESET	Input Trigger: SYS_OK Delay time=8ms		

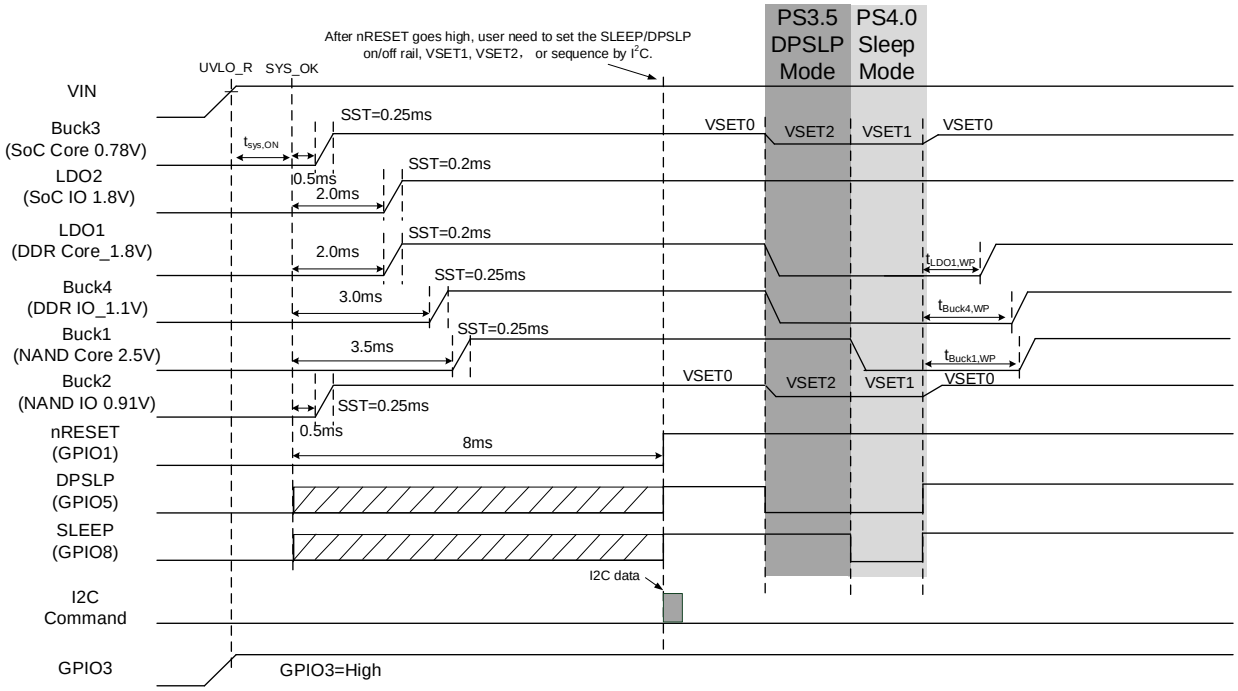


Figure 8. Power Sequence of Sequence A

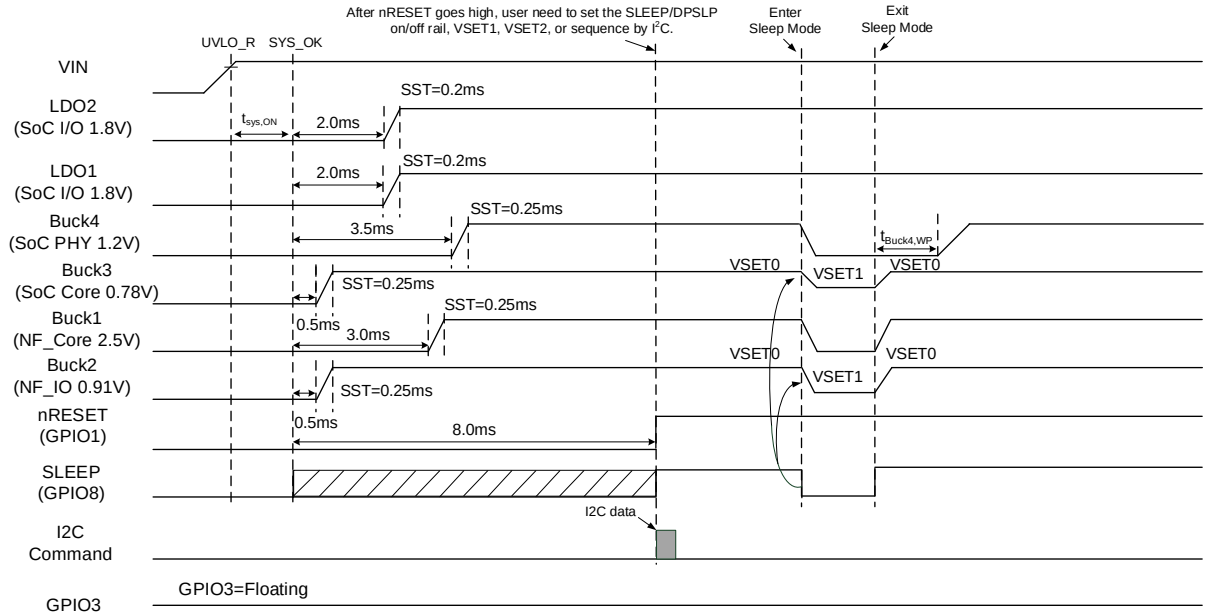


Figure 9. Power Sequence of Sequence B

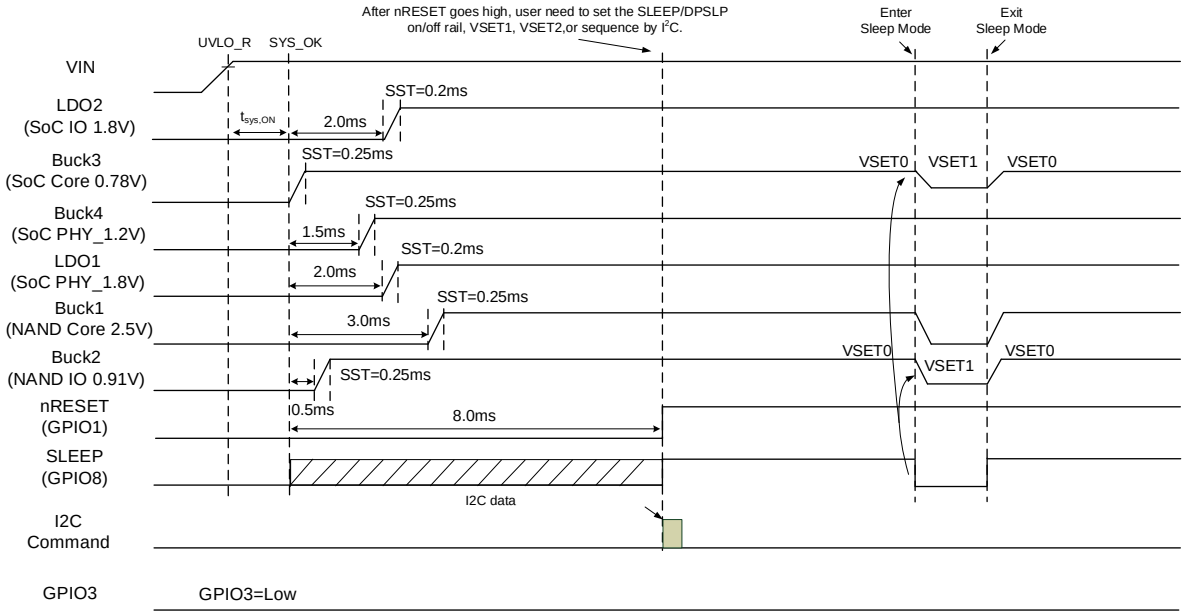


Figure 10. Power Sequence of Sequence C

GPIO4:

Input pin, as a Buck4 and LDO1 function select pin. The Buck4 can be set operating on buck or LDO mode by B4_Mode. If the Buck4 operating on Buck mode, the output voltage can be set by B4_VSET. The Buck4 output voltage increase can be set by B4_Add, and only Buck mode can be set. And, the LDO1 can be set operating on LDO or PLSW mode by LDO1_Mode. If the LDO1 operating on LDO mode, the output voltage can be set by LDO1_VSET. Buck4 and LDO1 have three options for user to select the different default configuration. The GPIO4 status must be set before UVLO and cannot be changed while the converter is running. After the converter is running, the setting of the Buck operating mode and output voltage can be changed by I²C.

Table 4. GPIO4 Function Selection

GPIO4	Buck4 Mode and Output Voltage	LDO1 Mode and Output Voltage
High	B4_Add=0, B4_Mode=Buck Mode, B4_VSET=1.1V	LDO1_Mode=LDO Mode LDO1_VSET=1.8V
Floating	B4_Add=0, B4_Mode=Buck Mode, B4_VSET=1.2V	LDO1_Mode=LDO Mode LDO1_VSET=1.8V
Low	B4_Mode= LDO Mode, B4_VSET=1.8V	LDO1_Mode=PLSW

GPIO5:

GPIO5 can be configured as a DPSLP mode input pin, a nIRQ(SYSWARN) output pin, or an I²C controlled output pin by bit [7:6] at register 0x15h. User can modified the function of GPIO5 by I²C after nRESET goes high.

DPSLP mode: Input pin. The DPSLP function is level trigger. If the GPIO5 is pulled high (>1.2V), the device operates at ACTIVE mode; if the GPIO5 is pulled low (<0.55V), the device operates at DPSLP mode.

I²C Controlled Output: GPIO5 can be configured as the I²C controlled open drain output. The output can be selected HIGH or LOW by bit [1] at register 0x15h.

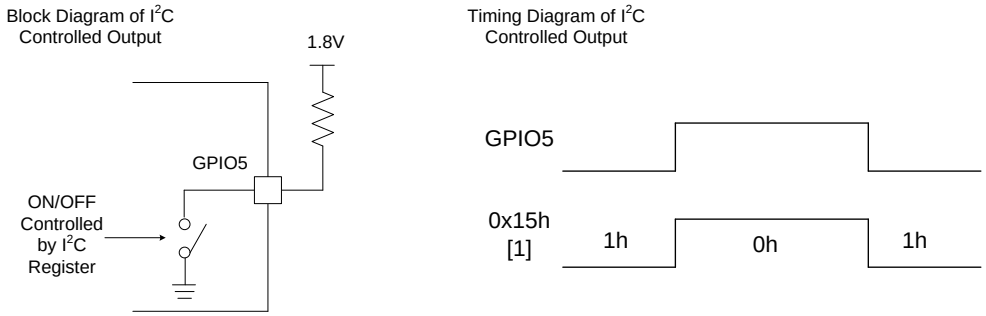


Figure 11. Block Diagram and Timing Diagram of I²C Controlled Output Function

nIRQ(SYSWARN) Output: GPIO5 can be configured as the nIRQ(SYSWARN) open drain output. If AVIN < SYSWARN (typ=2.9V), the IC asserts the nIRQ interrupt. GPIO5 will goes low. The nIRQ pin only de-asserts after the fault condition is no longer present and the corresponding fault bit is read via I²C.

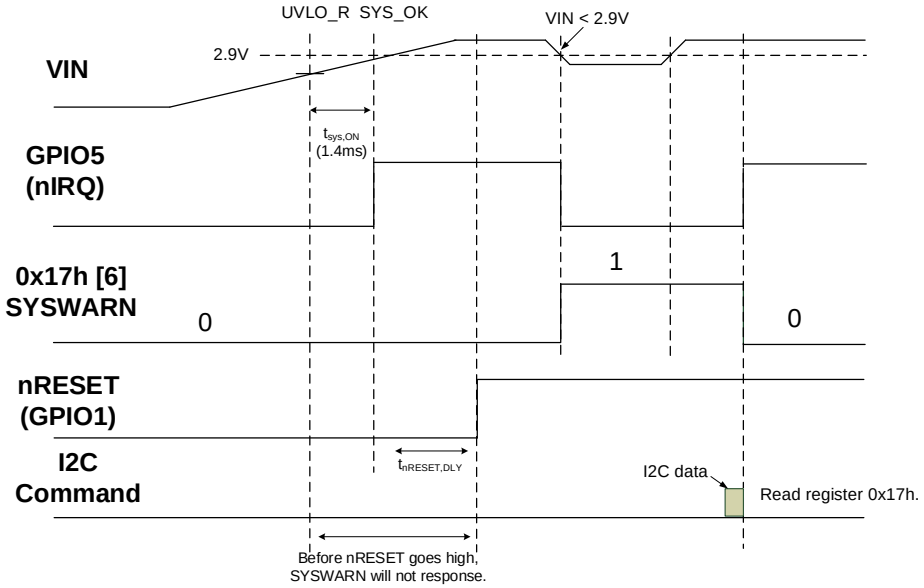


Figure 16. Timing Diagram of nIRQ (SYSWARN)

GPIO6:

Input pin, as a LDO2 mode select pin. LDO2 operating status can be configured by GPIO6. If the GPIO6 is pulled high, it operates at LDO mode; if the GPIO6 is pulled low, it operates at PLSW mode. The LDO2 mode will be latched after LDO2 power-on delay.

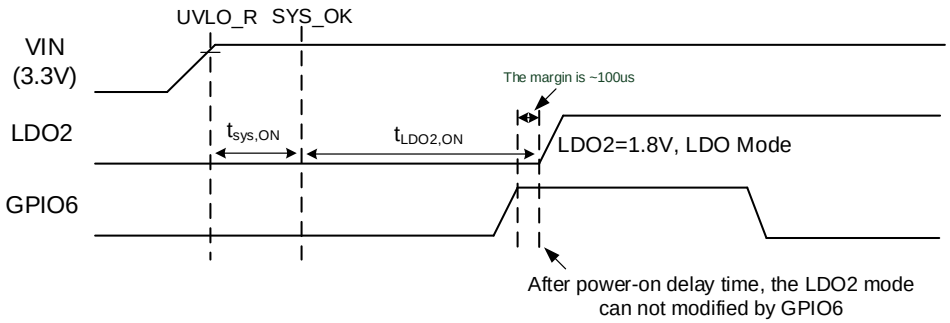


Figure 12. Timing Diagram of GPIO6 Function

GPIO7:

GPIO7 can be configured as an EXT_EN output pin, an I²C controlled output pin, or a PWRDIS input pin by bit [5:4] at register 0x15h. User can be modified the function of GPIO7 by I²C after nRESET goes high.

I²C Controlled Output: GPIO7 can be configured as the I²C controlled open drain output. The output can be selected HIGH or LOW by bit [0] at register 0x15h.

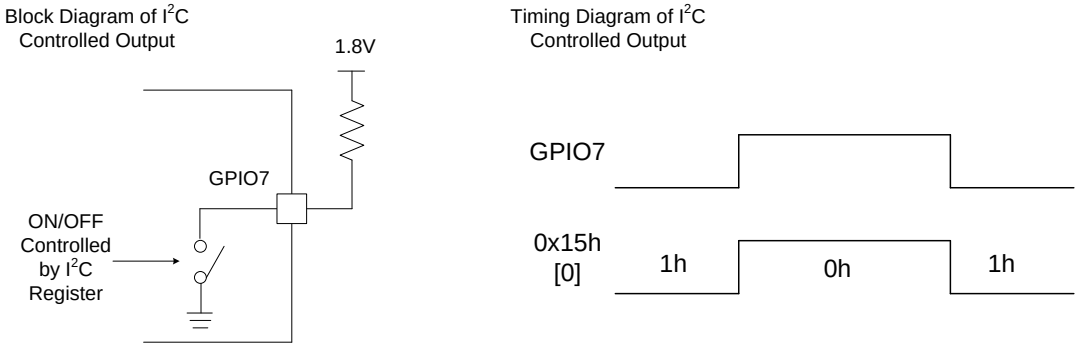


Figure 13. Block Diagram and Timing Diagram of I²C Controlled Output Function

PWRDIS Input: GPIO7 can be configured as the PWRDIS input. If the GPIO7 is pulled high (>1.2V), all rails will be shut down; if the GPIO7 is pulled low (<0.55V), all rails will power up with sequence. PWRDIS can be considered a global enable for the device. If PWRDIS is high during power-on, this will hold off the device from powering on the rails.

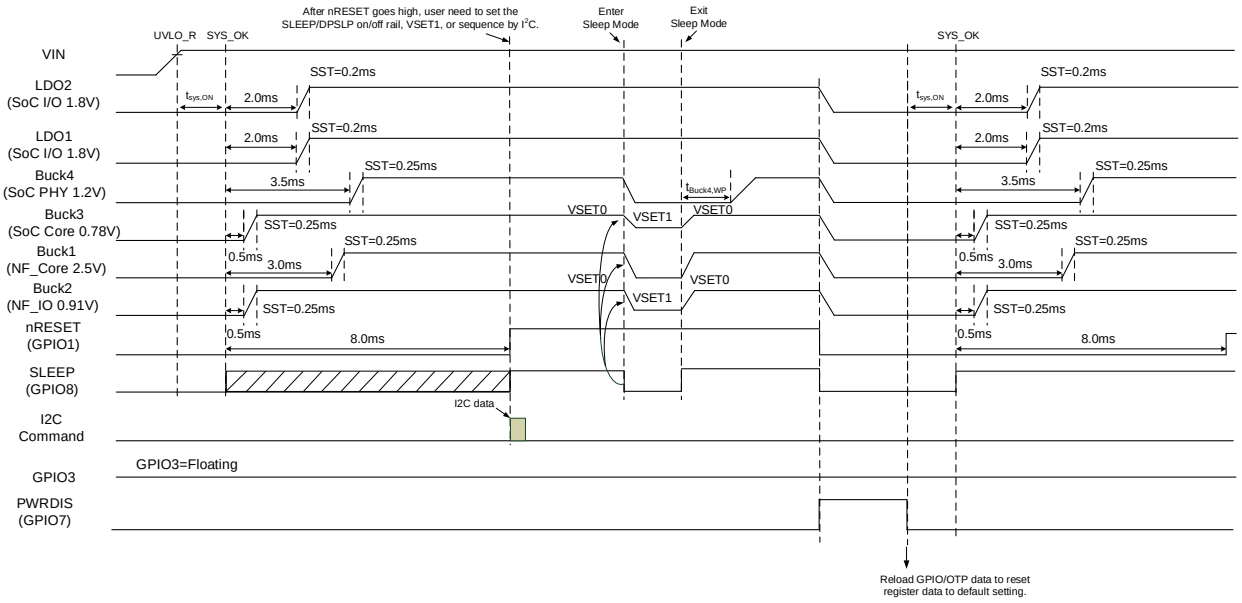


Figure 14. Conceptual of Timing Diagram for PWRDIS during Operating

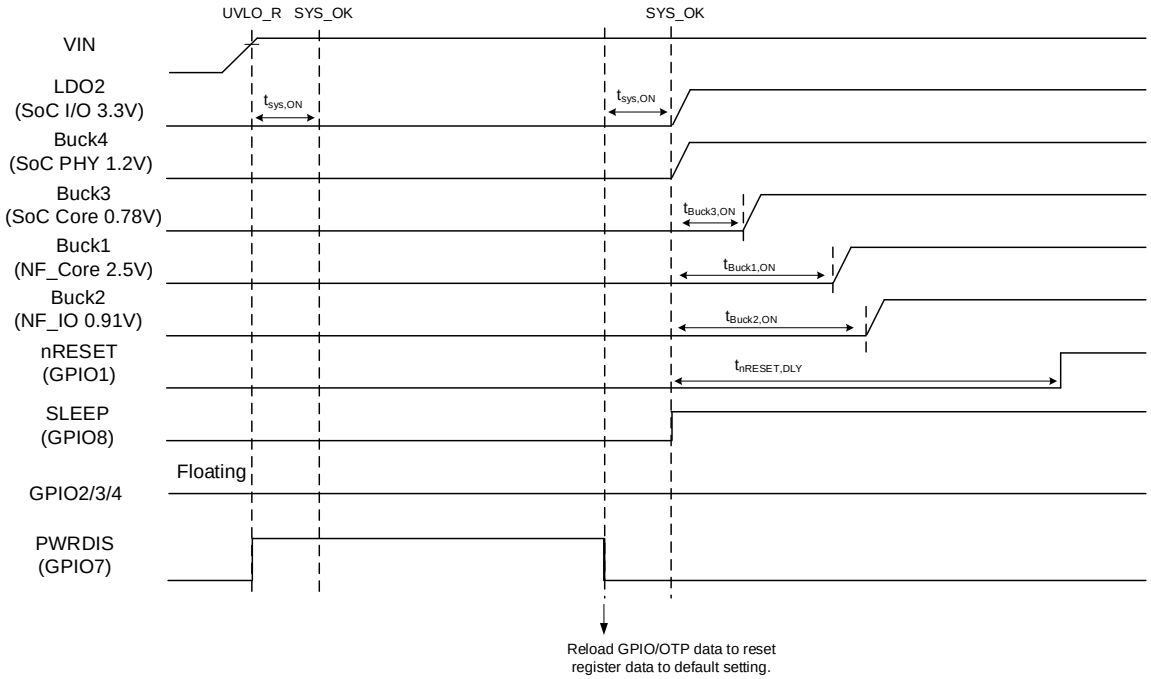


Figure 15. Conceptual of Timing Diagram for PWRDIS during V_{IN} Power-on

GPIO8:

Input pin, as a SLEEP pin. The sleep function is level trigger. If the GPIO8 is pulled high (>1.2V), the device operates at ACTIVE mode; if the GPIO8 is pulled low (<0.55V), the device operates at SLEEP mode.

GPIO Initial Status

GPIO	Function	Pin	Initial Status
GPIO1	nRESET	Open drain output	NA
GPIO2	Buck1 and Buck2 Bank	Input	NA
GPIO3	Buck3 and Power on delay Bank	Input	
GPIO4	Buck4 and LDO1 Bank	Input	
GPIO5	DPSLP, I2C Control Output, or nIRQ(SYSWARN)	Input or Open drain output	NA
GPIO6	LDO2 Mode	Input	Internal 1Mohm pull low
GPIO7	EXT_EN, I2C Control Output, or PWRDIS	Input or Open drain output	PWRDIS: External 10kohm pull low
GPIO8	SLEEP	Input	Internal 1Mohm pull low

State Machine

The SY70202S contains six internal states. In the RESET state, the device is waiting for the input voltage on VIN to be within a valid range between VIN_UVLO and VIN OVP threshold. At this state, all regulators will be off. The ACTIVE state is the normal operating state when the input voltage is within the allowable range, all outputs are turned on, and no faults will be presented. When entering the ACTIVE state from the RESET, THERMAL, OV/SCP fault, all regulators are powered on following their power up sequence. The regulators will not be sequenced when entering ACTIVE form SLEEP or DPSLP.

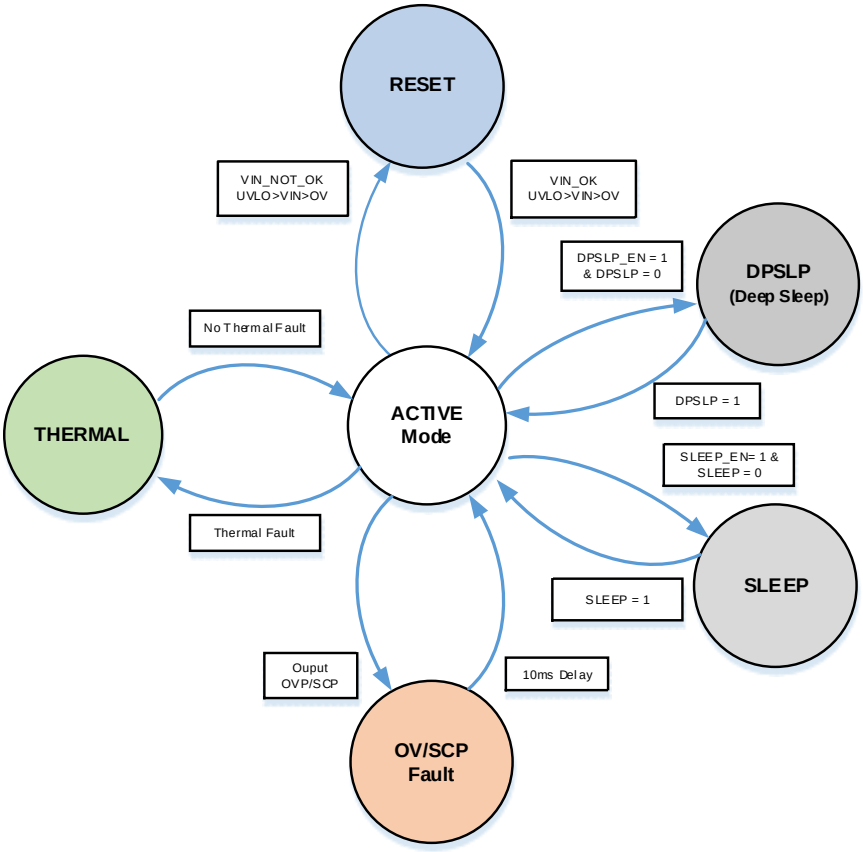


Figure 16. State Machine

Sleep Mode State

Each output can be programmed to be on or off in the sleep state. The regulators follow their programmed sequencing delay times when turning on or off as they exit or enter the SLEEP state. Buck 1~4, LDO1/2, and EXT_EN can be programmed to turn off or turn on in the sleep state by I²C. The IC can enter SLEEP state via the I²C register SLEEP bit or by a GPIO input. Each individual regulator output can be programmed to be either on or off in the SLEEP state. Buck3 can also be programmed to regulate to its VSET0 voltage, or VSET1 voltage (DVS), or be turned off in the SLEEP state. Table 5 shows the conditions to enter SLEEP state. The device I²C stays enabled in SLEEP state. The device exits the SLEEP state when the conditions to enter SLEEP state are no longer present.

Table 5. SLEEP Mode Truth Table

SLEEP	0x10h[1] SLEEP_EN	Result
0	1	Sleep Mode
1	1	Active Mode

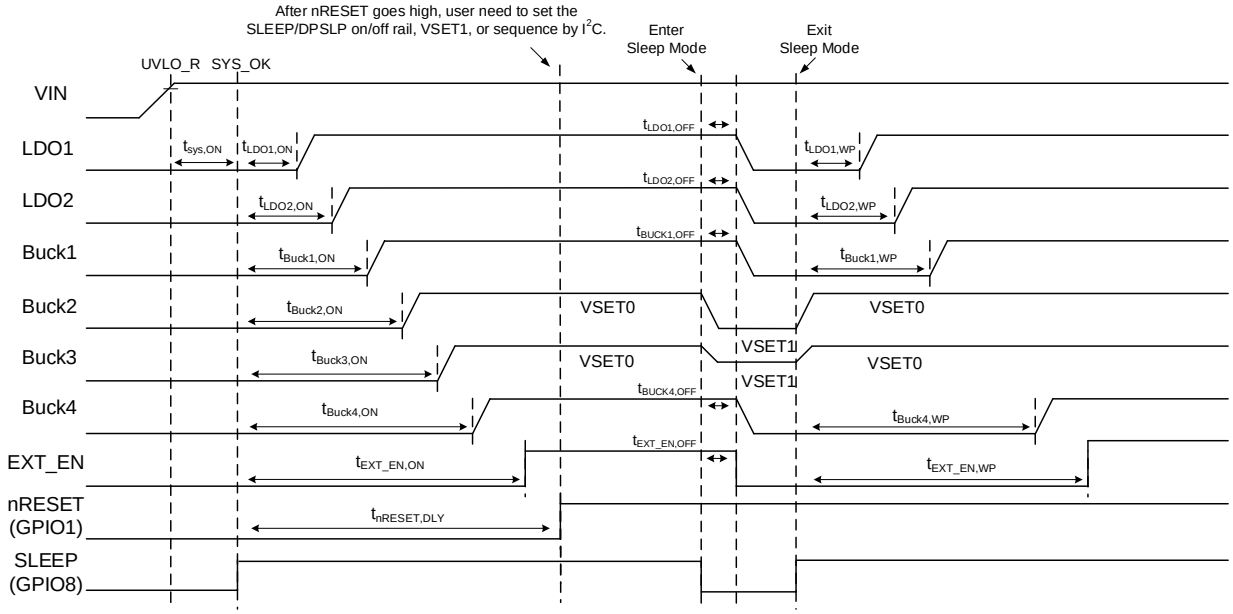


Figure 17. Conceptual of Sequence for Enter/Exit SLEEP Mode

- Power-on delay time:

$t_{LDO1,ON}$/ $t_{LDO2,ON}$/ $t_{Buck1,ON}$/ $t_{Buck2,ON}$/ $t_{Buck3,ON}$/$t_{Buck4,ON}$/$t_{EXT\_EN,ON}$ =0~7.5ms, 0.5ms/step.

- Power-off delay time:

$t_{LDO1,OFF}$/ $t_{LDO2,OFF}$/ $t_{Buck1,OFF}$/ $t_{Buck2,OFF}$/ $t_{Buck3,OFF}$/$t_{Buck4,OFF}$/$t_{EXT\_EN,OFF}$ =0ms, 0.25ms, 0.5ms, or 1ms.

- nRESET delay time:

$t_{nRESET,DLY}$ =0.5ms, 1ms, 2ms, 4ms, 8ms, or 16ms.

- Wake up delay time:

$t_{LDO1,WP}$/ $t_{LDO2,WP}$/ $t_{Buck1,WP}$/ $t_{Buck2,WP}$/ $t_{Buck3,WP}$/$t_{Buck4,WP}$/$t_{EXT\_EN,WP}$ =0~1.5ms, 0.5ms/step.

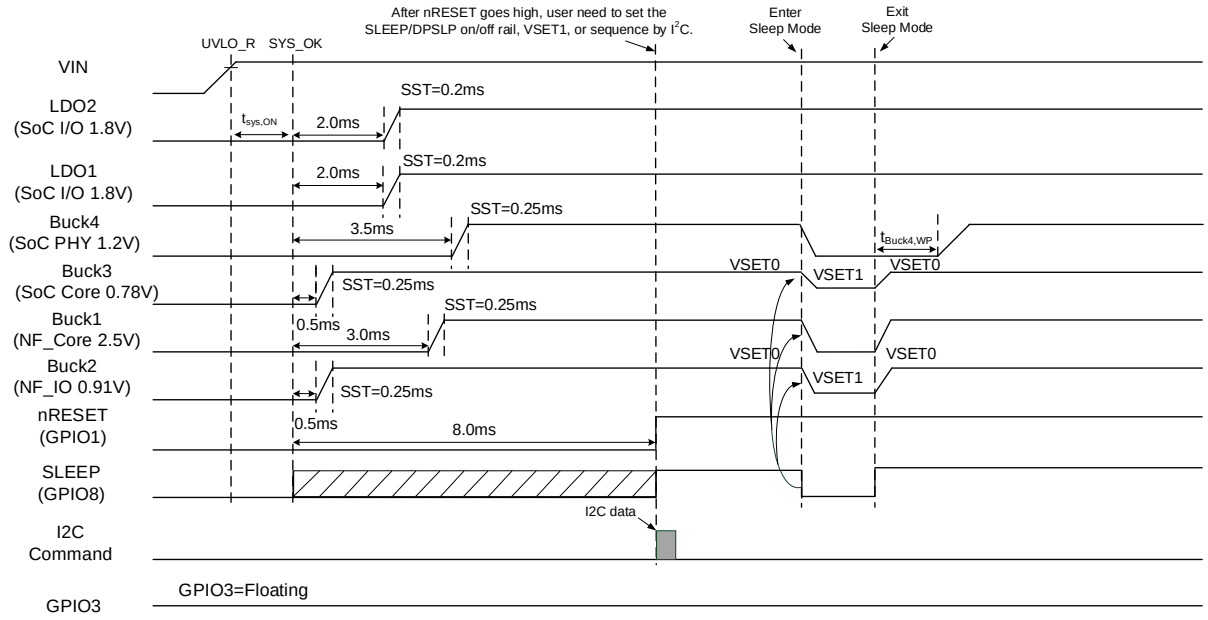


Figure 18. SLEEP Sequence for Application B

Deep Sleep (DPSLP) Mode State

The DPSLP state is another low power operating mode for the operating system. It is similar to the SLEEP state. Each output can be programmed to be on or off in the DPSLP state. This programming can be different from the SLEEP state. The regulators follow their programmed sequencing delay times when turning on or off as they exit or enter the SLEEP state.

The device can enter DPSLP state via I²C registers DPSLE_EN and DPSLP pin. Table 6 shows the conditions to enter DPSLP state. Device I²C stays enabled in DPSLP state. The device exits the DPSLP state when the conditions to enter DPSLP state are no longer present.

Between enter two SLEEP/DPSLP states must greater than 4ms. Within 4ms of entering the SLEEP/DPSLP state, the internal clock blocks the next instruction to enter the SLEEP/DPSLP state. However, power-off delay time is greater than 0ms, this can be ignored.

Table 6. DPSLP Mode Truth Table

DPSLP	0x10h[0]	Result
	DPSLP_EN	
0	1	Deep Sleep Mode
1	1	Active Mode

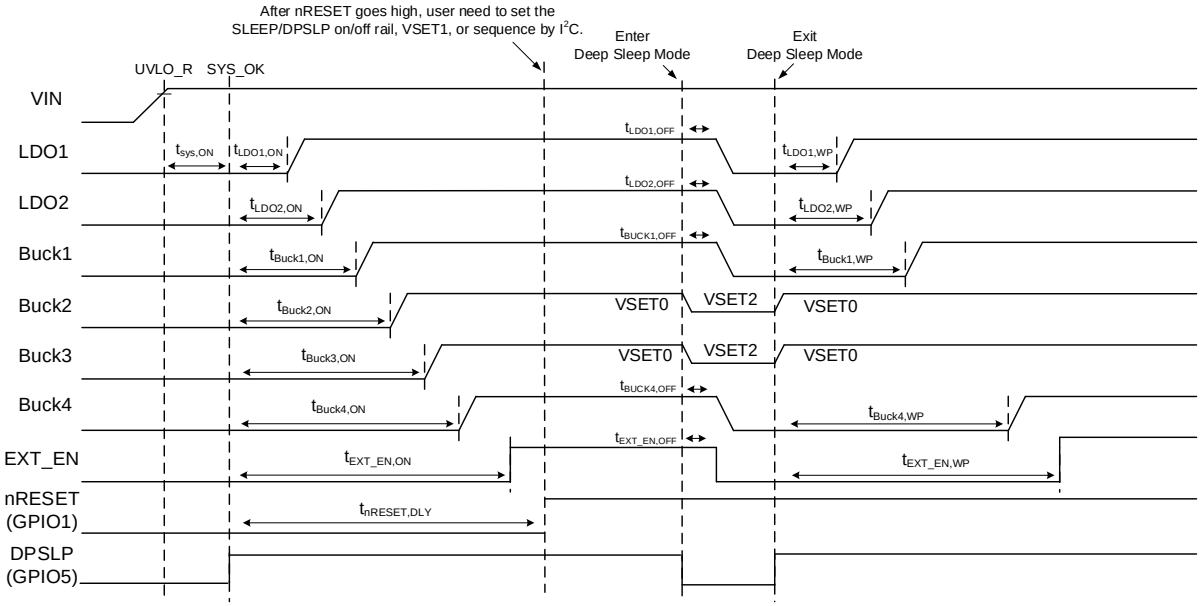


Figure 19. Conceptual of Sequence for Enter/Exit DPSLP Mode

- Power-on delay time:

$t_{LDO1,ON}$/ $t_{LDO2,ON}$/ $t_{Buck1,ON}$/ $t_{Buck2,ON}$/ $t_{Buck3,ON}$/$t_{Buck4,ON}$/$t_{EXT\_EN,ON}$ =0~7.5ms, 0.5ms/step.

- Power-off delay time:

$t_{LDO1,OFF}$/ $t_{LDO2,OFF}$/ $t_{Buck1,OFF}$/ $t_{Buck2,OFF}$/ $t_{Buck3,OFF}$/$t_{Buck4,OFF}$/$t_{EXT\_EN,OFF}$ =0ms, 0.25ms, 0.5ms, or 1ms.

- nRESET delay time:

$t_{nRESET,DLY}$ =0.5ms, 1ms, 2ms, 4ms, 8ms, or 16ms.

- Wake up delay time:

$t_{LDO1,WP}$/ $t_{LDO2,WP}$/ $t_{Buck1,WP}$/ $t_{Buck2,WP}$/ $t_{Buck3,WP}$/$t_{Buck4,WP}$/$t_{EXT\_EN,WP}$ =0~1.5ms, 0.5ms/step.

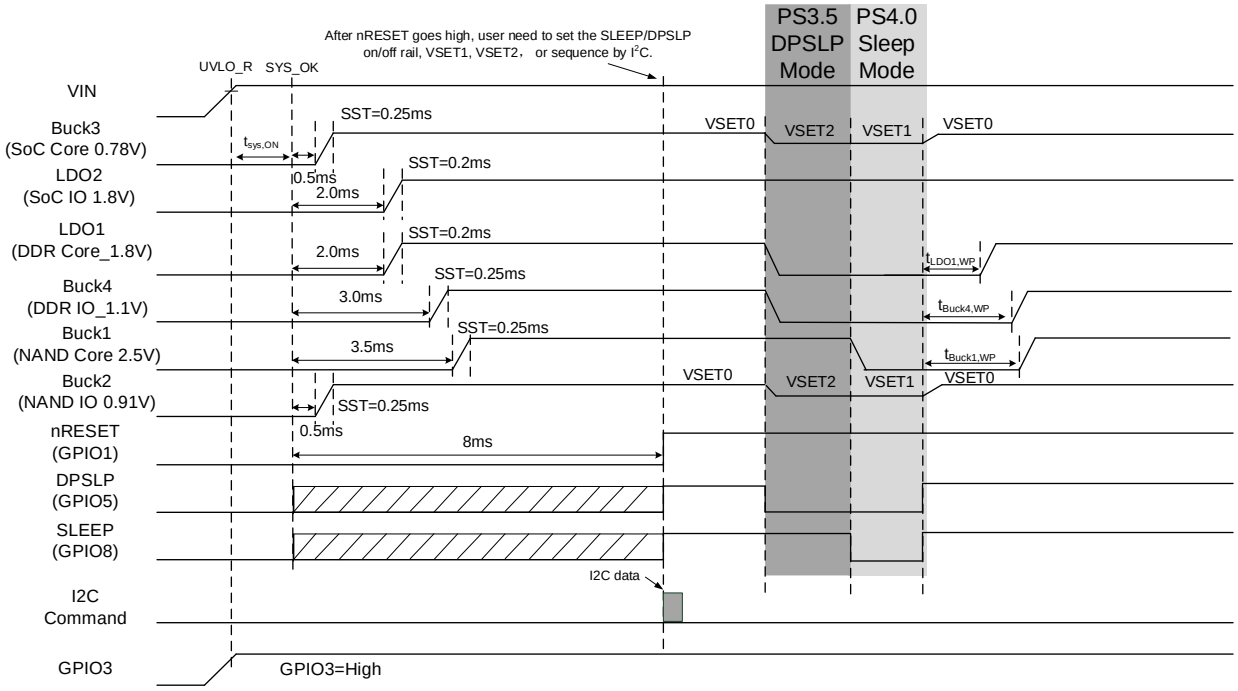


Figure 20. SLEEP and DPSLP Sequence for Application A

Protection Function

Protection		Mechanism
VIN Over Voltage Protection (VINOVP)		When VIN rise above 3.9V, shutdown all. When VIN decreases to 3.6V, restart with power up sequence.
Over Temperature Protection (OTP)		When temperature exceeds 155°C, shutdown all. When temperature cool down to 140°C, restart following the power up sequence.
Output Over Voltage Protection (OVP)		>125% with 10μs deglitch time, shutdown all for 10ms then restart with power up sequence.
Output Short Circuit Protection (SCP)		Buck: <30% with 50μs deglitch time, shutdown all for 10ms then restart with power up sequence. LDO: <60% with 50μs deglitch time, shutdown all for 10ms then restart with power up sequence.
Over Current Protection (OCP)	Buckx	Inductor current peak current limit, and then keep regulation.
	LDO	Limit LDO current. If I_{out}=0.5A another 200us, the IC shuts down all for 10ms then restart with power up sequence.
	LDO1/2 PSLW Mode	Limit load switch current. If Iout=0.5A over 200us, the IC shuts down all for 10ms then restart with power up sequence.

The device will reset to default setting when VINOVP, OTP, OVP, SCP, or OCP shutdown.

.Output Over Voltage and Short Circuit Protection

If anyone output occurs short or over voltage condition, this device will be shut down without power off sequence for 10ms then will restart with power up sequence. If the short or over voltage condition still exists in the ACTIVE state, this device will be shut down again for 10ms then restart, until the fault condition is removed.

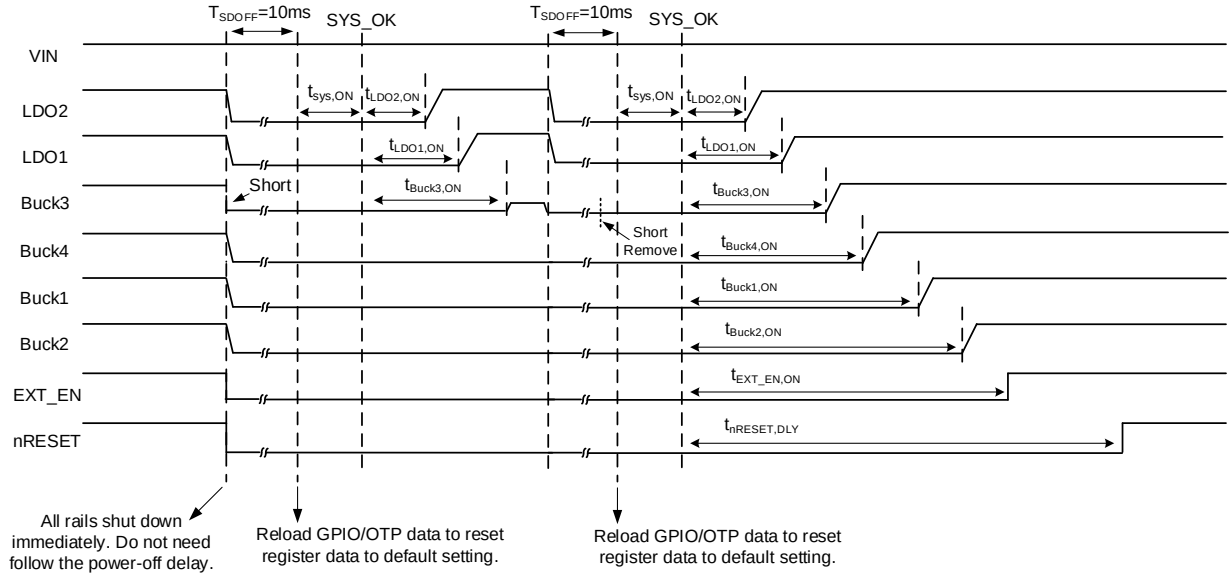


Figure 21. Conceptual of Buck3 Occurring Output Short Circuit Event in Active Mode

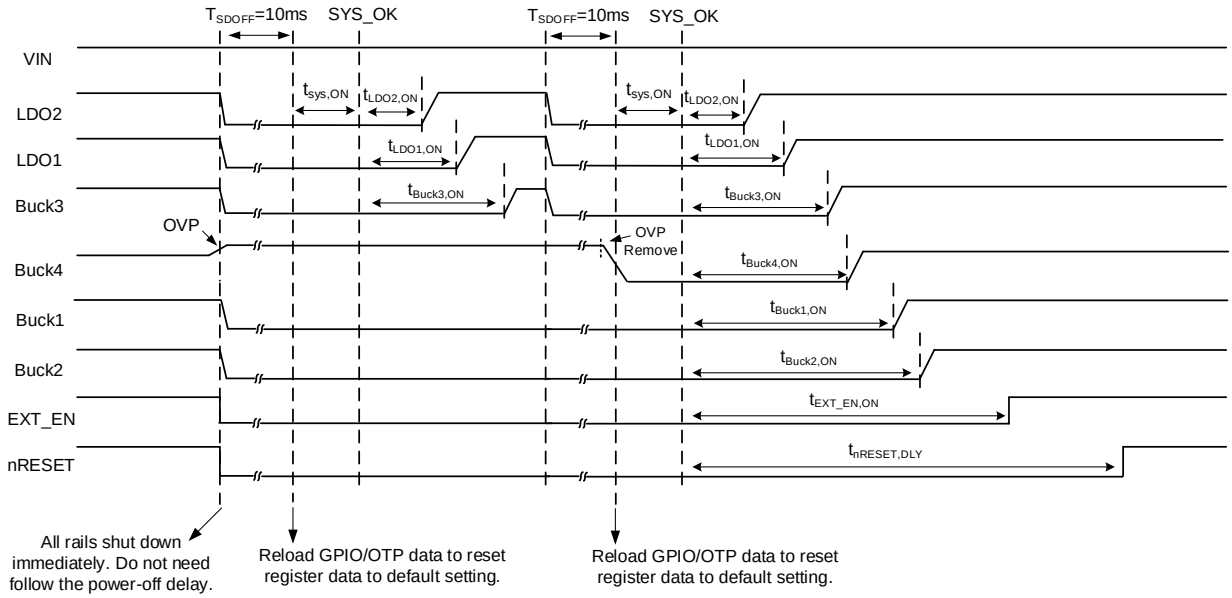


Figure 22. Conceptual of Buck4 Occurring Output over Voltage Event in Active Mode

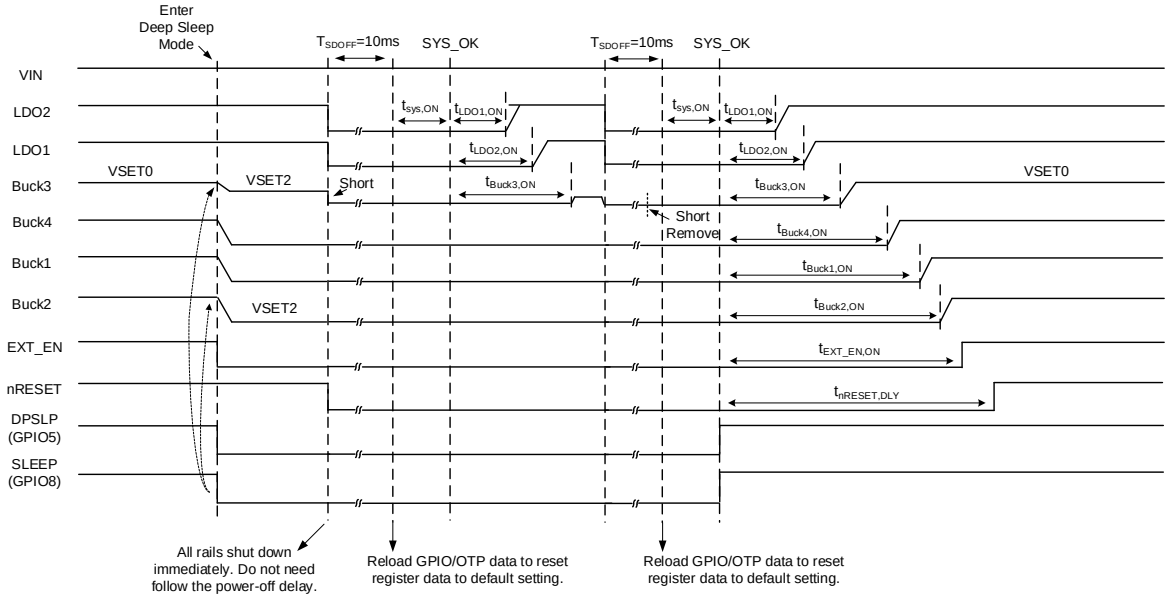


Figure 23. Conceptual of Buck3 Occurring Output Short Circuit Event in Deep Sleep Mode

.Input Over Voltage Protection

VIN OVP threshold is 3.9V. When VIN exceeds 3.9V, all channels will be turned off. The OVP hysteresis is 0.3V. When VIN decreases to 3.6V, all channels will restart follow power on sequence.

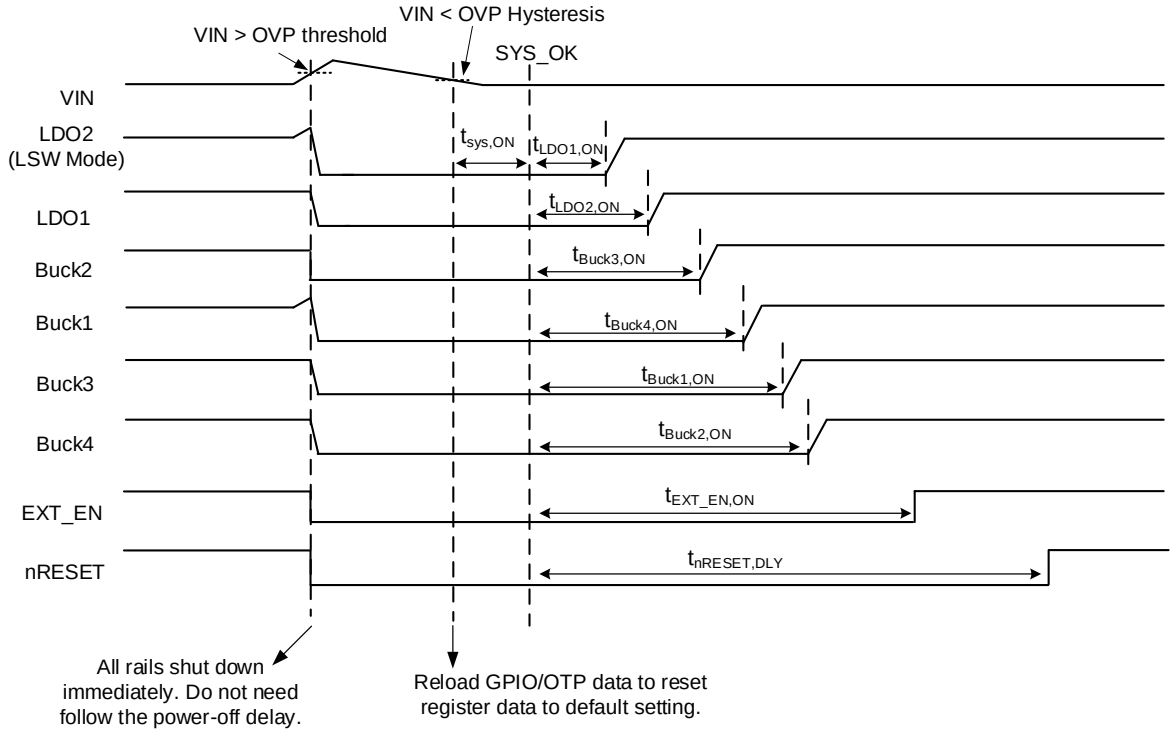


Figure 24. Conceptual of INPUt over Voltage Protection Mechanism

.Output Current Limit

The Buck converter limits the HS switch current and LS switch current in each switching cycle. This reduces the effective duty cycle and causes the output voltage to drop, potentially creating a short circuit condition, and causing the IC to turn off all supplies off for 10ms then restart with sequence.

For LDO, when the output current reaches the current limit threshold, the LDO will limit the output current. If current limit loop functions for 200μs or short circuit is detected, the IC will be shut down for 10ms then restart with sequence.

For load switch (bypass mode) of buck1, when the output current exceeds 4.5A, the IC will limit the current. If current limit loop functions for 200μs the IC will be shut down for 10ms then restart with sequence.

.Thermal Shutdown

A thermal shutdown is implemented to prevent damage because of excessive heat and power dissipation. Once the junction temperature exceeds 155°C the device will be shut down without power off sequence. When the temperature cold down to 140°C the device will automatically restart performing the startup sequence with the default configuration.

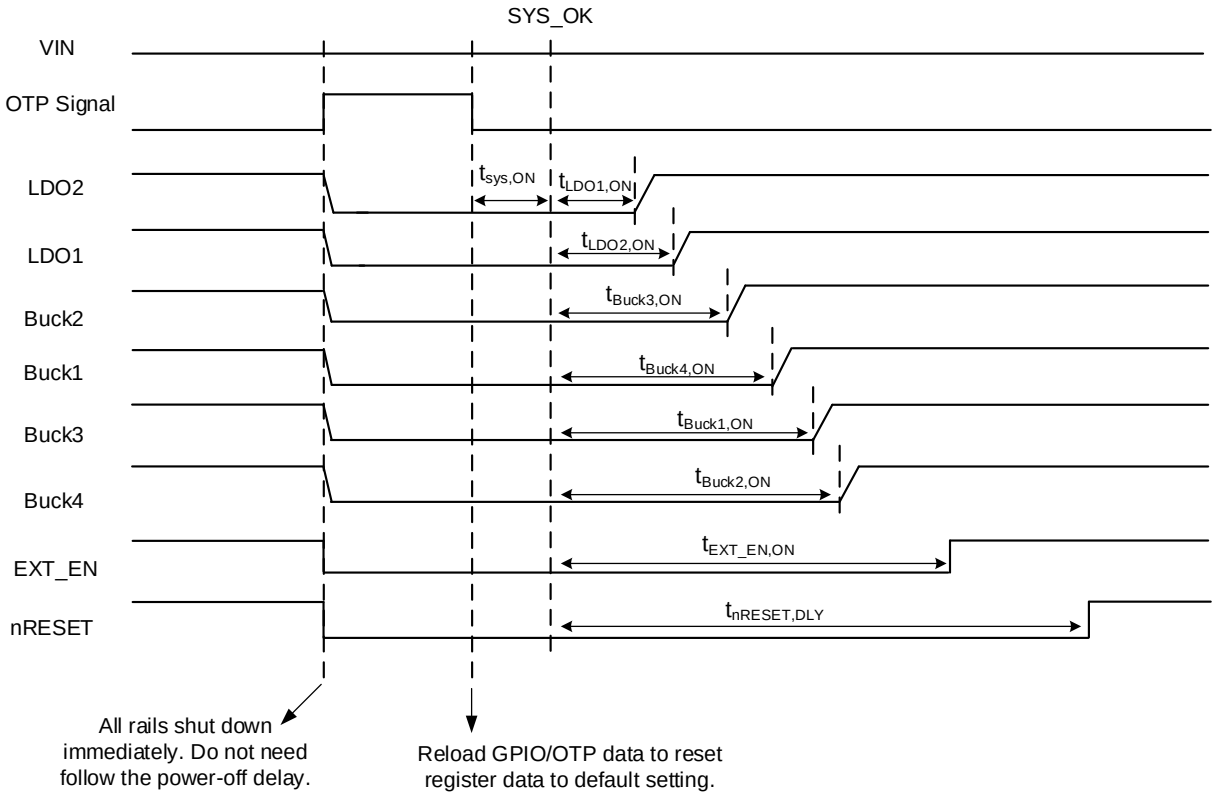


Figure 25. Conceptual of over Temperature Protection Mechanism

Design Procedure

The following paragraphs provide information on selecting the external components for each of the buck converters, to match the application requirements.

Input Capacitor C_{INX}

For the best performance, select typical X5R or better grade ceramic capacitors with a 6.3V or higher rating, and at least 10µF capacitance. The capacitor should be placed as close as possible to the corresponding pin on the device, while also minimizing the loop area formed by CINx and the IN/GND pins.

When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability, and high RMS current rating over a wide temperature and voltage range.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current. The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLECAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at D = 0.5, the

$$V_{IN\_RIPPLE,CAP} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 10µF X5R capacitor is sufficient for each of the buck converters in most applications.

Output Inductor L_X

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L_1 = \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{0.4 \times f_{SW} \times I_{OUT,MAX}}$$

where f_{SW} is the switching frequency and IOUT,MAX is the maximum load current.

The SY70202S has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Use an inductor with DCR less than 20mΩ to achieve good overall efficiency.

Output Capacitor C_{OUTX}

Select the output capacitor COUT to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting COUT. For the best performance, use two X5R or better grade ceramic capacitors with a 10V rating, and capacitance of at least 22µF for each converter output.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed:

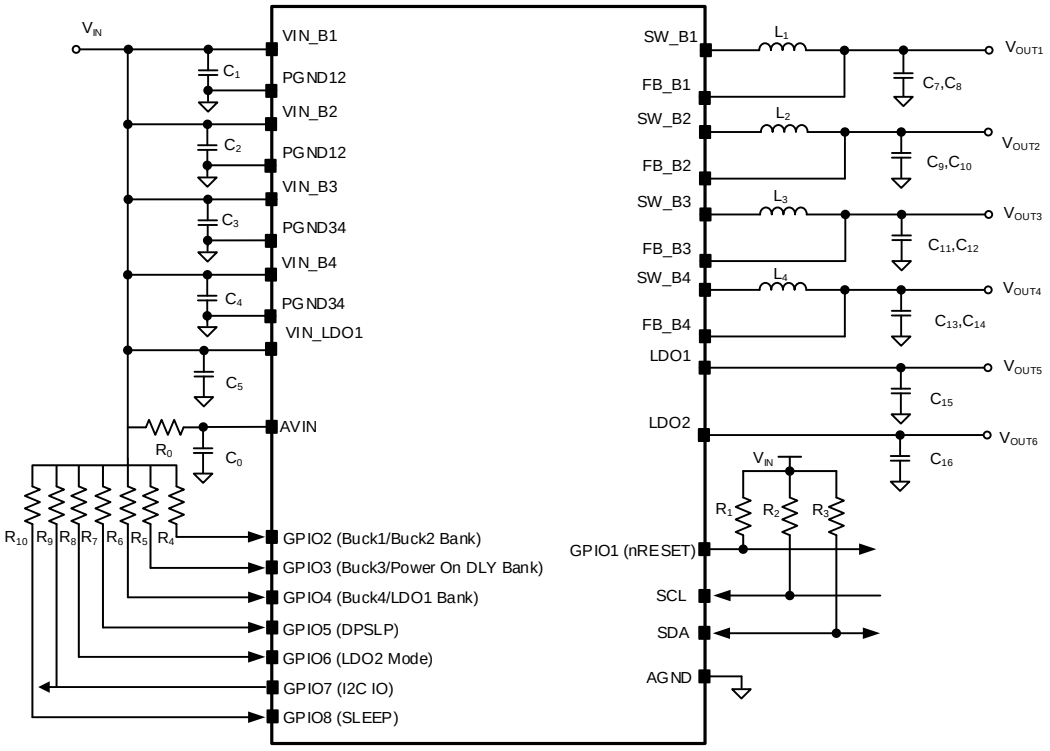
The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔIL) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, consider both.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times f_{SW} \times C_{OUT}} \times ESR$$

The measured capacitive ripple might be higher than the theoretical value because the effective capacitance for ceramic capacitors decreases with the voltage across its terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Application Schematic



BOM List

Reference Designator	Description	Part Number	Manufacturer
U_1	PMIC	SY70202SVTS	Silergy
C_1, C_2, C_3, C_4	10μF/6.3V,0402,X5R	GRM155R60J106ME47D	Murata
C_0, C_5, C_{15}, C_{16}	1μF/10V, 0603, X5R	GRM188R61A105KA61D	Murata
C_7, C_8, C_9, C_{10}, C_{11}, C_{12}, C_{13}, C_{14}	22μF/6.3V, 0603, X5R	GRM186R60J226ME15D	Murata
L_1, L_2, L_3, L_4	0.47μH, 26mohm, 4A 2016	DFE201612E-R47M	Murata
R_1	10k, 0603		
R_2, R_3	4.7k, 0603		
R_4, R_5, R_6, R_7, R_8, R_9, R_{10}	100k, 0603		

Layout Design

- Follow these PCB layout guidelines for optimal performance:
- Place CINX COUTX and L as close as possible to the device to improve efficiency and provide better noise immunity.
- Maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance.
- Place the decoupling capacitor of VIN_B1 close to the VIN_B1 and PGND12 pins. Minimize the loop area formed by the input capacitors, input pins, and PGND pins. Apply the same principle of decoupling capacitor placement for all buck converters and LDOs.
- Minimize the PCB copper area associated with the LX pin to improve noise immunity.

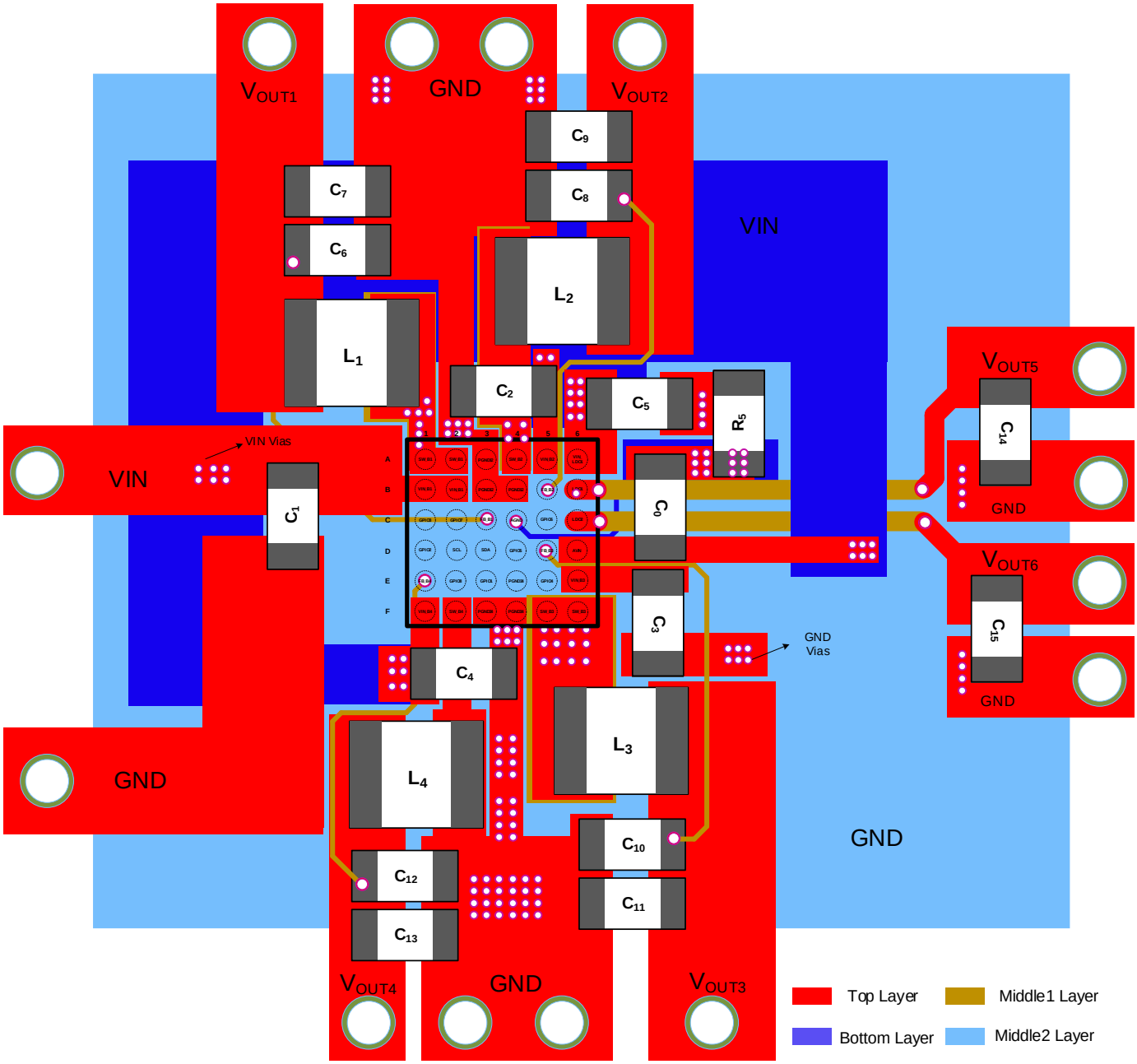


Figure 26. Suggested PCB Layout

I²C Compatible Interface

The SY70202S integrates an I²C compatible interface. The PMIC should support I²C interface that allows the host to control the output voltage level of all channels using DVS function. I²C interface should support clock speeds up to 3.4MHz and use standard I²C commands. High speed mode at 3.4MHz is entered from the master by issuing a special one byte address. All transactions start with a control byte sent from the I²C master device. The control byte begins with a START condition, followed by 7-bits of slave address which is 0100101x for this PMIC.
The I²C interface is fully functional after VIN is above UVLO threshold.

I²C Interface Timing Diagram

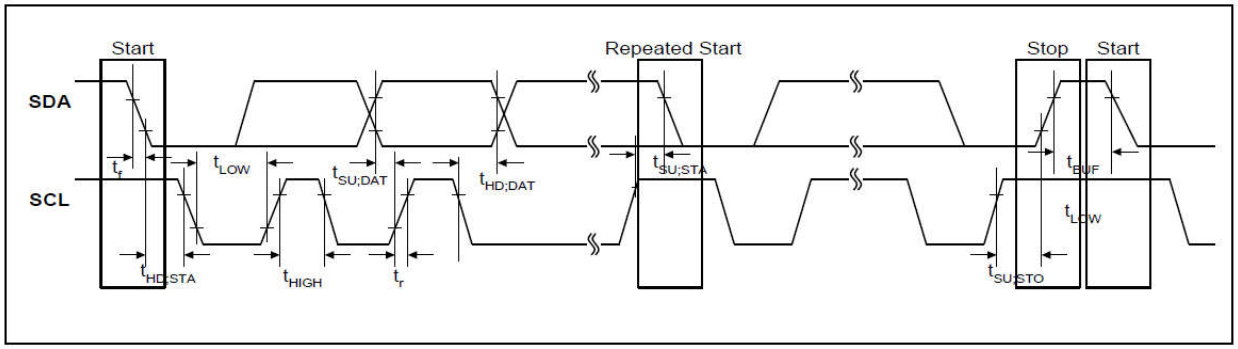


Figure 27. I²C Interface Timing Diagram

I²C EC Table

Characteristics	Symbol	Units	Standard Mode		Fast Mode		High-Speed Mode	
			Min	Max	Min	Max	Min	Max
Vin Voltage	V_{IN}	V	3.3V					
Pull-up Voltage	V_{PU}	V	1.7V to 3.6V					
SCL clock frequency	f_{SCL}	Hz	0 to 100k		0 to 400k		0 to 3.4M	
Hold time (repeated) START condition.	$t_{HD,STA}$	µs	4	-	0.6	-	0.16	-
LOW period of the SCL clock	t_{LOW}	µs	4.7	-	1.3	-	0.16	-
HIGH period of the SCL clock	t_{HIGH}	µs	4	-	0.6	-	0.06	-
Set-up time for a repeated START condition	$t_{SU,STA}$	µs	4.7	-	0.6	-	0.16	-
DATA in Hold time	$t_{HD;DI}$	ns	0	900	0	900	0	70
DATA out Hold time	$t_{HD;DO}$	ns		900		900		70
Data set-up time	$t_{SU;DAT}$	ns	250	-	100	-	10	-
Rise time of both SDA and SCL signals	t_r	ns	-	1000	5	300	5	40
Fall time of both SDA and SCL signals	t_f	ns	-	300	5	300	5	40
Set-up time for STOP condition	$t_{SU;STO}$	µs	4	-	0.6	-	0.16	1
Bus free time between STOP and START Conditions	t_{BUF}	µs	4.7	-	1.3	-	-	-

Capacitive load for each bus line	C_b	pF	-	400	-	400	-	100
Low Level Input Voltage	V_{IL}	V	-	0.4	-	0.4	-	0.4
High Level Input Voltage	V_{IH}	V	1.4	-	1.4	-	1.4	-

I²C Device Address

When communicating with multiple devices using the I²C interface, each device must have its own unique address so the host can distinguish between the devices. The device slave address is <0100101x> where 'x' is the read/write control bit.

START and STOP Conditions

The START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition. The I²C master always generates the START and STOP conditions.

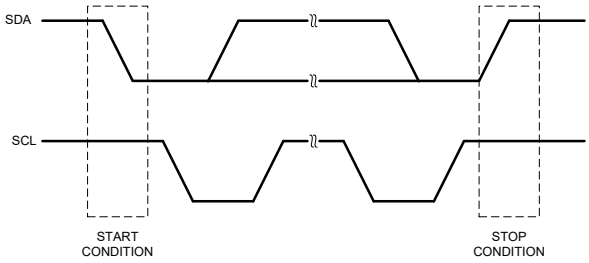


Figure 28. Start and Stop Conditions

Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

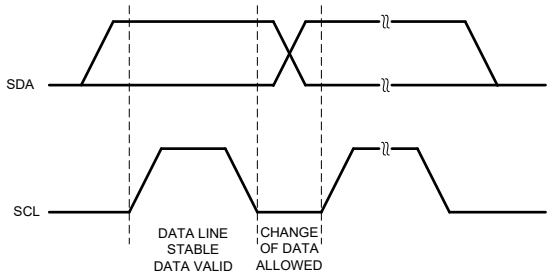


Figure 29. Data Validity

Acknowledge

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the master sends 7-slave address bits and an R/$\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.

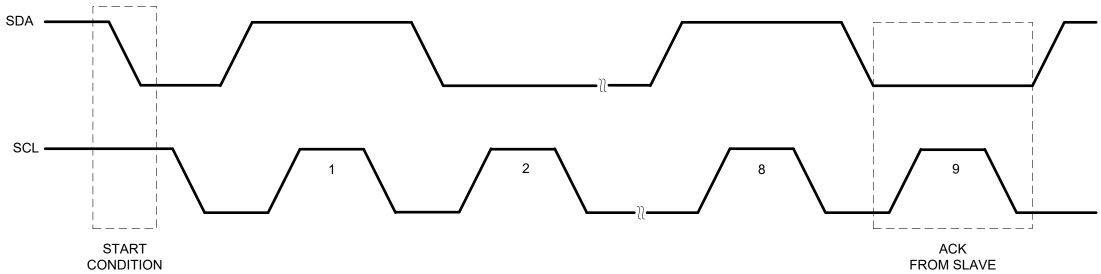


Figure 30. I²C Acknowledge

PMIC I²C Protocol

<table>
<tr><td rowspan="2">Write operation</td><td rowspan="2">Start</td><td colspan="7">Device address</td><td>R/W</td><td>ACK</td><td>Byte address</td><td>ACK</td><td rowspan="2" colspan="11">N-bytes DATA</td><td>ACK</td><td rowspan="2">STOP</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>N-bytes address</td><td>0</td><td>0</td></tr>
<tr><td rowspan="2">Read operation</td><td rowspan="2">Start</td><td colspan="7">Device address</td><td>R/W</td><td>ACK</td><td>Byte address</td><td>ACK</td><td rowspan="2">Repeated Start</td><td colspan="7">Device address</td><td>R/W</td><td>ACK</td><td rowspan="2">N-bytes DATA</td><td>ACK</td><td rowspan="2">STOP</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>N-bytes address</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
</table>

- Data is written from the address that mentioned in the second byte as much as following N-bytes.

 (ACK is occurred every 1-bytes)

- Data is read from the address that mentioned in the second byte to N-bytes address.

 (ACK is occurred every 1-bytes)

Register Description

Address	D7	D6	D5	D4	D3	D2	D1	D0
0x00h	x	x	B1_VSET					
0x01h	x	B2_VSET						
0x02h	x	B3_VSET0						
0x03h	x	B3_VSET1						
0x04h	x	B4_Add	B4_Mode	B4_VSET				
0x05h	x	LDO1_Mode	LDO1_VSET					
0x06h	x	x	LDO2_VSET					
0x07h	x	x	LDO2_CH_EN	LDO1_CH_EN	Buck4_CH_EN	Buck3_CH_EN	Buck2_CH_EN	Buck1_CH_EN
0x08h	B2_VID、B3_VID@SLEEP_EN	EXT_EN_SLEEP_EN	LDO2_SLEEP_EN	LDO1_SLEEP_EN	Buck4_SLEEP_EN	Buck3_SLEEP_EN	Buck2_SLEEP_EN	Buck1_SLEEP_EN
0x09h	B2_VID、B3_VID@DPSLP_EN	EXT_EN_DPSLP_EN	LDO2_DPSLP_EN	LDO1_DPSLP_EN	Buck4_DPSLP_EN	Buck3_DPSLP_EN	Buck2_DPSLP_EN	Buck1_DPSLP_EN
0x0Ah	x	x	x	x	B4_PWM_EN	B3_PWM_EN	B2_PWM_EN	B1_PWM_EN
0x0Bh	x	x	LDO2_SST	LDO1_SST	B4_SST	B3_SST	B2_SST	B1_SST
0x0Ch	Buck1_Power OFF_DLY		Buck2_Power OFF_DLY		Buck3_Power OFF_DLY		Buck4_Power OFF_DLY	
0x0Dh	LDO1_Power OFF_DLY		LDO2_Power OFF_DLY		EXT_EN_Power OFF_DLY		nRESET_Power OFF_DLY	
0x0Eh	Buck1_Wake Up_DLY		Buck2_Wake Up_DLY		Buck3_Wake Up_DLY		Buck4_Wake Up_DLY	
0x0Fh	x	x	LDO1_Wake Up_DLY		LDO2_Wake Up_DLY		EXT_EN_Wake Up_DLY	
0x10h	DIS_OVUV	DIS_OTP	DIS_VNOVP	x	x	x	SLEEP_EN	DPSLP_EN
0x11h	B1_Power ON_DLY				B2_Power ON_DLY			
0x12h	B3_Power ON_DLY				B4_Power ON_DLY			
0x13h	LDO1_Power ON_DLY				LDO2_Power ON_DLY			
0x14h	nRESET_Input Trigger	nRESET_Power ON_DLY			EXT_EN_ Power ON_DLY			
0x15h	GPIO5 function		GPIO7 function		x	GPIO6 Lock	GPIO5 Open drain	GPIO7 Open drain
0x18h	x	B2_VSET1						
0x19h	x	B2_VSET2						
0x1Ah	x	B3_VSET2						
0x34h	x	x	x	Vendor ID	CMI Version			

Fault Register Map

Address	D7	D6	D5	D4	D3	D2	D1	D0
0x16h	TSP	VIN_ OVP	LDO2_ OVP	LDO1_ OVP	Buck4_ OVP	Buck3_ OVP	Buck2_ OVP	Buck1_ OVP
0x17h	x	SYSWARN	LDO2_ UVP(SCP)	LDO1_ UVP(SCP)	Buck4_ UVP(SCP)	Buck3_ UVP(SCP)	Buck2_ UVP(SCP)	Buck1_ UVP(SCP)

Note: The fault bit is latched status bit and keep asserted until read by I^2C.

Register Address Map

Address	Register	Default GPIO2 =High	Default GPIO2 =Floating	Default GPIO2 =Low	EEPROM Bit	Range	Resolution
0x00h	B1_VSET [5:0]	2.6V/28h	2.5V/24h	2.5V/24h	6bits	Buck1 output range is 1.6V-3.0V	25mV
0x01h	B2_VSET0 [6:0]	0.91V/29h	0.91V/29h	1.2V/46h	7bits	Buck2 output range is 0.5V-1.6V	10mV
0x18h	B2_VSET1 [6:0]	0.91V/29h	0.91V/29h	1.2V/46h	7bits	Buck2 output range is 0.5V-1.6V	10mV
0x19h	B2_VSET2 [6:0]	0.91V/29h	0.91V/29h	1.2V/46h	7bits	Buck2 output range is 0.5V-1.6V	10mV

Address	Register	Default GPIO3 =High	Default GPIO3 =Floating	Default GPIO3 =Low	EEPROM Bit	Range	Resolution
0x02h	B3_VSET0 [6:0]	0.78V/1Ch	0.78V/1Ch	0.78V/1Ch	7bits	Buck3 output range is 0.5V-1.2V	10mV
0x03h	B3_VSET1 [6:0]	0.78V/1Ch	0.78V/1Ch	0.78V/1Ch	7bits	Buck3 output range is 0.5V-1.2V	10mV
0x1Ah	B3_VSET2 [6:0]	0.78V/1Ch	0.78V/1Ch	0.78V/1Ch	7bits	Buck3 output range is 0.5V-1.2V	10mV
0x11h	B1_Power ON_DLY [7:4]	3.5ms/07h	3.0ms/06h	3.0ms/06h	4bits	0000: 0ms, 0001: 0.5ms, …. 1110: 7.0ms, 1111: 7.5ms	0.5ms
	B2_Power ON_DLY [3:0]	0.5ms/01h	0.5ms/01h	0.5ms/01h	4bits	0000: 0ms, 0001: 0.5ms, …. 1110: 7.0ms, 1111: 7.5ms	0.5ms
0x12h	B3_Power ON_DLY [7:4]	0.5ms/01h	0.5ms/01h	0.0ms/00h	4bits	0000: 0ms, 0001: 0.5ms, …. 1110: 7.0ms, 1111: 7.5ms	0.5ms
	B4_Power ON_DLY [3:0]	3.0ms/06h	3.5ms/07h	1.5ms/03h	4bits	0000: 0ms, 0001: 0.5ms, …. 1110: 7.0ms, 1111: 7.5ms	0.5ms
0x13h	LDO1_Power ON_DLY [7:4]	2.0ms/04h	2.0ms/04h	2.0ms/04h	4bits	0000: 0ms, 0001: 0.5ms, …. 1110: 7.0ms, 1111: 7.5ms	0.5ms
	LDO2_Power ON_DLY [3:0]	2.0ms/04h	2.0ms/04h	2.0ms/04h	4bits	0000: 0ms, 0001: 0.5ms, …. 1110: 7.0ms, 1111: 7.5ms	0.5ms
0x14h	nRESET_ Input Trigger [7]	SYS_OK/ 01h	SYS_OK/ 01h	SYS_OK/ 01h	1bit	0: Buck2_PG 1: SYS_OK	-
	nRESET_ Power ON_ DLY [6:4]	8.0ms/04h	8.0ms/04h	8.0ms/04h	3bits	000: 0.5ms, 001: 1.0ms, 010: 2.0ms, 011: 4.0ms, 100: 8.0ms, 101: 16.0ms	-
	EXT_EN_ Power ON_ DLY [3:0]	1.5ms/03h	1.5ms/03h	1.5ms/03h	4bits	0000: 0ms, 0001: 0.5ms, …. 1110: 7.0ms, 1111: 7.5ms	0.5ms

Address	Register	Default GPIO4 =High	Default GPIO4 =Floating	Default GPIO4 =Low	EEPROM Bit	Range	Resolution
0x04h	B4_Add [6]	0mV/00h	0mV/00h	0mV/00h	1bit	0 – Buck4 output voltage increase ΔV_{OUT4}=0mV 1 – Buck4 output voltage increase ΔV_{OUT4}=24mV	
	B4_Mode [5]	Buck/00h	Buck/00h	LDO/01h	1bit	0 – Buck4 operating on Buck mode 1 – Buck4 operating on LDO mode	-
	B4_VSET [4:0]	1.1V/04h	1.2V/06h	1.8V/12h	5bits	Buck4 output range is 0.9V-2.0V	50mV
0x05h	LDO1_Mode [6]	LDO/00h	LDO/00h	PLSW/01h	1bit	00h: LDO Mode, 01h: PLSW Mode,	-
	LDO1_VSET [5:0]	1.8V/10h	1.8V/10h	1.8V/10h	6bits	LDO1 output range is 1.0V-2.7V	50mV

Address	Register	Default	EEPROM Bit	Range	Resolution
0x06h	LDO2_VSET [5:0]	1.8V/10h	6bits	LDO2 output range is 1.0V-2.7V	50mV
0x07h	LDO2_CH_EN[5]	Enable/01h	1bit	0 – LDO2 Disable 1 – LDO2 Enable.	-
	LDO1_CH_EN[4]	Enable/01h	1bit	0 – LDO1 Disable, 1 – LDO1 Enable.	-
	Buck4_CH_EN[3]	Enable/01h	1bit	0 – Buck4 Disable, 1 –Buck4 Enable.	-
	Buck3_CH_EN[2]	Enable/01h	1bit	0 –Buck3 Disable, 1 –Buck3 Enable.	-
	Buck2_CH_EN[1]	Enable/01h	1bit	0 –Buck2 Disable, 1 –Buck2 Enable.	-
	Buck1_CH_EN[0]	Enable/01h	1bit	0 –Buck1 Disable, 1 –Buck1 Enable.	-
0x08h	B2_VID、B3_VID@SLEEP_EN [7]	Enable/01h	1bit	0 – Buck2 and Buck3 disable VID function; Buck3 output keep VSET0 when the IC enters Sleep mode 1 –Buck2 and Buck3 enable VID function; Buck3 output change to VSET1 when the IC enters Sleep mode	-
	EXT_EN_SLEEP_EN [6]	Stays on/00h	1bit	0 – EXT_EN stays on when the IC enters Sleep mode 1 – EXT_EN turns off when the IC enters Sleep mode	-
	LDO2_SLEEP_EN [5]	Stays on/00h	1bit	0 – LDO2 stays on when the IC enters Sleep mode 1 – LDO2 turns off when the IC enters Sleep mode	-
	LDO1_SLEEP_EN [4]	Stays on/00h	1bit	0 – LDO1 stays on when the IC enters Sleep mode 1 – LDO1 turns off when the IC enters Sleep mode	-
	Buck4_SLEEP_EN [3]	Stays on/00h	1bit	0 – Buck4 stays on when the IC enters Sleep mode 1 – Buck4 turns off when the IC enters Sleep mode	-
	Buck3_SLEEP_EN [2]	Stays on/00h	1bit	0 – Buck3 stays on when the IC enters Sleep mode 1 – Buck3 turns off when the IC enters Sleep mode	-
	Buck2_SLEEP_EN [1]	Stays on/00h	1bit	0 – Buck2 stays on when the IC enters Sleep mode 1 – Buck2 turns off when the IC enters Sleep mode	-
	Buck1_SLEEP_EN [0]	Stays on/00h	1bit	0 – Buck1 stays on when the IC enters Sleep mode 1 – Buck1 turns off when the IC enters Sleep mode	-

Address	Register	Default	EEPROM Bit	Range	Resolution
0x09h	B2_VID、B3_VID@DPSLP_EN [7]	Enable/01h	1bit	0 –Buck2 and Buck3 disable VID function; Buck2 and Buck3 output keep VSET0 when the IC enters deep sleep mode 1 –Buck2 and Buck3 enable VID function; Buck2 and Buck3 output change to VSET2 when the IC enters deep sleep mode	
	EXT_EN_DPSLP_EN [6]	Stays on/00h	1bit	0 – EXT_EN stays on when the IC enters Deep Sleep mode 1 – EXT_EN turns off when the IC enters Deep Sleep mode	-
	LDO2_ DPSLP_EN [5]	Stays on/00h	1bit	0 – LDO2 stays on when the IC enters Deep Sleep mode 1 – LDO2 turns off when the IC enters Deep Sleep mode	-
	LDO1_ DPSLP_EN [4]	Stays on/00h	1bit	0 – LDO1 stays on when the IC enters Deep Sleep mode 1 – LDO1 turns off when the IC enters Deep Sleep mode	-
	Buck4_ DPSLP_EN [3]	Stays on/00h	1bit	0 – Buck4 stays on when the IC enters Deep Sleep mode 1 – Buck4 turns off when the IC enters Deep Sleep mode	-
	Buck3_ DPSLP_EN [2]	Stays on/00h	1bit	0 – Buck3 stays on when the IC enters Deep Sleep mode 1 – Buck3 turns off when the IC enters Deep Sleep mode	-
	Buck2_ DPSLP_EN [1]	Stays on/00h	1bit	0 – Buck2 stays on when the IC enters Deep Sleep mode 1 – Buck2 turns off when the IC enters Deep Sleep mode	-
	Buck1_ DPSLP_EN [0]	Stays on/00h	1bit	0 – Buck1 stays on when the IC enters Deep Sleep mode 1 – Buck1 turns off when the IC enters Deep Sleep mode	-
0x0Ah	B4_PWM_EN [3]	LPM/00h	1bit	0 – Buck4 enters LPM at light load 1 – Buck4 forced into PWM at light load	-
	B3_PWM_EN [2]	LPM/00h	1bit	0 – Buck3 enters LPM at light load 1 – Buck3 forced into PWM at light load	-
	B2_PWM_EN [1]	LPM/00h	1bit	0 – Buck2 enters LPM at light load 1 – Buck2 forced into PWM at light load	-
	B1_PWM_EN [0]	LPM/00h	1bit	0 – Buck1 enters LPM at light load 1 – Buck1 forced into PWM at light load	-
0x0Bh	LDO2_SST [5]	200μs/00h	1bit	0 – LDO2 SST=200μs 1 – LDO2 SST=360μs	160μs
	LDO1_SST [4]	200μs/00h	1bit	0 – LDO1 SST=200μs 1 – LDO1 SST=360μs	160μs
	B4_SST [3]	250μs/00h	1bit	0 – Buck4 SST=250μs 1 – Buck4 SST=500μs	250μs
	B3_SST [2]	250μs/00h	1bit	0 – Buck3 SST=250μs 1 – Buck3 SST=500μs	250μs
	B2_SST [1]	250μs/00h	1bit	0 – Buck2 SST=250μs 1 – Buck2 SST=500μs	250μs
	B1_SST [0]	250μs/00h	1bit	0 – Buck1 SST=250μs 1 – Buck1 SST=500μs	250μs

Address	Register	Default	EEPROM Bit	Range	Resolution
0x0Ch	Buck1_Power OFF_DLY [7:6]	0ms/00h	2bits	00: 0ms, 01: 0.25ms, 10: 0.5ms, 11: 1.0ms	-
	Buck2_Power OFF_DLY [5:4]	0ms/00h	2bits	00: 0ms, 01: 0.25ms, 10: 0.5ms, 11: 1.0ms	-
	Buck3_Power OFF_DLY [3:2]	0ms/00h	2bits	00: 0ms, 01: 0.25ms, 10: 0.5ms, 11: 1.0ms	-
	Buck4_Power OFF_DLY [1:0]	0ms/00h	2bits	00: 0ms, 01: 0.25ms, 10: 0.5ms, 11: 1.0ms	-

0x0Dh	LDO1_ Power OFF_ DLY [7:6]	0ms/00h	2bits	00: 0ms, 01: 0.25ms, 10: 0.5ms, 11: 1.0ms	-
	LDO2_Power OFF_ DLY [5:4]	0ms/00h	2bits	00: 0ms, 01: 0.25ms, 10: 0.5ms, 11: 1.0ms	-
	EXT _EN _Power OFF_ DLY [3:2]	0ms/00h	2bits	00: 0ms, 01: 0.25ms, 10: 0.5ms, 11: 1.0ms	-
	nRESET_ Power OFF_ DLY [1:0]	0ms/00h	2bits	00: 0ms, 01: 0.25ms, 10: 0.5ms, 11: 1.0ms	-
0x0Eh	Buck1Wake Up_ DLY [7:6]	0ms/00h	2bits	00: 0ms, 01: 0.5ms, 10: 1.0ms, 11: 1.5ms	-
	Buck2_Wake Up_ DLY [5:4]	1ms/02h	2bits	00: 0ms, 01: 0.5ms, 10: 1.0ms, 11: 1.5ms	-
	Buck3_Wake Up_ DLY [3:2]	0ms/00h	2bits	00: 0ms, 01: 0.5ms, 10: 1.0ms, 11: 1.5ms	-
	Buck4_Wake Up_ DLY [1:0]	0ms/00h	2bits	00: 0ms, 01: 0.5ms, 10: 1.0ms, 11: 1.5ms	-
0x0Fh	LDO1_Wake Up_ DLY [5:4]	0ms/00h	2bits	00: 0ms, 01: 0.5ms, 10: 1.0ms, 11: 1.5ms	
	LDO2_Wake Up_ DLY [3:2]	0ms/00h	2bits	00: 0ms, 01: 0.5ms, 10: 1.0ms, 11: 1.5ms	
	EXT_EN_ Wake Up_ DLY [1:0]	0ms/00h	2bits	00: 0ms, 01: 0.5ms, 10: 1.0ms, 11: 1.5ms	
0x10h	DIS_OVUV [7]	Enable/00h	1bit	0 – Enable hiccup mode or OVUVFLT state in ACTIVE Mode 1 – Disable hiccup mode or OVUVFLT state in ACTIVE Mode	-
	DIS_OTP [6]	Enable/00h	1bit	0 – Enable OTP 1 – Disable OTP	-
	DIS_VINOVP [5]	Enable/00h	1bit	0 – Enable VINOVP 1 – Disable VINOVP	-
	SLEEP_EN [1]	Enable/01h	1bit	0 – SLEEP Mode is disabled 1 – SLEEP Mode is enabled	-
	DPSLP_EN [0]	Enable/01h	1bit	0 – DPSLP Mode is disabled 1 – DPSLP Mode is enabled	-

Address	Register	Default	EEPROM Bit	Range	Resolution
0x15h	GPIO5 Function [7:6]	DPSLP/00h	2bits	00: DPSLP Input. 01: I²C Controlled Output. 10: nIRQ(SYSWARN) Output	-
	GPIO7 Function [5:4]	I²C IO/01h	2bits	00: EXT_EN Output. 01: I²C Controlled Output. 10: PWRDIS Input	-
	GPIO6 Lock [2]	Lock/01h	1bit	0-GPIO6 status not lock and LDO2 mode can be changed when GPIO6 status change after power on (Not recommended due to trigger protection). 1-GPIO6 status lock and LDO mode will not change with GPIO6 status after power on.	-
	GPIO5 Open drain [1]	Turn off/00h	1bit	0 – Open drain turn off 1 – Open drain turn on	-
	GPIO7 Open drain [0]	Turn off/00h	1bit	0 – Open drain turn off 1 – Open drain turn on	-
0x34h	Vendor ID [4]	0x01	1bit	01h	-

	CMI Version [3:0]	0x100	4bits	04h	-

Fault Flag

Address	Register	Default	EEPROM Bit	Range	Resolution
0x16h	TSP [7]	Normal/00h	1bit	Thermal shutdown protection indicator. 0: Normal (default) 1: Fault	-
	VIN_OVP [6]	Normal/00h	1bit	Input over voltage protection indicator 0: Normal (default) 1: Fault	-
	LDO2_OVP [5]	Normal/00h	1bit	LDO2 over voltage protection indicator 0: Normal (default) 1: Fault	-
	LDO1_OVP [4]	Normal/00h	1bit	LDO1 over voltage protection indicator 0: Normal (default) 1: Fault	-
	Buck4_OVP [3]	Normal/00h	1bit	Buck4 over voltage protection indicator 0: Normal (default) 1: Fault	-
	Buck3_OVP [2]	Normal/00h	1bit	Buck3 over voltage protection indicator 0: Normal (default) 1: Fault	-
	Buck2_OVP [1]	Normal/00h	1bit	Buck2 over voltage protection indicator 0: Normal (default) 1: Fault	-
	Buck1_OVP [0]	Normal/00h	1bit	Buck1 over voltage protection indicator 0: Normal (default) 1: Fault	-
0x17h	SYSWARN [6]	Normal/00h	1bit	SYSWARN indicator 0: Normal (default) 1: Fault	-
	LDO2_UVP(SCP) [5]	Normal/00h	1bit	LDO2 over load protection indicator 0: Normal (default) 1: Fault	-
	LDO1_UVP(SCP) [4]	Normal/00h	1bit	LDO1 over load protection indicator 0: Normal (default) 1: Fault	-
	Buck4_UVP(SCP) [3]	Normal/00h	1bit	Buck4 over load protection indicator 0: Normal (default) 1: Fault	-
	Buck3_UVP(SCP) [2]	Normal/00h	1bit	Buck3 over load protection indicator 0: Normal (default) 1: Fault	-
	Buck2_UVP(SCP) [1]	Normal/00h	1bit	Buck2 over load protection indicator 0: Normal (default) 1: Fault	-
	Buck1_UVP(SCP) [0]	Normal/00h	1bit	Buck1 over load protection indicator 0: Normal (default) 1: Fault	-

Buck1 Output Voltage Adjustment

Address – 0x00h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	RFU	B1_VSET					
READ/WRITE	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck1 Output Voltage VSET [5:0]
The output voltage is equal to B1_VSET*0.025+1.6V.

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
00h	1.6V	10h	2V	20h	2.4V	30h	2.8V
01h	1.625V	11h	2.025V	21h	2.425V	31h	2.825V
02h	1.65V	12h	2.05V	22h	2.45V	32h	2.85V
03h	1.675V	13h	2.075V	23h	2.475V	33h	2.875V
04h	1.7V	14h	2.1V	24h	2.5V	34h	2.9V
05h	1.725V	15h	2.125V	25h	2.525V	35h	2.925V
06h	1.75V	16h	2.15V	26h	2.55V	36h	2.95V
07h	1.775V	17h	2.175V	27h	2.575V	37h	2.975V
08h	1.8V	18h	2.2V	28h	2.6V	38h	3V
09h	1.825V	19h	2.225V	29h	2.625V	-	-
0Ah	1.85V	1Ah	2.25V	2Ah	2.65V	-	-
0Bh	1.875V	1Bh	2.275V	2Bh	2.675V	-	-
0Ch	1.9V	1Ch	2.3V	2Ch	2.7V	-	-
0Dh	1.925V	1Dh	2.325V	2Dh	2.725V	-	-
0Eh	1.95V	1Eh	2.35V	2Eh	2.75V	-	-
0Fh	1.975V	1Fh	2.375V	2Fh	2.775V	-	-

Buck2 Output Voltage Adjustment

Address – 0x01h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	B2_VSET0						
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

The output voltage is equal to B2_VSET*0.01+0.5V

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
00h	0.5V	20h	0.82V	40h	1.14V	60h	1.46V
01h	0.51V	21h	0.83V	41h	1.15V	61h	1.47V
02h	0.52V	22h	0.84V	42h	1.16V	62h	1.48V
03h	0.53V	23h	0.85V	43h	1.17V	63h	1.49V
04h	0.54V	24h	0.86V	44h	1.18V	64h	1.5V
05h	0.55V	25h	0.87V	45h	1.19V	65h	1.51V
06h	0.56V	26h	0.88V	46h	1.2V	66h	1.52V
07h	0.57V	27h	0.89V	47h	1.21V	67h	1.53V
08h	0.58V	28h	0.9V	48h	1.22V	68h	1.54V
09h	0.59V	29h	0.91V	49h	1.23V	69h	1.55V
0Ah	0.6V	2Ah	0.92V	4Ah	1.24V	6Ah	1.56V
0Bh	0.61V	2Bh	0.93V	4Bh	1.25V	6Bh	1.57V
0Ch	0.62V	2Ch	0.94V	4Ch	1.26V	6Ch	1.58V
0Dh	0.63V	2Dh	0.95V	4Dh	1.27V	6Dh	1.59V
0Eh	0.64V	2Eh	0.96V	4Eh	1.28V	6Eh	1.6V
0Fh	0.65V	2Fh	0.97V	4Fh	1.29V		
10h	0.66V	30h	0.98V	50h	1.3V		
11h	0.67V	31h	0.99V	51h	1.31V		
12h	0.68V	32h	1.0V	52h	1.32V		
13h	0.69V	33h	1.01V	53h	1.33V		
14h	0.70V	34h	1.02V	54h	1.34V		
15h	0.71V	35h	1.03V	55h	1.35V		
16h	0.72V	36h	1.04V	56h	1.36V		
17h	0.73V	37h	1.05V	57h	1.37V		
18h	0.74V	38h	1.06V	58h	1.38V		
19h	0.75V	39h	1.07V	59h	1.39V		
1Ah	0.76V	3Ah	1.08V	5Ah	1.8V		
1Bh	0.77V	3Bh	1.09V	5Bh	1.41V		
1Ch	0.78V	3Ch	1.1V	5Ch	1.42V		
1Dh	0.79V	3Dh	1.11V	5Dh	1.43V		
1Eh	0.8V	3Eh	1.12V	5Eh	1.44V		
1Fh	0.81V	3Fh	1.13V	5Fh	1.45V		

Buck3 Output Voltage Adjustment

Address – 0x02h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	B3_VSET0						
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

The output voltage is equal to B3_VSET*0.01+0.5V

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
00h	0.50V	14h	0.70V	28h	0.90V	3Ch	1.10V
01h	0.51V	15h	0.71V	29h	0.91V	3Dh	1.11V
02h	0.52V	16h	0.72V	2Ah	0.92V	3Eh	1.12V
03h	0.53V	17h	0.73V	2Bh	0.93V	3Fh	1.13V
04h	0.54V	18h	0.74V	2Ch	0.94V	40h	1.14V
05h	0.55V	19h	0.75V	2Dh	0.95V	41h	1.15V
06h	0.56V	1Ah	0.76V	2Eh	0.96V	42h	1.16V
07h	0.57V	1Bh	0.77V	2Fh	0.97V	43h	1.17V
08h	0.58V	1Ch	0.78V	30h	0.98V	44h	1.18V
09h	0.59V	1Dh	0.79V	31h	0.99V	45h	1.19V
0Ah	0.60V	1Eh	0.80V	32h	1.00V	46h	1.20V
0Bh	0.61V	1Fh	0.81V	33h	1.01V		
0Ch	0.62V	20h	0.82V	34h	1.02V		
0Dh	0.63V	21h	0.83V	35h	1.03V		
0Eh	0.64V	22h	0.84V	36h	1.04V		
0Fh	0.65V	23h	0.85V	37h	1.05V		
10h	0.66V	24h	0.86V	38h	1.06V		
11h	0.67V	25h	0.87V	39h	1.07V		
12h	0.68V	26h	0.88V	3Ah	1.08V		
13h	0.69V	27h	0.89V	3Bh	1.09V		

Buck3 Output Voltage Adjustment

Address – 0x03h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	B3_VSET1						
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

The output voltage is equal to B3_VSET*0.01+0.5V

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
00h	0.50V	15h	0.71V	2Ah	0.92V	3Fh	1.13V
01h	0.51V	16h	0.72V	2Bh	0.93V	40h	1.14V
02h	0.52V	17h	0.73V	2Ch	0.94V	41h	1.15V
03h	0.53V	18h	0.74V	2Dh	0.95V	42h	1.16V
04h	0.54V	19h	0.75V	2Eh	0.96V	43h	1.17V
05h	0.55V	1Ah	0.76V	2Fh	0.97V	44h	1.18V
06h	0.56V	1Bh	0.77V	30h	0.98V	45h	1.19V
07h	0.57V	1Ch	0.78V	31h	0.99V	46h	1.20V
08h	0.58V	1Dh	0.79V	32h	1.00V		
09h	0.59V	1Eh	0.80V	33h	1.01V		
0Ah	0.60V	1Fh	0.81V	34h	1.02V		
0Bh	0.61V	20h	0.82V	35h	1.03V		
0Ch	0.62V	21h	0.83V	36h	1.04V		
0Dh	0.63V	22h	0.84V	37h	1.05V		
0Eh	0.64V	23h	0.85V	38h	1.06V		
0Fh	0.65V	24h	0.86V	39h	1.07V		
10h	0.66V	25h	0.87V	3Ah	1.08V		
11h	0.67V	26h	0.88V	3Bh	1.09V		
12h	0.68V	27h	0.89V	3Ch	1.10V		
13h	0.69V	28h	0.90V	3Dh	1.11V		
14h	0.70V	29h	0.91V	3Eh	1.12V		

Buck4 Output Voltage Adjustment

Address – 0x04h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	B4_Add	B4_Mode	B4_VSET				
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck4 Output Voltage Increase ΔV_{OUT4} B4_Add [6]

Code	Buck4 Add
00h	Buck4 output voltage increase ΔV_{OUT4}=0mV
01h	Buck4 output voltage increase ΔV_{OUT4}=24mV

Set Buck4 Operating Mode B4_Mode [5]

Code	Buck4 Mode
00h	Buck4 operating on Buck mode
01h	Buck4 operating on LDO mode

Set Buck4 Output Voltage VSET [4:0]
The output voltage is equal to B4_VSET*0.05+0.9V

Code	Voltage	Code	Voltage	Code	Voltage
00h	0.90V	08h	1.30V	10h	1.70V
01h	0.95V	09h	1.35V	11h	1.75V
02h	1.00V	0Ah	1.40V	12h	1.80V
03h	1.05V	0Bh	1.45V	13h	1.85V
04h	1.10V	0Ch	1.50V	14h	1.90V
05h	1.15V	0Dh	1.55V	15h	1.95V
06h	1.20V	0Eh	1.60V	16h	2.00V
07h	1.25V	0Fh	1.65V	-	-

LDO1 Output Voltage Adjustment

Address – 0x05h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	LDO1_Mode	LDO1_VSET					
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO1 Mode [6]

Code	LDO1 Mode
00h	LDO1 operating on LDO mode
01h	LDO1 operating on PLSW mode

Set LDO Output Voltage VSET [5:0]
The output voltage is equal to LDO1_VSET*0.05+1.0V

Code	Voltage	Code	Voltage	Code	Voltage
00h	1.00V	10h	1.80V	20h	2.60V
01h	1.05V	11h	1.85V	21h	2.65V
02h	1.10V	12h	1.90V	22h	2.70V
03h	1.15V	13h	1.95V	-	-
04h	1.20V	14h	2.00V	-	-
05h	1.25V	15h	2.05V	-	-
06h	1.30V	16h	2.10V	-	-
07h	1.35V	17h	2.15V	-	-
08h	1.40V	18h	2.20V	-	-
09h	1.45V	19h	2.25V	-	-
0Ah	1.50V	1Ah	2.30V	-	-
0Bh	1.55V	1Bh	2.35V	-	-
0Ch	1.60V	1Ch	2.40V	-	-
0Dh	1.65V	1Dh	2.45V	-	-
0Eh	1.70V	1Eh	2.50V	-	-
0Fh	1.75V	1Fh	2.55V	-	-

LDO2 Output Voltage Adjustment

Address – 0x06h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	RFU	LDO2_VSET					
READ/WRITE	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO Output Voltage VSET [5:0]
The output voltage is equal to LDO2_VSET*0.05+1.0V

Code	Voltage	Code	Voltage	Code	Voltage
00h	1.00V	10h	1.80V	20h	2.60V
01h	1.05V	11h	1.85V	21h	2.65V
02h	1.10V	12h	1.90V	22h	2.70V
03h	1.15V	13h	1.95V	-	-
04h	1.20V	14h	2.00V	-	-
05h	1.25V	15h	2.05V	-	-
06h	1.30V	16h	2.10V	-	-
07h	1.35V	17h	2.15V	-	-
08h	1.40V	18h	2.20V	-	-
09h	1.45V	19h	2.25V	-	-
0Ah	1.50V	1Ah	2.30V	-	-
0Bh	1.55V	1Bh	2.35V	-	-
0Ch	1.60V	1Ch	2.40V	-	-
0Dh	1.65V	1Dh	2.45V	-	-
0Eh	1.70V	1Eh	2.50V	-	-
0Fh	1.75V	1Fh	2.55V	-	-

Rail ON/OFF Adjustment

Address – 0x07h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	RFU	LDO2_CH_EN	LDO1_CH_EN	Buck4_CH_EN	Buck3_CH_EN	Buck2_CH_EN	Buck1_CH_EN
READ/WRITE	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO2 Enable/Disable [5]

Code	LDO2 ON/OFF
00h	LDO2 is disable
01h	LDO2 is enable

Set LDO1 Enable/Disable [4]

Code	LDO1 ON/OFF
00h	LDO1 is disable
01h	LDO1 is enable

Set Buck4 Enable/Disable [3]

Code	Buck4 ON/OFF
00h	Buck4 is disable
01h	Buck4 is enable

Set Buck3 Enable/Disable [2]

Code	Buck3 ON/OFF
00h	Buck3 is disable
01h	Buck3 is enable

Set Buck2 Enable/Disable [1]

Code	Buck2 ON/OFF
00h	Buck2 is disable
01h	Buck2 is enable

Set Buck1 Enable/Disable [0]

Code	Buck1 ON/OFF
00h	Buck1 is disable
01h	Buck1 is enable

Rail ON/OFF Adjustment on SLEEP Mode and Buck3 VID Adjustment

Address – 0x08h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	B2_VID、B3_VID@ SLEEP_EN	EXT_EN_ SLEEP_EN	LDO2_ SLEEP_EN	LDO1_ SLEEP_EN	Buck4_ SLEEP_EN	Buck3_ SLEEP_EN	Buck2_ SLEEP_EN	Buck1_ SLEEP_EN
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck2 and Buck3 VID ON/OFF in Sleep Mode [7]

Code	Buck2 and Buck3 VID ON/OFF in Sleep Mode
00h	Buck2 and Buck3 disable VID function; Buck2 and Buck3 output keep VSET0 when the IC enters sleep mode
01h	Buck2 and Buck3 enable VID function; Buck2 and Buck3 output change to VSET1 when the IC enters sleep mode

Set EXT_EN ON/OFF in Sleep Mode [6]

Code	EXT_EN ON/OFF in Sleep Mode
00h	EXT_EN stays on when IC enters sleep mode
01h	EXT_EN turns off when IC enters sleep mode

Set LDO2 ON/OFF in Sleep Mode [5]

Code	LDO2 ON/OFF in Sleep Mode
00h	LDO2 stays on when IC enters sleep mode
01h	LDO2 turns off when IC enters sleep mode

Set LDO1 ON/OFF in Sleep Mode [4]

Code	LDO1 ON/OFF in Sleep Mode
00h	LDO1 stays on when IC enters sleep mode
01h	LDO1 turns off when IC enters sleep mode

Set Buck4 ON/OFF in Sleep Mode [3]

Code	Buck4 ON/OFF in Sleep Mode
00h	Buck4 stays on when IC enters sleep mode
01h	Buck4 turns off when IC enters sleep mode

Set Buck3 ON/OFF in Sleep Mode [2]

Code	Buck3 ON/OFF in Sleep Mode
00h	Buck3 stays on when IC enters sleep mode
01h	Buck3 turns off when IC enters sleep mode

Set Buck2 ON/OFF in Sleep Mode [1]

Code	Buck2 ON/OFF in Sleep Mode
00h	Buck2 stays on when IC enters sleep mode
01h	Buck2 turns off when IC enters sleep mode

Set Buck1 ON/OFF in Sleep Mode [0]

Code	Buck1 ON/OFF in Sleep Mode
00h	Buck1 stays on when IC enters sleep mode
01h	Buck1 turns off when IC enters sleep mode

Rail ON/OFF Adjustment on DPSLP Mode

Address – 0x09h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	B2_VID、B3_VID@ DPSLP_EN	EXT_EN_ DPSLP_EN	LDO2_ DPSLP_EN	LDO1_ DPSLP_EN	Buck4_ DPSLP_EN	Buck3_ DPSLP_EN	Buck2_ DPSLP_EN	Buck1_ DPSLP_EN
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck2 and Buck3 VID ON/OFF in Deep Sleep Mode [7]

Code	Buck2 and Buck3 VID ON/OFF in Deep Sleep Mode
00h	Buck2 and Buck3 disable VID function; Buck2 and Buck3 output keep VSET0 when the IC enters sleep mode
01h	Buck2 and Buck3 enable VID function; Buck2 and Buck3 output change to VSET1 when the IC enters sleep mode

Set EXT_EN ON/OFF in Deep Sleep Mode [6]

Code	EXT_EN ON/OFF in Deep Sleep Mode
00h	EXT_EN stays on when IC enters deep sleep mode
01h	EXT_EN turns off when IC enters deep sleep mode

Set LDO2 ON/OFF in Deep Sleep Mode [5]

Code	LDO2 ON/OFF in Deep Sleep Mode
00h	LDO2 stays on when IC enters deep sleep mode
01h	LDO2 turns off when IC enters deep sleep mode

Set LDO1 ON/OFF in Deep Sleep Mode [4]

Code	LDO1 ON/OFF in Deep Sleep Mode
00h	LDO1 stays on when IC enters deep sleep mode
01h	LDO1 turns off when IC enters deep sleep mode

Set Buck4 ON/OFF in Deep Sleep Mode [3]

Code	Buck4 ON/OFF in Deep Sleep Mode
00h	Buck4 stays on when IC enters deep sleep mode
01h	Buck4 turns off when IC enters deep sleep mode

Set Buck3 ON/OFF in Deep Sleep Mode [2]

Code	Buck3 ON/OFF in Deep Sleep Mode
00h	Buck3 stays on when IC enters deep sleep mode
01h	Buck3 turns off when IC enters deep sleep mode

Set Buck2 ON/OFF in Deep Sleep Mode [1]

Code	Buck2 ON/OFF in Deep Sleep Mode
00h	Buck2 stays on when IC enters deep sleep mode
01h	Buck2 turns off when IC enters deep sleep mode

Set Buck1 ON/OFF in Deep Sleep Mode [0]

Code	Buck1 ON/OFF in Sleep Mode

00h	Buck1 stays on when IC enters deep sleep mode
01h	Buck1 turns off when IC enters deep sleep mode

PWM ON/OFF

Address – 0x0Ah

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	RFU	RFU	RFU	B4_PWM_EN	B3_PWM_EN	B2_PWM_EN	B1_PWM_EN
READ/WRITE	R	R	R	R	R/W	R/W	R/W	R/W

Description

Set Buck4 LPM/FCCM [3]

Code	Buck4 LPM/FCCM Selection
00h	Buck4 enters LPM at light load
01h	Buck4 forced into PWM at light load

Set Buck3 PM/FCCM [2]

Code	Buck3 LPM/FCCM Selection
00h	Buck3 enters LPM at light load
01h	Buck3 forced into PWM at light load

Set Buck2 PM/FCCM [1]

Code	Buck2 LPM/FCCM Selection
00h	Buck2 enters LPM at light load
01h	Buck2 forced into PWM at light load

Set Buck1 LPM/FCCM [0]

Code	Buck1 LPM/FCCM Selection
00h	Buck1 enters LPM at light load
01h	Buck1 forced into PWM at light load

Rail SST Adjustment

Address – 0x0Bh

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	RFU	LDO2_SST	LDO1_SST	B4_SST	B3_SST	B2_SST	B1_SST
READ/WRITE	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO2 Soft Start Time [5]

Code	LDO2 Soft Start Time
00h	200μs
01h	360μs

Set LDO1 Soft Start Time [4]

Code	LDO1 Soft Start Time
00h	200μs
01h	360μs

Set Buck4 Soft Start Time [3]

Code	Buck4 Soft Start Time
00h	250μs
01h	500μs

Set Buck3 Soft Start Time [2]

Code	Buck3 Soft Start Time
00h	250μs
01h	500μs

Set Buck2 Soft Start Time [1]

Code	Buck2 Soft Start Time
00h	250μs
01h	500μs

Set Buck1 Soft Start Time [0]

Code	Buck1 Soft Start Time
00h	250μs
01h	500μs

Rail Power off Delay Time Adjustment

Address – 0x0Ch

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Buck1_Power Off_ DLY		Buck2_Power Off_ DLY		Buck3_Power Off_ DLY		Buck4_Power Off_ DLY	
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck1 Power off Delay Time [7:6]

Code	Buck1 Power off Delay Time
00h	0ms
01h	0.25ms
02h	0.5ms
03h	1.0ms

Set Buck2 Power off Delay Time [5:4]

Code	Buck2 Power off Delay Time
00h	0ms
01h	0.25ms
02h	0.5ms
03h	1.0ms

Set Buck3 Power off Delay Time [3:2]

Code	Buck3 Power off Delay Time
00h	0ms
01h	0.25ms
02h	0.5ms
03h	1.0ms

Set Buck4 Power off Delay Time [1:0]

Code	Buck4 Power off Delay Time
00h	0ms
01h	0.25ms
02h	0.5ms
03h	1.0ms

Rail Power off Delay Time Adjustment

Address – 0x0Dh

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	LDO1_Power Off_ DLY		LDO2_Power Off_ DLY		EXT_EN_Power Off_ DLY		nRESET_Power Off_DLY	
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO1 Power off Delay Time [7:6]

Code	LDO1 Power off Delay Time
00h	0ms
01h	0.25ms
02h	0.5ms
03h	1.0ms

Set LDO2 Power off Delay Time [5:4]

Code	LDO2 Power off Delay Time
00h	0ms
01h	0.25ms
02h	0.5ms
03h	1.0ms

Set EXT_EN Power off Delay Time [3:2]

Code	EXT_EN Power off Delay Time
00h	0ms
01h	0.25ms
02h	0.5ms
03h	1.0ms

Set nRESET Power off Delay Time [1:0]

Code	nRESET Power off Delay Time
00h	0ms
01h	0.25ms
02h	0.5ms
03h	1.0ms

Rail Wake Up Delay Time Adjustment

Address – 0x0Eh

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Buck1_Wake Up_ DLY		Buck2_Wake Up_ DLY		Buck3_Wake Up_ DLY		Buck4_Wake Up_ DLY	
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck1 Wake Up Delay Time [7:6]

Code	Buck1 Wake Up Delay Time
00h	0ms
01h	0.5ms
02h	1.0ms
03h	1.5ms

Set Buck2 Wake Up Delay Time [5:4]

Code	Buck2 Wake Up Delay Time
00h	0ms
01h	0.5ms
02h	1.0ms
03h	1.5ms

Set Buck3 Wake Up Delay Time [3:2]

Code	Buck3 Wake Up Delay Time
00h	0ms
01h	0.5ms
02h	1.0ms
03h	1.5ms

Set Buck4 Wake Up Delay Time [1:0]

Code	Buck4 Wake Up Delay Time
00h	0ms
01h	0.5ms
02h	1.0ms
03h	1.5ms

Rail Wake up Delay Time Adjustment

Address – 0x0Fh

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	RFU	LDO1_Wake Up_ DLY		LDO2_Wake Up_ DLY		EXT_EN_Wake Up_DLY	
READ/WRITE	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO1 Wake Up Delay Time [5:4]

Code	LDO1 Wake Up Delay Time
00h	0ms
01h	0.5ms
02h	1.0ms
03h	1.5ms

Set LDO2 Wake Up Delay Time [3:2]

Code	LDO2 Wake Up Delay Time
00h	0ms
01h	0.5ms
02h	1.0ms
03h	1.5ms

Set EXT_EN Wake Up Delay Time [1:0]

Code	EXT_EN Wake Up Delay Time
00h	0ms
01h	0.5ms
02h	1.0ms
03h	1.5ms

Protection ON/OFF, and SLEEP/DPSLP Adjustment

Address – 0x10h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	DIS_OVUV	DIS_OTP	DIS_VINOVP	RFU	RFU	RFU	SLEEP_EN	DPSLP_EN
READ/WRITE	R/W	R/W	R/W	R	R	R	R/W	R/W

Description

Set OVUV Fault [7]

Code	OVUV Fault
00h	Enable hiccup mode or OVUVFLT state in ACTIVE Mode
01h	Disable hiccup mode or OVUVFLT state in AC-TIVE Mode

Set OTP [6]

Code	OTP
00h	Enable
01h	Disable

Set VINOVP [5]

Code	VIN_OVP
00h	Enable
01h	Disable

Set Sleep Mode EN [1]

Code	Sleep EN
00h	Sleep mode is disable
01h	Sleep mode is enable

Set Deep Sleep Mode EN [0]

Code	Deep Sleep EN
00h	Deep sleep mode is disable
01h	Deep sleep mode is enable

Power on Delay Time Adjustment

Address – 0x11h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	B1_Power ON_ DLY				B2_Power ON_ DLY			
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck1 Power on Delay Time [7:4]

Code	Buck1 Power on Delay Time	Code	Buck1 Power on Delay Time
00h	0ms	08h	4.0ms
01h	0.5ms	09h	4.5ms
02h	1.0ms	0Ah	5.0ms
03h	1.5ms	0Bh	5.5ms
04h	2.0ms	0Ch	6.0ms
05h	2.5ms	0Dh	6.5ms
06h	3.0ms	0Eh	7.0ms
07h	3.5ms	0Fh	7.5ms

Set Buck2 Power on Delay Time [3:0]

Code	Buck2 Power on Delay Time	Code	Buck2 Power on Delay Time
00h	0ms	08h	4.0ms
01h	0.5ms	09h	4.5ms
02h	1.0ms	0Ah	5.0ms
03h	1.5ms	0Bh	5.5ms
04h	2.0ms	0Ch	6.0ms
05h	2.5ms	0Dh	6.5ms
06h	3.0ms	0Eh	7.0ms
07h	3.5ms	0Fh	7.5ms

Power on Delay Time Adjustment

Address – 0x12h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	B3_Power ON_ DLY				B4_Power ON_ DLY			
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck3 Power on Delay Time [7:4]

Code	Buck3 Power on Delay Time	Code	Buck3 Power on Delay Time
00h	0ms	08h	4.0ms
01h	0.5ms	09h	4.5ms
02h	1.0ms	0Ah	5.0ms
03h	1.5ms	0Bh	5.5ms
04h	2.0ms	0Ch	6.0ms
05h	2.5ms	0Dh	6.5ms
06h	3.0ms	0Eh	7.0ms
07h	3.5ms	0Fh	7.5ms

Set Buck4 Power on Delay Time [3:0]

Code	Buck4 Power on Delay Time	Code	Buck4 Power on Delay Time
00h	0ms	08h	4.0ms
01h	0.5ms	09h	4.5ms
02h	1.0ms	0Ah	5.0ms
03h	1.5ms	0Bh	5.5ms
04h	2.0ms	0Ch	6.0ms
05h	2.5ms	0Dh	6.5ms
06h	3.0ms	0Eh	7.0ms
07h	3.5ms	0Fh	7.5ms

Power on Delay Time Adjustment

Address – 0x13h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	LDO1_Power ON_ DLY				LDO2_Power ON_ DLY			
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO1 Power on Delay Time [7:4]

Code	LDO1 Power on Delay Time	Code	LDO1 Power on Delay Time
00h	0ms	08h	4.0ms
01h	0.5ms	09h	4.5ms
02h	1.0ms	0Ah	5.0ms
03h	1.5ms	0Bh	5.5ms
04h	2.0ms	0Ch	6.0ms
05h	2.5ms	0Dh	6.5ms
06h	3.0ms	0Eh	7.0ms
07h	3.5ms	0Fh	7.5ms

Set LDO2 Power on Delay Time [3:0]

Code	LDO2 Power on Delay Time	Code	LDO2 Power on Delay Time
00h	0ms	08h	4.0ms
01h	0.5ms	09h	4.5ms
02h	1.0ms	0Ah	5.0ms
03h	1.5ms	0Bh	5.5ms
04h	2.0ms	0Ch	6.0ms
05h	2.5ms	0Dh	6.5ms
06h	3.0ms	0Eh	7.0ms
07h	3.5ms	0Fh	7.5ms

Power on Delay Time Adjustment

Address – 0x14h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	nRESET_ Input Trigger	nRESET_Power ON_ DLY			EXT_EN_Power ON_ DLY			
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set nRESET Input Trigger [7]

Code	nRESET Input Trigger
00h	Buck2_PG
01h	SYS_OK

Set nRESET Power on Delay Time [6:4]

Code	nRESET Power on Delay Time
00h	0.5ms
01h	1ms
02h	2ms
03h	4ms
04h	8ms
05h	16ms

Set EXT_EN Power on Delay Time [3:0]

Code	EXT_EN Power on Delay Time	Code	EXT_EN Power on Delay Time
00h	0ms	08h	4.0ms
01h	0.5ms	09h	4.5ms
02h	1.0ms	0Ah	5.0ms
03h	1.5ms	0Bh	5.5ms
04h	2.0ms	0Ch	6.0ms
05h	2.5ms	0Dh	6.5ms
06h	3.0ms	0Eh	7.0ms
07h	3.5ms	0Fh	7.5ms

GPIO5 and GPIO7 Adjustment

Address – 0x15h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	GPIO5 Function		GPIO7 Function		RFU	GPIO6 Lock	GPIO5 Open Drain	GPIO7 Open Drain
READ/WRITE	R/W	R/W	R/W	R/W	R	R	R/W	R/W

Description

Set GPIO5 Function [7:6]

Code	GPIO5 Function
00h	DPSLP Input
01h	I^2C Controlled Output
02h	nIRQ(SYSWARN) Output

Set GPIO7 Function [5:4]

Code	GPIO7 Function
00h	EXT_EN Output
01h	I^2C Controlled Output
02h	PWRDIS Input

Set GPIO6 Lock Function [2]

Code	GPIO6 Lock Function
00h	GPIO6 status not lock and LDO2 mode can be changed when GPIO6 status change after power on. (Not recommended due to trigger protection).
01h	GPIO6 status lock and LDO mode will not change with GPIO6 status after power on.

Set GPIO5 Open Drain ON/OFF [1]

Code	GPIO5 Open Drain ON/OFF
00h	Open drain turn off
01h	Open drain turn on

Set GPIO7 Open Drain ON/OFF [0]

Code	GPIO7 Open Drain ON/OFF
00h	Open drain turn off
01h	Open drain turn on

Buck2 Output Voltage Adjustment

Address – 0x18h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	B2_VSET1						
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

The output voltage is equal to B2_VSET1*0.01+0.5V

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
00h	0.5V	20h	0.82V	40h	1.14V	60h	1.46V
01h	0.51V	21h	0.83V	41h	1.15V	61h	1.47V
02h	0.52V	22h	0.84V	42h	1.16V	62h	1.48V
03h	0.53V	23h	0.85V	43h	1.17V	63h	1.49V
04h	0.54V	24h	0.86V	44h	1.18V	64h	1.5V
05h	0.55V	25h	0.87V	45h	1.19V	65h	1.51V
06h	0.56V	26h	0.88V	46h	1.2V	66h	1.52V
07h	0.57V	27h	0.89V	47h	1.21V	67h	1.53V
08h	0.58V	28h	0.9V	48h	1.22V	68h	1.54V
09h	0.59V	29h	0.91V	49h	1.23V	69h	1.55V
0Ah	0.6V	2Ah	0.92V	4Ah	1.24V	6Ah	1.56V
0Bh	0.61V	2Bh	0.93V	4Bh	1.25V	6Bh	1.57V
0Ch	0.62V	2Ch	0.94V	4Ch	1.26V	6Ch	1.58V
0Dh	0.63V	2Dh	0.95V	4Dh	1.27V	6Dh	1.59V
0Eh	0.64V	2Eh	0.96V	4Eh	1.28V	6Eh	1.6V
0Fh	0.65V	2Fh	0.97V	4Fh	1.29V		
10h	0.66V	30h	0.98V	50h	1.3V		
11h	0.67V	31h	0.99V	51h	1.31V		
12h	0.68V	32h	1.0V	52h	1.32V		
13h	0.69V	33h	1.01V	53h	1.33V		
14h	0.70V	34h	1.02V	54h	1.34V		
15h	0.71V	35h	1.03V	55h	1.35V		
16h	0.72V	36h	1.04V	56h	1.36V		
17h	0.73V	37h	1.05V	57h	1.37V		
18h	0.74V	38h	1.06V	58h	1.38V		
19h	0.75V	39h	1.07V	59h	1.39V		
1Ah	0.76V	3Ah	1.08V	5Ah	1.8V		
1Bh	0.77V	3Bh	1.09V	5Bh	1.41V		
1Ch	0.78V	3Ch	1.1V	5Ch	1.42V		
1Dh	0.79V	3Dh	1.11V	5Dh	1.43V		
1Eh	0.8V	3Eh	1.12V	5Eh	1.44V		
1Fh	0.81V	3Fh	1.13V	5Fh	1.45V		

Buck2 Output Voltage Adjustment

Address – 0x19h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	B2_VSET2						
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

The output voltage is equal to B2_VSET2*0.01+0.5V

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
00h	0.5V	20h	0.82V	40h	1.14V	60h	1.46V
01h	0.51V	21h	0.83V	41h	1.15V	61h	1.47V
02h	0.52V	22h	0.84V	42h	1.16V	62h	1.48V
03h	0.53V	23h	0.85V	43h	1.17V	63h	1.49V
04h	0.54V	24h	0.86V	44h	1.18V	64h	1.5V
05h	0.55V	25h	0.87V	45h	1.19V	65h	1.51V
06h	0.56V	26h	0.88V	46h	1.2V	66h	1.52V
07h	0.57V	27h	0.89V	47h	1.21V	67h	1.53V
08h	0.58V	28h	0.9V	48h	1.22V	68h	1.54V
09h	0.59V	29h	0.91V	49h	1.23V	69h	1.55V
0Ah	0.6V	2Ah	0.92V	4Ah	1.24V	6Ah	1.56V
0Bh	0.61V	2Bh	0.93V	4Bh	1.25V	6Bh	1.57V
0Ch	0.62V	2Ch	0.94V	4Ch	1.26V	6Ch	1.58V
0Dh	0.63V	2Dh	0.95V	4Dh	1.27V	6Dh	1.59V
0Eh	0.64V	2Eh	0.96V	4Eh	1.28V	6Eh	1.6V
0Fh	0.65V	2Fh	0.97V	4Fh	1.29V		
10h	0.66V	30h	0.98V	50h	1.3V		
11h	0.67V	31h	0.99V	51h	1.31V		
12h	0.68V	32h	1.0V	52h	1.32V		
13h	0.69V	33h	1.01V	53h	1.33V		
14h	0.70V	34h	1.02V	54h	1.34V		
15h	0.71V	35h	1.03V	55h	1.35V		
16h	0.72V	36h	1.04V	56h	1.36V		
17h	0.73V	37h	1.05V	57h	1.37V		
18h	0.74V	38h	1.06V	58h	1.38V		
19h	0.75V	39h	1.07V	59h	1.39V		
1Ah	0.76V	3Ah	1.08V	5Ah	1.8V		
1Bh	0.77V	3Bh	1.09V	5Bh	1.41V		
1Ch	0.78V	3Ch	1.1V	5Ch	1.42V		
1Dh	0.79V	3Dh	1.11V	5Dh	1.43V		
1Eh	0.8V	3Eh	1.12V	5Eh	1.44V		
1Fh	0.81V	3Fh	1.13V	5Fh	1.45V		

Buck3 Output Voltage Adjustment

Address – 0x1Ah

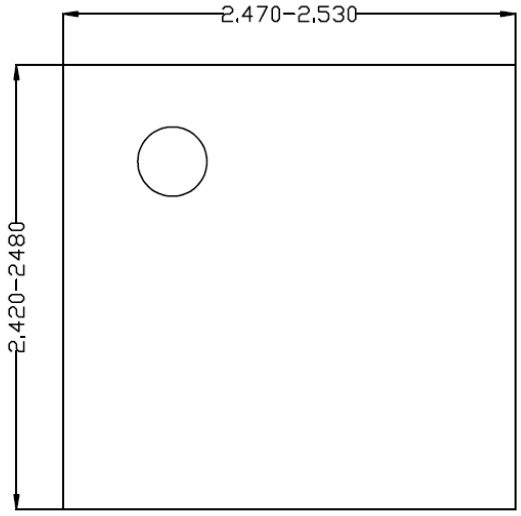
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	B3_VSET2						
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

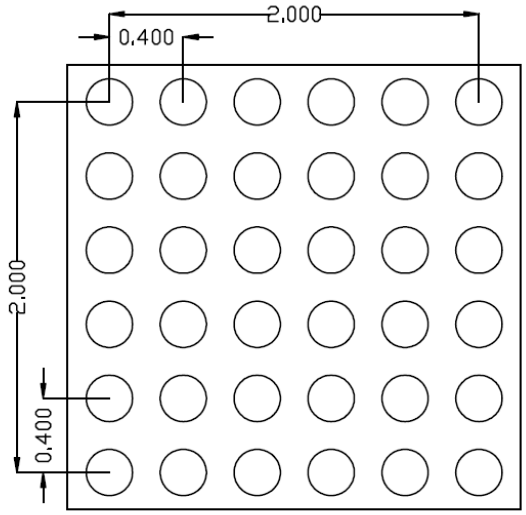
The output voltage is equal to B3_VSET2*0.01+0.5V

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
00h	0.50V	15h	0.71V	2Ah	0.92V	3Fh	1.13V
01h	0.51V	16h	0.72V	2Bh	0.93V	40h	1.14V
02h	0.52V	17h	0.73V	2Ch	0.94V	41h	1.15V
03h	0.53V	18h	0.74V	2Dh	0.95V	42h	1.16V
04h	0.54V	19h	0.75V	2Eh	0.96V	43h	1.17V
05h	0.55V	1Ah	0.76V	2Fh	0.97V	44h	1.18V
06h	0.56V	1Bh	0.77V	30h	0.98V	45h	1.19V
07h	0.57V	1Ch	0.78V	31h	0.99V	46h	1.20V
08h	0.58V	1Dh	0.79V	32h	1.00V		
09h	0.59V	1Eh	0.80V	33h	1.01V		
0Ah	0.60V	1Fh	0.81V	34h	1.02V		
0Bh	0.61V	20h	0.82V	35h	1.03V		
0Ch	0.62V	21h	0.83V	36h	1.04V		
0Dh	0.63V	22h	0.84V	37h	1.05V		
0Eh	0.64V	23h	0.85V	38h	1.06V		
0Fh	0.65V	24h	0.86V	39h	1.07V		
10h	0.66V	25h	0.87V	3Ah	1.08V		
11h	0.67V	26h	0.88V	3Bh	1.09V		
12h	0.68V	27h	0.89V	3Ch	1.10V		
13h	0.69V	28h	0.90V	3Dh	1.11V		
14h	0.70V	29h	0.91V	3Eh	1.12V		

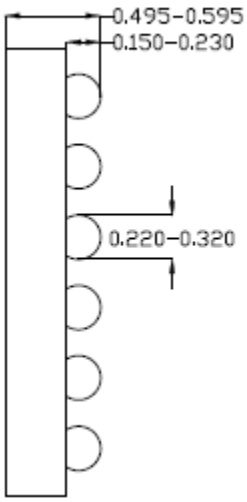
CSP2.5×2.45-36 Package Outline Drawing



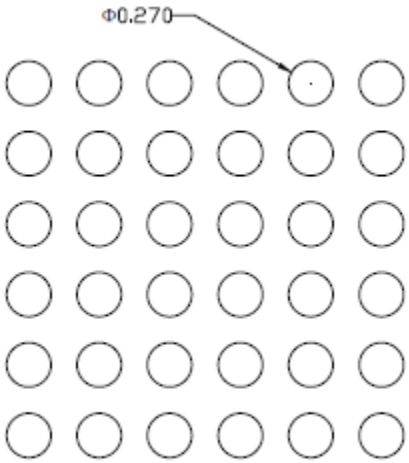
Top View



Bottom View



Side View

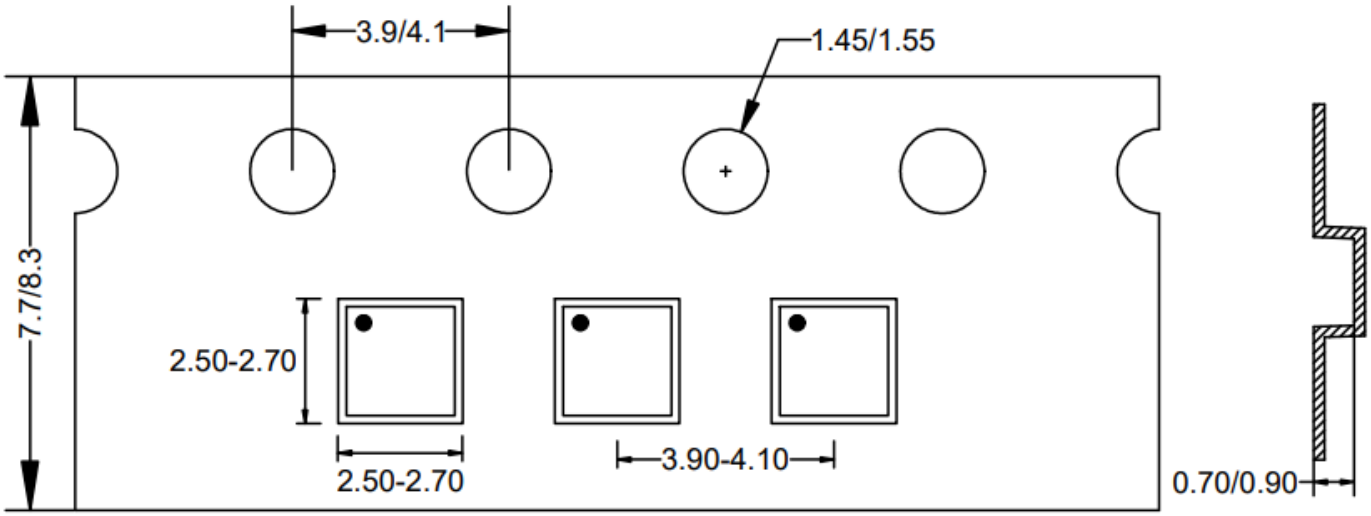


Recommended PCB Layout (Reference only)

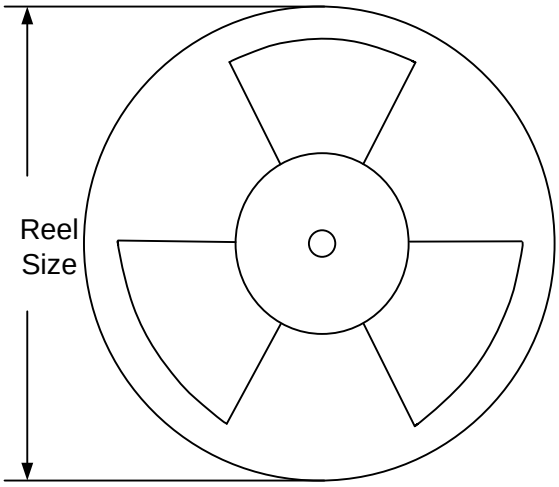
Notes: *All dimension in millimeter and exclude mold flash & metal burr.*

Tape and Reel Specification

Tape Dimensions and Pin 1 Orientation



Reel Dimensions



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
CSP2.5×2.45-36	8	4	7"	400	400	3000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
Nov.12, 2024	Revision 0.0D	-	-
Dec.20, 2024	Revision 0.1	No changes.	-
May.30, 2025	Revision 1.0	1. The package size has been changed from CSP 2.6×2.6 to CSP 2.5×2.45, it's a writing error for this change.	P1-2, 77-78
		2. Correct the writing error of ESD Specification, add "±" in Table.	P3
		3. Add MSL rating in Features.	P1
		4. Add Note 5 in Electrical Characteristics Table.	P5-10
		5. Add a description of the built-in 4ms clock masking logic for DPSLP mode and SLP mode.	P33
		6. Add test waveform, design procedure, and layout design etc. to make the design easier.	P11-16, 38-40

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