SY8665D

High Efficiency, 28V Input USB PD PMIC

General Description

The SY8665DTTQ is a wide input voltage range, high efficiency PMIC for USB power delivery applications. The device integrates a 5A buck regulator, an external P-MOSFET driver and an external NMOS driver to achieve power path control.

The buck regulator adopts fixed switching frequency peak current mode control. The output voltage can be either configured by the I^2C interface from 3.0V to 21V in 200mV per step or programmed by the FB pin. With high switching frequency and low $R_{DS(ON)}$ power switches, the device is able to achieve both small size and high efficiency solution.

The device integrates an I^2C compatible interface for mode selecting, output voltage setting, frequency setting, protection setting, etc.

The device is available in compact QFN3x3-19.

Ordering Information

SY8665 □(□□□)

Package Code

Optional Spec Code

Ordering Number	Package type	Note
SY8665DTTQ	QFN3x3-19	

Features

- 4.5-28V wide input voltage range
- Bidirectional power path control
- 5A buck regulator
  - Low $R_{DS(ON)}$ internal switch: HSFET: 33mΩ, LSFET: 23 mΩ
  - I^2C programmable output range from 3.0V to 21V in 200mV per step
  - Cable impedance compensation
  - Selectable switching frequency: 250kHz/500kHz/750kHz/1MHz
  - Internal soft-start limits the input inrush current
  - Output OCP, SCP, OVP
- External NFET driver for reverse blocking
- External PFET driver for power bypass
- I^2C compatible interface
- Support interrupt for status feedback
- Programmable discharge
- Programmable current limit
- Thermal shutdown protection
- Compact package QFN3x3-19
- UL Certificate Number: E491480
- UL 2367 Certified
- IEC/ EN 62368-1 Certified

Applications

- Notebook
- Monitor
- Desktop

Typical Applications

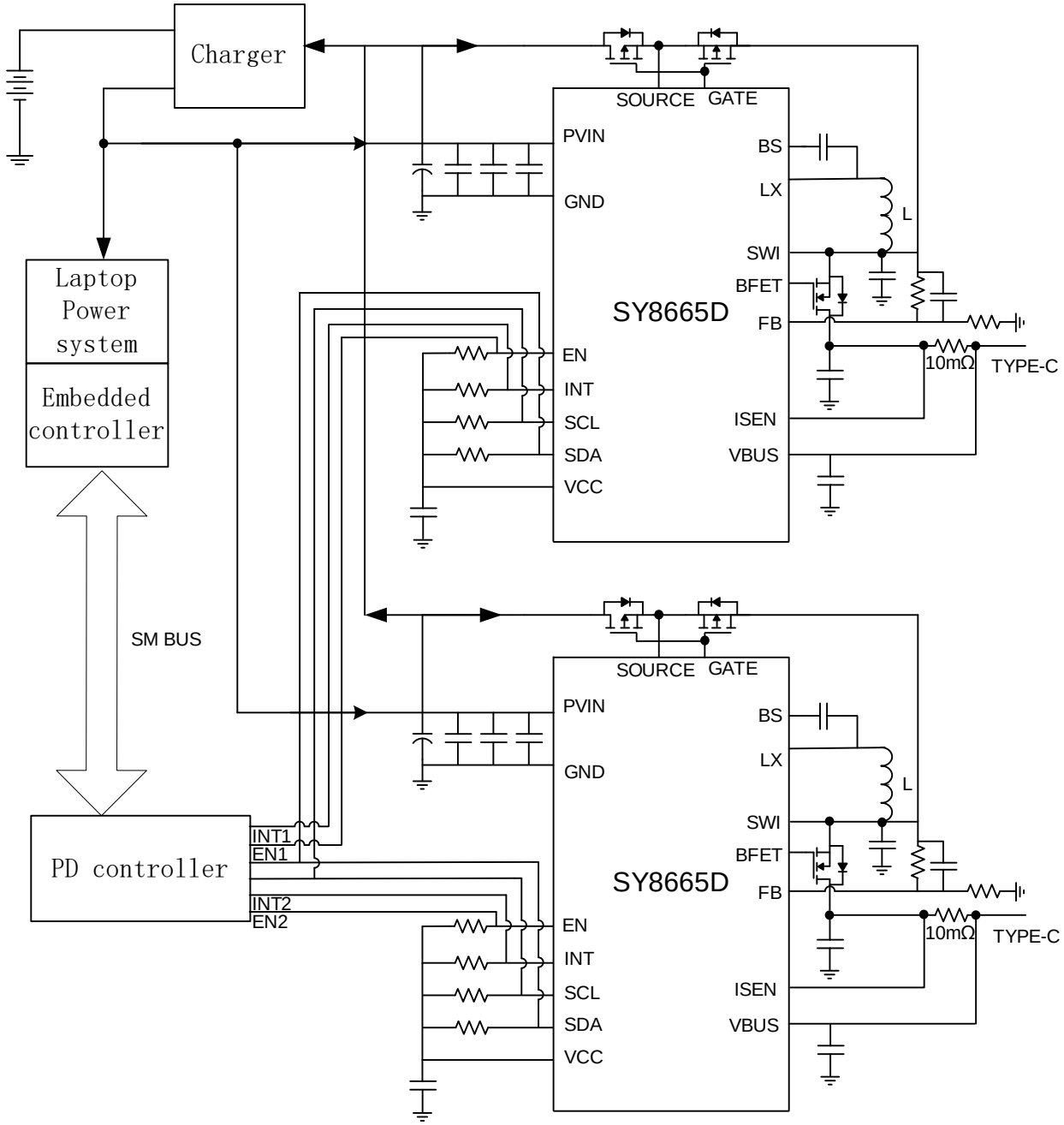


Fig.1-1 Schematic for laptop application

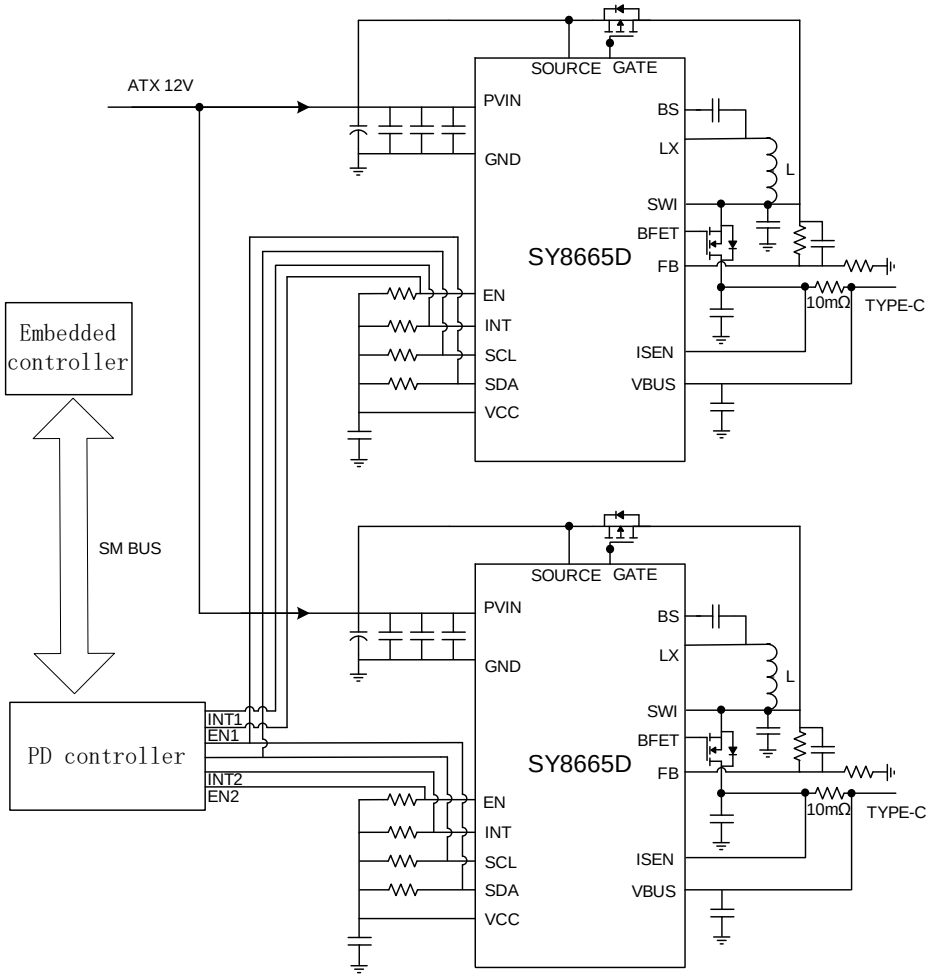


Fig. 1-2 Schematic for desktop application

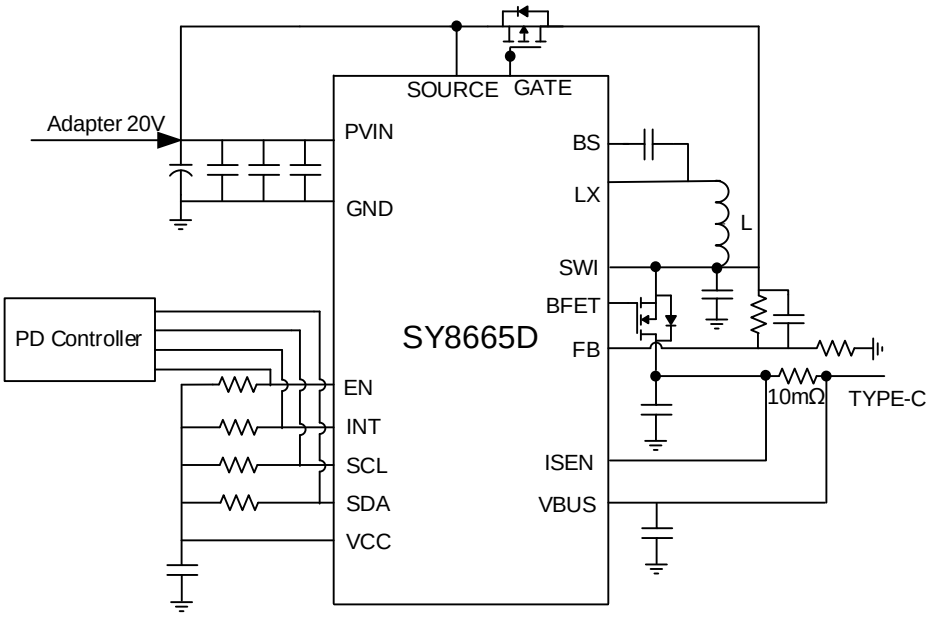
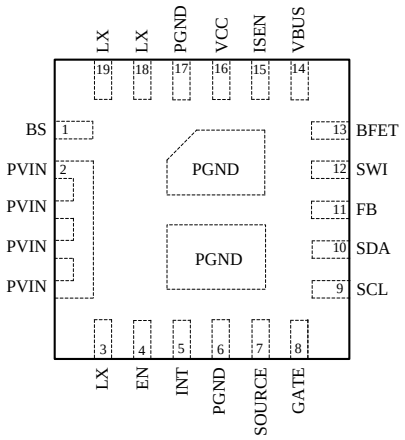


Fig.1-3 Schematic for monitor application

PINOUT (Top View)



Top Mark: ENY*xyz* (Device code: ENY, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Description
BS	1	Boot-Strap pin. Supply high side gate driver. Decouple this pin to LX pin with 0.1μF ceramic cap.
PVIN	2	Supply voltage for power stage.
LX	3,18,19	Connect this node to switching node of the inductor.
EN	4	Enable control pin, logic high enable. This pin is internally pulled low by 1000kΩ resistor.
INT	5	The INT pin is an open-drain output. When an interrupt event happens, the INT pin is internally pulled low to inform the host. After the host reads the interrupt register, the INT pin will be pulled high by external pull-up resistor. This pin is also used as device address set pin. Connect this pin to the VCC pin by a pull up resistor to program device address, $R_{pull-up}$=10k selects 0x10, $R_{pull-up}$=39k selects 0x11, $R_{pull-up}$=150k selects 0x12, $R_{pull-up}$=470k selects 0x13
PGND	6,17, exposed pad	Power ground
SOURCE	7	External P-MOS source pin
GATE	8	External P-MOS gate pin
SCL	9	I^2C Interface serial clock pin. Logic level input.
SDA	10	I^2C Interface serial data pin. Logic level input/output
FB	11	Source mode 1 output voltage feedback pin. Connect this pin to the center point of the output resistor divider. If 0x02[3]='0', which is default setting, output voltage is adjusted by I^2C and cable impedance is functional. If 0x02[3]='1', output voltage is programmed by resistor divider and cable impedance compensation is disabled., notice that the voltage divider should be connected to the SWI pin, $V_{SWI}=0.6V*(1+R_{TOP}/R_{BOT})$
SWI	12	The Source of the external blocking NFET. This pin is also the buck regulator output filter pin, connect at least 50μF or above ceramic capacitor to PGND.
BFET	13	Gate of the external blocking NFET.
VBUS	14	Type C connector port. This pin is power output in source mode and power input in sink mode. This pin is also the current sense pin, connect a 10mΩ resister between this pin and ISEN. Connect at least 100nF ceramic capacitor to GND.
ISEN	15	Current sense pin, connect a 10mΩ resister between this pin and VBUS.

VCC	16	Internal 3.3V LDO output. Power supply for internal analog and driving circuits. Decouple this pin to PGND with a 2.2uF ceramic capacitor.

Absolute Maximum Ratings (Note 1)

PVIN, LX, ISEN, VBUS, GATE, SOURCE, SWI, EN, FB ---------- -0.3V to 30V
BFET---------- -0.3V to 36V
BS-LX---------- -0.3V to 4V
VCC ---------- -0.3V to 4V
SCL, SDA, ADDR, INT---------- -0.3V to 7V
Power Dissipation, PD @ TA = 25°C ---------- 3W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 30℃/W
θ_{JC} ---------- 2.8℃/W
Junction Temperature Range ---------- ---------- 150°C
Lead Temperature (Soldering 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
ESD Susceptibility (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

PVIN Voltage ----------4.5V to 28V
VBUS Voltage ----------3.0V to 28V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{PVIN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}	V_{PVIN} or V_{VBUS}	4.5		28	V
Input UVLO Threshold	V_{UVLO}	V_{PVIN} rising		3.8	4.2	V
		V_{VBUS} rising		3.8	4.2	V
Input UVLO Hysteresis	V_{HYS}			0.2		V
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.6	V
Quiescent Current	IQ	Source mode1, no switching		240	300	uA
Shutdown Current	$I_{shutdown}$	IC is disabled		5	10	uA
VBUS Output Voltage Range	V_{VBUS}	Source mode 1	3		21	V
V_{VBUS} Voltage Accuracy	$V_{VBUS,acc}$	Source mode 1, VBUS set 5V	-1.5		1.5	%
V_{VBUS} Voltage OVP	$V_{VBUS,OVP}$	Source mode 1 OVP Point set 125%'	118	125	132	%
OVP Delay	T_{OVP_delay}	Source mode 1		125		us
VBUS Absolute Maximum OVP Latch-off			28		32	V
VBUS Absolute Maximum OVP Latch-off Delay				600		ns
High Side FET RON	$R_{DS(ON)\_HS}$			33		mΩ
Low Side FET RON	$R_{DS(ON)\_LS}$			23		mΩ
Inductor Peak Current Limit	I_{peak}	Inductor peak current limit set 12.5A	11.5	13	14.6	A
Min On Time	T_{ON_MIN}	Buck minimum on time		80		ns
Min Off Time	T_{OFF_MIN}	Buck minimum off time		100		ns
Soft Start Time	T_{ss}	Source mode 1 soft start, V_{VBUS} set 5V		12.5		ms
Switching Frequency Accuracy		Switching frequency set 500kHz	-15		15	%
UVP Threshold	T_{UVP_th}	Source mode 1,UVP set 60%		60		%
UVP Delay	T_{UVP_delay}	Source mode 1		200		us
VBUS Slew Rate Control		Source mode 1		0.4		V/ms
		Source mode 2		5		V/ms
		Source mode 3		5		V/ms
Cable Impedance Compensation Accuracy		6A load current, R_{SENSE}=10mΩ	-12		+12	%
Output Current Limit	V_{ILIM}	0x04[7:5]='000'	5	10	15	mV
		0x04[7:5]='001'	10	15	20	mV
		0x04[7:5]='010'	15	20	25	mV
		0x04[7:5]='011'	21	25	29	mV
		0x04[7:5]='100'	26	30	34	mV
		0x04[7:5]='101'	36	40	44	mV
		0x04[7:5]='110'	46	50	54	mV
		0x04[7:5]='111'	56	60	64	mV

Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C
Reverse Voltage Threshold	V_{RC}			50		mV
Reverse Block Delay Time	T_{delay_block}			5		us
Output Current Limit Protection Delay	T_{OCP_delay}			1		ms
External P-MOSFET Driver						
GATE Output Low	V_{GS}	V_{SOURCE}-V_{GATE}		7		V
GATE to SOURCE Pull Up Resistance	R_{GS_SCP}				27	Ω
Gate sink current (sink mode soft start)	I_{G_SINK}			6		uA
External NMOS Driver						
BFET Charging Current	I_{CHG}			4		uA
BFET Clamp Voltage		V_{BFET}-V_{SWI}		6		V
BFET Discharge Resistance		BFET short to SWI resistance		27	37	Ω
I2C COMPATIBLE INTERFACE						
Maximum Operating Frequency				400		kHz
SDA and SCL Input Logic Threshold	Logic_L				0.4	V
	Logic_H		2			V
SDA Output Low Voltage		3mA sink current			0.4	V

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

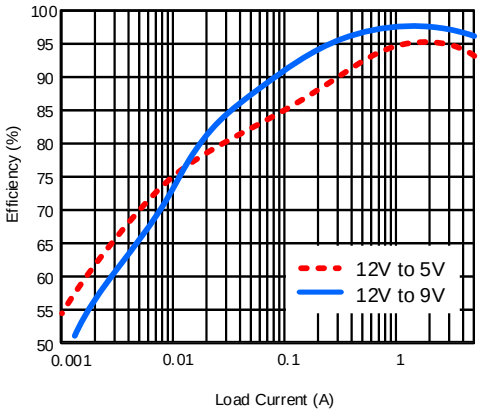
Note 2: θ_{JA} is measured in the natural convection at TA = 25°C on a two-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

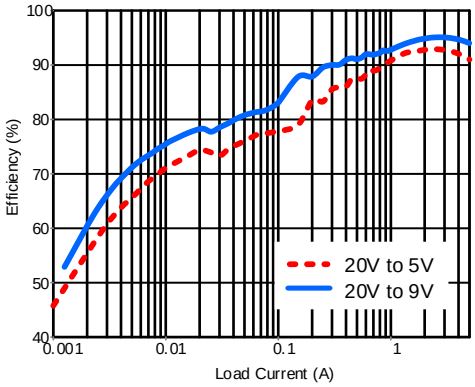
Efficiency vs Output Current

(Vin=12V)



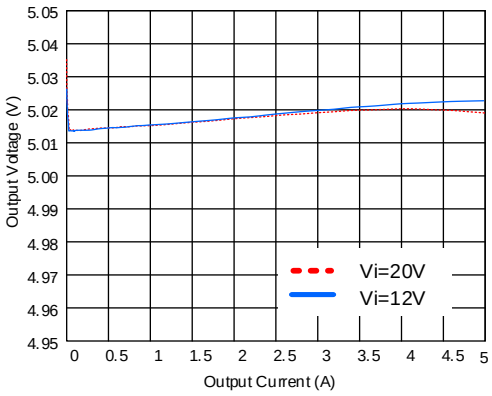
Efficiency vs Output Current

(Vin=20V)



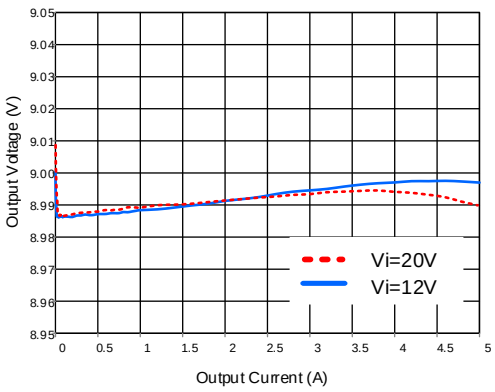
Output Voltage vs Output Current

（V_{OUT}=5V）



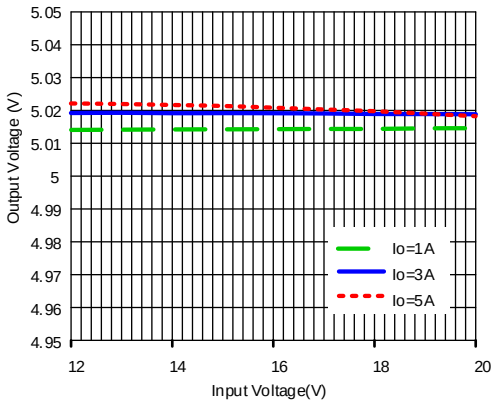
Output Voltage vs Output Current

（V_{OUT}=9V）



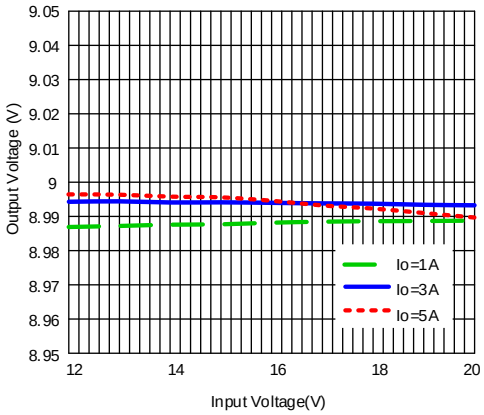
Output Voltage vs Input Current

（V_{OUT}=5V）



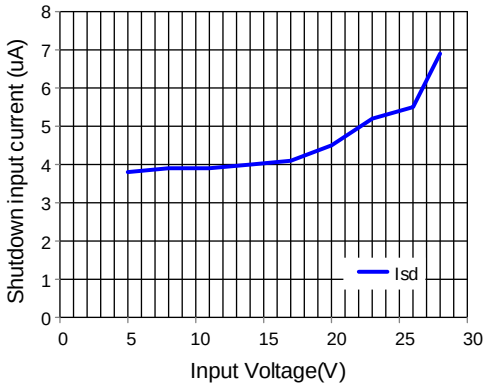
Output Voltage vs Input Current

（V_{OUT}=9V）



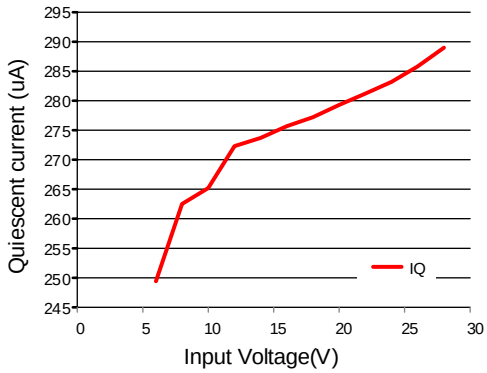
Shutdown input current

（EN=Low）



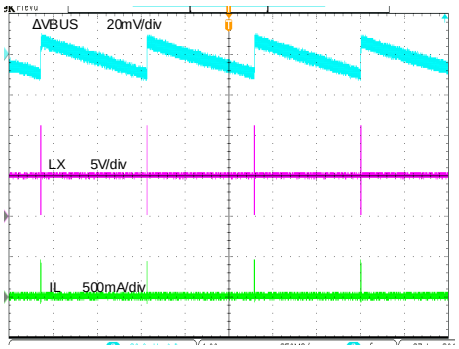
Quiescent Current

（Source mode 1 & no switching）



Output Ripple

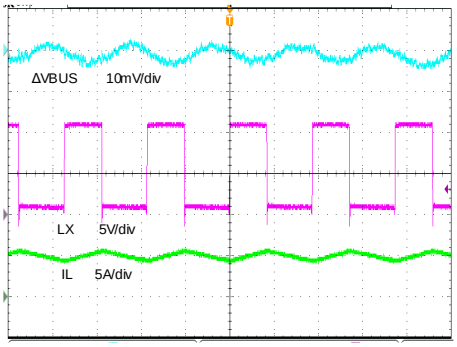
(Vin=12V, VBUS=5V, Fsw=500kHz,Iout=0A)



Time (4ms/div)

Output Ripple

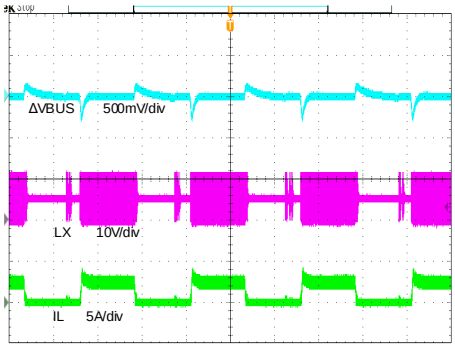
(Vin=12V, VBUS=5V, Fsw=500kHz,Iout=5A)



Time (1μs/div)

Load Transient

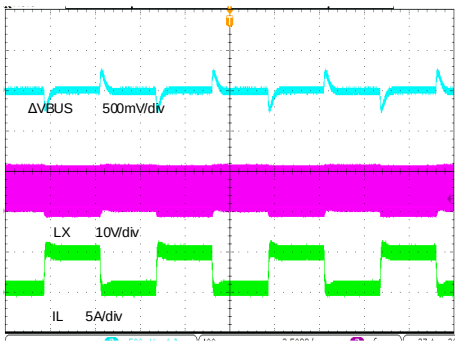
(Vin=12V, VBUS=5V, Fsw=500kHz,Iout=0~2.5A)



Time (400μs/div)

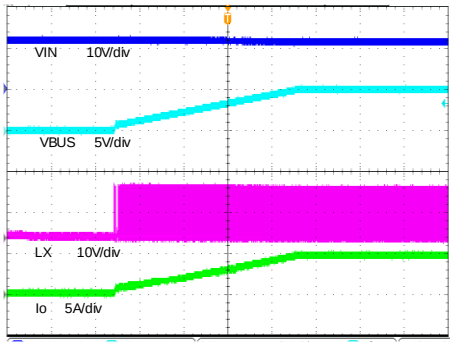
Load Transient

(Vin=12V, VBUS=5V, Fsw=500kHz,Iout=0.5~5A)



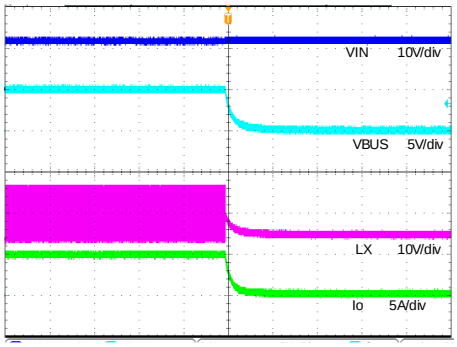
Time (400μs/div)

Source Mode 1 I²C Enable On
(Vin=12V, VBUS=5V, Fsw=500kHz,Iout=5A)



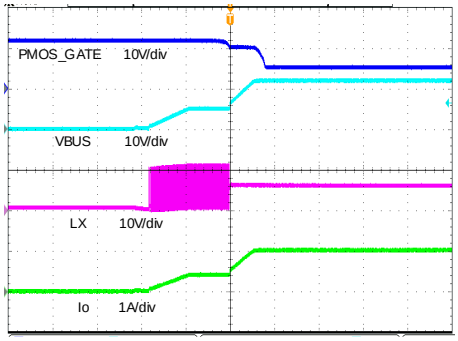
Time (2ms/div)

Source Mode 1 I²C Enable On
(Vin=12V, VBUS=5V, Fsw=500kHz,Iout=5A)



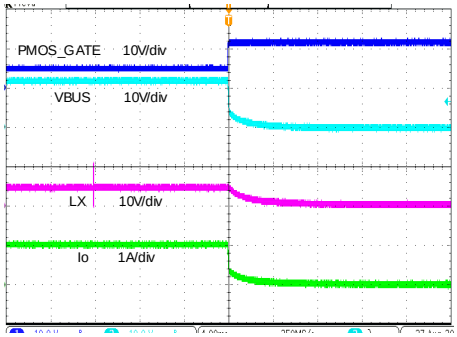
Time (2ms/div)

Source Mode 2 I²C Enable On
(Vin=12V, VBUS=12V,Iout=1A)



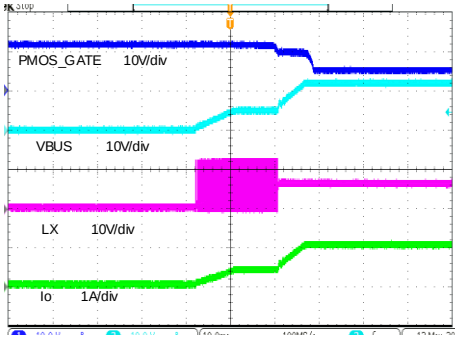
Time (10ms/div)

Source Mode 2 I²C Enable Off
(Vin=12V, VBUS=12V,Iout=1A)



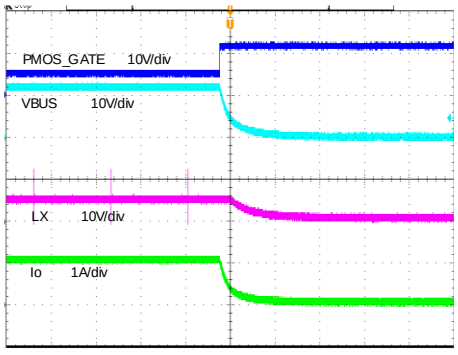
Time (4ms/div)

Source Mode 3 I²C Enable On
(Vin=12V, VBUS=12V,Iout=1A)



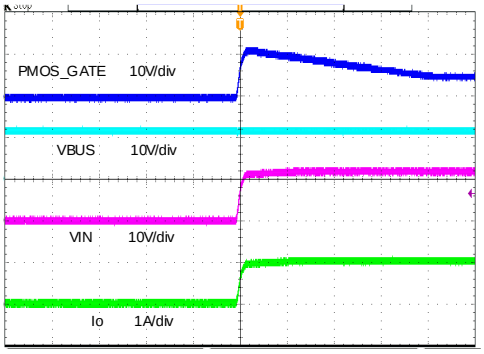
Time (4ms/div)

Source Mode 3 I²C Enable Off
(Vin=12V, VBUS=12V,Iout=1A)



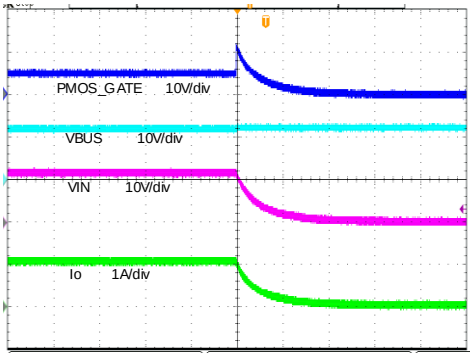
Time (10ms/div)

Sink Mode 1 I²C Enable On
(Vin=12V, VBUS=12V,Iout=1A)



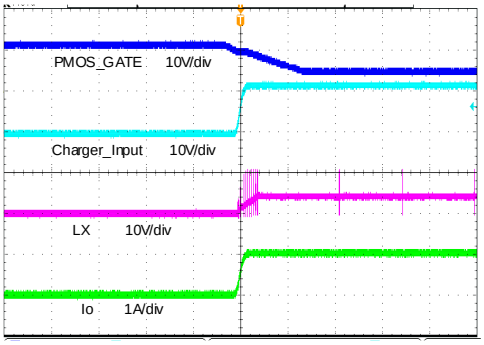
Time (4ms/div)

Sink Mode 1 I²C Enable Off
(Vin=12V, VBUS=12V,Iout=1A)



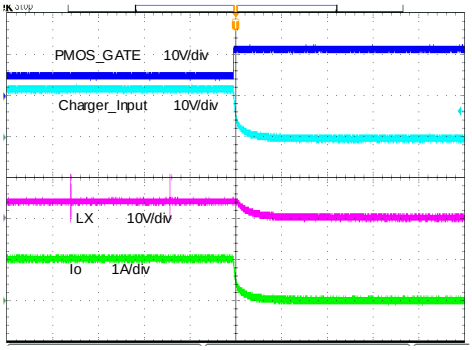
Time (4ms/div)

Sink Mode 2 I²C Enable On
(Vin=12V, VBUS=12V,Iout=1A)



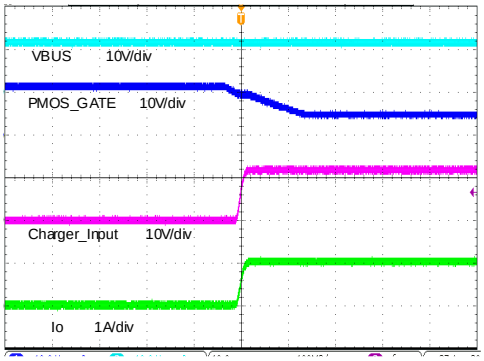
Time (10ms/div)

Sink Mode 2 I²C Enable Off
(Vin=12V, VBUS=12V,Iout=1A)



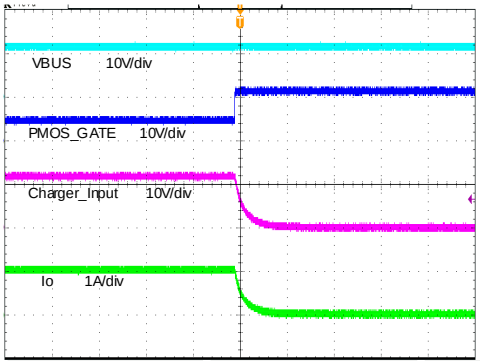
Time (10ms/div)

Sink Mode 3 I²C Enable On
(Vin=12V, VBUS=12V,Iout=1A)



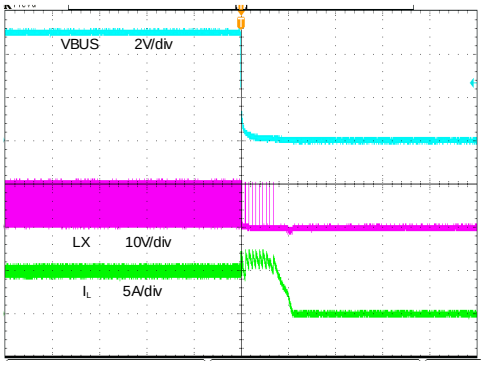
Time (10ms/div)

Sink Mode 3 I²C Enable Off
(Vin=12V, VBUS=12V,Iout=1A)



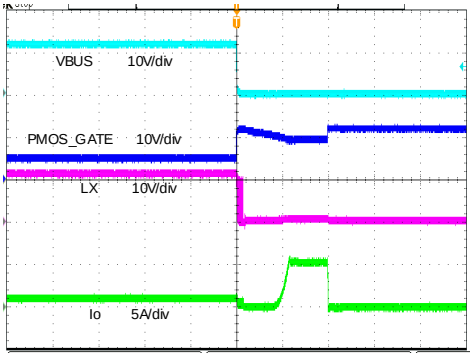
Time (4ms/div)

Source Mode 1 Short
(Vin=12V, VBUS=5V, Fsw=500kHz,Iout=5A to short)



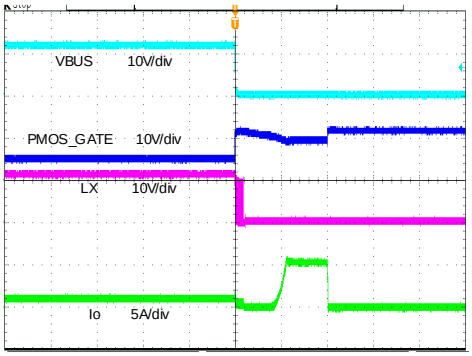
Time (200µs/div)

Source Mode 2 Short
(Vin=12V, VBUS=12V,Iout=1A~short)



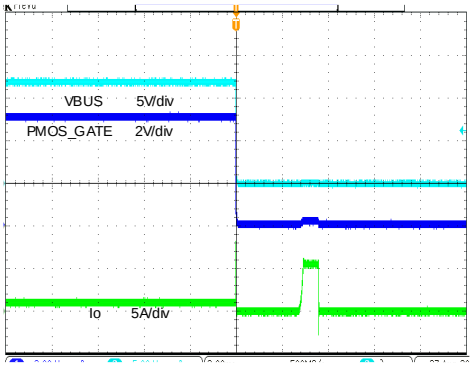
Time (800µs/div)

Source Mode 3 Short
(Vin=12V, VBUS=12V,Iout=1A~short)



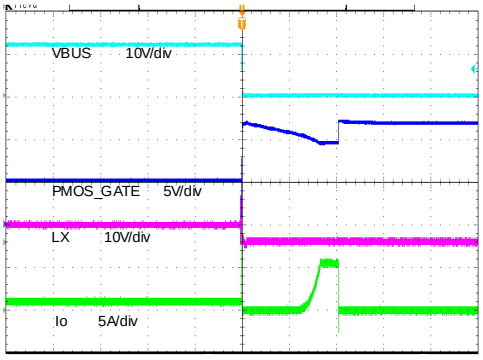
Time (800µs/div)

Sink Mode 1 Short
(Vin=12V, VBUS=12V,Iout=1A~short)



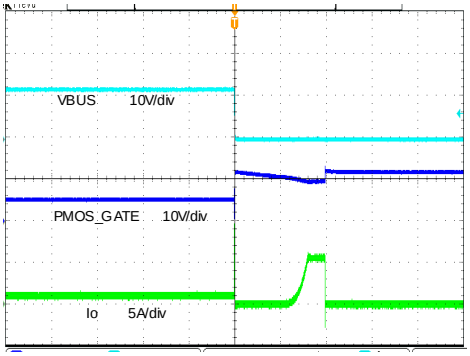
Time (2ms/div)

Sink Mode 2 Short
(Vin=12V, VBUS=12V,Iout=1A~short)



Time (2ms/div)

Sink Mode 3 Short
(Vin=12V, VBUS=12V,Iout=1A~short)



Time (2ms/div)

Applications Information

IC Enable

When the device is enabled, VCC is turned on, and then the I²C interface is fully functional. The device can be enabled when PVIN voltage is above 4V and EN voltage is greater than 1.2V, or VBUS voltage exceeds 4V. To disable the device, the regulator should be disabled through the I²C first, and then the device will automatically discharge VBUS. After V_{VBUS} falls below 4 V, pull EN low to totally disable the device.

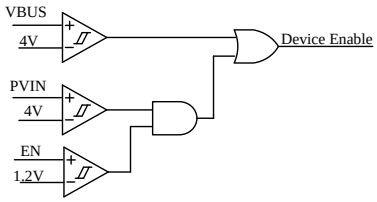


Fig.4 Description of IC Enable Function

Source mode 1

After source mode 1 is selected by I²C, the external NFET turns on first, then the converter is enabled and the HSFET and LSFET start switching. Every time the buck converter is started, the device applies soft-start to avoid any overshoot on output. The output voltage can be selected by I²C or programmed by external resistor divider. Once write all off command is received, the external NFET turns off, the HSFET turns off and the LSFET turns on until LSFET zero-current is detected, the discharge FET is automatically turned on.

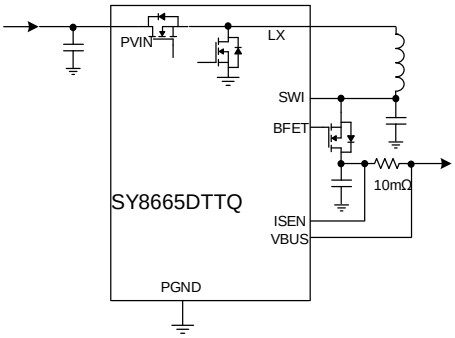


Fig.5-1 Source mode1

Source mode2

When enable source mode 2, the external NFET turns on first, then the buck regulator initiate soft-start. After the buck converter soft-start finished, the external P-MOSFET turns on slowly. VBUS voltage will ramp up above the buck output set point and make the buck converter enter sleep mode (stop switching). When all off command is received, the buck regulator shutdown, the external NFET and the external P-MOSFET turn off, the discharge FET is automatically turned on. Note: Buck OVP function is disabled in source mode 2.

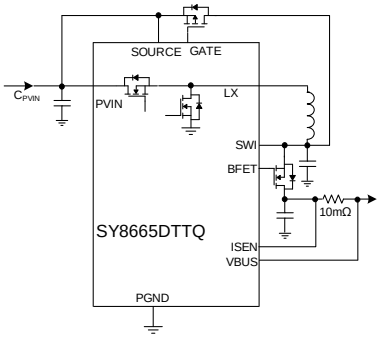


Fig.5-2 Source mode 2

Source mode 3

When source mode 3 is selected, the external NFET turns on first, then the buck converter initiate soft-start. After the buck soft-start finished, the external back-to back P-MOSFET are turned on slowly, when V_{VBUS} exceeds OVP threshold, the external NFET turns off. When write all off to shutdown source mode 3, the buck regulator is disabled, the external NFET and the external back-to back P-MOSFET are turned off, the discharge FET is automatically turned on.

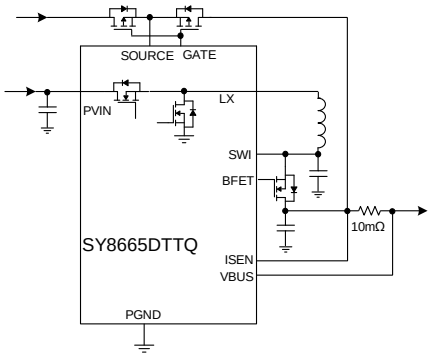


Fig.5-3 Source mode 3

Sink mode 1

In sink mode 1, the power is delivered from VBUS to PVIN through the external P-MOSFET and the external NFET. When power up, the external P-MOSFET and the external NFET are turned on. When shutdown sink mode 1, both the external NFET and the external P-MOSFET are turned off

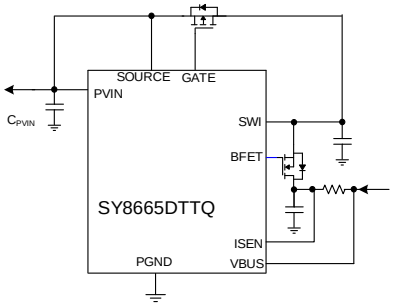


Fig.5-4 sink mode 1

Sink mode 2

The device supports mode transition from sink mode 2 to source mode 1. At initial sink mode 2, the external back-to-back P-MOSFET are turned on, the external NFET is turned off, the buck remains activated to regulate SWI at 4.4V. Once the adaptor is removed, V_{VBUS} will drop, after the V_{VBUS} drop below V_{SWI}, the external NFET will turn on and the buck regulator will regulate the VBUS pin. On adaptor removal, PD controller should enable source mode 1 through the I^2C interface to change the operation mode from sink mode 2 to source mode 1, then the buck regulator will regulate the VBUS pin at 5V. Note: in sink mode 2, no reverse current protection.

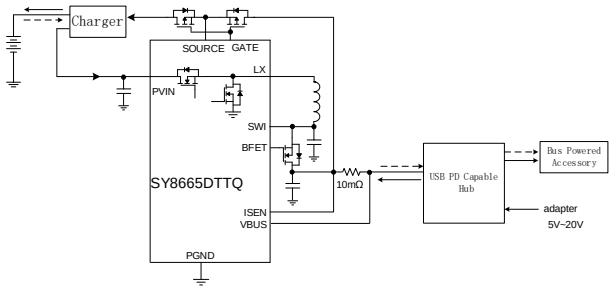


Fig.5-5 Sink mode 2

Sink mode 3

In sink mode 3, only the external back-to-back P-MOSFET are turned on .the buck regulator is disabled, the external NFET is turned off.

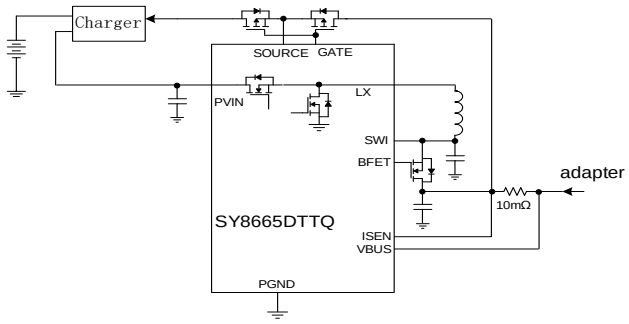


Fig.5-6 Sink mode 3

Mode Transition Flow

Source mode 1 can switch to source mode 2 and source mode 3 and sink mode 2 directly, also source mode 2 and source mode 3 and sink mode 2 can switch back to source mode 1. However, all other modes are not allowed to transit directly, as the mode transition flow shows below:

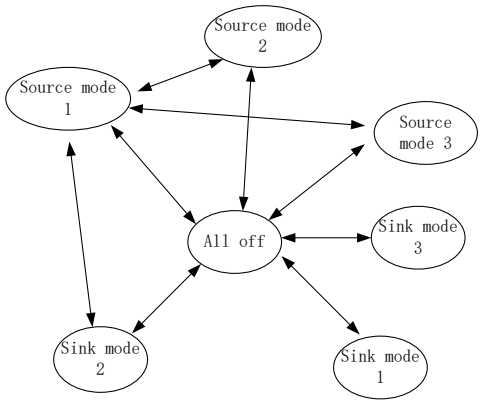


Fig.6-1 mode transition flow

SY8665DTTQ + SY6502 Application

The device also supports external current sense for bypass mode current limit control, as the schematic below, use SY6052 for external current sense, customer can program the over current protection according to system requirement.

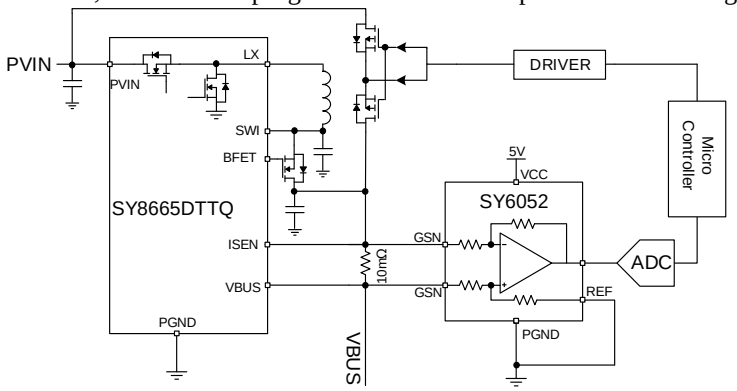


Fig.6-2 SY8665DTTQ+ SY6502 application schematic

Cable Impedance Compensation

To compensate cable voltage drop, the device incorporates cable impedance compensation function. As the load current increases, the regulated output voltage will increase linearly and the relationship is

$$V_{VBUS} = V_{VBUS\_SET} + \frac{V_{ISEN} - V_{VBUS}}{10m\Omega} \cdot R_{CMP}$$

Where R_{CMP} is configured by register 0x02[6:4]. Notice that the cable impedance compensation only functions in source mode 1 and output voltage is adjusted by I^2C,(Go_bit='0').

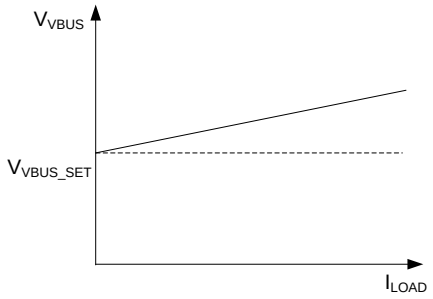


Fig.7 Cable impedance compensation.

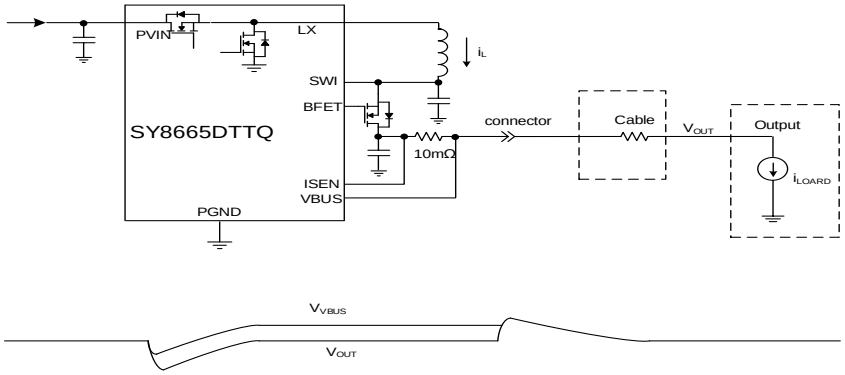


Fig.8 Load transient response

Slew Rate Control

The device integrated slew rate control to match USB PD specification. Positive transition is shown below, the slew rate control apply to both a transition from 0V to source mode 2 or source mode 3 and a transition from source mode 1 to source mode 2 or source mode 3.

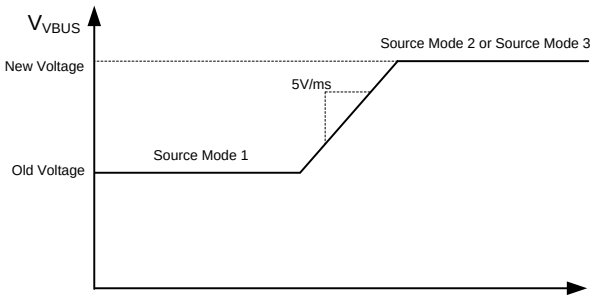


Fig.9 Positive voltage transition

Negative transition is shown below, the slew rate control apply to a transition from source mode 2 or source mode 3 to source mode 1.

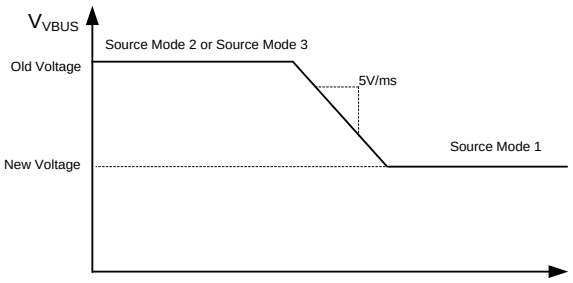


Fig.10 Negative voltage transition

Source mode 1 Output Voltage Setting

Under source mode1, the output voltage can be either configured through I²C or programmed by external resister divider. The FB pin is always connected to the input of the error amplifier, the internal feedback point connect or disconnect to the error amplifier depends on I²C register setting. When operated in internal mode (Go_bit='0'), which is default setting, the internal feedback point is connected to the FB pin and the output voltage is adjusted by I²C. If Go_bit='1', the internal feedback point is disconnected to the error amplifier and the output voltage is programmed by external resistor divider: $V_{SWI}=0.6V*(1+R_{TOP}/R_{BOT})$. Since the FB pin is always connected to the input of the error amplifier, do not use external resister divider under internal mode.

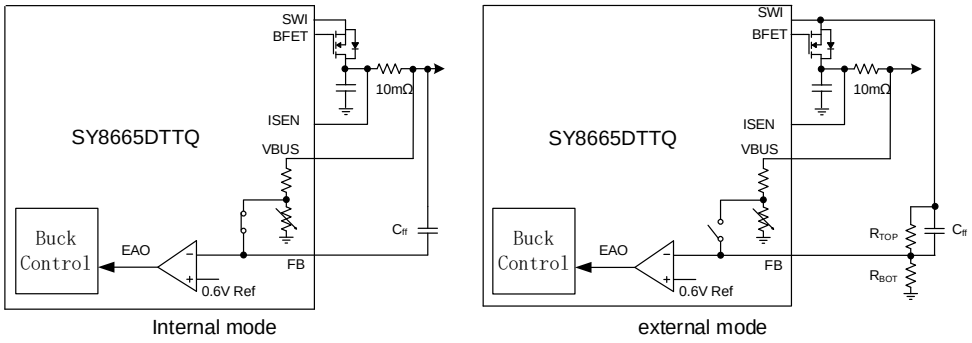


Fig.11. Source mode 1 output voltage setting.

Device Address Setting

Connect the INT pin to the VCC pin by a pull up resistor to program device address. When power up, the internal LDO VCC initiate soft start and it takes 1.3ms to ramp up to 3.3V, after 0.7ms delay, an internal amplifier holds this pin at a fixed voltage(2.7V) for 100us to detect the pull-up resistor: $R_{pull-up}$=10k selects 0x10, $R_{pull-up}$=39k selects 0x11, $R_{pull-up}$=150k selects 0x12, $R_{pull-up}$=470k selects 0x13. After the detect is done, the INT pin resume normal open drain output.

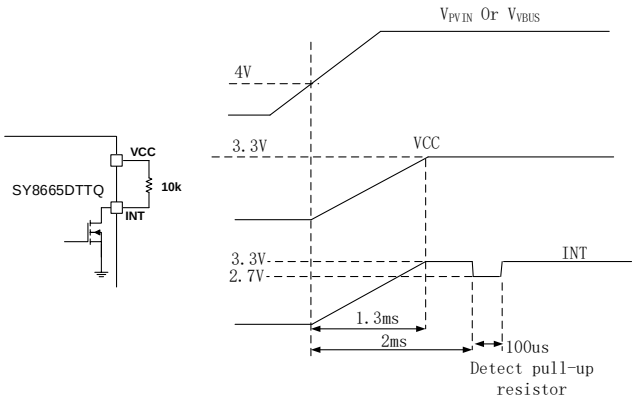


Fig.12. Device address setting

Output Current Limit

The device detects output current by sensing the voltage drop between the ISEN pin and the VBUS pin. The voltage threshold is configured by register 0x04[7:5]. In source mode 1, once the voltage difference exceeds the voltage threshold, the internal control loop will regulate the output current by decreasing duty cycle until UVP or OTP is triggered. In power bypass mode (source mode 2, source mode 3, sink mode 1, sink mode 2 and sink mode 3), the device limit output current by decreasing external P-MOSFET or external NMOS gate to source voltage, if the current limit loop functions lasted for 1ms, the device latch off.

Discharge Logic

The discharge FET turns on under the following conditions:

Source mode 1 FB over voltage;

I^2C control, 0x00[3]='1': turn on discharge at all off

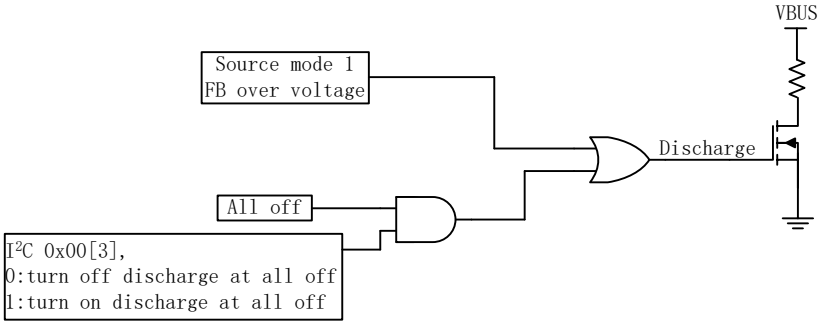


Fig.13. Discharge logic

I²C Compatible Interface

SY8665DTTQ integrates an I²C compatible interface. To ensure compatibility with a wide range of system processors, the I²C interface supports clock speeds of up to 400kHz ("Fast-Mode") and uses standard I²C commands. The PumSY8665DTTQ always operates as a slave device, and is addressed using a 7-bit slave address followed by an 8th bit, which indicates whether the transaction is a read-operation or a write-operation.
The I²C interface is fully functional after IC is enabled.

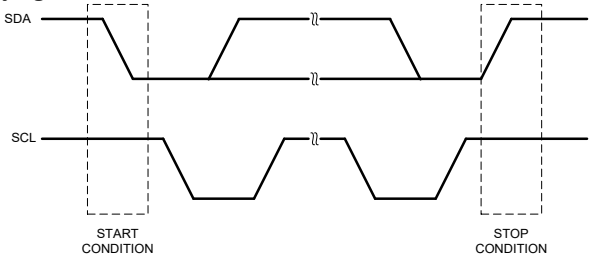
I²C Device Address:

When communicating with multiple devices using the I²C interface, each device must have its own unique address so the host can distinguish between the devices. The most significant 5-bits of the device address is '00100' The6th and 7th-bit device address of SY8665DTTQ is selected by INT pin pull up resistor.

Rpull-up between INT and VCC	Device Address
Rpull-up=10k	0010000
Rpull-up=39k	0010001
Rpull-up=150k	0010010
Rpull-up=470k	0010011

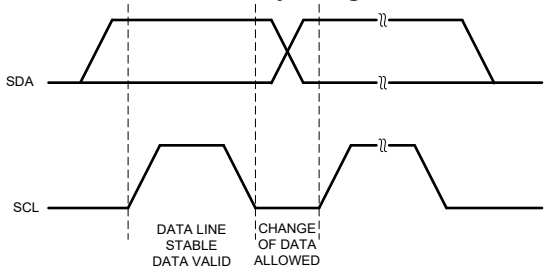
START and STOP Conditions:

The START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition. The I²C master always generates the START and STOP conditions.



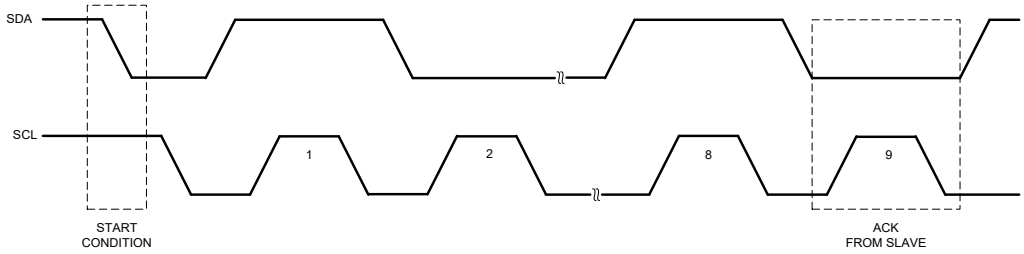
Data Validity:

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.



Acknowledge:

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the master sends 7-slave address bits and an $R/\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.

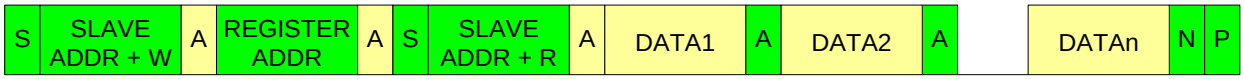


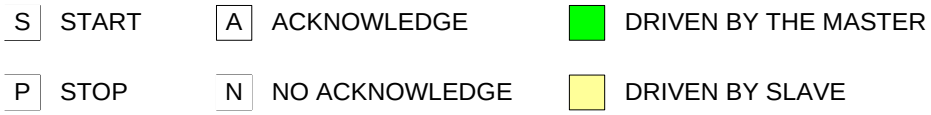
Data Transactions:

All transactions start with a control byte sent from the I^2C master device. The control byte begins with a START condition, followed by 7-bits of slave address followed by the R/W bit. The R/W bit is 0 for a write or 1 for a read. If any slave devices on the I^2C bus recognize their address, they will acknowledge by pulling the SDA line low for the last clock cycle in the control byte. If no slaves exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition. Once the control byte is sent, and the SY8665DTTQ acknowledges it, the 2nd byte sent by the master must be a register address byte. The register address byte tells the SY8665DTTQ which register the master will write or read. Once the SY8665DTTQ receives a register address byte it responds with an acknowledge. If a STOP condition is detected after the register address byte is received, the SY8665DTTQ takes no further action but storing the register address byte. The register address byte auto increase when multiple date bytes are transited.

Write

Random Read





Register Map

Address	Data	Note
0x00	Function setting1	R/W
0x01	Function setting2	R/W
0x02	Function setting3	R/W
0x03	Protection setting 1	R/W
0x04	Protection setting 2	R/W
0x05	State Register	R

Function setting1 (0x00)

Name	# of Bits	Access	Default	Description
I^2C Reset	7	R/W	0	0: None 1: Reset all registers to default value. Automatically clear to "0" after reset is done.
Discharge Resistor Setting	6:5	R/W	00	00: 1.80kΩ 01: 1.44kΩ 10: 1.08kΩ 11: 0.72kΩ
Reserved	4	R/W	0	
Discharge Enable at All Off	3	R/W	1	0: turn off discharge at all off 1: turn on discharge at all off
Mode	2:0	R/W	000	000: All off 001: Source mode 1, buck switching, NFET turn on, PFET turn off 010: Source mode 2, buck standby, NFET turn on, PFET turn on 011: Source mode 3, buck standby, NFET turn off, PFET turn on 100: All off 101: Sink mode 1, buck is disabled, NFET and PFET turn on 110: Sink mode 2, buck standby, NFET turn off, PFET turn on 111: Sink mode 3, buck is disabled, NFET turn off, PFET turn on

Function Setting2 (0x01)

Name	# of Bits	Access	Default	Description
Output Voltage Setting (3.0V~21V @ 0.2V/Step)	7	R/W	0	Reserved
	6:0	R/W	0001011 (5.0V)	0000000: 0V 0000001: 3.0V 0000010: 3.2V 0000011: 3.4V 0000100: 3.6V 0000101: 3.8V 0000110: 4.0V 0000111: 4.2V 0001000: 4.4V …… 1011011: 21V …… 1111111: 21V the device automatically reset to 5V under OTP,UVP In all off mode, output voltage setting is reset to 5V and cannot be changed by the I^2C interface In sink mode 2, the device automatically change output voltage setting to 4.4V and cannot be changed by the I^2C interface When transition from sink mode 2 to source mode 1, the device automatically reset output voltage setting to 5V.

Function Setting3(0x02)

Name	# of Bits	Access	Default	Description
Light Load Operation	7	R/W	1	0: pulse skip 1: burst mode
Cable Impedance Compensation (Source mode 1)	6	R/W	0	000: R_{CMP} =0mΩ 001: R_{CMP} =50mΩ 010: R_{CMP} =100mΩ 011: R_{CMP} =125mΩ 100: R_{CMP} =150mΩ 101 R_{CMP} =175mΩ 110: R_{CMP} =200mΩ 111 R_{CMP} =225mΩ $V_{CMP}=\frac{V_{ISEN}-V_{VBUS}}{10m\Omega}\cdot R_{CMP}$
	5	R/W	0	
	4	R/W	0	
Go_bit	3	R/W	0	0:internal mode, output voltage is adjustable by I^2C, cable impedance compensation is functional 1: external mode, output voltage is programmed by external resistor divider connected to the SWI pin: V_{SWI}=0.6V*(1+R_{TOP}/R_{BOT}), cable impedance compensation is disabled.
Interrupt Enable	2	R/W	0	0:Active 1: Inactive, INT remain open drain output
Reserved	1:0	R/W	00	

Protection setting 1 (0x03)

Name	# of Bits	Access	Default	Description
Reverse Current Protection mode	7	R/W	0	0: Latch-Off , the device automatically reset Mode Bits to all off(0x00[2:0]='000') 1: Auto recover in source mode 1 Latch off in power bypass mode
OTP	6	R/W	0	0: Latch-Off , the device automatically reset Mode Bits to all off(0x00[2:0]='000') 1: Auto recover in source mode1, the device automatically reset output voltage setting to 5V Latch off in power bypass mode
OVP((Source Mode 1)	5	R/W	1	0: Latch off, the device automatically reset Mode Bits to all off(0x00[2:0]='000') 1: Auto recover
UVP((Source Mode 1)	4	R/W	0	0: Latch-Off, the device automatically reset Mode Bits to all off, 0x00[2:0]='000' 1:Auto recover, the device automatically reset output voltage setting to 5V
Buck Switching Frequency Setting	3:2	R/W	01	00= 250kHz 01= 500kHz 10= 750kHz 11= 1 MHz
Reserved	1:0	R/W	00	

(1) Power bypass mode: source mode 2, source mode 3 and sink mode.

Protection setting 2 (0x04)

Name	# of Bits	Access	Default	Description
Output Current Limit	7:5	R/W	111	000: 10mV 001: 15mV 010: 20mV 011: 25mV 100: 30mV 101: 40mV 110: 50mV

				111: 60mV
V_{VBUS} OVP Threshold (buck mode)	4:3	R/W	00	00: 125% 01: 120% 10: 115% 11: 110%
V_{SWI} UVP Threshold (buck mode)	2:1	R/W	01	00: 50% 01: 60% 10: 70% 11: 80%
Inductor Peak Current Limit	0	R/W	0	0:9A 1:12.5A

State Register (0x05)

Name		# of Bits	Access	Description
Power Good		7	R	0: Power not good 1: Power good (sourcemode1,V_{FB}=90%~110%Vref)
INT Flag(Active Interrupt)	Reserved	6	R	
	VBUS absolute maximum OVP	5	R	0:Normal 1: VBUS absolute maximum OVP
	Voltage reversed	4	R	0: Normal 1:Voltage reversed
	Over temperature protection	3	R	0: Normal 1: OTP
	OVP	2	R	0: Normal 1: OVP
	OCP	1	R	0: Normal 1: Output current is limited
	UVP	0	R	0: Normal 1: UVP

Layout Design

The layout design of SY8665DTTQ is very important for proper operation. Following are the tips for good PCB layout.

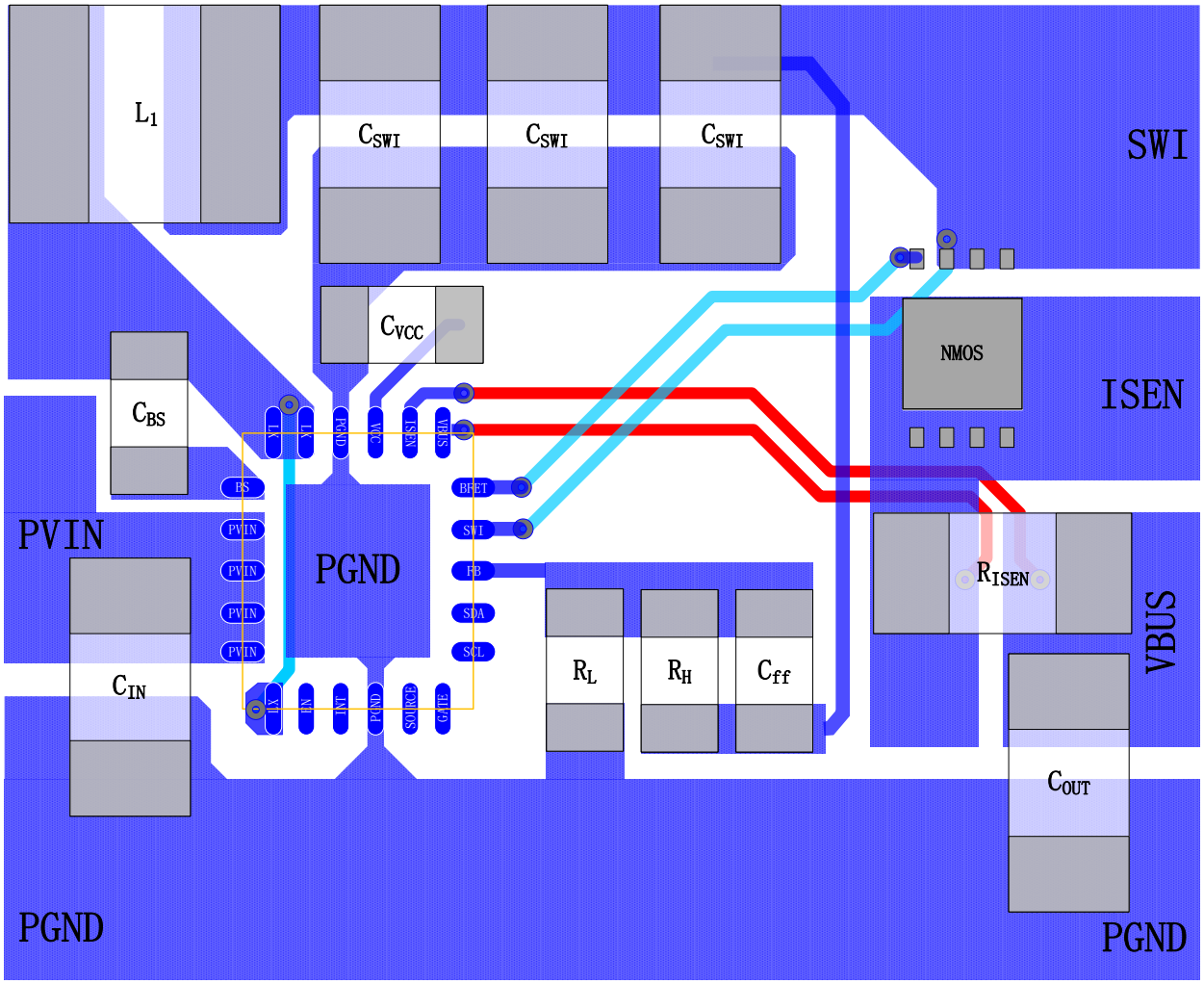
1) It is recommended to maximize the PCB copper area connected to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly recommended.

2) C_{IN} must be close to Pin PVIN and GND. The loop area formed by C_{IN} and GND must be minimized.

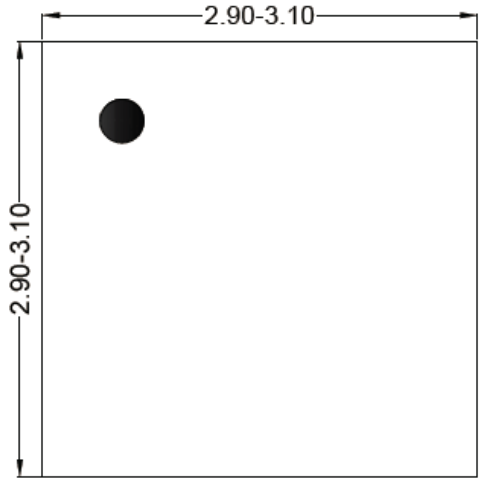
3) C_{VCC} should be placed close to VCC pin and GND pin.

4) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

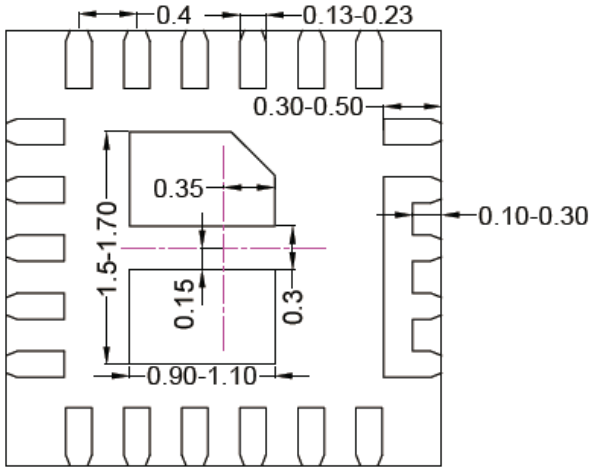
5) The feedback components R_H and R_L, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.



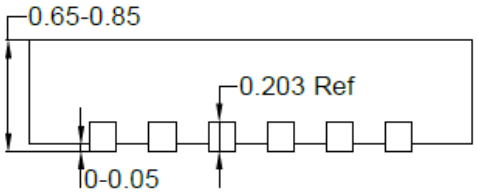
QFN3X3-19 Package Outline Drawing



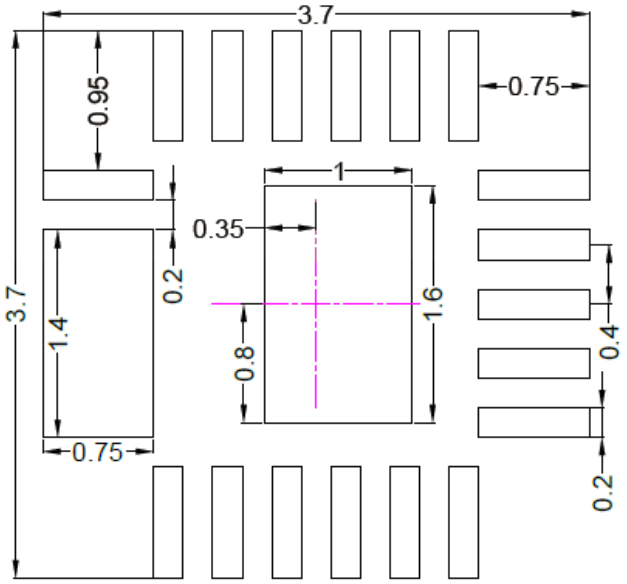
Top view



Bottom view



Front view



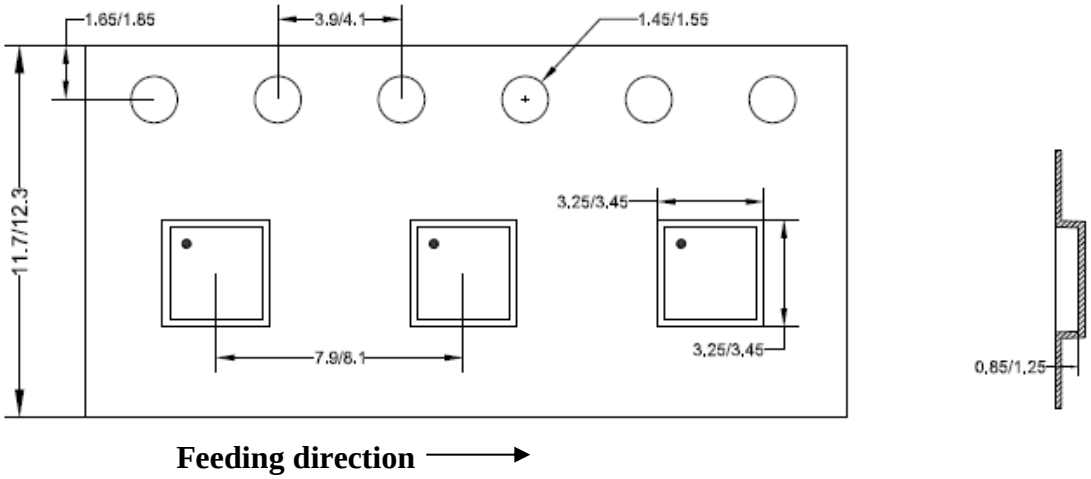
Recommended PCB layout
(Reference only)

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr;
2, the center line on PCB refers the chip body center.

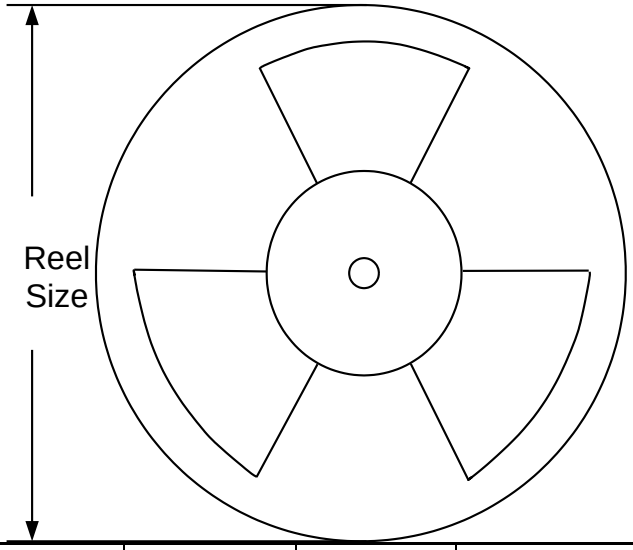
Taping & Reel Specification

1. Taping Orientation

QFN3x3



2. Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3x3	12	8	13"	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change	Pages Changed
Jan.18, 2021	Revision 0.9	Initial risk production release.	-
May.06, 2022	Revision 0.9A	Added description of “UL 2367 Certified”	Page1
Mar.20, 2025	Revision 1.0	Initial production release.	-

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