SY8970

High Efficiency High Integration PMIC for SSD System

General Description

The SY8970 is an integrated power management unit. It is designed to power a wide range of microcontrollers and solid-state drive applications.

The device includes a load switch, 3 buck converters using integrated power FETs and a low-dropout regulator (LDO). Each buck converter switches at 2 MHz, requiring three small components for operation. All regulators can be configured for a wide range of output voltages through the I^2C interface.

The SY8970 is available in a Fan-out CSP3.2x4.2-48 package.

Ordering Information

SY8970 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8970UBC	Fan-out CSP3.2x4.2-48	

Features

- 2.4V to 5.5V Input Voltage Range
- Channel 1 Load Switch:
  - 4.0A Output Current Capability.
  - 25mohm R_{DS}(ON)
  - 0.5ms Soft-start Time
- Channel 2 Synchronous Buck:
  - 2.5A Maximum Output Current Capability.
  - 0.8V to 2V Programmable, 12.5mV Step.
  - 50mohm/35mohm R_{DS}(ON)
  - Default output voltage V_{OUT2}=1.15V
- Channel 3 Synchronous Buck:
  - 2.5a Maximum Output Current Capability.
  - 0.8V to 2V Programmable, 12.5mV Step.
  - 50mohm/35mohm R_{DS}(ON)
  - Default output voltage V_{OUT3}=1.5V/1.35V
- Channel 4 Synchronous Buck:
  - 2.5A Maximum Output Current Capability.
  - 0.8V to 2V Programmable, 12.5mV Step
  - 50mohm/35mohm R_{DS}(ON)
  - Default Output Voltage V_{OUT4}=1.8V
- Channel 6 LDO:
  - 200mA Maximum Output Current Capability.
  - 0.8V to 2V Programmable, 25mV Step.
  - Default Output Voltage V_{OUT5}=1.8V
- I^2C Interface up to 3.4MHz
- Auto PWM/PFM or Forced PWM Controlled by I^2C Interface
- Output Voltage Level of Each Channel Controlled by I^2C Interface
- Reliable Protections:
  - Input / Output over Voltage Protection (OVP)
  - Short Circuit Protection (SCP)
  - Over Temperature Protection (OTP)
- Compact Package: Fan-out CSP3.2x4.2-48

Applications

- SSD Power System
- Microcontroller

Typical Applications

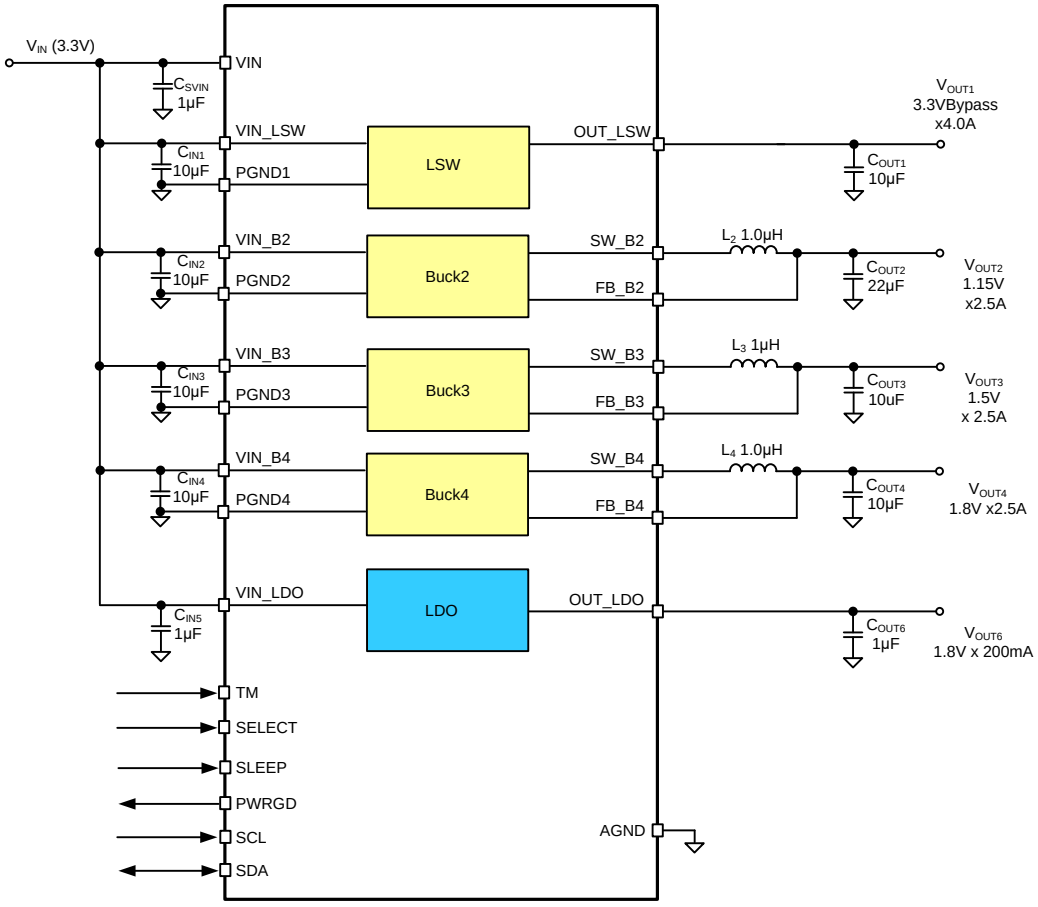
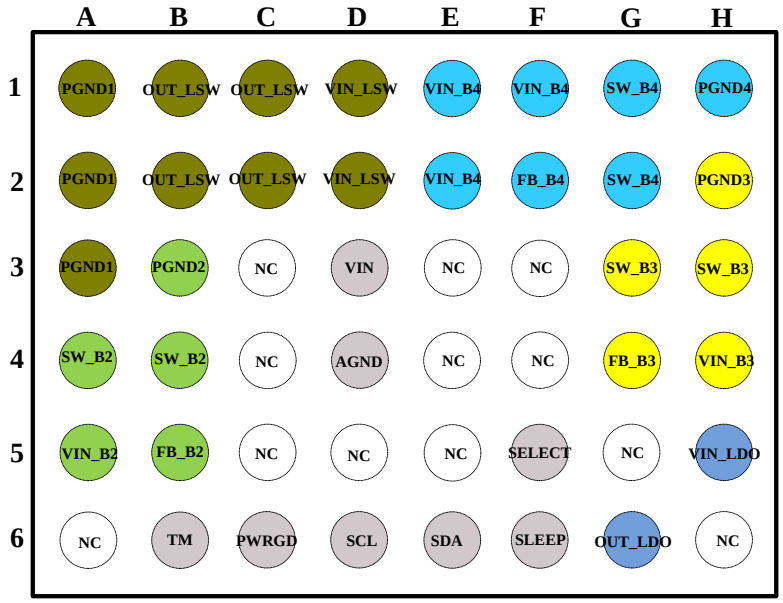


Figure1. Schematic Diagram

Pin out (Top View)



(Fan-out CSP3.2x4.2-48)

Top mark: **CCW*xyz***(Device code: CCW, ***x=year code, y=week code, z= lot number code***)

Pin Number	Pin Name	Pin Description
A1,A2,A3	PGND1	Power ground for LSW.
B1,B2,C1,C2	OUT_LSW	Output pin for LSW.
D1,D2	VIN_LSW	Power input pin for LSW.
E3	NC	Not connected.
B3	PGND2	Power ground for Buck2.
A4,B4	SW_B2	Switch node pin for Buck2.
A5	VIN_B2	Power input pin for Buck2.
B5	FB_B2	Feedback pin for Buck2.
H2	PGND3	Power ground for Buck3.
H4	VIN_B3	Power input pin for Buck3.
G3,H3	SW_B3	Switch node pin for Buck3.
G4	FB_B3	Feedback pin for Buck3.
H1	PGND4	Power ground pin for Buck4.
E1,E2,F1	VIN_B4	Power input pin of Buck4.
G1,G2	SW_B4	Switch node pin for Buck4.
F2	FB_B4	Feedback pin for Buck4.
A6	NC	Not connected.
B6	TM	Test mode pin, factory use only. This pin is internally pulled low, leave it floating.
H5	VIN_LDO	Power input pin for LDO.
G6	OUT_LDO	Power output pin for LDO (Leave it unconnected if LDO is not used and disabled).
H6	NC	Not connected.

C3	NC	Not connected.
C4	NC	Not connected.
C5	NC	Not connected.
C6	PWRGD	Power good indicator, open drain output. This pin is pulled high when all outputs are above power good threshold and below over voltage threshold. Otherwise, it is pulled low.
D3	VIN	Analog input supply.
D4	AGND	Analog ground.
D5	NC	Not connected.
D6	SCL	I^2C clock input.
E4	NC	Not connected.
E5	NC	Not connected.
E6	SDA	I^2C data input and output.
F3	NC	Not connected.
F4	NC	Not connected.
F5	SELECT	Buck3 default voltage select pin. Pulling low sets the default Buck3 voltage to 1.5V. Pulling high sets the Buck3 default voltage to 1.35V.
F6	SLEEP	The SLEEP pin controls the IC's sleep state. Pulling SLEEP low to enter sleep, pulling SLEEP high to quit sleep.
G5	NC	Not connected.

Absolute Maximum Ratings (Note 1)

All Pins Voltage---------- -0.3V to 6.0V

Power Dissipation,

P_D @ T_A = 25°C Fan-out CSP3.2x4.2-48---------- TBD

Package Thermal Resistance (Note 2)

θ_{JA}, Fan-out CSP3.2x4.2-48---------- TBD

θ_{JC}, Fan-out CSP3.2x4.2-48 ---------- TBD

Junction Temperature Range ---------- -40°C to 150°C

Lead Temperature (Soldering, 10 sec.) ---------- 260°C

Storage Temperature Range ---------- -55°C to 150°C

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 2.6V to 3.9V

Junction Temperature Range ---------- -40°C to 125°C

Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN}=3.3V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
UVLO						
VIN Rising Threshold	$V_{UVLO,RISING}$			2.5	2.6	V
VIN UVLO Hysteresis	$V_{UVLO,HYS}$	Buck UVLO hysteresis		100		mV
Quiescent Current						
Supply Current		All OFF		40		µA
		All ON, No load, PFM		180		
SLEEP , SELECT						
Logic Level High	V_{HIGH}		1.2			V
Logic Level Low	V_{LOW}				0.4	V
Deglitch Time				5		µs
I²C COMPATIBLE I/O (SDA,SCL)						
Maximum Operating Frequency	f_{SCL}				3.4	MHz
SDA And SCL Pin Input Logic Thresholds	Logic low				0.4	V
	Logic high		1.2			V
Load Switch						
Load Switch Current Limit			5			A
Load Switch R_{ON}				25		mΩ
Load Switch Current Shutdown Deglitch Time		Shut down all after deglitch time		200		µs
Short Circuit Protection Threshold	V_{SCP1}			70		$\%V_{IN}$
Short Circuit Protection Deglitch Time	t_{SCP1}			50		µs
Power Good Threshold		V_{OUT_LSW} rising		85		$\%V_{IN}$
Power Good Hysteresis		V_{OUT_LSW} falling		3		$\% V_{IN}$
Soft Start Time		10% to 90% of V_{NOM}		500		µs
Discharge Resistor	R_{DIS1}	V_{IN}=3.3V		8		Ω
BUCK2						
Output Voltage Default Value	$V_{OUT2,DEF}$			1.15		V
Voltage Step	$V_{OUT2\ STEP}$	Controllable by I²C interface		12.5		mV
Voltage Range	V_{OUT2}	Controllable by I²C interface	0.8		2.0	V
Output voltage Accuracy	ΔV_{OUT2}	PWM mode operation	-1		+1	%
Power Good Threshold		V_{OUT2} rising		90		$\%V_{NOM}$
Power Good Hysteresis		V_{OUT2} falling		3		$\%V_{NOM}$
Switching Frequency	f_{OSC2}			2		MHz
Main PFET R_{ON}	$R_{DS(ON),P2}$			50		mΩ
Synchronous NFET R_{ON}	$R_{DS(ON),N2}$			35		mΩ
High side FET Current Limit	I_{LIM2_HS}		4			A
Low side FET Current Limit	I_{LIM2_LS}		2.5			A
Max Output DC Load Current	I_{OUT2}		2.5			A
Internal Soft-start Time	t_{SS2}	10% to 90% of V_{NOM}		500		µs

Ripple Noise at Load Transient between 0A to 2.5A.		Rising and falling time from 0% to 100%: 10μs	-5		+5	%
Start-up Default Delay Time	t_{DELAY2}	Default delay time		1500		μs
Discharge Resistor	R_{DIS2}	V_{IN}=3.3V		10		Ω
OVP Threshold	V_{OVP2}		115	120	125	%
OVP Deglitch Time	t_{OVP2}			10		μs
Short Circuit Protection Threshold	V_{SCP2}			30		%
Short Circuit Protection Deglitch Time	t_{SCP2}			50		μs
BUCK3						
Output Voltage Default Value	$V_{OUT3,DEF}$			1.5		V
Voltage Step	$V_{OUT3,STEP}$	Controllable by I²C interface		12.5		mV
Voltage Range		Controllable by I²C interface	0.8		2.0	V
Output Voltage Accuracy	ΔV_{OUT3}	PWM mode operation	-1		+1	%
Power Good Threshold		V_{OUT3} rising		90		$\%V_{NOM}$
Power Good Hysteresis		V_{OUT3} falling		3		$\%V_{NOM}$
Switching Frequency	f_{OSC3}			2		MHz
Main PFET R_{ON}	$R_{DS(ON),P3}$			50		mΩ
Synchronous NFET R_{ON}	$R_{DS(ON),N3}$			35		mΩ
High Side FET Current Limit	I_{LIM3_HS}		4			A
Low Side FET Current Limit	I_{LIM2_LS}		2.5			A
Max Output DC Load Current	I_{OUT3}		2.5			A
Internal Soft-start Time	t_{SS3}	10% to 90% of V_{NOM}		500		μs
Ripple Noise at Load Transient between 0A to 2.5A.		Rising and falling time from 0% to 100%: 10μs	-5		+5	%
Start-up Default Delay Time	t_{DELAY3}	Default delay time		4500		us
Discharge Resistor	R_{DIS3}	V_{IN}=3.3V		10		Ω
OVP Threshold	V_{OVP3}		115	120	125	%
OVP Deglitch Time	t_{OVP3}			10		μs
Short Circuit Protection Threshold	V_{SCP3}			30		%
Short Circuit Protection Deglitch Time	t_{SCP3}			50		μs
BUCK4						
Output Voltage Default Value	$V_{OUT4,DEF}$			1.8		V
Voltage Step	$V_{OUT4,STEP}$	Controllable by I²C interface		12.5		mV
Voltage Range		Controllable by I²C interface	0.8		2.0	V
Output voltage Accuracy	ΔV_{OUT4}	PWM mode operation	-1		+1	%
Power Good Threshold		V_{OUT_B4} rising		90		$\%V_{NOM}$
Power Good Hysteresis		V_{OUT_B4} falling		3		$\%V_{NOM}$
Switching frequency	f_{OSC4}			2		MHz
Main PFET R_{ON}	$R_{DS(ON),P4}$			50		mΩ
Synchronous NFET R_{ON}	$R_{DS(ON),N4}$			35		mΩ

High side FET Current Limit	I_{LIM4_HS}		4			A
Low side FET Current Limit	I_{LIM4_LS}		2.5			A
Max output DC load current	I_{OUT4}		2.5			A
Internal Softstart Time	t_{SS4}	10% to 90% of V_{NOM}		500		µs
Ripple Noise at load transient between 0A to 2.5A.		Rising and falling time from 0% to 100%: 10µs	-5		+5	%
Start-up default delay time	t_{DELAY4}	Default delay time		3500		us
Discharge Resistor	R_{DIS4}	V_{IN}=3.3V		10		Ω
OVP Threshold	V_{OVP4}		115	120	125	%
OVP Deglitch Time	t_{OVP4}			10		µs
Short Circuit Protection Threshold	V_{SCP4}			30		%
Short Circuit Protection Deglitch Time	t_{SCP4}			50		µs
LDO						
Output Voltage Range		Controllable by I^2C interface	0.8		2.0	V
Output Voltage Accuracy		V_{IN_LDO}-V_{OUT_LDO}>0.4V	-1	V_{SET}	1	%
Power Good Threshold		V_{OUT_LDO} rising		90		%V_{NOM}
Power Good Hysteresis		V_{OUT_LDO} falling		3		%V_{NOM}
Output Voltage Step				25		mV
Current Limit	I_{LIM5}		0.29			A
Current Limit Shutdown Deglitch Time		Asserts SCP		200		µs
Max output DC load current	I_{OUT5}		0.2			A
Dropout Voltage		V_{IN}=3.3V,I_{OUT}=0.15A		285	500	mV
Internal Soft-start Time	t_{SS5}	10% to 90% of V_{NOM}		200		µs
Start-up Default Delay Time	t_{DELAY5}	Default delay time		500		us
Discharge Resistor	R_{DIS5}	V_{IN}=3.3V		30		Ω
OVP Threshold	V_{OVP5}		115	120	125	%
OVP Deglitch Time	t_{OVP5}		-	10	-	µs
Short Circuit Protection Threshold	V_{SCP5}			30		%
Short Circuit Protection Deglitch Time	t_{SCP5}			50		µs
Power Supply Rejection Rate	PSRR	f=100Hz, I_{LOAD}=100mA, V_{OUT_LDO}=1.8V		-50		dB
		f=100kHz, I_{LOAD}=100mA, V_{OUT_LDO}=1.8V		-25		
Overall Protection						
Thermal Shutdown Temperature				160		°C
Thermal Shutdown Hysteresis				15		°C
VIN OVP Threshold			3.8	3.9	4.0	V
VIN OVP Hysteresis				0.3		V
VIN OVP Deglitch Time				20		µs

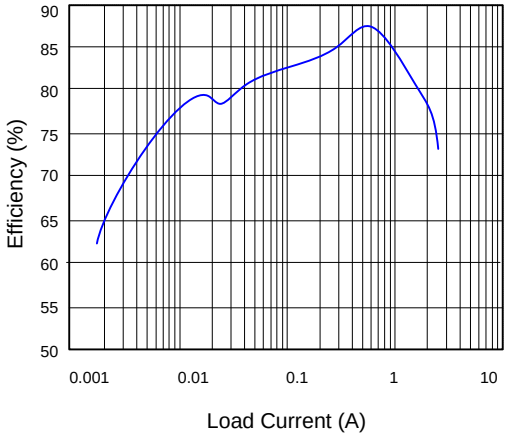
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a four-layer Silergy Evaluation Board.

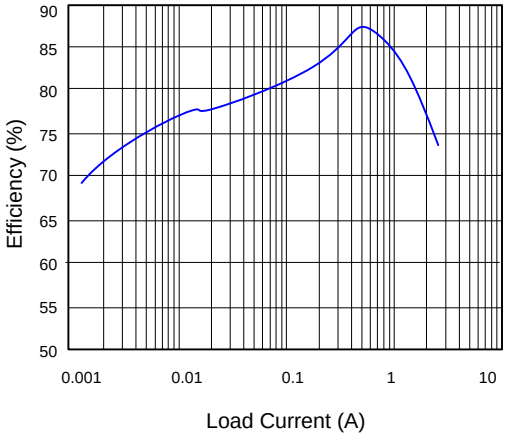
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

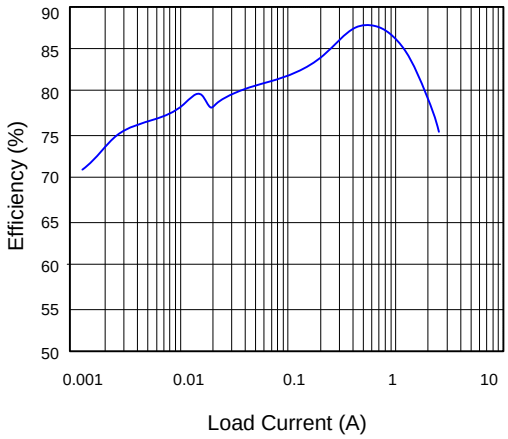
CH2 Buck(1.15V) Efficiency @3.3VIN



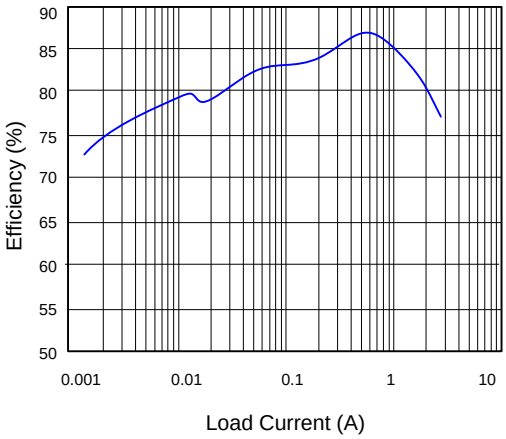
CH3 Buck(1.35V) Efficiency @3.3VIN



CH3 Buck(1.5V) Efficiency @3.3VIN

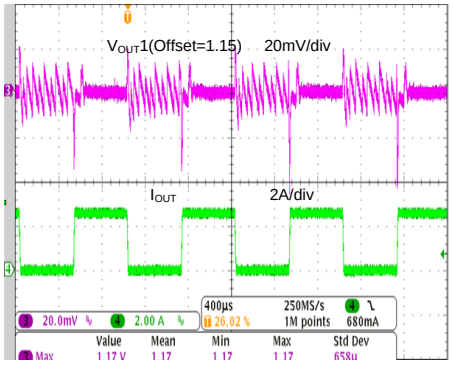


CH4 Buck(1.8V) Efficiency @3.3VIN



Load Transient

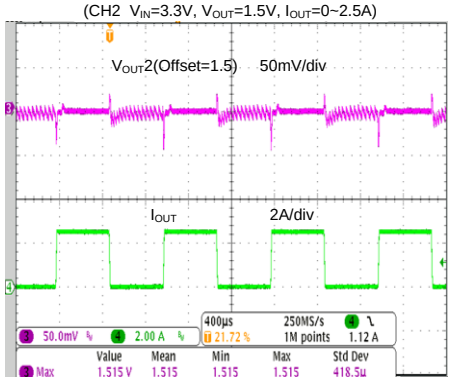
(CH1 V_{IN}=3.3V, V_{OUT}=1.15V, I_{OUT}=0~2.5A)



Time (400µs/div)

Load Transient

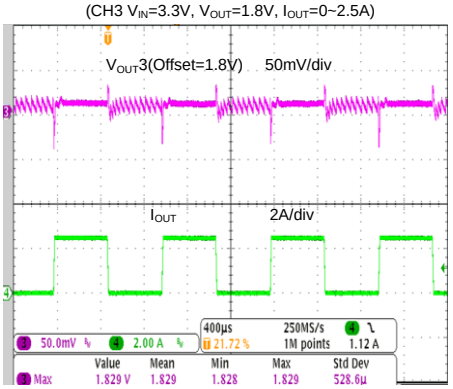
(CH2 V_{IN}=3.3V, V_{OUT}=1.5V, I_{OUT}=0~2.5A)



Time (400µs/div)

Load Transient

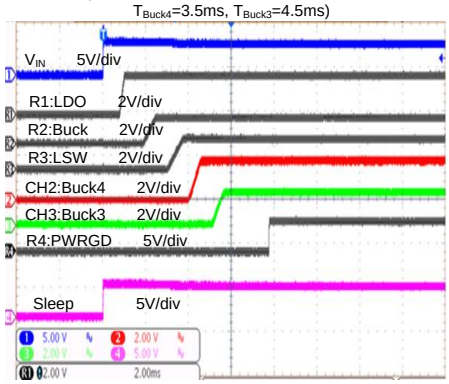
(CH3 V_{IN}=3.3V, V_{OUT}=1.8V, I_{OUT}=0~2.5A)



Time (400µs/div)

Startup Sequence

(T_{LDO}=0.5ms, T_{Buck2}=1.5ms, T_{LSW}=2.5ms, T_{Buck4}=3.5ms, T_{Buck3}=4.5ms)



Time (2ms/div)

Application Information

1. Overview

The SY8970 is an integrated power management unit. It is designed to power a wide range of microcontrollers and solid-state drive applications. It includes a load switch and 3 buck converters with integrated power FETs and a low-dropout regulator (LDO). Each buck converter switches at 2MHz, requiring three small components for operation. All regulators can be configured for a wide range of output voltages through the I^2C interface.

SY8970 Ouptut voltage and maximum current and delay time is as below table:

	Output Program range (V)	Output Program Step (mV)	Default Voltage (V)	IOUT MAX (A)	ILIM (A)	Discharge Resistor (Ω)	Startup Delay (ms)	Soft Start Time (ms)
LSW	-	-	bypass	4	6	4.4	2.5	0.5
BUCK2	0.8-2	12.5	1.15	2.5	4	9.4	1.5	0.5
BUCK3	0.8-2	12.5	1.5/1.35	2.5	4	9.4	4.5	0.5
BUCK4	0.8-2	12.5	1.8	2.5	4	9.4	3.5	0.5
LDO	0.8-2	25	1.8	0.2	0.29	50	0.5	0.2

SELECT pin is used to select Buck3 default output voltage. Pull it low to set the default Buck3 voltage to 1.5V. and pull it high to set Buck3 default voltage to 1.35V.

	SELECT	V_{OUT3}
Buck3	0	1.5V
	1	1.35V

2. VIN Power-on / Power-off Sequence

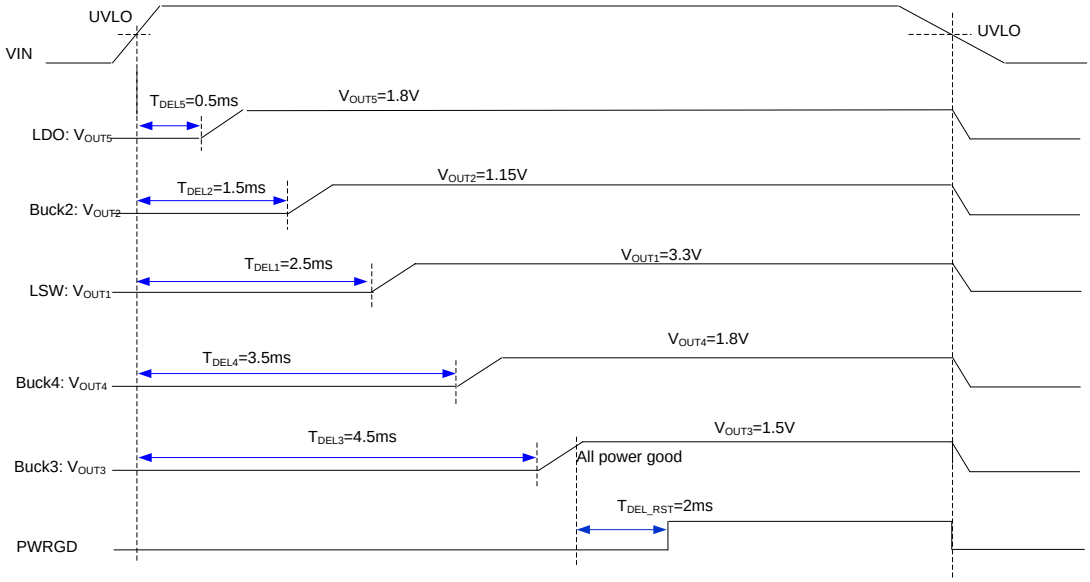


Figure2. VIN Power on/off Sequence

(1) When VIN exceeds UVLO rising threshold, every channel will start up after a fixed delay time T_{DELn} which are listed below table. If VIN is smaller than UVLO falling threshold, all channels will be turned off immediately.

	Start-up delay time	Soft-start time
LSW	T_{DEL1}=2.5ms	0.5ms
BUCK2	T_{DEL2}=1.5ms	0.5ms
BUCK3	T_{DEL3}=4.5ms	0.5ms
BUCK4	T_{DEL4}=3.5ms	0.5ms
LDO	T_{DEL5}=0.5ms	0.2ms

(2) PWRGD is open drain output. It will be high impedance when all outputs are above power good threshold and below over voltage threshold. The delay from all power good to PWRGD pulled high is typically 2ms. It will be pulled low immediately when any output goes out of regulation. Note that PWRGD stays high in sleep mode.

(3) If VIN_Bx/SW_Bx/FB_Bx pins are in floating status, the channel will be disabled at VIN power on, and the floating channel will not affect PWRGD.

3 Sleep Control

SLEEP pin is used to control PMIC enter dedicated sleep mode to save power consumption in some low power requirement application. The IC enters sleep mode when pulling the SLEEP pin low, and exit sleep while pulling the SLEEP pin high.

Each channel can be set on or off in the sleep mode. The channel will turn off at same time if they are set off at sleep mode as they enter the sleep state. And they will turn on with power up sequence when they exit the sleep state. Buck 2~4 can be programmed to regulate to VSET1 voltage or turned off in the sleep state. The LDO can be programmed to regulate to their VSET voltage or can be programmed to be turned off.

Under no fault condition, PWRGD will stay high in sleep mode although some channels are turned off. If any channel that stay on in sleep mode goes out of regulation, the PWRGD pin will be pulled low.

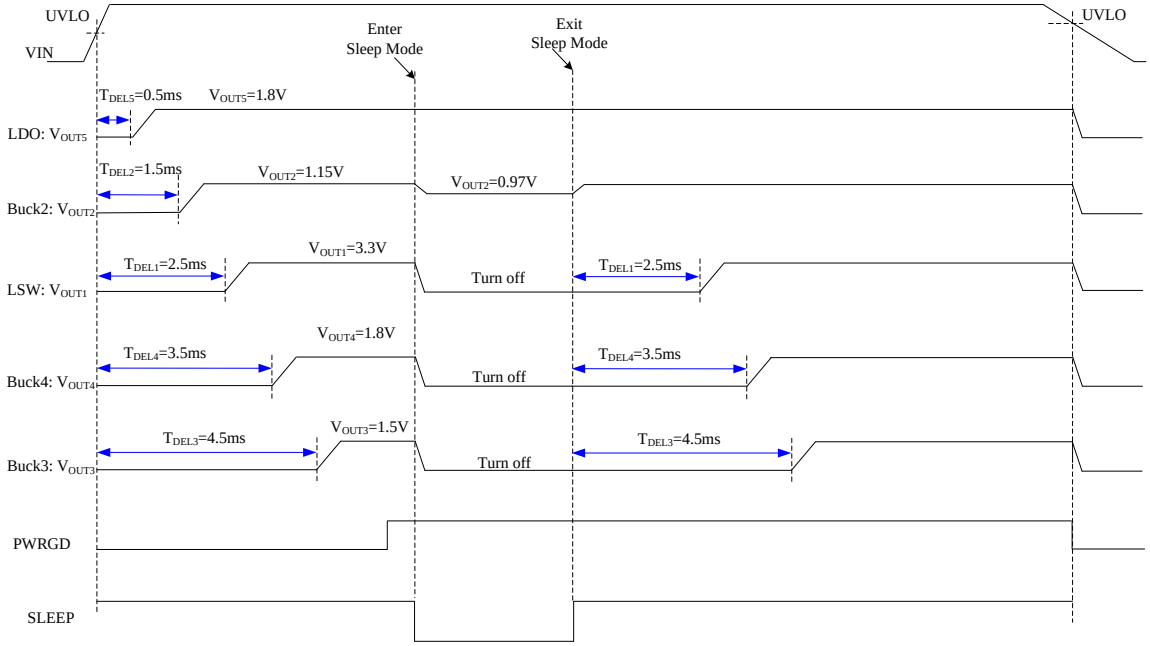


Figure 1. Sleep Control

4. Protection Function

SY8970 protection mode is as below table.

	Threshold	Action
Output OVP	120%	Shutdown all for 100ms then restart with power up sequence
Output short circuit	30%	Shutdown all for 100ms then restart with power up sequence
Input OVP	3.9V	When VIN rise above 3.9V, shutdown all. When VIN decrease below falling threshold, restart with power up sequence.
Thermal Shutdown	160 ℃	When temperature exceeds 160℃, shutdown all. When temperature decreases to 145℃.Restart following the power up sequence
Current Limit	Buck	Limit HS and LS current cycle by cycle
	LDO	Limit LDO current
	LSW	Limit load switch current

4.1. Output Over Voltage and Short Circuit Protection

If one output enters short or over voltage condition, the IC shuts down all outputs for 100ms then restarts with power up sequence. If the short or over voltage condition still exists in the active state the IC returns to the shutdown all for 100ms until the fault condition is removed.

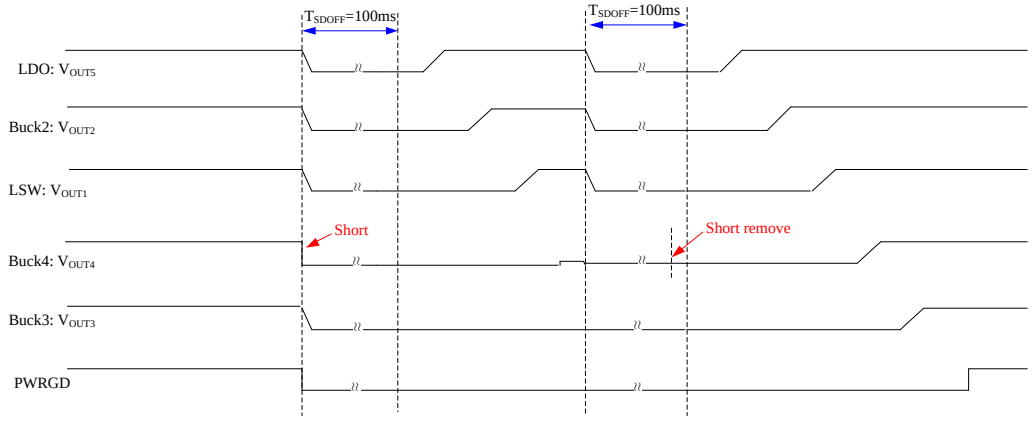


Figure 7. Short circuit protection

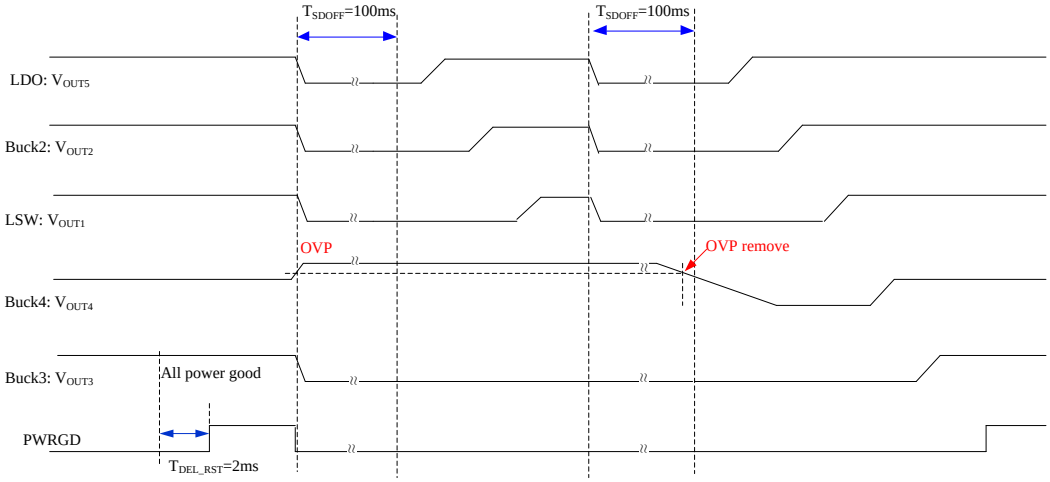


Figure 8. Output over voltage protection

4.2. Input Over Voltage Protection

VIN OVP threshold is 3.9V. When VIN exceeds 3.9V, all channels will be turned off. The OVP hysteresis is 0.3V. When VIN decreases to 3.6V, all channels will restart follow power on sequence.

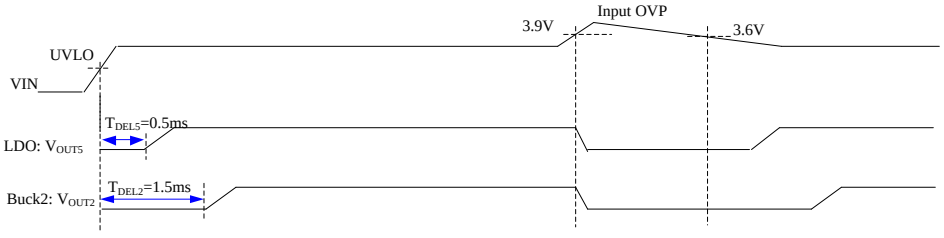


Figure 9. Input over voltage protection

4.3. Thermal Shutdown

A thermal shutdown is implemented to prevent damage because of excessive heat and power dissipation. Once the junction temperature exceeds 150℃ the device shuts down whole chip. When the temperature decreases to 135℃ the device automatically restarts performing the start-up sequencing with the same voltages .

4.4 Output Current Limit

The Buck converter limits the HS switch current and LS switch current in each switching cycle. This reduces the effective duty cycle and causes the output voltage to drop, potentially creating a short circuit condition, and causing the IC to turn off all supplies off for 100ms then restart with sequence.

For LDO, when the output current reaches the current limit threshold, the LDO will limit the output current. If current limit loop functions for 200μs or short circuit is detected, the IC will be shut down for 100ms then restart with sequence

For load switch, when the output current exceeds 6A, the IC will limit the current. If current limit loop functions for 200μs the IC will be shut down for 100ms then restart with sequence.

I²C Compatible Interface

The SY8970 features an I²C interface that allows the HOST processor to control the output voltage level of all channels. The I²C interface supports clock speeds up to 3.4MHz and uses standard I²C commands. The Device always operates as a slave device, and is addressed using a 7-bit slave address followed by an 8th bit, which indicates whether the transaction is a read-operation or a write-operation.

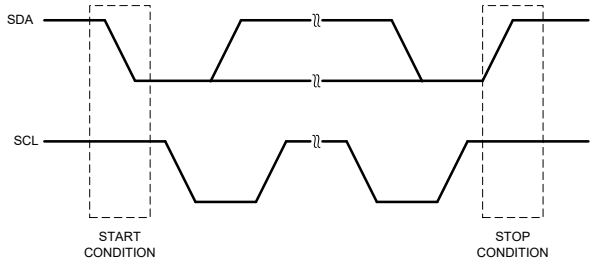
I²C address of the device consists of 8-bit data. The LSB determines the read or write mode. LSB=0 indicates Write mode and LSB=1 indicates Read mode.

The slave address is as below table:

Binary	Hex	Read/Write
0101 1010	0x5A	Write
0101 1011	0x5B	Read

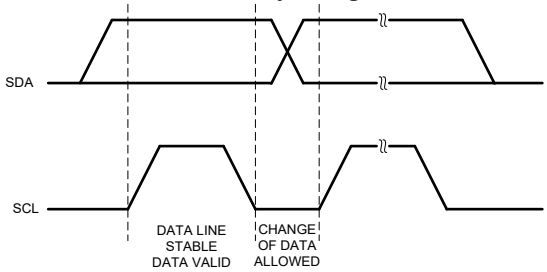
START and STOP Conditions

The device is controlled via an I²C compatible interface. The START condition is a HIGH to LOW transition on the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition. The I²C master always generates the START and STOP conditions.



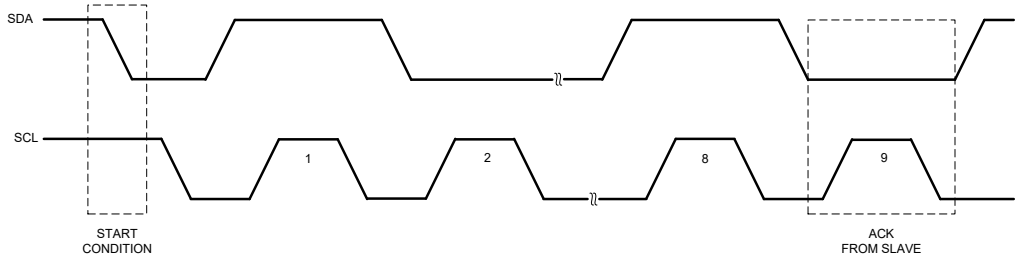
Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.



Acknowledge

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the master sends 7-slave address bits and an R/$\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address will hold the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.

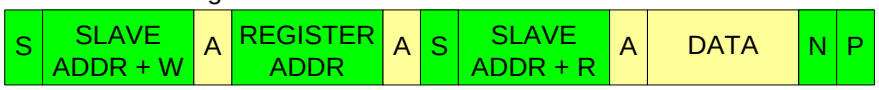


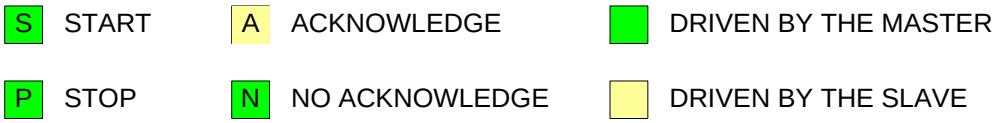
Data Transactions

All transactions start with a control byte sent from the I²C master device. The control byte begins with a START condition, followed by 7-bit of slave address (0101101x) for the device (this address can be changed if necessary) followed by the 8th bit, R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a write or 1 for a read. If any slave devices on the I²C bus recognize their address, they will acknowledge by pulling the SDA line low for the last clock cycle in the control byte. If no slaves exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition. Once the control byte is sent, and the device acknowledges it, the 2nd byte sent by the master must be a register address byte. The register address byte tells the device which registers the master will write or read. Once the device receives a register address byte will respond with an Acknowledge.

Write To A Register

Read From A Register





Register Map summary

Major register	Register Address
Master Reg	0x00h to 0x2Fh
LSW Reg	0x30h to 0x3Fh
Buck2 Reg	0x40h to 0x4Fh
Buck3 Reg	0x50h to 0x5Fh
Buck4 Reg	0x60h to 0x6Fh
Discharge Reg	0x70h to 0x7Fh
LDO Reg	0x80h to 0x8Fh

Master Registers

MSTR00 – Master Configuration Register

Address=0x00h	Default =0x80h	

Bit	7	6	5	4	3	2	1	0
Name	PWRGD_ MASK	RFU	RFU	RFU	RFU	RFU	RFU	RFU
Default	1	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
PWRGD_MASK	0 – Masks PWRGD output 1 –Unmasks PWRGD output	When masked, PWRGD will not be asserted low when its associated power supplies drop out of regulation When unmasked, PWRGD will not be pulled low when normal turn off some channel in sleep mode until fault is triggered.
RFU[6:0]	Reserved for future use	

MSTR0C – Master Configuration Register

Address=0x0Ch		

Bit	7	6	5	4	3	2	1	0
Name	LSW_OC	BUCK2_SCP	BUCK3_SCP	BUCK4_SCP	LDO_SCP	TSD	RFU	RFU
Default	-	-	-	-	-	-	-	-
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
LSW_OC	0-LSW not triggered current shutdown 1-LSW triggered current shutdown	It latches a 1 when current shutdown is triggered until the VIN power is recycled
BUCK2_SCP	0 –BUCK2 not detected short circuit 1 –BUCK2 detected short circuit	It latches a 1 when short circuit is detected until the VIN power is recycled
BUCK3_SCP	0 –BUCK3 not detected short circuit 1 –BUCK3 detected short circuit	It latches a 1 when short circuit is detected until the VIN power is recycled
BUCK4_SCP	0 –BUCK4 not detected short circuit 1 –BUCK4 detected short circuit	It latches a 1 when short circuit is detected until the VIN power is recycled
LDO_SCP	0 –LDO not detected short circuit 1 –LDO detected short circuit	It latches a 1 when short circuit is detected until the VIN power is recycled
TSD	0 –IC temperature is below the thermal shutdown temperature 1 –IC temperature is above the thermal shutdown temperature	It latches a 1 when thermal shutdown temperature is exceeded until the VIN power is recycled
RFU[1:0]	Reserved for future use	

MSTR0D – Master Configuration Register

Address=0x0Dh		

Bit	7	6	5	4	3	2	1	0
Name	VIN_OV	BUCK2_OV	BUCK3_OV	BUCK4_OV	LDO_OV	RFU	RFU	RFU
Default	-	-	-	-	-	-	-	-
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
VIN_OV	0-VIN voltage is below the input OVP threshold 1- VIN voltage is above the input OVP threshold	It latches a 1 when over voltage is detected until the VIN power is recycled
BUCK2_OV	0 –BUCK2 not detected over voltage 1 –BUCK2 detected over voltage	It latches a 1 when over voltage is detected until the VIN power is recycled
BUCK3_OV	0 –BUCK3 not detected over voltage 1 –BUCK3 detected over voltage	It latches a 1 when over voltage is detected until the VIN power is recycled
BUCK4_OV	0 –BUCK4 not detected over voltage 1 –BUCK4 detected over voltage	It latches a 1 when over voltage is detected until the VIN power is recycled
LDO_OV	0 –LDO not detected over voltage 1 –LDO detected over voltage	It latches a 1 when over voltage is detected until the VIN power is recycled
RFU[2:0]	Reserved for future use	

LSW Registers

LSW_REG03 – LSW Configuration Register

Address=0x33h	Default =0x52h	

Bit	7	6	5	4	3	2	1	0
Name	RFU	RFU	RFU	SLEEPEN	RFU	RFU	RFU	RFU
Default	0	1	0	1	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU[7:5]]	Reserved for future use	
SLEEPEN	0 – LSW stays on when the IC enters Sleep mode 1 – LSW turns off when the IC enters Sleep mode	
RFU[3:0]	Reserved for future use	

Buck2 Registers

B2_VSET01 – Buck2 Voltage Set1 Register

Address=0x41h	Default =0x1Ch	

Bit	7	6	5	4	3	2	1	0
Name	B2_VSET1[7:0]							
Default	0	0	0	1	1	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Buck2 output voltage setting in sleep mode

The output voltage is equal to B2_VSET1*0.0125+0.8V

Code	Vout(V)	Code	Vout(V)	Code	Vout(V)	Code	Vout(V)
0	0.8	100000	1.2	1000000	1.6	1100000	2
1	0.8125	100001	1.2125	1000001	1.6125	1100001	2
10	0.825	100010	1.225	1000010	1.625	1100010	2
11	0.8375	100011	1.2375	1000011	1.6375	1100011	2
100	0.85	100100	1.25	1000100	1.65	1100100	2
101	0.8625	100101	1.2625	1000101	1.6625	1100101	2
110	0.875	100110	1.275	1000110	1.675	1100110	2
111	0.8875	100111	1.2875	1000111	1.6875	1100111	2
1000	0.9	101000	1.3	1001000	1.7	1101000	2
1001	0.9125	101001	1.3125	1001001	1.7125	…	…
1010	0.925	101010	1.325	1001010	1.725	11111111	2
1011	0.9375	101011	1.3375	1001011	1.7375		
1100	0.95	101100	1.35	1001100	1.75		
1101	0.9625	101101	1.3625	1001101	1.7625		
1110	0.975	101110	1.375	1001110	1.775		
1111	0.9875	101111	1.3875	1001111	1.7875		
10000	1	110000	1.4	1010000	1.8		
10001	1.0125	110001	1.4125	1010001	1.8125		
10010	1.025	110010	1.425	1010010	1.825		
10011	1.0375	110011	1.4375	1010011	1.8375		
10100	1.05	110100	1.45	1010100	1.85		
10101	1.0625	110101	1.4625	1010101	1.8625		
10110	1.075	110110	1.475	1010110	1.875		
10111	1.0875	110111	1.4875	1010111	1.8875		
11000	1.1	111000	1.5	1011000	1.9		
11001	1.1125	111001	1.5125	1011001	1.9125		
11010	1.125	111010	1.525	1011010	1.925		
11011	1.1375	111011	1.5375	1011011	1.9375		
11100	1.15	111100	1.55	1011100	1.95		
11101	1.1625	111101	1.5625	1011101	1.9625		
11110	1.175	111110	1.575	1011110	1.975		
11111	1.1875	111111	1.5875	1011111	1.9875		

B2_VSET00 – Buck2 Voltage Set0 Register

Address=0x42h	Default =0x1Ch	

Bit	7	6	5	4	3	2	1	0
Name	B2_VSET0[7:0]							
Default	0	0	0	1	1	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Buck2 output voltage setting in active mode

The output voltage is equal to B2_VSET0*0.0125+0.8V

Code	Vout(V)	Code	Vout(V)	Code	Vout(V)	Code	Vout(V)
0	0.8	100000	1.2	1000000	1.6	1100000	2
1	0.8125	100001	1.2125	1000001	1.6125	1100001	2
10	0.825	100010	1.225	1000010	1.625	1100010	2
11	0.8375	100011	1.2375	1000011	1.6375	1100011	2
100	0.85	100100	1.25	1000100	1.65	1100100	2
101	0.8625	100101	1.2625	1000101	1.6625	1100101	2
110	0.875	100110	1.275	1000110	1.675	1100110	2
111	0.8875	100111	1.2875	1000111	1.6875	1100111	2
1000	0.9	101000	1.3	1001000	1.7	1101000	2
1001	0.9125	101001	1.3125	1001001	1.7125	…	…
1010	0.925	101010	1.325	1001010	1.725	11111111	2
1011	0.9375	101011	1.3375	1001011	1.7375		
1100	0.95	101100	1.35	1001100	1.75		
1101	0.9625	101101	1.3625	1001101	1.7625		
1110	0.975	101110	1.375	1001110	1.775		
1111	0.9875	101111	1.3875	1001111	1.7875		
10000	1	110000	1.4	1010000	1.8		
10001	1.0125	110001	1.4125	1010001	1.8125		
10010	1.025	110010	1.425	1010010	1.825		
10011	1.0375	110011	1.4375	1010011	1.8375		
10100	1.05	110100	1.45	1010100	1.85		
10101	1.0625	110101	1.4625	1010101	1.8625		
10110	1.075	110110	1.475	1010110	1.875		
10111	1.0875	110111	1.4875	1010111	1.8875		
11000	1.1	111000	1.5	1011000	1.9		
11001	1.1125	111001	1.5125	1011001	1.9125		
11010	1.125	111010	1.525	1011010	1.925		
11011	1.1375	111011	1.5375	1011011	1.9375		
11100	1.15	111100	1.55	1011100	1.95		
11101	1.1625	111101	1.5625	1011101	1.9625		
11110	1.175	111110	1.575	1011110	1.975		
11111	1.1875	111111	1.5875	1011111	1.9875		

B2_REG03 – Buck2 Configuration Register

Address=0x43h	Default =0xC2h	

Bit	7	6	5	4	3	2	1	0
Name	RFU	RFU	RFU	SLEEPEN	RFU	RFU	RFU	RFU
Default	1	1	0	0	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU[7:5]]	Reserved for future use	
SLEEPEN	0 – Buck2 stays on when the IC enters sleep mode 1 – Buck2 turns off when the IC enters sleep mode	
RFU[3:0]	Reserved for future use	

B2_REG06 – Buck2 Configuration Register

Address=0x46h	Default =0x5Eh	

Bit	7	6	5	4	3	2	1	0
Name	RFU	RFU	DISLPM	RFU	RFU	RFU	RFU	RFU
Default	0	1	0	1	1	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU[7:6]]	Reserved for future use	
DISLPM	0 – Low power mode enabled (PFM) 1 – Low power mode disabled (Forced PWM)	
RFU[4:0]	Reserved for future use	

Buck3 Registers

B3_VSET00 – Buck3 Voltage Set0 Register

Address=0x51h	Default =0x2Ch/0x38h	

Bit	7	6	5	4	3	2	1	0
Name	B3_VSET0[7:0]							
Default	0	1	0	1	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Buck3 output voltage setting in active mode
Pulling SELECT low sets the default voltage to 1.5V, default code=00111000
Pulling SELECT high sets the default voltage to 1.35V, default code=00101100

Code	Vout(V)	Code	Vout(V)	Code	Vout(V)	Code	Vout(V)
0	0.8	100000	1.2	1000000	1.6	1100000	2
1	0.8125	100001	1.2125	1000001	1.6125	1100001	2
10	0.825	100010	1.225	1000010	1.625	1100010	2
11	0.8375	100011	1.2375	1000011	1.6375	1100011	2
100	0.85	100100	1.25	1000100	1.65	1100100	2
101	0.8625	100101	1.2625	1000101	1.6625	1100101	2
110	0.875	100110	1.275	1000110	1.675	1100110	2
111	0.8875	100111	1.2875	1000111	1.6875	1100111	2
1000	0.9	101000	1.3	1001000	1.7	1101000	2
1001	0.9125	101001	1.3125	1001001	1.7125	…	…
1010	0.925	101010	1.325	1001010	1.725	11111111	2
1011	0.9375	101011	1.3375	1001011	1.7375		
1100	0.95	101100	1.35	1001100	1.75		
1101	0.9625	101101	1.3625	1001101	1.7625		
1110	0.975	101110	1.375	1001110	1.775		
1111	0.9875	101111	1.3875	1001111	1.7875		
10000	1	110000	1.4	1010000	1.8		
10001	1.0125	110001	1.4125	1010001	1.8125		
10010	1.025	110010	1.425	1010010	1.825		
10011	1.0375	110011	1.4375	1010011	1.8375		
10100	1.05	110100	1.45	1010100	1.85		
10101	1.0625	110101	1.4625	1010101	1.8625		
10110	1.075	110110	1.475	1010110	1.875		
10111	1.0875	110111	1.4875	1010111	1.8875		
11000	1.1	111000	1.5	1011000	1.9		
11001	1.1125	111001	1.5125	1011001	1.9125		
11010	1.125	111010	1.525	1011010	1.925		
11011	1.1375	111011	1.5375	1011011	1.9375		
11100	1.15	111100	1.55	1011100	1.95		
11101	1.1625	111101	1.5625	1011101	1.9625		
11110	1.175	111110	1.575	1011110	1.975		
11111	1.1875	111111	1.5875	1011111	1.9875		

B3_VSET01 – Buck3 Voltage Set1 Register

Address=0x52h	Default =0x2Ch/0x38h	

Bit	7	6	5	4	3	2	1	0
Name	B3_VSET1[7:0]							
Default	0	1	0	1	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Buck3 output voltage setting in sleep mode.
Pulling SELECT low sets the default voltage to 1.5V, default code=00111000
Pulling SELECT high sets the default voltage to 1.35V, default code=00101100

Code	Vout(V)	Code	Vout(V)	Code	Vout(V)	Code	Vout(V)
0	0.8	100000	1.2	1000000	1.6	1100000	2
1	0.8125	100001	1.2125	1000001	1.6125	1100001	2
10	0.825	100010	1.225	1000010	1.625	1100010	2
11	0.8375	100011	1.2375	1000011	1.6375	1100011	2
100	0.85	100100	1.25	1000100	1.65	1100100	2
101	0.8625	100101	1.2625	1000101	1.6625	1100101	2
110	0.875	100110	1.275	1000110	1.675	1100110	2
111	0.8875	100111	1.2875	1000111	1.6875	1100111	2
1000	0.9	101000	1.3	1001000	1.7	1101000	2
1001	0.9125	101001	1.3125	1001001	1.7125	…	…
1010	0.925	101010	1.325	1001010	1.725	11111111	2
1011	0.9375	101011	1.3375	1001011	1.7375		
1100	0.95	101100	1.35	1001100	1.75		
1101	0.9625	101101	1.3625	1001101	1.7625		
1110	0.975	101110	1.375	1001110	1.775		
1111	0.9875	101111	1.3875	1001111	1.7875		
10000	1	110000	1.4	1010000	1.8		
10001	1.0125	110001	1.4125	1010001	1.8125		
10010	1.025	110010	1.425	1010010	1.825		
10011	1.0375	110011	1.4375	1010011	1.8375		
10100	1.05	110100	1.45	1010100	1.85		
10101	1.0625	110101	1.4625	1010101	1.8625		
10110	1.075	110110	1.475	1010110	1.875		
10111	1.0875	110111	1.4875	1010111	1.8875		
11000	1.1	111000	1.5	1011000	1.9		
11001	1.1125	111001	1.5125	1011001	1.9125		
11010	1.125	111010	1.525	1011010	1.925		
11011	1.1375	111011	1.5375	1011011	1.9375		
11100	1.15	111100	1.55	1011100	1.95		
11101	1.1625	111101	1.5625	1011101	1.9625		
11110	1.175	111110	1.575	1011110	1.975		
11111	1.1875	111111	1.5875	1011111	1.9875		

B3_REG03 – Buck3 Configuration Register

Address=0x53h	Default =0x52h	

Bit	7	6	5	4	3	2	1	0
Name	RFU	RFU	RFU	SLEEPEN	RFU	RFU	RFU	RFU
Default	0	1	0	1	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU[7:5]]	Reserved for future use	
SLEEPEN	0 – Buck3 stays on when the IC enters sleep mode 1 – Buck3 turns off when the IC enters sleep mode	
RFU[3:0]	Reserved for future use	

B3_REG06 – Buck3 Configuration Register

Address=0x56h	Default =0x96h	

Bit	7	6	5	4	3	2	1	0
Name	RFU	RFU	DISLPM	RFU	RFU	RFU	RFU	RFU
Default	1	0	0	1	0	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU[7:6]]	Reserved for future use	
DISLPM	0 – Low power mode enabled (PFM) 1 – Low power mode disabled (Forced PWM)	
RFU[4:0]	Reserved for future use	

Buck4 Registers

B4_VSET00 – Buck4 Voltage Set0 Register

Address=0x61h	Default =0x50h	

Bit	7	6	5	4	3	2	1	0
Name	B4_VSET0[7:0]							
Default	0	1	0	1	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Buck4 output voltage setting in active mode

The output voltage is equal to B4_VSET0*0.0125+0.8V

Code	V_{OUT}(V)	Code	V_{OUT} (V)	Code	V_{OUT} (V)	Code	V_{OUT} (V)
0	0.8	100000	1.2	1000000	1.6	1100000	2
1	0.8125	100001	1.2125	1000001	1.6125	1100001	2
10	0.825	100010	1.225	1000010	1.625	1100010	2
11	0.8375	100011	1.2375	1000011	1.6375	1100011	2
100	0.85	100100	1.25	1000100	1.65	1100100	2
101	0.8625	100101	1.2625	1000101	1.6625	1100101	2
110	0.875	100110	1.275	1000110	1.675	1100110	2
111	0.8875	100111	1.2875	1000111	1.6875	1100111	2
1000	0.9	101000	1.3	1001000	1.7	1101000	2
1001	0.9125	101001	1.3125	1001001	1.7125	…	…
1010	0.925	101010	1.325	1001010	1.725	11111111	2
1011	0.9375	101011	1.3375	1001011	1.7375		
1100	0.95	101100	1.35	1001100	1.75		
1101	0.9625	101101	1.3625	1001101	1.7625		
1110	0.975	101110	1.375	1001110	1.775		
1111	0.9875	101111	1.3875	1001111	1.7875		
10000	1	110000	1.4	1010000	1.8		
10001	1.0125	110001	1.4125	1010001	1.8125		
10010	1.025	110010	1.425	1010010	1.825		
10011	1.0375	110011	1.4375	1010011	1.8375		
10100	1.05	110100	1.45	1010100	1.85		
10101	1.0625	110101	1.4625	1010101	1.8625		
10110	1.075	110110	1.475	1010110	1.875		
10111	1.0875	110111	1.4875	1010111	1.8875		
11000	1.1	111000	1.5	1011000	1.9		
11001	1.1125	111001	1.5125	1011001	1.9125		
11010	1.125	111010	1.525	1011010	1.925		
11011	1.1375	111011	1.5375	1011011	1.9375		
11100	1.15	111100	1.55	1011100	1.95		
11101	1.1625	111101	1.5625	1011101	1.9625		
11110	1.175	111110	1.575	1011110	1.975		
11111	1.1875	111111	1.5875	1011111	1.9875		

B4_VSET01 – Buck4 Voltage Set1 Register

Address=0x62h	Default =0x50h	

Bit	7	6	5	4	3	2	1	0
Name	B4_VSET1[7:0]							
Default	0	1	0	1	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Buck4 output voltage setting in sleep mode

The output voltage is equal to B4_VSET1*0.0125+0.8V

Code	V_{OUT} (V)	Code	V_{OUT} (V)	Code	V_{OUT} (V)	Code	V_{OUT} (V)
0	0.8	100000	1.2	1000000	1.6	1100000	2
1	0.8125	100001	1.2125	1000001	1.6125	1100001	2
10	0.825	100010	1.225	1000010	1.625	1100010	2
11	0.8375	100011	1.2375	1000011	1.6375	1100011	2
100	0.85	100100	1.25	1000100	1.65	1100100	2
101	0.8625	100101	1.2625	1000101	1.6625	1100101	2
110	0.875	100110	1.275	1000110	1.675	1100110	2
111	0.8875	100111	1.2875	1000111	1.6875	1100111	2
1000	0.9	101000	1.3	1001000	1.7	1101000	2
1001	0.9125	101001	1.3125	1001001	1.7125	…	…
1010	0.925	101010	1.325	1001010	1.725	11111111	2
1011	0.9375	101011	1.3375	1001011	1.7375		
1100	0.95	101100	1.35	1001100	1.75		
1101	0.9625	101101	1.3625	1001101	1.7625		
1110	0.975	101110	1.375	1001110	1.775		
1111	0.9875	101111	1.3875	1001111	1.7875		
10000	1	110000	1.4	1010000	1.8		
10001	1.0125	110001	1.4125	1010001	1.8125		
10010	1.025	110010	1.425	1010010	1.825		
10011	1.0375	110011	1.4375	1010011	1.8375		
10100	1.05	110100	1.45	1010100	1.85		
10101	1.0625	110101	1.4625	1010101	1.8625		
10110	1.075	110110	1.475	1010110	1.875		
10111	1.0875	110111	1.4875	1010111	1.8875		
11000	1.1	111000	1.5	1011000	1.9		
11001	1.1125	111001	1.5125	1011001	1.9125		
11010	1.125	111010	1.525	1011010	1.925		
11011	1.1375	111011	1.5375	1011011	1.9375		
11100	1.15	111100	1.55	1011100	1.95		
11101	1.1625	111101	1.5625	1011101	1.9625		
11110	1.175	111110	1.575	1011110	1.975		
11111	1.1875	111111	1.5875	1011111	1.9875		

B4_REG03 – Buck4 Configuration Register

Address=0x63h	Default =0x52h	

Bit	7	6	5	4	3	2	1	0
Name	RFU	RFU	RFU	SLEEPEN	RFU	RFU	RFU	RFU
Default	0	1	0	1	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU[7:5]]	Reserved for future use	
SLEEPEN	0 – Buck4 stays on when the IC enters sleep mode 1 – Buck4 turns off when the IC enters sleep mode	
RFU[3:0]	Reserved for future use	

B4_REG06 – Buck4 Configuration Register

Address=0x66h	Default =0xD6h	

Bit	7	6	5	4	3	2	1	0
Name	RFU	RFU	DISLPM	RFU	RFU	RFU	RFU	RFU
Default	1	1	0	1	0	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU[7:6]]	Reserved for future use	
DISLPM	0 – Low power mode enabled (PFM) 1 – Low power mode disabled (Forced PWM)	
RFU[4:0]	Reserved for future use	

Discharge control Register

DIS_REG0C – Discharge Configuration Register

Address=0x7Ch	Default =0x00h	

Bit	7	6	5	4	3	2	1	0
Name	RFU	RFU	RFU	RFU	B4_DisPulldown	B3_DisPulldown	B2_DisPulldown	B1_DisPulldown
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU[7:4]	Reserved for future use	
B4_DisPulldown	0 –Buck4 discharge switch is enabled with Buck4 is turned off 1 –Buck4 discharge switch is always disabled	
B3_DisPulldown	0 –Buck3 discharge switch is enabled with Buck3 is turned off 1 –Buck3 discharge switch is always disabled	
B2_DisPulldown	0 –Buck2 discharge switch is enabled with Buck2 is turned off 1 –Buck2 discharge switch is always disabled	
B1_DisPulldown	0 –LSW discharge switch is enabled with LSW is turned off 1 –LSW discharge switch is always disabled	

LDO Registers

LDO_VSET – LDO Voltage Set0 Register

Address=0x81h	Default =0x28h	

Bit	7	6	5	4	3	2	1	0
Name	RFU	LDO_VSET[6:0]						
Default	0	0	1	0	1	0	0	0
Access	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU	Reserved for future use	
LDO_VSET[6:0]	LDO output voltage setting	

The output voltage is equal to LDO_VSET*0.025+0.8V

Code	V_{OUT} (V)	Code	V_{OUT} (V)
0	0.8	11100	1.5
1	0.825	11101	1.525
10	0.85	11110	1.55
11	0.875	11111	1.575
100	0.9	100000	1.6
101	0.925	100001	1.625
110	0.95	100010	1.65
111	0.975	100011	1.675
1000	1	100100	1.7
1001	1.025	100101	1.725
1010	1.05	100110	1.75
1011	1.075	100111	1.775
1100	1.1	101000	1.8
1101	1.125	101001	1.825
1110	1.15	101010	1.85
1111	1.175	101011	1.875
10000	1.2	101100	1.9
10001	1.225	101101	1.925
10010	1.25	101110	1.95
10011	1.275	101111	1.975
10100	1.3	110000	2
10101	1.325	110001	2
10110	1.35	110010	2
10111	1.375	110011	2
11000	1.4	110100	2
11001	1.425	110101	2
11010	1.45	…	…
11011	1.475	1111111	2

LDO_REG02 – LDO Configuration Register

Address=0x82h	Default =0xC1h	

Bit	7	6	5	4	3	2	1	0
Name	RFU	RFU	RFU	SLEEPEN	RFU	RFU	RFU	RFU
Default	1	1	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU[7:5]]	Reserved for future use	
SLEEPEN	0 – LDO stays on when the IC enters sleep mode 1 – LDO turns off when the IC enters sleep mode	
RFU[3:0]	Reserved for future use	

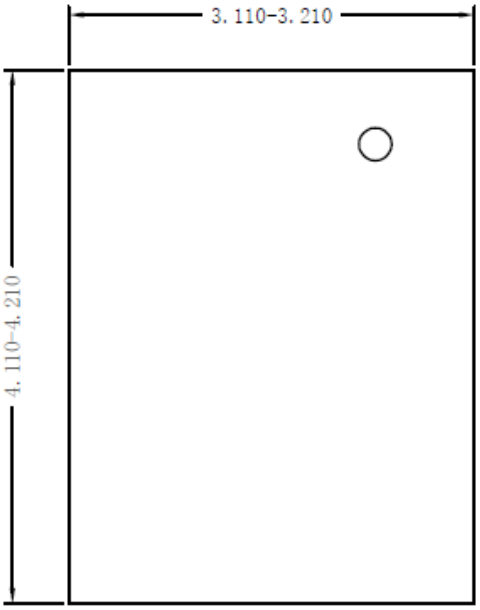
LDO_REG04 – LDO Configuration Register

Address=0x84h	Default =0x00h	

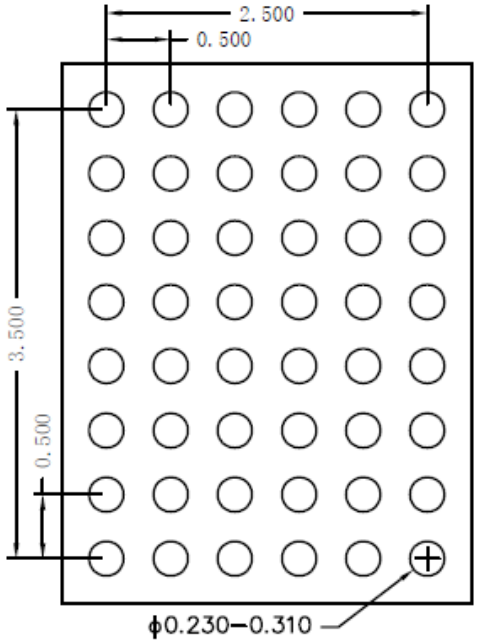
Bit	7	6	5	4	3	2	1	0
Name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	DIS_PULLDOWN
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU[7:6]	Reserved for future use	
DIS_PULLDOWN	0 – LDO discharge switch is enabled with LDO is turned off 1 – LDO discharge switch is always disabled	

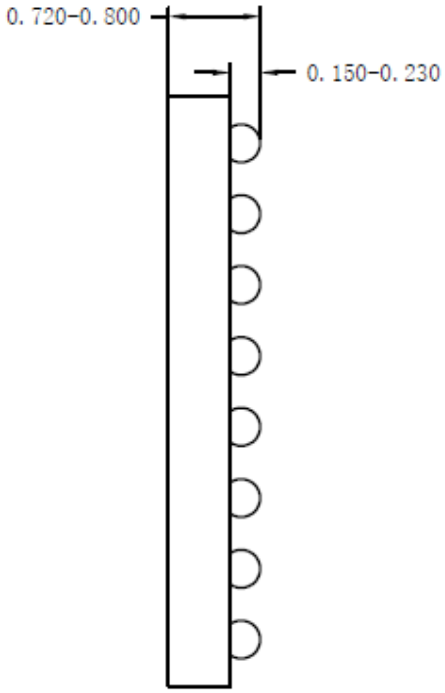
CSP3.2×4.2-48 Package Outline Drawing



Top view



Bottom view



Side view

Notes: **All dimensions in millimeter and exclude mold flash & metal burr.**

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change	Pages Changed
Jan.08, 2020	Revision 0.9	Initial risk production release.	-
Mar.07, 2025	Revision 1.0	Initial production release.	-

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