SY52542

Secondary Side Synchronous Rectifier

General Description

The SY52542 is a high performance synchronous rectification (SR) switcher, ideal for use in flyback converters operating in Continuous Conduction (CCM), Discontinuous Conduction (DCM), and Quasi-Resonant (QR) modes.

The SY52542 features DRAIN voltage falling slope rate detection to prevent false turn-on by parasitic ringing in DCM or QR modes. It also features DRAIN high voltage blanking time detection to enhance system ESD performance and prevent false turn-on of the SR MOSFET by external noise.

Under CCM operation, the SY52542 has an extremely short turn-off delay time while the DRAIN voltage regulation fully utilizes the SR MOSFET conduction time to optimize efficiency under DCM and QR modes.

During light load conditions, the device enters power saving mode to improve light load efficiency.

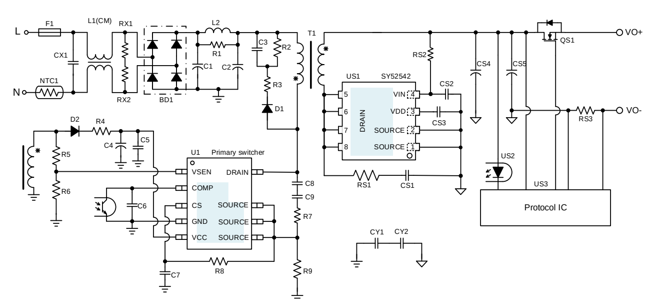
The SY52542 is available in a compact PDFN5*6-8 package.

Features

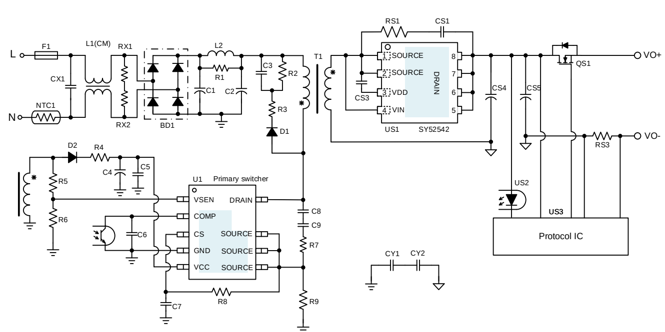
- Suitable for CCM, DCM, and QR Flyback Converters
- DRAIN Falling Slope Rate Detection to Avoid False Turn-On of SR MOSFET by Parasitic Ringing
- DRAIN High Voltage Blanking Time Detection to Enhance System ESD Performance
- Dual Source Power Supply for 3.3V to 21V Output Systems
- Compact Package: PDFN5*6-8

Applications

- AC/DC Adapters
- USB Type-C and Power Delivery AC Adapters
- Server and Telecom Power Supplies
- Auxiliary Power Supplies



SR MOSFET Location: Low Side



SR MOSFET Location: High Side

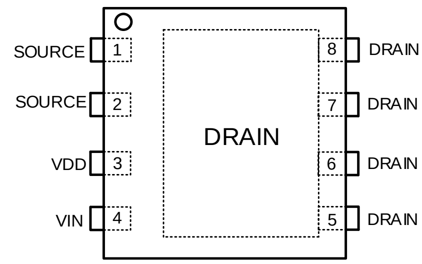
Figure 1. Typical Application Circuit

Ordering Information

Ordering Part Number	Package type	Top Mark
SY52542TVD	PDFN5*6-8 RoHS-Compliant and Halogen-Free	**AARN*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1,2	SOURCE	Source terminal of integrated SR MOS, also the analog GND.
3	VDD	Output of internal LDO, power supply for control unit and gate drive circuit. Connect a 0.47μF or larger ceramic capacitor between the VDD and SOURCE pins.
4	VIN	Power supply pin. Connect to the converter output when a low-side SR MOSFET is used. Connect to the SOURCE pin when a high-side SR MOSFET is used.
5,6,7,8	DRAIN	DRAIN terminal of integrated SR MOSFET, also used for power supply.

Block Diagram

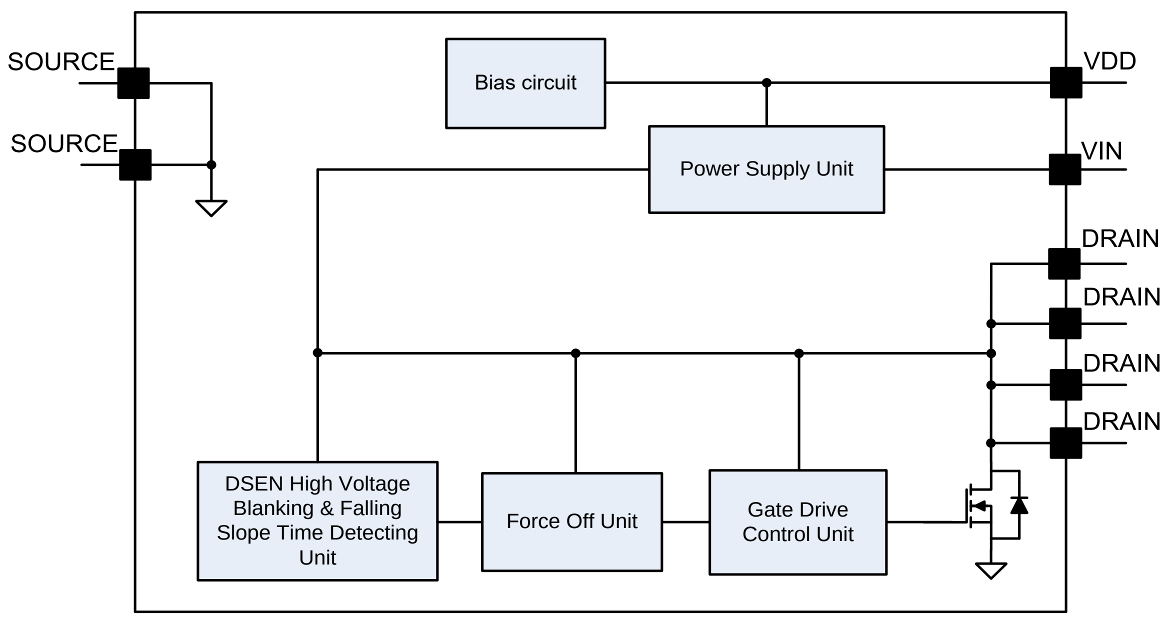


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VIN	-0.3	28	V
VDD	-0.3	16	V
DRAIN	-1	120	V
Junction Temperature, Operating	-45	150	°C
Lead Temperature (Soldering, 10s)		260	°C
Storage Temperature Range	-65	150	°C

Thermal Information

Parameter (Note 2)	Min	Max	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance		98	°C/W
θ_{JC} Junction-to-Case Thermal Resistance		14.5	°C/W
PD Power Dissipation TA = 25°C		1.3	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VIN	2.8	21	V
Junction Temperature	-40	125	°C

Electrical Characteristics

(V_{VIN} = 12V, T_A = 25°C unless otherwise specified (Note 4))

Parameter (Note 4)		Symbol	Test conditions	Min	Typ	Max	Unit
VIN	Threshold for Switching to VIN Supply	V_{VIN_VINSPY}	V_{VIN} is rising	4.35	4.6	4.85	V
	Threshold for Switching to DRAIN Supply	$V_{VIN\_DRAINSPY}$	V_{VIN} is falling	4.3	4.55	4.8	V
VDD	ON Threshold	V_{VDD_ON}		5	5.26	5.52	V
	UVLO Hysteresis	V_{VDD_HYS}		1.9	2.15	2.4	V
	VDD Regulation Voltage when VIN Pin is Active to Supply IC	$V_{VDD\_REG\_VIN}$		8.5	9	9.4	V
	VDD Regulation Voltage when DRAIN Pin is Active to Supply IC	$V_{VDD\_REG\_DRAIN}$		8.5	9	9.4	V
	Maximum VDD Pin Capacitor Charging Current	$I_{VDD\_CHARGE\_MAX}$	VIN pin is active to charge VDD capacitor	12	17		mA
			DRAIN pin is active to charge VDD capacitor	40	50		mA
	Quiescent Current	I_{VDD_STBY}	Under Standby Mode		230	280	µA
DRAIN	Blanking Time for Sample PVS Pin Voltage	t_{PVS_BLK}		210	310	410	ns
	Low Level Threshold to Sense V_{DRAIN} Falling Time	V_{DRAIN_LTH}	V_{DRAIN} is falling	10	20	30	mV
	Closed Loop V_{DRAIN} Regulation Voltage Level	V_{DS_REG}	SR MOSFET is conducting	-55	-40	-25	mV
	SR MOSFET Turn-Off Threshold	V_{OFF_TH}	V_{DRAIN} is rising	-10	0	10	mV
	Time Threshold IC Enter Sleep (Note 5)	$t_{STANDBY}$		15	20	25	µs
MOSFET	MOSFET Break down Voltage	$V_{DSS(BR)}$	V_{GS} = 0V, I_D = 0.25mA	120			V
	MOSFET On-State Resistor	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 60A		4.3	5.8	mΩ
	Continuous Drain Current (Note 5)	I_D				105	A
	Pulsed Drain Current (Note 5)	I_{DM}				420	A
Blanking Time	Minimum On-Time	t_{ON_MIN}		500	700	900	ns
	Minimum Off-Time	t_{OFF_MIN}		400	565	730	ns
OTP	Thermal Shutdown Temperature (Note 5)	T_{SD}			160		°C
	Hysteresis to Resume Operation (Note 5)	T_{OTP_HYS}			20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a 2oz two-layer Silergy evaluation board. Case temperature θ_{JC} is measured at pin 4. [Use the actual condition provided by package engineering.]

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \approx T_J$ = 25°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested. [Note 5 may be omitted if all EC parameters are tested in production.]

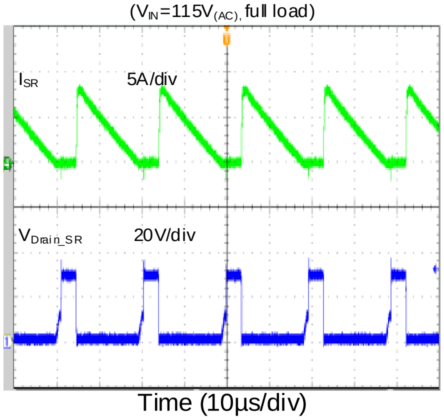
Typical Performance Characteristics

(Test condition: Input voltage: 90VAC–264VAC; Output spec: 5VDC_3A, 20VDC_3.25A; Ambient temperature: 25±5°C; Ambient humidity: 65±25 %.)

5VDC, 3A Output

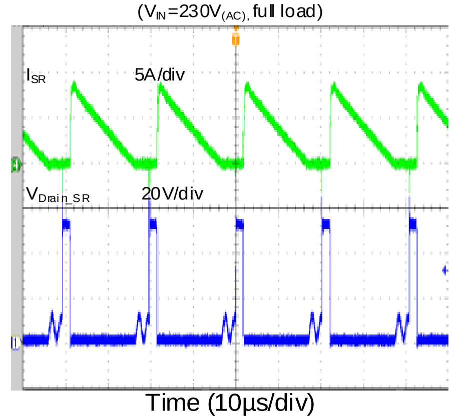
Steady States

(V_{IN}=115$V_{(AC)}$, full load)



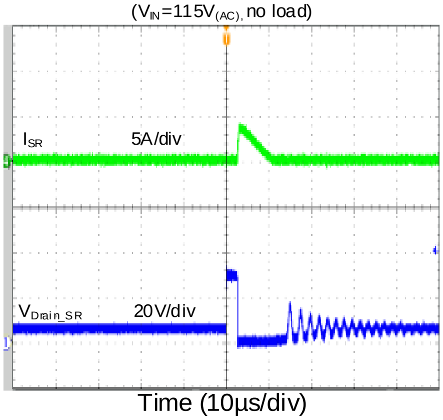
Steady States

(V_{IN}=230$V_{(AC)}$, full load)



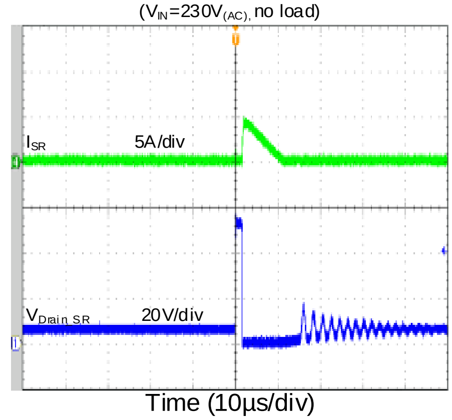
Steady States

(V_{IN}=115$V_{(AC)}$, no load)

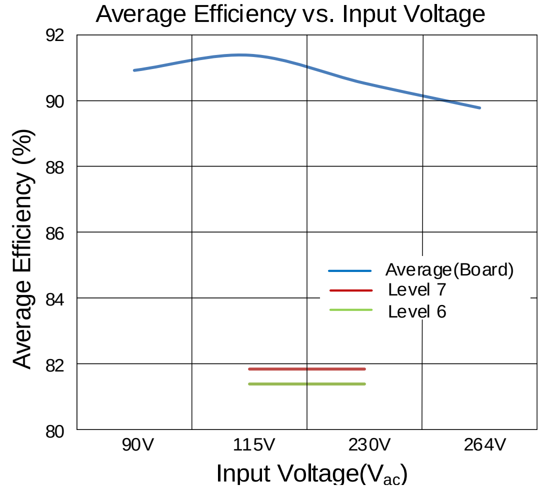


Steady States

(V_{IN}=230$V_{(AC)}$, no load)

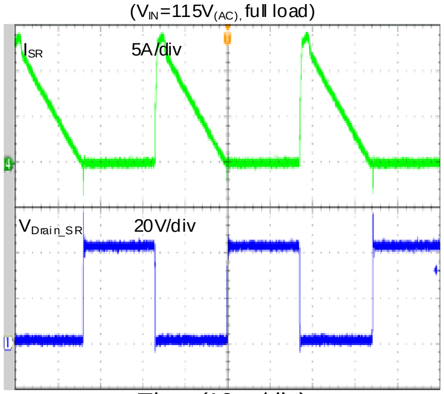


Average Efficiency vs. Input Voltage



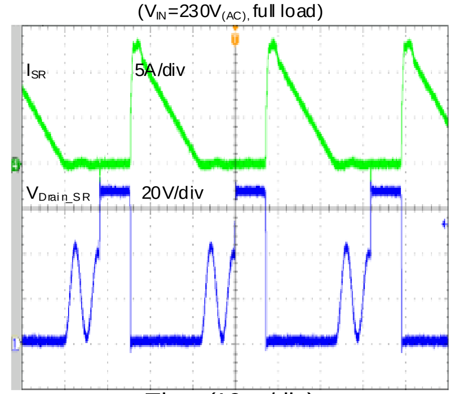
20VDC, 3.25A Output

Steady States
(V_{IN}=115$V_{(AC)}$, full load)



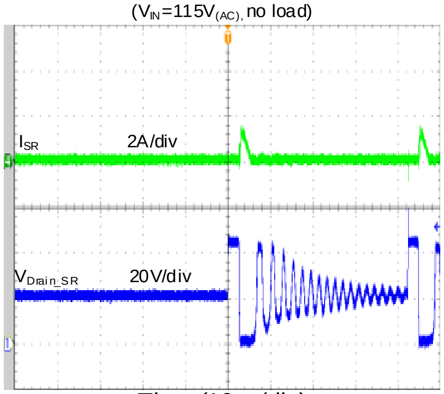
Time (10µs/div)

Steady States
(V_{IN}=230$V_{(AC)}$, full load)



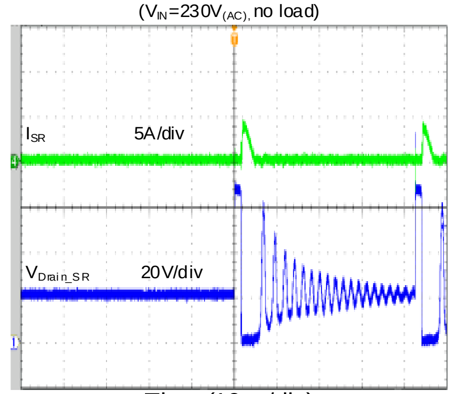
Time (10µs/div)

Steady States
(V_{IN}=115$V_{(AC)}$, no load)



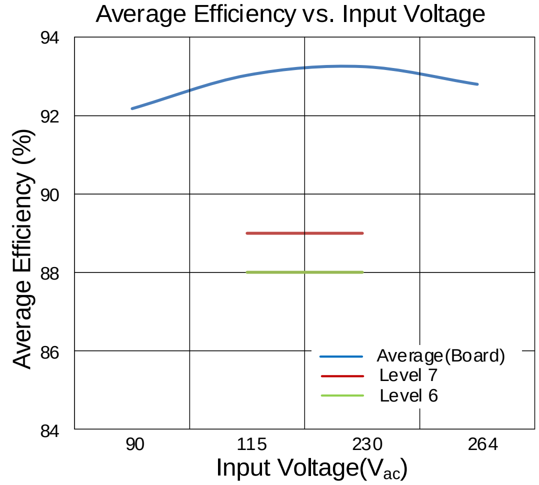
Time (10µs/div)

Steady States
(V_{IN}=230$V_{(AC)}$, no load)



Time (10µs/div)

Average Efficiency vs. Input Voltage



Detailed Description

Gate Drive

For proper operation, while $V_{VDD} < V_{VDD\_ON}$, the SR MOSFET gate is pulled down by the circuit shown in Figure 3.

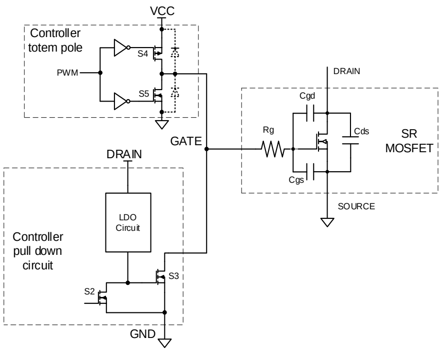


Figure 3. SR MOSFET Startup Control Circuit

When $V_{VDD} < V_{VDD\_ON}$, switch S2 is open and the DRAIN voltage charges the C_{GS} capacitor of the S3 switch. When S3 turns on, it pulls down the SR MOSFET gate. The S3 pulldown current is 200mA (@V_{GS} = 1V for the Power MOSFET) to optimize performance.

While $V_{VDD} > V_{VDD\_ON}$, the S2 switch is closed, leading to S3 being turned off (switch open). The GATE pin is controlled only by the driver circuit consisting of S4 and S5, as shown in Figure 3 and Figure 4.

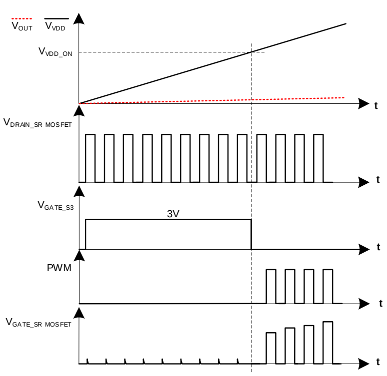


Figure 4. GATE Pin Timing Diagram

SR MOSFET Gate Control

The traditional method of turning on the SR MOSFET is to use a set turn-on threshold V_{ON_TH}. When the DRAIN voltage falls and reaches V_{ON_TH}, the SR MOSFET turns on after a short delay.

While in DCM or QR operating modes, a resonant waveform may appear after the transformer secondary current decreases to zero. Sometimes the amplitude of this resonant waveform can be large enough to cause the DRAIN voltage to drop below the turn-on threshold V_{ON_TH}, which may lead to the false turn-on of the SR MOSFET. The SY52542 uses a circuit to detect the falling slope rate of V_{DRAIN} and address this issue.

When the primary MOSFET Q1 is turned off, the V_{DRAIN} falling slope rate is very high, and the SR MOSFET will turn on. During the resonant phase, the V_{DRAIN} falling slope rate is relatively low, and the SR MOSFET will not turn on. The device uses a resistor divider circuit to sense the DRAIN voltage, where V_{PVS} is 0.02 × V_{DRAIN}.

Two thresholds are set to sense the V_{PVS} falling slope rate. △t is the time duration measured when V_{PVS} is falling between the high-level threshold V_{PVS_HTH} and the low-level threshold V_{DRAIN_LTH} (0mV). △t is compared with a falling slope reference time t_{REF} using a counter.

A blanking period is used to prevent external noise (such as ESD noise) from falsely turning on the SR MOSFET.

If V_{PVS} is greater than V_{PVS_HTH} for t_{PVS_BLK} (310ns) and the falling slope time △t < t_{REF}, the IC considers this action as a primary MOSFET turn-off event, and will turn on the SR MOSFET after a short delay. In all other cases, the SR MOSFET will not be turned on.

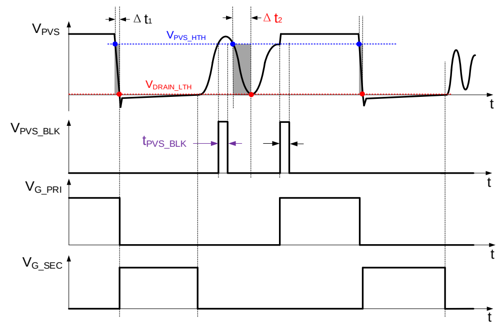


Figure 5. SR MOSFET Turn-On Timing

V_{PVS_HTH} is a dynamically adjusted value, and it has a value of 0.85 × V_{DRAIN}. The falling slope reference time threshold t_{REF} is 170ns (typ.).

In DCM mode, the current through the SR MOSFET decreases before the primary MOSFET is turned on. The closed-loop V_{DS} regulation circuit gradually reduces V_{GATE} once V_{DS} is above the V_{DS_REG} (-40mV) level. As the current through the SR MOSFET decreases, V_{GATE} drops close to the turn-off threshold of the SR MOSFET. At this point, the product (I_D × R_{DSON}) can no longer be regulated to V_{DS_REG}, causing V_{DS} to increase beyond V_{OFF_TH}. After a short delay time t_{OFF_DLY} (10ns), a large sink current pulls down the gate voltage to zero to turn off the SR MOSFET.

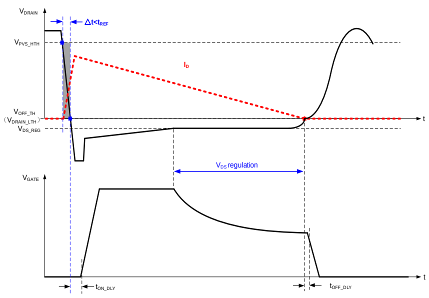


Figure 6. SR MOSFET Control in DCM Mode

During CCM mode, the primary MOSFET is turned on before secondary current decreases to zero, and V_{DRAIN} rapidly increases. The SY52542 compares V_{DRAIN} to another threshold, V_{OFF_TH}. Once V_{DRAIN} rises and crosses V_{OFF_TH}, after a short delay time t_{OFF_DLY} (10ns), the gate voltage is pulled down by a large sink current to achieve fast turn-off. The turn-off delay time t_{OFF_DLY} is designed to be very short to minimize the power loss caused by primary and secondary MOSFET overlap.

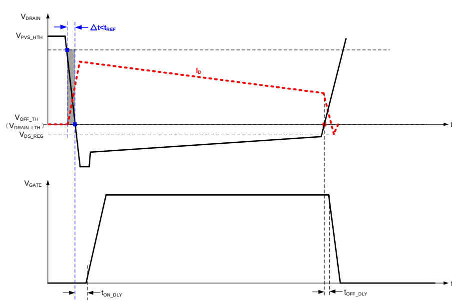


Figure 7. SR MOSFET in CCM Mode

Minimum On-Time and Minimum Off-Time

When the primary MOSFET is turned off, the DRAIN voltage of the secondary SR MOSFET drops rapidly to approximately -700mV due to the circuit parasitic resonance. To avoid false turn-off of the SR MOSFET, a blanking time t_{ON_MIN} is applied after the SR MOSFET is turned on. During this blanking time, the GATE pin output is latched off.

After the SR MOSFET is turned off, ringing will appear on the DRAIN voltage waveform. A blanking time t_{OFF_MIN} is used to prevent falsely triggering the internal logic circuit.

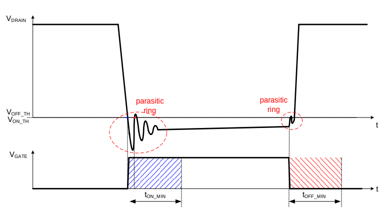


Figure 8. Minimum On-Time/Off-Time Timing

Dual-Source Power Supply

The SY52542 optimizes the overall efficiency by using two possible power sources during normal operation.

Before VDD voltage reaches the V_{VDD_ON} threshold, voltage is supplied by the DRAIN pin. When the voltage exceeds the V_{VIN_VINSPY} threshold, the VIN pin is used instead.

As VIN increases, VDD will follow VIN (with about 0.5V voltage drop). When the voltage exceeds 9V, the rail is regulated internally to this value.

When VIN decreases and crosses $V_{VIN\_DRAINSPY}$, the SY52542 switches to using the DRAIN pin, and VDD is regulated to 9V. The timing diagram is shown in Fig. 9.

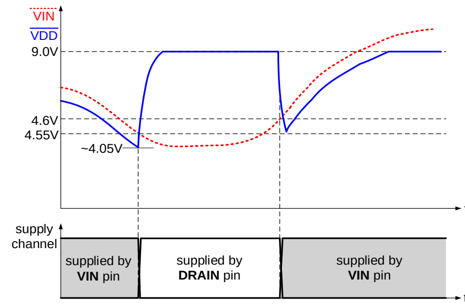


Figure 9. Dual-Source Supply Timing

Power Saving Mode

Under light load conditions, the SY52542 enters power saving mode to improve light load efficiency. During the switching cycle, a timer starts counting after the SR MOSFET is turned off. If the timer counts to 20μs before the next SR turn-on, the device enters power saving mode to reduce power consumption. The device will exit power saving mode on the next SR MOSFET turn-on event. The timing diagram is shown in Figure 10.

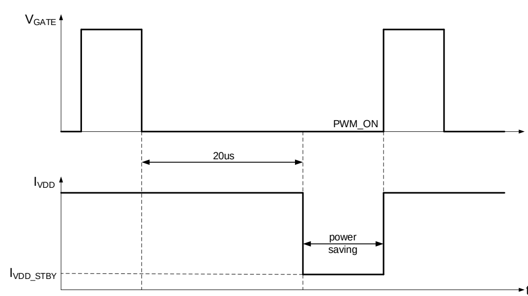


Figure 10. Power Saving Mode Timing

Over Temperature Protection

If IC die temperature rises above 160°C, the IC stops driving SR MOSFET and keeps gate voltage at 0V. When IC die temperature drops below 140°C, the IC resumes normal operation.

Application Information

RC Snubber Selection

The RC snubber components RS1 and CS1 are used to dampen the switching ringing caused by stray inductance (L_{STRAY}) and equivalent capacitance (C_{EQ}) in the secondary switching loop.

L_{STRAY} can be tested using an LCR meter. The C_{EQ} can be calculated considering the switching ringing period, based on the following formula:

$$C_{EQ} = \frac{T_r^2}{(2\pi)^2 \times L_{Stray}} = \frac{50ns^2}{(6.28)^2 * 50nH} = 1.27nF$$

Considering the Q of the circuit is equal to 1, the snubber resistor RS1 can be calculated using the following formula:

$$R_{RS1} = \frac{1}{Q}\sqrt{\frac{L_{stray}}{C_{EQ}}} = \sqrt{\frac{50nH}{1.27nF}} = 6.27\Omega$$

A value of 5.1Ω can be selected in this case.

CS1 will influence the spike of V_{DS} and thermal performance. The recommended value for CS1 is 1nF/250V.

External Components Selection

When used in the low-side configuration, the device uses two power inputs. The VIN pin is one of the supply sources, and a reservoir capacitor CS2 must be connected close to this pin.

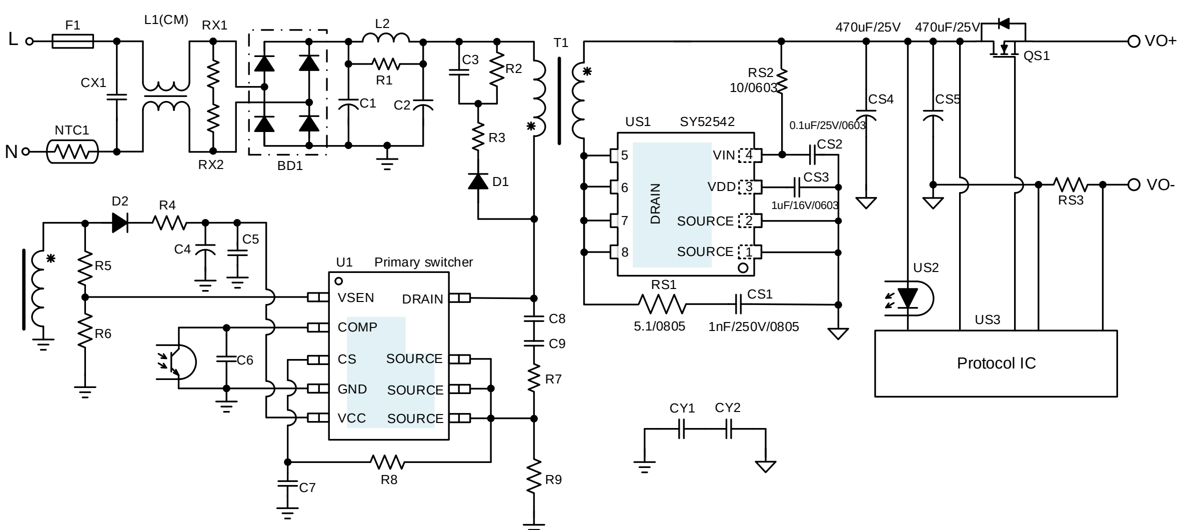
The recommended value and voltage rating for CS2 is 0.1µF/25V. The recommended value for RS2 is 10Ω. The recommended value and voltage rating for CS3 in most applications is 1µF/16V.

Design Notes

1. To prevent the SR from turning off later at no load, the SR freewheeling time should be more than the minimum on-time.
2. To improve the system ESD performance, use a 10Ω~51Ω resistor in series between the VIN pin and the output terminal, and a capacitor of at least 100nF in parallel between the VIN pin and the SOURCE pin.

Typical Application Schematic

Typical application circuit information for a 65W PD flyback design. The PD charger circuit includes a synchronous rectification switcher (SY52542).



Recommended BOM List

Designator	Description	Part Number	Manufacturer
RS1	5.1Ω/0805	0805W8F100JT5E	UNI-ROYAL
RS2	10Ω/0603	0603WAF100JT5E	UNI-ROYAL
CS1	1nF/250V/X7R, 0805	CC0805KRX7R0BB102	YAGEO

CS2	0.1uF/25V/X7R, 0603	CC0603KRX7R8BB104	YAGEO
CS3	1uF/16V/X7R, 0603	CC0603KRX7R0BB105	YAGEO
CS4, CS5	470uF/25V/Solid Cap	SPZ1EM471E14O000RAXXX	AISHI
US1	SY52542/PDFN5*6-8	SY52542TVD	Silergy

Layout Considerations

Follow these PCB Layout guidelines for optimal performance and thermal dissipation:

- Minimize the size of the switching loops: secondary power loop, secondary RC snubber circuit loop, and IC power supply loop.
- To achieve better EMI and efficiency performance, use a decoupling capacitor between the output connector and the SR MOSFET output.
- To reduce ringing, reduce the parasitic inductance by optimizing the layout and/or increasing the RC snubber.

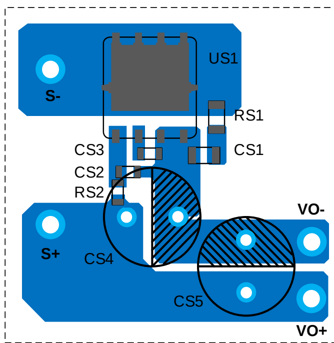
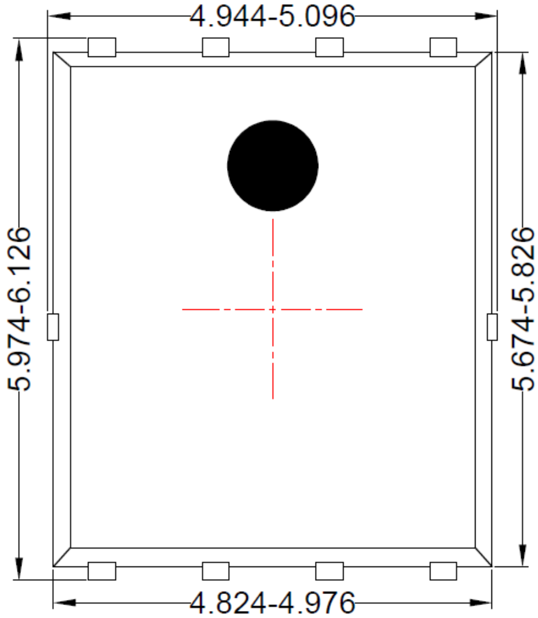
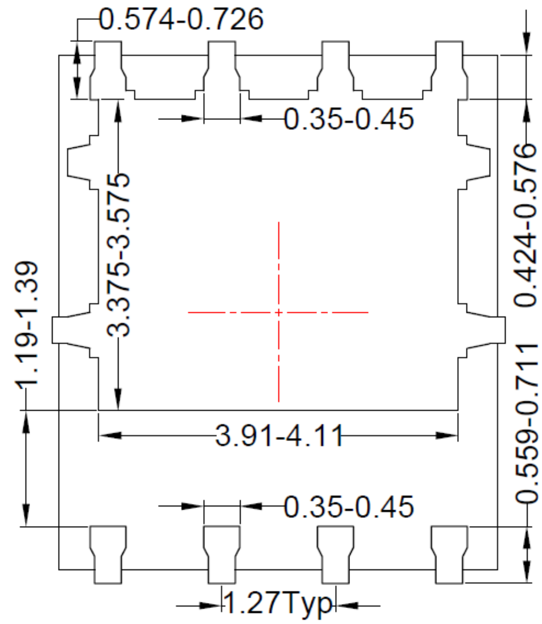


Figure 11. Suggested PCB Layout

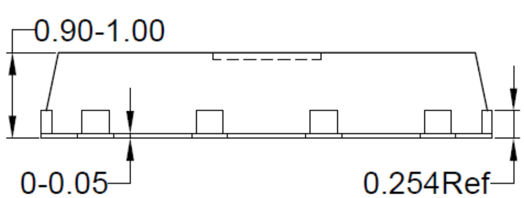
PDFN5x6-8 Package Outline & PCB Layout Design



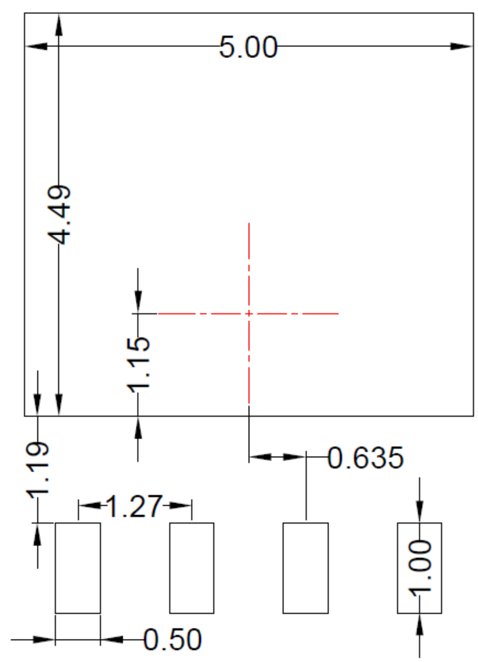
Top View



Bottom View



Front View

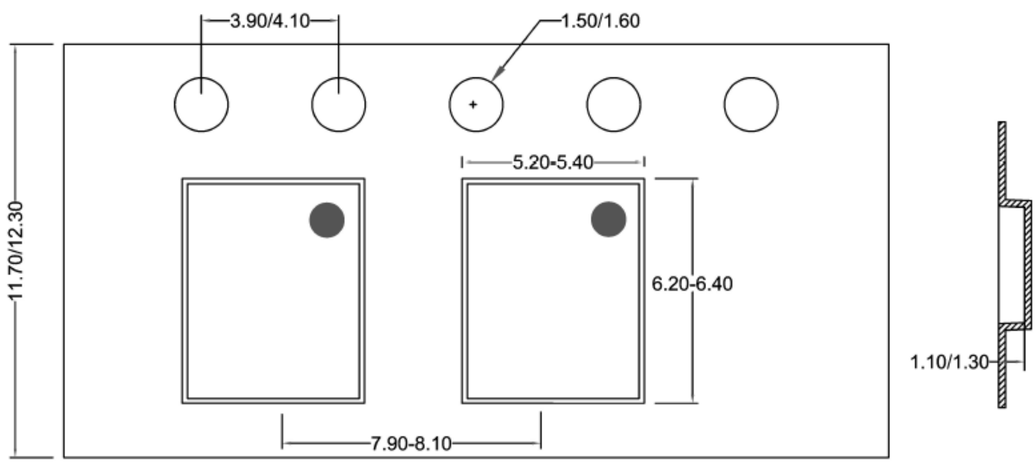


Recommended PCB layout (Reference only)

Notes: 1, all dimension in millimeter and exclude mold flash & metal burr.
2, centerline on PCB layout refers chip body center.

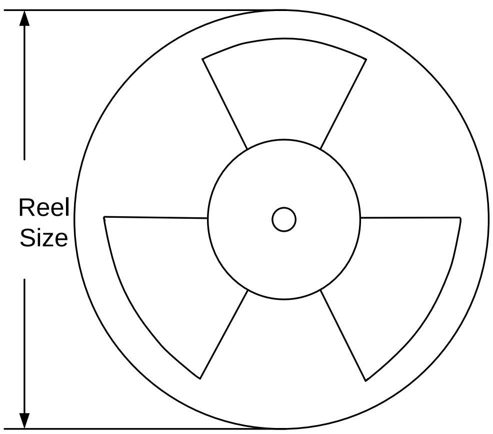
Taping & Reel Specification

1. Taping Orientation (PDFN5x6-8)



Feeding Direction

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
PDFN5*6-8	12	8	13"	400	400	5000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
March 12, 2026	Revision 1.0	Initial Release

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