SY50216N

Flyback Regulator With Primary Side CC/CV Control for Adapters and Chargers

General Description

The SY50216N is a single stage Flyback regulator targeting at Constant Current/Constant Voltage (CC/CV) applications. It integrates a 660V/2.2Ω MOSFET in a compact SO8 package to minimize the size. Both the output current and voltage are sensed on the primary side, eliminating the opto-isolator and the secondary side feedback circuitry, and minimizing the overall system cost.

The SY50216N adopts the quasi-resonant operation and the adaptive PWM/PFM control to achieve the highest average efficiency and the best EMI performance. The no-load switching frequency can be as low as 500Hz, minimizing the no-load power loss.

The SY50216N has programmable cable compensation to provide a better load regulation for the output voltage at the cable terminals.

The SY50216N provides reliable protections including VIN Over Voltage Protection, Short Circuit Protection (SCP), Over Temperature Protection (OTP), Output voltage OVP/UVP (OVP/UVP), VSEN/ISEN pin short protection, VSEN pin upper divider resistor disconnect protection, secondary side schottky diode short protection, etc.

Features

- Tight PSR CC/CV Regulation Over Entire Operating Range
- QR-mode Operation for High Efficiency
- PWM/PFM Control for High Average Efficiency
- Fast Dynamic Load Transient Response
- Cable Compensation for Better Load Regulation
- Low Start Up Current: 5μA Max
- Minimum Frequency Limitation 500Hz
- No-load Power Less Than 50mW
- Reliable Protections for OVP, UVP, SCP, OTP, OCP
- Reliable Protections for Safety Requirement
- Maximum Switching Frequency Limitation 125kHz
- Integrated 660V/2.2Ω MOSFET
- Compact Package: SO8

Applications

- AC/DC Adapters
- Battery Chargers

Recommended Operating Output Power		
Products	90~264Vac	176~264Vac
SY50216N	18W	24W

Typical Application

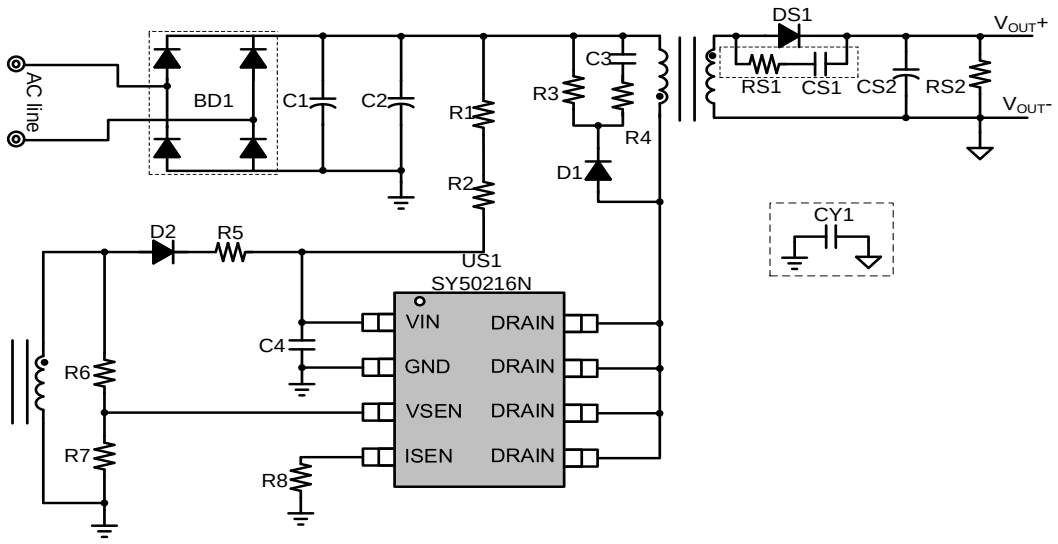


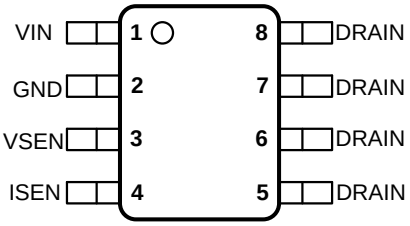
Figure 1. Typical Application Circuit

Ordering Information

Ordering Part Number	Package type	Top Mark
SY50216NFAP	SO8 RoHS-Compliant and Halogen-Free	**GKF*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	VIN	Power supply pin. Bypass this pin to the GND pin with a ceramic capacitor
2	GND	Ground pin
3	VSEN	Output voltage sense pin. This pin receives the auxiliary winding voltage by a resistor divider. The value of the resistor divider also programs the cable impedance. This pin also senses the winding voltage to provide the QR operation
4	ISEN	Current sense pin. The current sense resistor is placed between this pin and the GND pin
5	DRAIN	Drain of the internal power MOSFET
6	DRAIN	Drain of the internal power MOSFET
7	DRAIN	Drain of the internal power MOSFET
8	DRAIN	Drain of the internal power MOSFET

Block Diagram

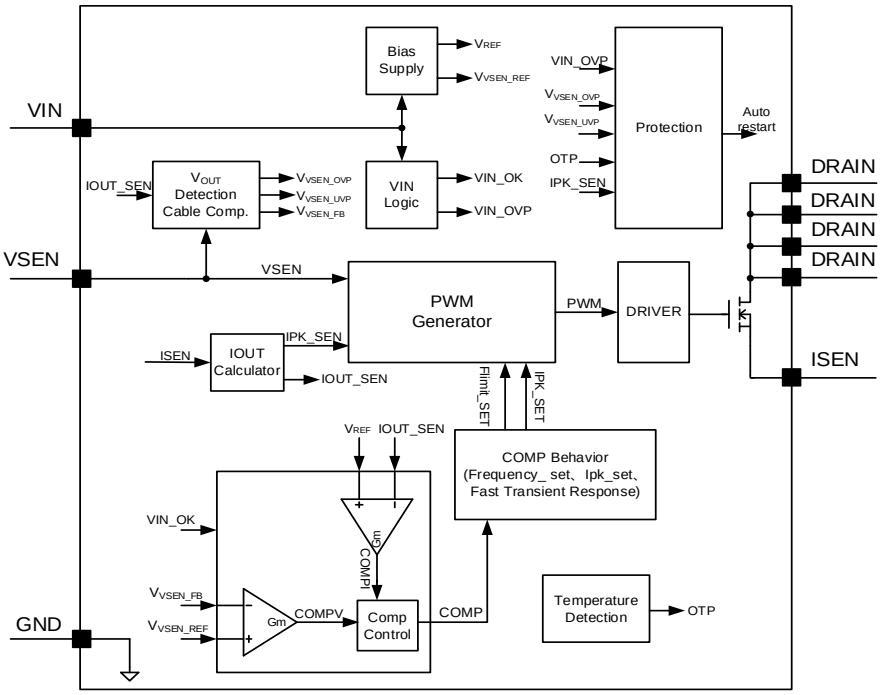


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VIN	-0.3	26	V
VSEN	-1 (*1)	7	
ISEN	-0.3	3.6	
DRAIN		660	
I_{VIN}		20	mA
Junction Temperature, Operating	-45	150	°C
Lead Temperature (Soldering, 10 sec.)		260	
Storage Temperature	-65	150	
(*1)Dynamic VSEN Negative Voltage in 50us Duration	-1		V
(*1)Dynamic VSEN Negative Current in 50us Duration	-2		mA

Thermal Information

Parameter (Note 2)	Min	Max	Unit
θ_{JA} Junction-to-ambient Thermal Resistance		150	°C/W
θ_{JC} Junction-to-case Thermal Resistance		60	
PD Power Dissipation T_A = 25°C		1.1	W

Recommended Operating Conditions

Parameter	Min	Max	Unit
VIN	9	20	V
ISEN	0	1	
Junction Temperature	-40	125	°C
Ambient Temperature	-40	105	

Electrical Characteristics

(V_{VIN}=12V(Note 3), T_A=25°C unless otherwise specified.)

Parameter		Symbol	Test conditions	Min	Typ	Max	Unit
VIN	VIN Turn-on Threshold	V_{VIN_ON}	V_{VIN} increasing	19.5	21.2	22.9	V
	VIN Turn-off Threshold	V_{VIN_OFF}	V_{VIN} decreasing	6.7	7.7	8.7	V
	VIN OVP Voltage	V_{VIN_OVP}	V_{VIN} increasing	22.7	24	25.5	V
	VIN OVP Voltage Hysteresis	$V_{VIN\_OVP\_HYS}$	V_{VIN_OVP} - V_{VIN_ON}	2	3	4.5	V
	VIN OVP Blanking Time(Note4)	T_{VIN_OVP}		85	128	152	us
	Start Up Current	I_{ST}	V_{VIN}<V_{VIN_OFF}		2	5	μA
	Operating Current(Note5)	I_{VIN}	f=100kHz,C_{DRV}=560pF		1.73		mA
	Quiescent Current(Note5)	I_Q	f=500Hz, C_{DRV}=560pF		130		μA
	Discharge Current in OVP Mode	I_{VIN_OVP}	V_{VIN}=12V	3.9	5.2	6.6	mA
ISEN	Internal Reference Voltage	V_{REF}		0.41	0.42	0.43	V
	Current Maximum Protection Threshold Voltage	$V_{ISEN\_LIM\_PRO}$		1.2	1.3	1.4	V
	Number of Consecutive Diode Short Enter Hiccup Mode(Note4)	$N_{ISEN\_LIM\_PRO}$			4		
	Current Limit Voltage	V_{ISEN_LIM}	V_{FBV}<0.4V,V_{ISEN} increasing	0.7	0.75	0.8	V
			V_{FBV}>0.4V,V_{ISEN} increasing	0.92	0.95	0.98	V
	Current Min Voltage	V_{ISEN_MIN}		0.22	0.26	0.3	V
	Min ON Time	T_{ON_MIN}	DRV min width	330	430	520	ns
	Voltage Threshold for V_{ISEN_LIM} Switch	V_{ISEN_SWITCH}	V_{ISEN} increasing	310	400	510	mV
	Detection Time for V_{ISEN_LIM} Switch	T_{ISEN_SWITCH}		1.2	1.8	2.4	us
	CC Feedforward Resistor (Note 4)	R_{INT}		400	480	560	Ω
	Voltage Threshold for ISEN Pin Short	V_{ISEN_SHORT}		100	150	190	mV
	Time Threshold for ISEN Pin Short (Note 4)	T_{ISEN_SHORT}		2.4	3.6	4.8	us
	Enable Time for ISEN Pin Short (Note 4)	$T_{ISEN\_SHORT\_EN}$	Timer start V_{VIN_ON}	49	62	78	ms
	Modulation Minimum Range (Note 4)	$V_{ISEN\_JITTER\_MIN}$	V_{ISEN} = V_{ISEN_MIN}	4	10	16	mV
	Modulation Maximum Range (Note 4)	$V_{ISEN\_JITTER\_MAX}$	V_{ISEN} = V_{ISEN_LIM}	80	100	140	mV
	Modulation Period (Note 4)	T_{JITTER}		200	250	300	us
VSEN	OVP Voltage Threshold	V_{VSEN_OVP}		1.4	1.5	1.6	V
	Number of Consecutive VSEN OVP Enter Hiccup Mode (Note 4)	N_{VSEN_OVP}		-	4	-	
	UVP Voltage Threshold (Note 4)	V_{VSEN_UVP}		0.75	0.8	0.85	V
	Blanking Time for VSEN UVP (Note 4)	T_{VSEN_UVP}		49	62	78	ms
	Internal Reference Voltage	V_{VSEN_REF}		1.232	1.25	1.268	V
	Cable Compensation Coefficient	K3		36	50	64	μA/V

Parameter		Symbol	Test conditions	Min	Typ	Max	Unit
VSEN	Sourcing Current Threshold for VSEN Pin Short Detection	I_{VSEN_SHORT}		60	100	140	μA
	Voltage Threshold for VSEN Pin Short Detection (Note 4)	V_{VSEN_SHORT}		30	60	90	mV
	Blanking Time for VSEN Pin Short Detection (Note 4)	T_{VSEN_SHORT}		85	128	152	us
	Sourcing Current Threshold for Upper Resistor Open	I_{BO}		10	18	26	μA
	Number of Consecutive Upper Resistor Open Enter Hiccup Mode (Note 4)	N_{BO}		-	8	-	
	Voltage Threshold for Current Cross Zero (Note 4)	V_{VSEN_CCZ}		65	100	135	mV
	Voltage Threshold for Zero Zoltage Detection (Note 4)	V_{ZERO}		-70	-40	-10	mV
	Number of Consecutive SCP Enter Hiccup Mode (Note 4)	N_{SCP}		-	8	-	
	Turn On Delay After Zero Voltage Detection (Note 4)	T_{DELAY}		170	200	270	ns
DRAIN	Breakdown Voltage	V_{BV}	V_{GS}=0V,I_{DS}=250μA	660			V
	Static Drain-Source On-Resistance	R_{DSON}	V_{GS}=12V,I_{DS}=0.1A		2.2	2.6	Ω
SWITCHING	Max ON Time (Note 4)	T_{ON_MAX}		19	22	33	μs
	Min OFF Time1	T_{OFF_MIN1}	V_{ISEN} = V_{ISEN_MIN}	1.6	1.9	2.3	us
	Min OFF Time2	T_{OFF_MIN2}	V_{ISEN} = V_{ISEN_LIM}	3	3.6	4.3	us
	Max OFF Time	T_{OFF_MAX}		1.58	2	2.42	ms
	Max OFF Time for Start Up (Note 4)	$T_{OFF\_MAX\_ST}$		24.3	36	47.6	us
	Max OFF Time for Load Transient 1 (Note 4)	$T_{OFF\_MAX\_LT1}$		90	125	160	us
	Number of Consecutive Max OFF Time for Load Transient 1 (Note 4)	$N_{OFF\_MAX\_LT1}$		-	4	-	
	Max OFF Time for Load Transient 2 (Note 4)	$T_{OFF\_MAX\_LT2}$		190	250	310	us
	Working Time for Load Transient 2 (Note 4)	$T_{OFF\_MAX\_LT2}$		6.3	8.0	9.7	ms
	Minimum Switching Period	T_{PERIOD_MIN}		6.9	8	9.1	μs
OTP	Thermal Shutdown Temperature(Note4)	T_{SD}	Temperature increasing		150		°C
	Hysteresis to Resume Operating(Note4)	T_{OTP_HYS}	Temperature decreasing		20		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on “2x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal via to bottom layer ground plane.

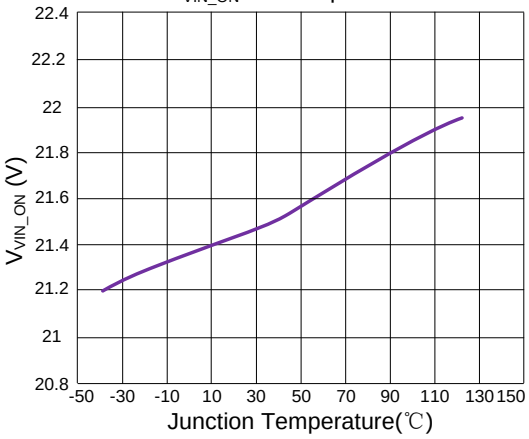
Note 3: Increase VIN pin voltage gradually higher than V_{VIN_ON} voltage to start the IC first, then set VIN to 12V.

Note 4: Guaranteed by design.

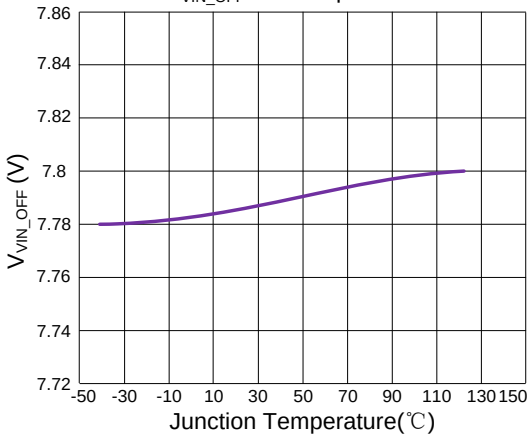
Note 5: Application test result.

Typical Characteristics

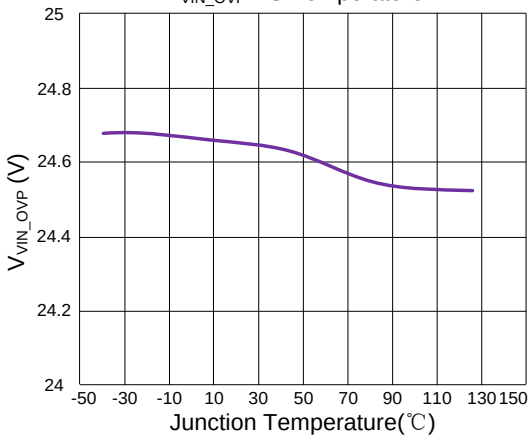
V_{VIN_ON} VS.Temperature



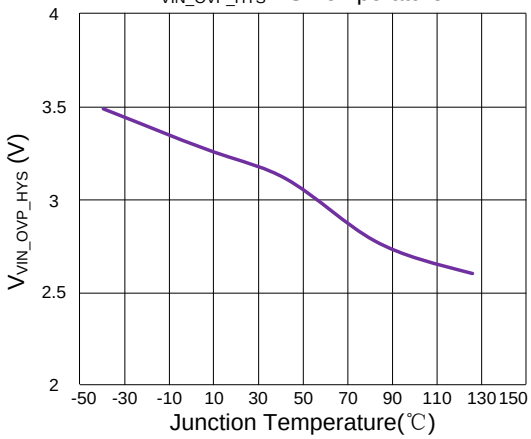
V_{VIN_OFF} VS.Temperature



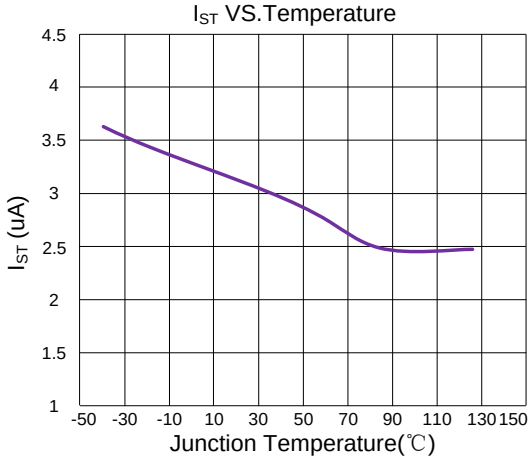
V_{VIN_OVP} VS.Temperature



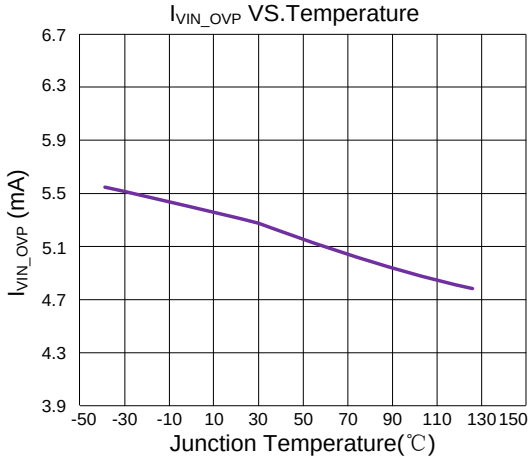
$V_{VIN\_OVP\_HYS}$ VS.Temperature



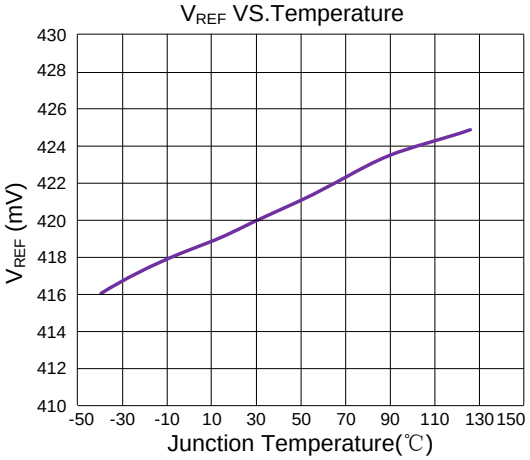
I_{ST} VS.Temperature



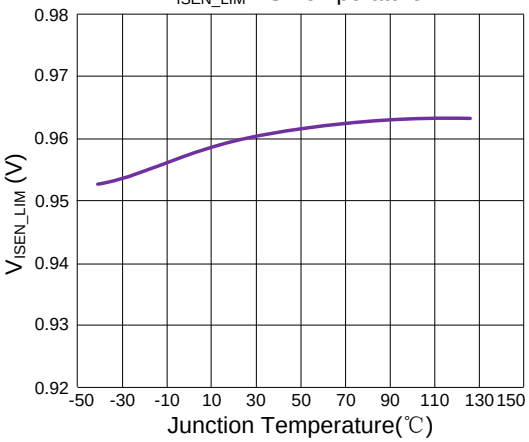
I_{VIN_OVP} VS.Temperature



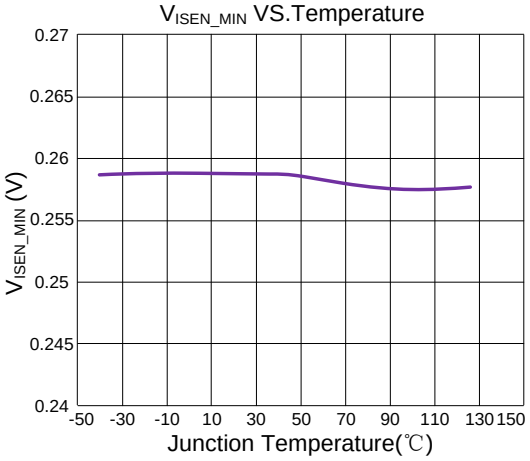
V_{REF} VS.Temperature



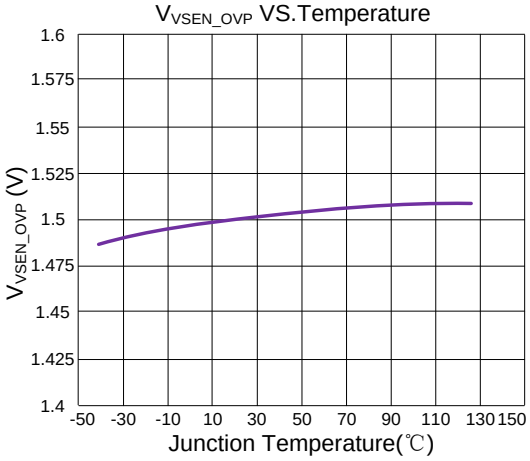
V_{ISEN_LIM} VS.Temperature



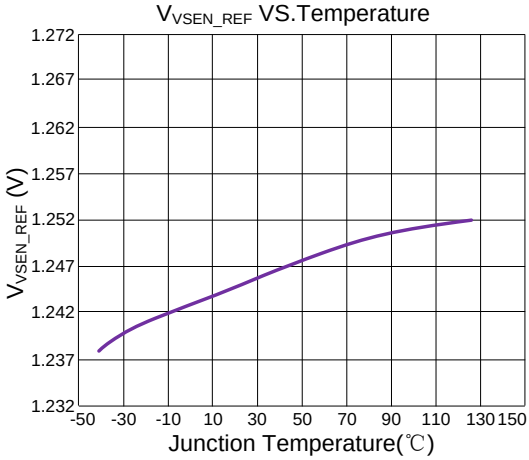
V_{ISEN_MIN} VS.Temperature



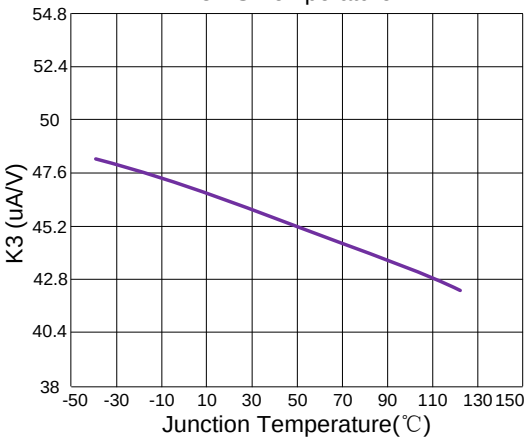
V_{VSEN_OVP} VS.Temperature

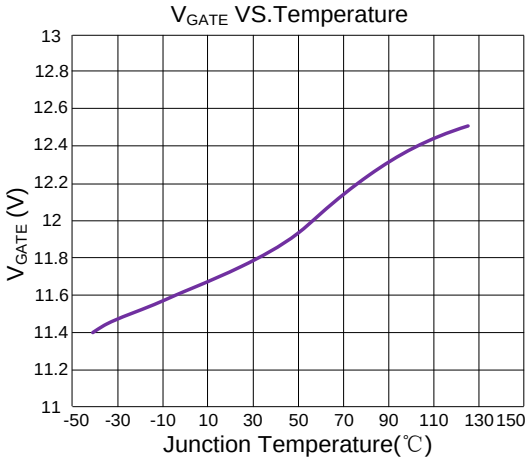


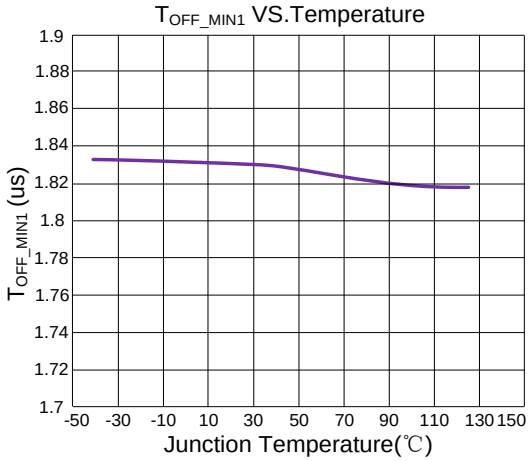
V_{VSEN_REF} VS.Temperature

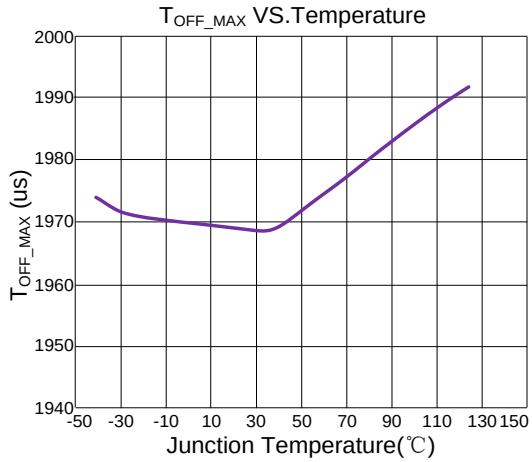


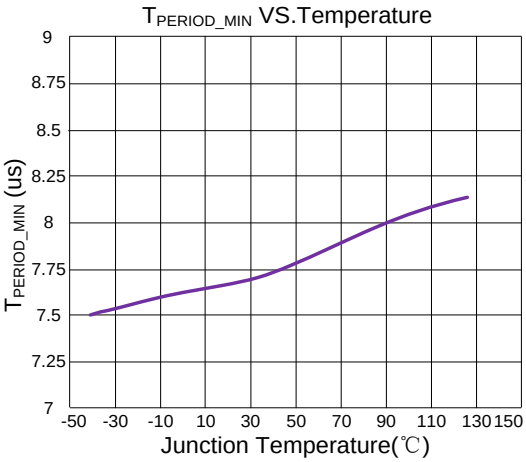
K3 VS.Temperature





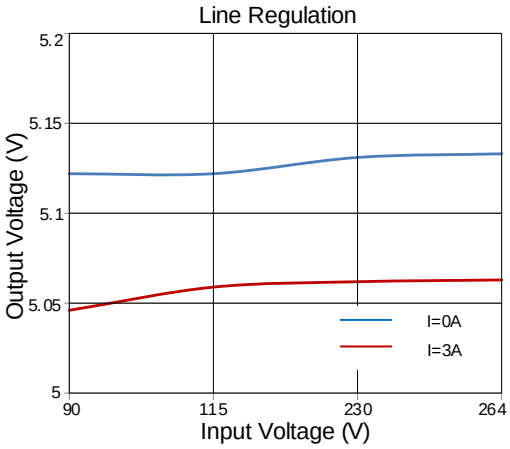


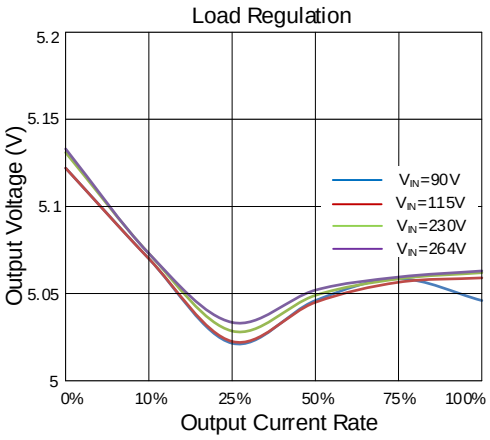




Typical Performance Characteristics

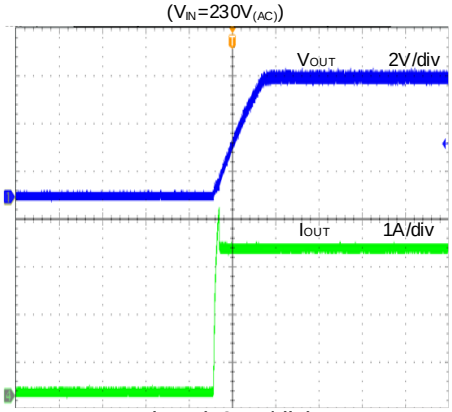
(Test condition: input voltage: 90~264Vac; output spec: 5Vdc_3A; output cable: 22AWG_1.2m; Ambient temperature: 25±5 ℃; Ambient humidity: 65±25 %.)





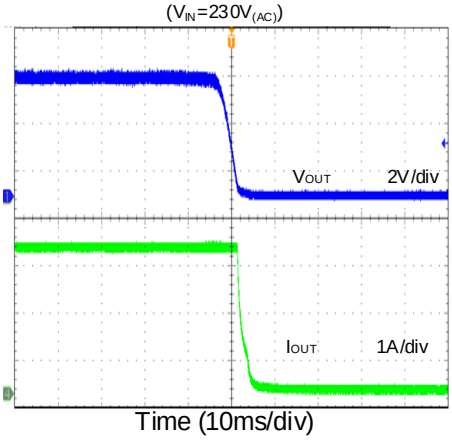
Startup

(V_{IN}=230$V_{(AC)}$)



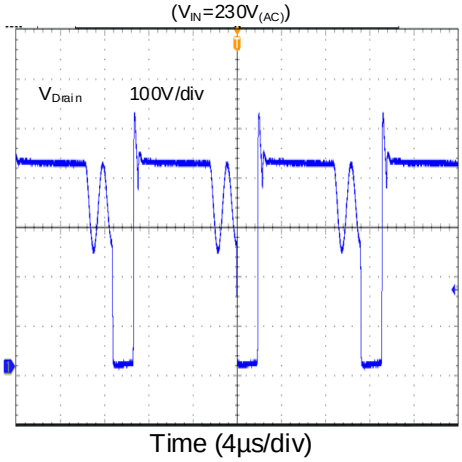
Shutdown

(V_{IN}=230$V_{(AC)}$)



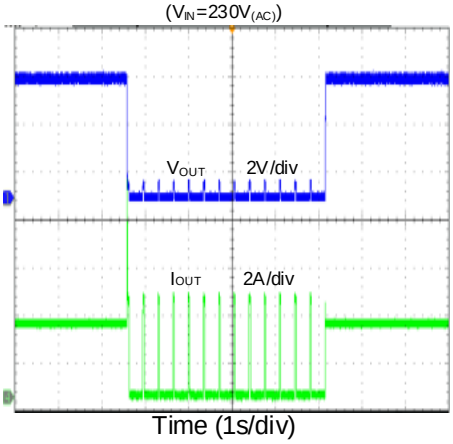
Steady States

(V_{IN}=230$V_{(AC)}$)

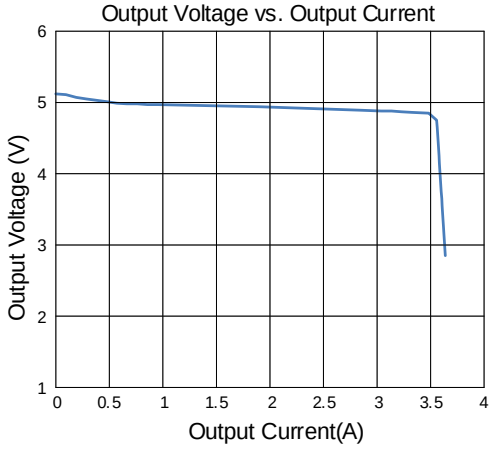


Short Circuit Protection

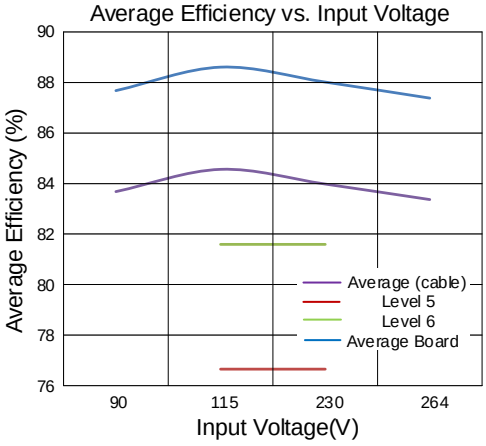
(V_{IN}=230$V_{(AC)}$)



Output Voltage vs. Output Current



Average Efficiency vs. Input Voltage



Detailed Description

General Features

Start-up Operation

After AC supply is powered on, the rectified BUS voltage ramps up. The capacitor across VIN and GND pins, C_{VIN}, is charged up by the BUS voltage through a start up resistor R_{ST}. Once V_{VIN}, the voltage on the VIN pin, rises up to V_{VIN_ON}, the internal blocks starts the operation. V_{VIN} will subsequently be pulled down by the power consumption of the circuitry until the auxiliary winding of Flyback transformer can supply sufficient energy to maintain V_{VIN} above V_{VIN_OFF}.

The start-up procedure is divided into two sections, as shown in Figure 3: t_{STC} is the C_{VIN} charged up section, and t_{STO} is the output voltage built-up section. The start up time t_{ST} composes of t_{STC} and t_{STO}, and usually t_{STO} is much smaller than t_{STC}.

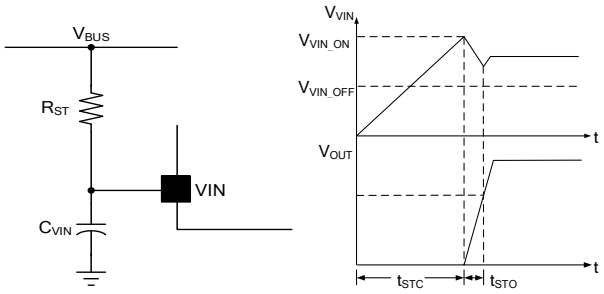


Figure 3. Start up

The start up resistor R_{ST} and C_{VIN} are designed by the following rules:

(a) Preset start-up resistor R_{ST}, make sure that the current through R_{ST} is larger than I_{ST} and smaller than I_{VIN_OVP}

$$\frac{V_{BUS\_MAX}}{I_{VIN\_OVP}} < R_{ST} < \frac{V_{BUS\_MIN}}{I_{ST}} \quad (1)$$

Where V_{BUS} is the BUS line voltage.

(b) Select C_{VIN} to obtain an ideal start-up time $t_{ST,}$ and ensure the output voltage is built up with only one time.

$$C_{VIN} = \frac{(\frac{V_{BUS\_MIN}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}} \quad (2)$$

(c) If the C_{VIN} is not big enough to build up the output voltage with one try, increase C_{VIN} and decrease R_{ST}, go back to step (a) and repeat the same design flow until the ideal start up procedure is obtained.

Shut-down Operation

After AC supply is powered off, the energy stored in the BUS capacitor will be discharged. When the auxiliary winding of Flyback transformer cannot supply enough energy to the VIN pin, V_{VIN} will decrease. Once V_{VIN} is below V_{VIN_OFF}, the IC will stop working.

Quasi-Resonant Operation (Valley Detection)

The Quasi-Resonant switching mode is applied, which means to turn on MOSFET at voltage valley. QR mode operation provides the low turn-on switching losses for Flyback converter.

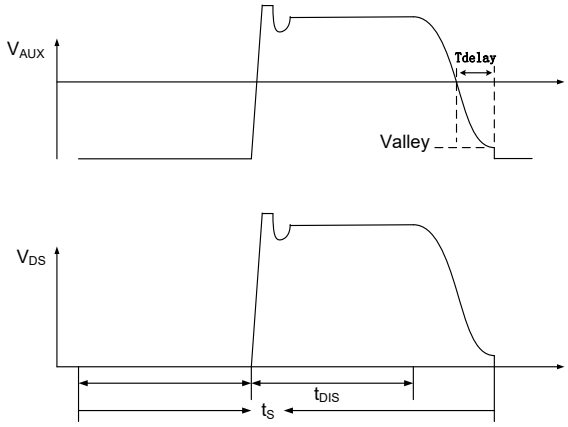


Figure 4. QR Mode Operation

The voltage across drain and source of the primary MOSFET is reflected to the auxiliary winding of the Flyback transformer. VSEN pin detects the voltage across the auxiliary winding by a resistor divider. As shown in Figure 4, when the voltage on VSEN pin across zero, the MOSFET would be turned on after 200ns delay.

Output Voltage Control (CV Control)

In order to achieve primary side constant voltage control, the output voltage is sensed by the auxiliary winding.

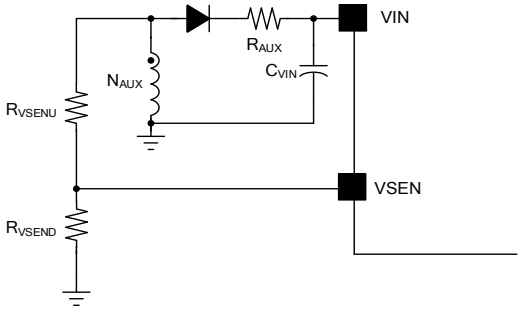


Figure 5. VSEN Pin Connection

As shown in Figure 6, during OFF time, the voltage across the auxiliary winding is

$$V_{AUX} = (V_{OUT} + V_{D\_F}) \times \frac{N_{AUX}}{N_S} \quad (3)$$

N_{AUX} is the turns of auxiliary winding; N_S is the turns of secondary winding; V_{D_F} is the forward voltage of the power diode.

At the current zero-crossing point, V_{D_F} is zero, so V_{OUT} is proportional to V_{AUX}. The voltage of this point is sampled by the IC as the feedback of output voltage. The resistor divider is designed by

$$\frac{V_{VSEN\_REF}}{V_{OUT}} = \frac{R_{VSEND}}{R_{VSENU} + R_{VSEND}} \times \frac{N_{AUX}}{N_S} \quad (4)$$

Where R_{VSEND} and R_{VSENU} are the low side and high resistors at the VSEN pin, respectively, and V_{VSEN_REF} is the internal voltage reference at 1.25V

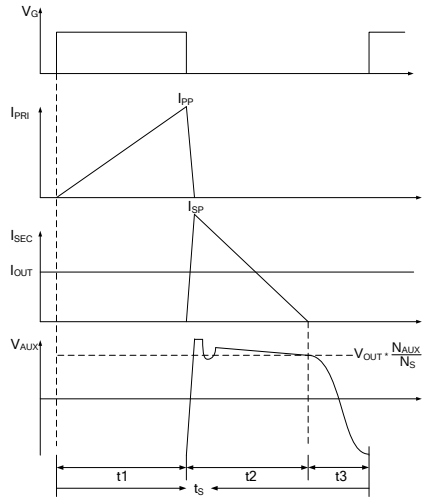


Figure 6. Auxiliary Winding Voltage Waveforms

Output Current Control (CC Control)

The output current is regulated by SY50216N with primary side detection technology, the maximum output current I_{OUT_LIM} can be set by

$$I_{OUT\_LIM} = \frac{k_1 \times V_{REF} \times N_{PS}}{R_S} \quad (5)$$

Where k_1 is the output current weight coefficient; V_{REF} is the internal reference voltage; R_S is the current sense resistor.

k_1 and V_{REF} are all internal constant parameters, I_{OUT_LIM} can be programmed by N_{PS} and R_S.

$$R_S = \frac{k_1 \times V_{REF} \times N_{PS}}{I_{OUT\_LIM}} \quad (6)$$

K_1 is set to 0.5

When the over current operation or short circuit operation takes place, the output current will be limited at I_{OUT_LIM}. The V-I curve is shown as Figure 7.

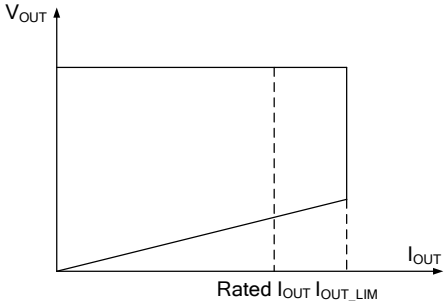


Figure 7. V-I Curve

The IC provides line regulation modification function to improve line regulation performance of the output current limit.

Cable Impedance Compensation

The SY50216N incorporates the cable impedance compensation to provide a better load regulation of output voltage at cable terminals. When the converter output load increases from no load to full load, the resulting voltage decrease on the output cables are compensated by decreasing the voltage feedback signals, which is shown by Figure 8.

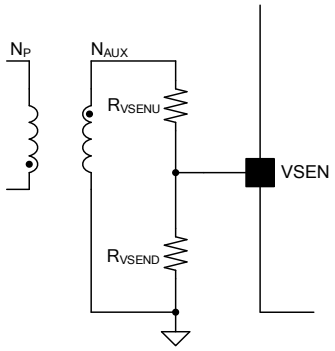


Figure 8. Cable Compensation

$$R_{VSENU} = \frac{R_{Cable}}{2k_3 \cdot R_S} \cdot \frac{N_P}{N_S} \cdot \frac{N_{AUX}}{N_S} \quad (7)$$

Where k_3 is set to 50μA/V, R_S is the current sense resistor connecting to the ISEN pin.

R_{cable} is the resistance on the cable. The cable compensation effect can be adjusted by change the resistance of R_{VSENU} to achieve good load regulation of different output cables. The larger R_{VSENU}, the stronger cable compensation effect will be.

If the output current is below 10% the OCP point, the cable compensation is disabled.

Over-temperature Protection (OTP)

The SY50216N includes over-temperature protection (OTP) circuitry to prevent the overheating due to the excessive power dissipation. It will shut down the switching operation when the IC temperature exceeds the OTP threshold, about 150°C. In OTP mode, if the IC temperature decreases by approximately 20°C, the IC will resume the normal operation. For a continuous normal operation, provide an adequate cooling so that the IC temperature does not exceed the OTP threshold.

Short Circuit Protection (SCP)

When the output is shorted to ground, the output voltage is clamped to zero. The valley signal of the auxiliary winding voltage might not be detected by the VSEN pin. In this case, MOSFET cannot be turned on until maximum off time is reached. IC will shut down until VIN is below V_{VIN_OFF}, and then enter the hiccup mode.

When the output voltage is not low enough to disable the valley detection in short condition, SY50216N will operate in CC mode until VIN decreases below V_{VIN_OFF}.

As shown in Figure 9, a filter resistor R_{AUX} is needed to prevent the SCP function from being affected by the voltage spikes of the auxiliary winding.

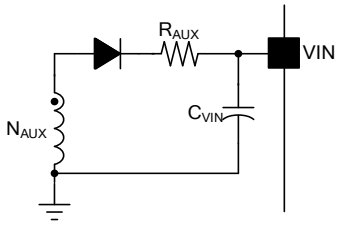


Figure 9. Filter Resistor R_{AUX}

VIN Voltage OVP

When the VIN voltage exceeds V_{VIN_OVP} threshold, SY50216N will stop switching and discharge the VIN voltage. Once V_{VIN} is below V_{VIN_OFF}, the SY50216N will shut down and VIN will be charged again.

Output Voltage OVP

When the VSEN pin signal exceeds V_{VSEN_OVP} threshold, reflecting an output over-voltage conditions, SY50216N will stop switching and discharge the VIN voltage. Once V_{VIN} is below V_{VIN_OFF}, the IC will shut down and then enter the hiccup mode.

Output Voltage UVP

When the VSEN pin signal less than V_{VSEN_UVP}, reflecting an output under-voltage conditions, SY50216N will stop switching and discharge the VIN voltage. Once V_{VIN} is below V_{VIN_OFF}, the IC will shut down and then enter the hiccup mode.

VSEN Pin Short Protection

The SY50216N has a protection against the faults caused by shorting VSEN pin to GND. When the VSEN voltage does not reach the sense protection trigger level at the end of startup, the VSEN pin is deemed shorting to GND, and the protection is activated: the IC stops switching and discharge the VIN voltage. Once V_{VIN} decreases below V_{VIN_OFF}, the IC will shut down and then enter the hiccup mode. In order to ensure reliable detection, the pull-down resistor at VSEN pin should be larger than 2kΩ.

ISEN Pin Short Protection

The SY50216N has a protection against the faults caused by shorting ISEN pin to GND. If ISEN short is detected at startup, the IC stops switching and discharge the VIN voltage. Once V_{VIN} decreases below V_{VIN_OFF}, the IC will shut down and then enter the hiccup mode.

VSEN Pin Upper Divider Resistor Disconnect Protection

If the upper divider resistor disconnected lasting for 8 switching cycles, the IC will stop switching and discharge the VIN voltage. Once V_{VIN} is below V_{VIN_OFF}, the SY50216N will shut down and VIN will be charged again.

Secondary Side Schottky Diode Short Protection

If secondary side schottky diode short lasting for 4 switching cycles, the IC will stop switching and discharge the VIN voltage. Once V_{VIN} decreases below V_{VIN_OFF}, the IC will shut down and then enter the hiccup mode.

Typical Application Schematic

Typical application circuit information is displayed in a 15W design. The adapter circuit includes a primary side regulator (SY50216N).

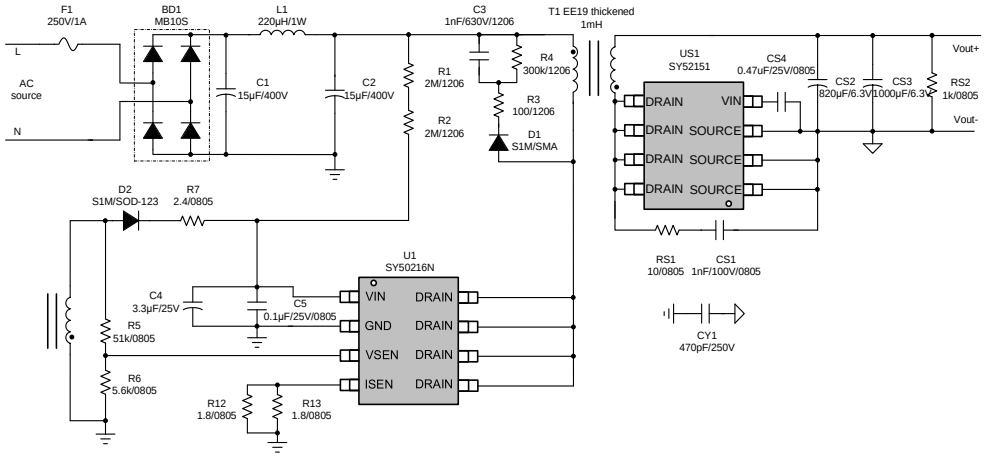


Figure 10. 15W Adapter Typical Application Circuit

Recommended BOM List

Designator	Description	Part Number	Manufacturer
C1	15μF/400V	EWH2GM150G12OT	AISHI
C2	15μF/400V	EWH2GM150G12OT	AISHI
C3	1nF/630V/ X7R,1206	CC1206JKX7RZBB102	YAGEO
C4	3.3μF/25V	EWH1EM3R3D11OT	AISHI
C5	0.1μF/25V/X7R,0805	CC0805KRX7R8BB104	YAGEO
CS1	1nF/100V/ X7R,0805	CC0805KRX7R0BB102	YAGEO
CS2	820μF/16V	SPZ0JM821E09O00R	AISHI
CS3	1000μF/16V	ERS0JM102F16C32T	AISHI
CS4	0.47μF/25V/X7R,0805	CC0805KRX7R8BB474	YAGEO
R1,R2	2M/1206	1206W8J0205T5E	UNI-ROYAL
R3	100Ω/1206	1206W4J0101T5E	UNI-ROYAL
R4	300kΩ/1206	1206W4J0304T5E	UNI-ROYAL
R5	51 kΩ/0805,1%	0805W8F5102T5E	UNI-ROYAL
R6	5.6 kΩ/0805,1%	0805W8F5601T5E	UNI-ROYAL
R7	2.4Ω/0805	0805W8J024JT5E	UNI-ROYAL
R12,R13	1.8Ω/0805,1%	0805W4F180KT5E	UNI-ROYAL
RS1	10Ω/0805	0805W4J0100T5E	UNI-ROYAL
RS2	1kΩ/0805	0805W8J0102T5E	UNI-ROYAL
D1	S1M/SMA	S1M	MDD
D2	S1M/SOD-123	S1M	MDD
US1	SY52151FAP/SO8	SY52151FAP	SILERGY
F1	250V/1A	MTS1100A	REOMAX
BD1	MB10S/MBS	MB10S	MDD
L1	220μH/1W	LGA0410-221KP52E	FH
U1	SY50216NFAC/SO8	SY50216NFAC	SILERGY
T1	EE19 thickened 1mH	/	/
CY1	470pF/250V	CS80-E2GA471MYVSA	TDK

Design Procedure and Example

Power Rating

A few applications are shown as below.

Products	Input range	Output		Temperature rise
SY50216N	90Vac~264Vac	15W	5V/3A	40℃
	90Vac~264Vac	17.5W	5V/3.5A	50℃
	90Vac~264Vac	18W	5V/3.6A	60℃
	90Vac~264Vac	18W	12V1.5A	40℃

The test is conducted in a natural cooling condition at 25 ℃ ambient temperature.

Identify Design Specification

A design example of typical application is shown below step by step.

Design Specification			
V_{AC}(RMS)	90V~264V	V_{OUT}	5V
I_{OUT}	3A	η	85%

Note: All selected parameter (set value) need to adjust according to the practical condition.

Transformer N_{PS} and L_M Selection

N_{PS} is limited by the electrical stress of the power MOSFET:

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2}V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (8)$$

Where $V_{MOS\_(BR)DS}$ is the breakdown voltage of MOSFET. V_{D_F} is the forward voltage of secondary power diode; ΔV_S is the overshoot voltage clamped by RCD snubber during OFF time.

In Quasi-Resonant mode, each switching period cycle, t_S, consists of three parts: current rising time t_1, current falling time t_2 and quasi-resonant time t_3 shown in Figure 11.

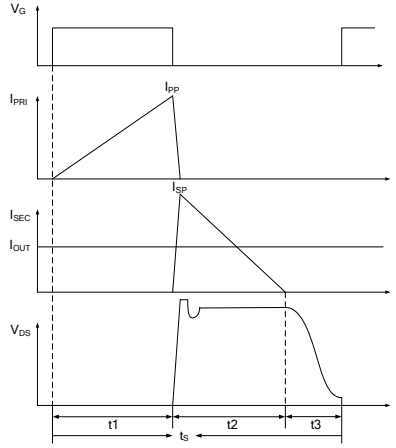


Figure 11. switching waveforms

Under the conditions of the minimum input AC RMS voltage and full load, the switching frequency is minimum while the peak current through MOSFET is maximum.

Once the minimum frequency f_{S_MIN} is set, the inductance of the transformer could be designed.

Conditions			
V_{AC_MIN}	90V	V_{AC_MAX}	264V
ΔV_S	70V	$V_{MOS\_(BR)DS}$	660V
P_{OUT} (Max)	15W	V_{D_F}	1V
C_{Drain}	100pF	f_{S_MIN}	55kHz
ΔV_{BUS}	30% V_{BUS_MIN}		

The design flow is shown below:

(a) Select N_{PS}

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2}V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}}$$

$$= \frac{660V \times 0.9 - \sqrt{2} \times 264V - 70V}{5V + 1V}$$

$$= 25.12$$

N_{PS} is set to 16

(b) Preset minimum frequency f_{S_MIN} is 55kHz

(c) Compute inductor L_M and maximum primary peak current $I_{P\_PK\_MAX}$

$$I_{P\_PK\_MAX} = \frac{2P_{OUT}}{\eta \times \left(\sqrt{2}V_{AC\_MIN} - \Delta V_{BUS}\right)} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D\_F})} + \pi\sqrt{\frac{2P_{OUT}}{\eta} \times C_{Drain} \times f_{S\_MIN}}$$

$$= \frac{2 \times 15W}{0.85 \times (\sqrt{2} \times 90V - 0.3 \times \sqrt{2} \times 90V)} + \frac{2 \times 15W}{0.85 \times 16 \times (5V + 1V)} + \pi \times \sqrt{\frac{2 \times 15W}{0.85} \times 100pF \times 55kHz}$$

$$= 0.808A$$

$$L_M = \frac{2P_{OUT}}{\eta \times I_{P\_PK\_MAX}^2 \times f_{S\_MIN}}$$

$$= \frac{2 \times 15W}{0.85 \times (0.808A)^2 \times 55kHz}$$

$$= 0.98mH$$

where C_{Drain} is the parasitic capacitance at drain of MOSFET, η is the efficiency, and P_{OUT} is the rated full load power. L_M is set to 0.94mH.(Note: the actual value generally less than the compute value)

(d) Compute current rising time t_1 and current falling time t_2

$$t_1 = \frac{L_M \times I_{P\_PK\_MAX}}{V_{BUS\_MIN} - \Delta V_{BUS}} = \frac{0.94mH \times 0.808A}{\sqrt{2} \times 90V - 0.3 \times \sqrt{2} \times 90V} = 8.52\mu s$$

$$t_2 = \frac{L_M \times I_{P\_PK\_MAX}}{N_{PS} \times (V_{OUT} + V_{D\_F})} = \frac{0.94mH \times 0.808A}{16 \times (5V + 1V)} = 7.907\mu s$$

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}} = \pi \times \sqrt{0.94mH \times 100pF} = 0.963\mu s$$

$$t_S = t_1 + t_2 + t_3 = 8.52\mu s + 7.907\mu s + 0.963\mu s = 17.39\mu s$$

(e) Compute primary maximum RMS current $I_{P\_RMS\_MAX}$ for the transformer fabrication.

$$I_{P\_RMS\_MAX} = \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_1}{t_S}}$$

$$= \frac{\sqrt{3}}{3} \times 0.808A \times \sqrt{\frac{8.52\mu s}{17.39\mu s}} = 0.326A$$

(f) Compute secondary maximum peak current $I_{S\_PK\_MAX}$ and RMS current $I_{S\_RMS\_MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 16 \times 0.808A = 12.92A$$

$$I_{S\_RMS\_MAX} = N_{PS} \times \frac{\sqrt{3}}{3} I_{P\_PK\_MAX} \times \sqrt{\frac{t_2}{t_S}}$$

$$= 16 \times \frac{\sqrt{3}}{3} \times 0.808A \times \sqrt{\frac{7.907\mu s}{17.39\mu s}} = 5.03A$$

Transformer Turns Selection

The key transformer parameters are shown below:

Necessary parameters	
Primary to Secondary Turns ratio	N_{PS}
Inductance	L_M
Primary maximum current	$I_{P\_PK\_MAX}$
Primary maximum RMS current	$I_{P\_RMS\_MAX}$
Secondary maximum RMS current	$I_{S\_RMS\_MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e. There select thickened EE19 for compute example. Its A_e is 46.5 mm². The thickened EE19 can be replaced by other reasonable magnetic core style.

(b) Preset the maximum magnetic flux ΔB is 0.255T.

Usually $\Delta B = 0.22 \sim 0.3T$

(c) Compute primary turn N_P

$$N_p = \frac{L_M \times I_{P\_PK\_MAX}}{\Delta B \times A_e} = \frac{0.94 \times 10^{-3} \times 0.808A}{0.255 \times 46.5 \times 10^{-6}} = 64.02$$

N_P is set to 64

(d) Compute secondary turn N_S

$$N_S = \frac{N_P}{N_{PS}} = \frac{64}{16} = 4$$

N_S is set to 4

(e) Compute auxiliary turn N_{AUX}

$$N_{AUX} = N_S \times \frac{V_{VIN}}{V_{OUT}} = 4 \times \frac{12.5}{5} = 10$$

N_{AUX} is set to 10

where V_{VIN} is the working voltage of VIN pin (9V~20V is recommended).

(f) Select an appropriate wire diameter

With $I_{P\_RMS\_MAX}$ and $I_{S\_RMS\_MAX}$, select appropriate wire to achieve the current density from 4A/mm² to 10A/mm².

Primary wire diameter selection: current density j is set to 9A/mm².The compute primary wire cross-sectional area:

$$S1 = \frac{I_{P\_RMS\_MAX}}{j} = \frac{0.326}{9} = 0.036mm^2$$

The compute primary wire diameter:

$$D1 = 2 \times \sqrt{\frac{S1}{\pi}} = 2 \times \sqrt{\frac{0.036}{\pi}} = 0.215mm$$

D1 is set to 0.22mm

Secondary wire diameter selection: current density j is set to 8A/mm².The compute secondary wire cross-sectional area:

$$S2 = \frac{I_{S\_RMS\_MAX}}{j} = \frac{5.03}{8} = 0.629mm^2$$

The compute secondary wire diameter:

$$D2\_1 = 2 \times \sqrt{\frac{S2}{\pi}} = 2 \times \sqrt{\frac{0.629/2}{\pi}} = 0.633mm$$

D2 = D2_1 × 2, D2 is set to 0.65mm × 2

Consider transformer style, the actual primary and secondary wire diameter can be adjusted for best production.

(g) If the window area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

(h) Other usually transformer inductance

Item	Specification	Remark
EE19 Thickened (90~264Vac,5V3A)		
Primary-Side Inductance	0.94mH±5%	40kHz,1V,25±5℃,Hum:65±25%
Primary-Side Leakage Inductance	45μH Maximum	Short One of Secondary Winding
N_P	64	
N_S	4	
N_A	10	
EE19 Thickened (90~264Vac,12V1.5A)		
Primary-Side Inductance	0.97mH±5%	40kHz,1V,25±5℃,Hum:65±25%
Primary-Side Leakage Inductance	50μH Maximum	Short One of Secondary Winding
N_P	70	
N_S	10	

N_A	11	
EE19-10 (90~264Vac,12V1.5A)		
Primary-Side Inductance	1.0mH±5%	40kHz,1V,25±5℃,Hum:65±25%
Primary-Side Leakage Inductance	50μH Maximum	Short One of Secondary Winding
N_P	75	
N_S	9	
N_A	11	

Diode Selection

Under the conditions of the maximum input voltage and full load, the voltage stress of secondary power diode is maximum.

Known conditions at this step			
V_{AC_MAX}	264V	N_{PS}	16
V_{OUT}	5V	V_{D_F}	1V
ΔV_S	70V		

$$V_{D\_R\_MAX}=\frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}}+V_{OUT}=\frac{\sqrt{2}\times 264V}{16}+5V=28.355V$$

Where V_{AC_MAX} is maximum input AC RMS voltage, N_{PS} is the primary to secondary turns ratio of the Flyback transformer and V_{OUT} is the rated output voltage.

Under the conditions of the minimum input voltage and full load, the current stress of power diode is maximum.

$$I_{D\_PK\_MAX}=N_{PS}\times I_{P\_PK\_MAX}=16\times 0.808A=12.921A$$

$$I_{D\_AVG}=I_{OUT}=3A$$

Where $I_{P\_PK\_MAX}$ is maximum primary peak current.

Input Capacitor C_{BUS} Selection

Generally, the input capacitor C_{BUS} is selected by

$C_{BUS}=2\sim 3\mu F/W$,

Or more accurately by

Known conditions at this step			
V_{AC_MIN}	90V	ΔV_{BUS}	30% V_{BUS_MIN}

$$C_{BUS}=\frac{\arcsin(1-\frac{\Delta V_{BUS}}{\sqrt{2}V_{AC\_MIN}})+\frac{\pi}{2}}{\pi}\times\frac{P_{OUT}}{\eta}\times\frac{1}{2f_{IN}V_{AC\_MIN}^2[1-(1-\frac{\Delta V_{BUS}}{\sqrt{2}V_{AC\_MIN}})^2]}$$

$$=\frac{\arcsin(1-\frac{0.3\times\sqrt{2}\times 90V}{\sqrt{2}\times 90V})+\frac{\pi}{2}}{\pi}\times\frac{15W}{0.85}\times\frac{1}{2\times 50Hz\times 90V^2\times[1-(1-\frac{0.3\times\sqrt{2}\times 90V}{\sqrt{2}\times 90V})^2]}$$

$$=31.9\mu F$$

C_{BUS} is set to 30μF

Where ΔV_{BUS} is the voltage ripple of BUS line.

Start up Resistor R_{ST} and Capacitor C_{VIN} Selection

The start up resistor R_{ST} and C_{VIN} are designed to achieve ideal start-up time t_{ST}, and ensure the output voltage is built up with only one time. Refer to the introduction of the **start up operation**.

Conditions			
V_{BUS_MIN}	$90V\times\sqrt{2}$	V_{BUS_MAX}	$264V\times\sqrt{2}$
I_{ST}	5μA (max)	V_{VIN_ON}	21.2V (typical)
I_{VIN_OVP}	5.2mA (typical)	t_{ST}	3s (designed by user)

$$R_{ST}<\frac{V_{BUS\_MIN}}{I_{ST}}=\frac{90V\times\sqrt{2}}{5\mu A}=25.452M\Omega$$

$$R_{ST}>\frac{V_{BUS\_MAX}}{I_{VIN\_OVP}}=\frac{264V\times\sqrt{2}}{5.2mA}=71.78k\Omega$$

R_{ST} is set to 4MΩ

$$C_{VIN}=\frac{(\frac{V_{BUS\_MIN}}{R_{ST}}-I_{ST})\times t_{ST}}{V_{VIN\_ON}}=\frac{(\frac{90V\times\sqrt{2}}{4M\Omega}-5\mu A)\times 3s}{21.2V}=3.79\mu F$$

C_{VIN} is set to 3.3μF

Current Sense Resistor Selection

Set current sense resistor to achieve ideal output current. Refer to the introduction of **output current control**.

Known conditions at this step			
k_1	0.5	N_{PS}	16
V_{REF}	0.42V	I_{OUT_LIM}	3.6A

$$R_S=\frac{k_1\times V_{REF}\times N_{PS}}{I_{OUT\_LIM}}=\frac{0.5\times 0.42V\times 16}{3.6A}=0.933\Omega$$

R_S is set to 0.9Ω

Voltage Sense Resistor Selection

Set vsen sense resistor to achieve ideal output voltage and cable compensation.

First set vsen upper resistor to achieve ideal cable impedance compensation. Refer to the introduction of **cable impedance compensation**.

Conditions			
V_{OUT}	5V	V_{VSEN_REF}	1.25V
R_{Cable}	0.13Ω(22AWG 1.2m)	N_S	4
N_{AUX}	10	K_3	50μA/V

$$R_{VSENU}=\frac{N_P}{N_S}\cdot R_{Cable}\cdot\frac{N_{AUX}}{N_S}\cdot\frac{1}{2K_3\cdot R_S}=57.8k\Omega$$

R_{VSENU} is set to 51kΩ

Then set vsen lower resistor to achieve ideal output voltage. Refer to the introduction of **output voltage control**.

$$R_{VSEND}=\frac{R_{VSENU}}{\frac{V_{OUT}N_{AUX}}{V_{VSEN\_REF}N_S}-1}=\frac{51k\Omega}{(\frac{5V\times10}{1.25V\times4}-1)}=5.67k\Omega$$

R_{VSEND} is set to 5.6kΩ

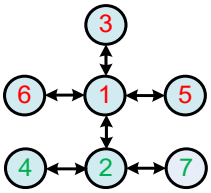
Layout Design

A proper PCB design must follow the below guidelines:

(a) To achieve a good EMI performance and to reduce the line frequency voltage ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

(b) The circuit loop of all switching circuit should be kept as small as possible: primary power loop, secondary loop and auxiliary power loop.

(c) The connection of primary ground is recommended as:



Ground ①: ground of BUS line capacitor.

Ground ②: ground of bias supply capacitor.

Ground ③: ground node of auxiliary winding.

Ground ④: ground node of divider resistor.

Ground ⑤: primary ground node of Y capacitor.

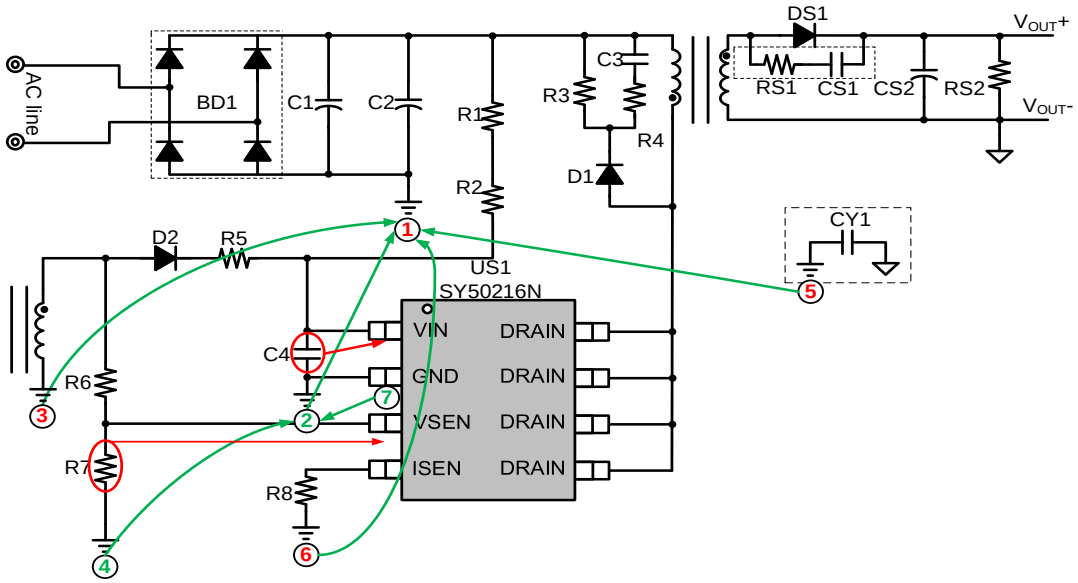
Ground ⑥: ground node of current sample resistor.

Ground ⑦: ground of IC GND.

(d) Bias supply trace should be connected to the bias supply capacitor first and then to the GND pin. The bias supply capacitor should be put right beside the IC.

(e) The loop consisting of 'Source pin – current sense resistor – GND pin' should be kept as small as possible.

(f) The resistor divider connected to VSEN pin is recommended to be put close to the IC.



Note: Ground node of current sample resistor must be connected to the ground of bus line capacitor

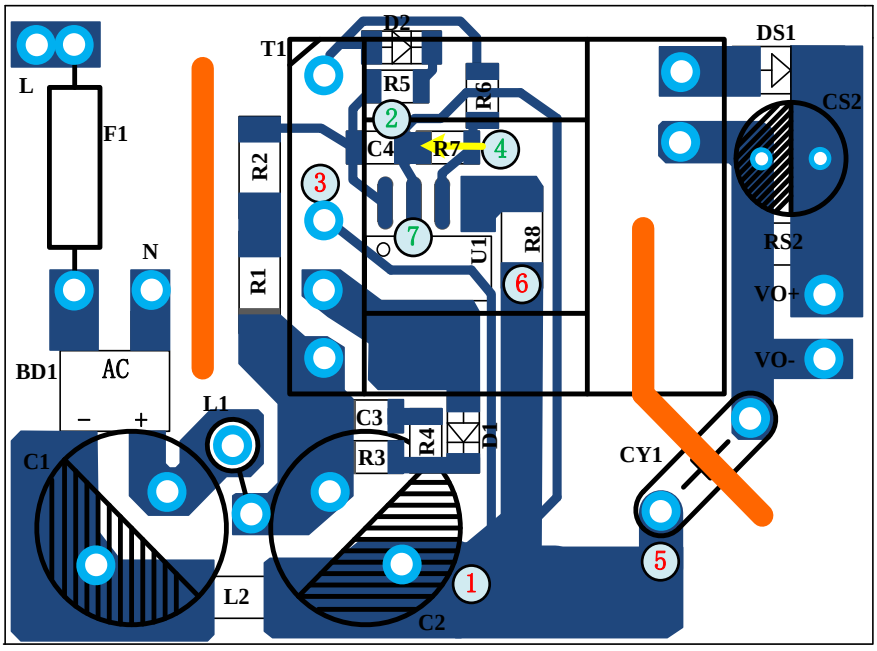


Figure 12. PCB Layout Suggestuion

Design Notes

1. At no load, the secondary side diode freewheeling time should be more than 2.3μs.

2. VIN voltage should be designed to higher than 11V for all conditions.

3. RCD snubber's influence:

At no load or light load, the off-time of main switch is very long and the snubber capacitor's voltage may be discharged to a small value. When the primary switch turns on and then turns off, the primary winding current needs a longer than normal time to charge up the snubber capacitor. This might affect the feedback voltage sensing. If Imin (Imin=0.26V/Rs) is 0.1A, the snubber capacitor should be no larger than 470pF.

4. At heavy load, the peak-to-peak voltage at the Vsen pin should be less than approximately 100mVp-p after off-min time (3.0μs). This can be guaranteed by decreasing the leakage inductance and using proper RCD snubber.

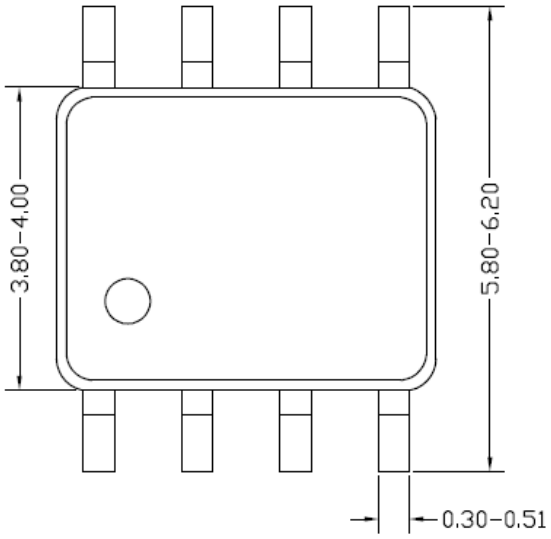
5. R_{VSENU} is the upper resistor of the divider. Normally, its value is recommended between 30Ω~91kΩ.

6. In order to ensure the CC/CV loop stability, the output capacitor should use the following formula to estimate:

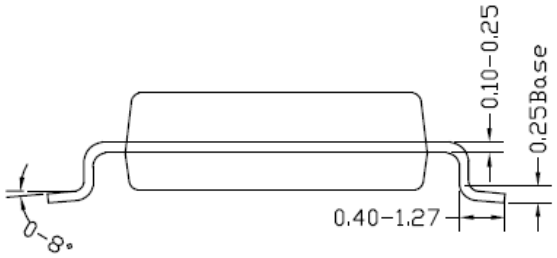
Cout= 3.7m × Iou t/Vout.

For example, in the 5V/2A output case, Cout=3.7 × 2/5=1.48mF. The output capacitor can choose from 1270μF to 1680μF. On the other hand, switching frequency ripple should also be considered. If the switching frequency ripple is too large, increase the capacitance of Cout properly or use low ESR capacitor.

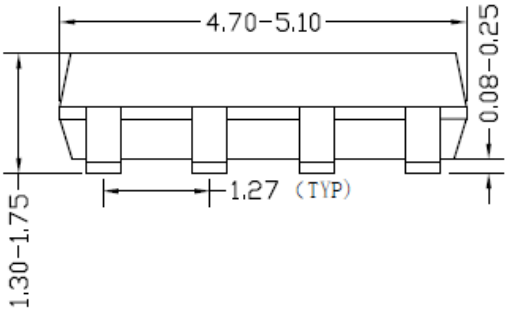
SO8 Package outline & PCB layout design



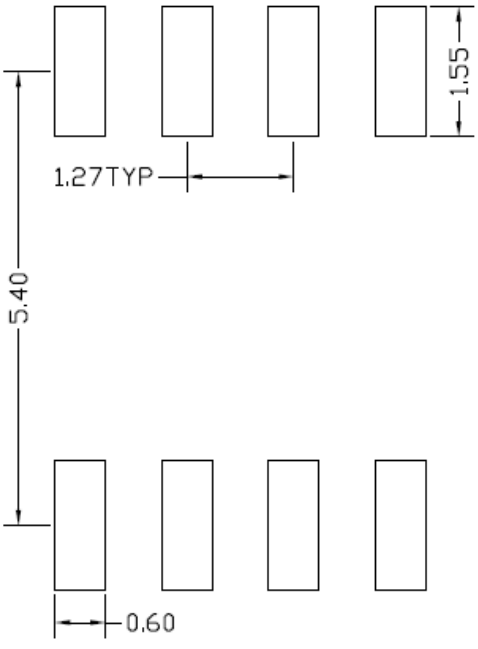
Top view



Side view



Front view

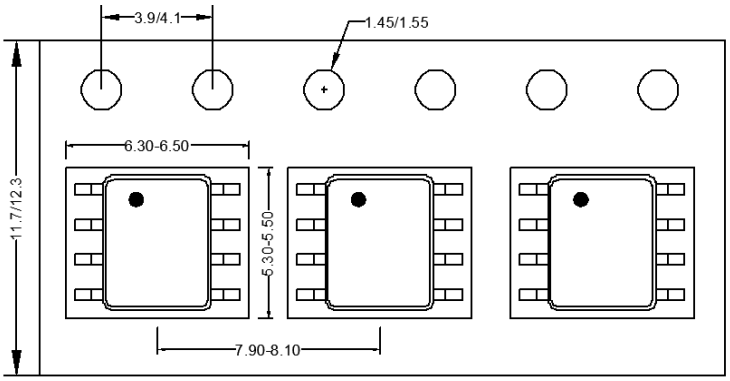


Recommended Pad Layout (Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

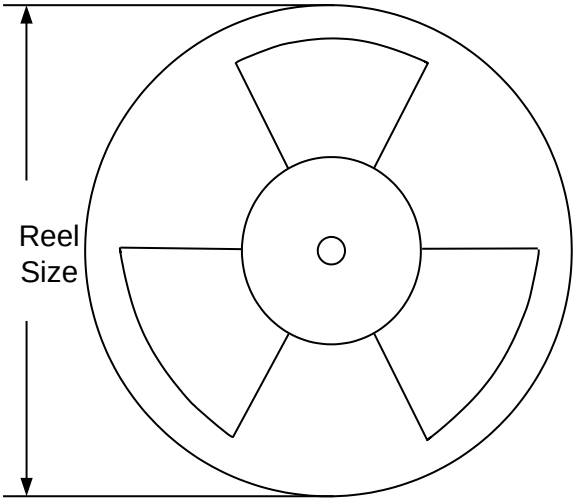
Taping & Reel Specification

1. Taping orientation for packages（SO8）



Feeding direction

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8	12	8	13"	400	400	2500

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
May 15, 2024	Revision 1.0	Initial Release

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