

General Description

The SY52151 is a high-performance synchronous rectifier which contains controller and MOSFET devices. This solution not only directly reduces power dissipation of the rectifier but also indirectly reduces primary-side losses, due to compounding of efficiency gains. The DRAIN pin of SY52151 can support 40V voltage stress.

The SY52151 will achieve the ultra-low power consumption when the circuit operates in no load.

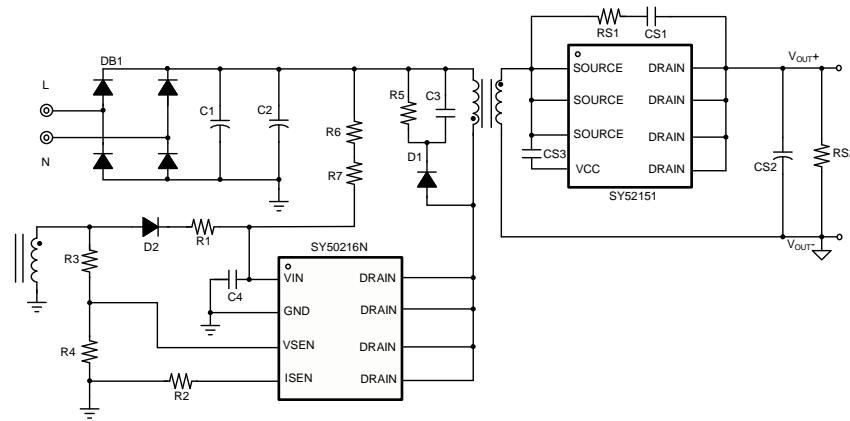
The SY52151 is available in a compact SO8 package.

Features

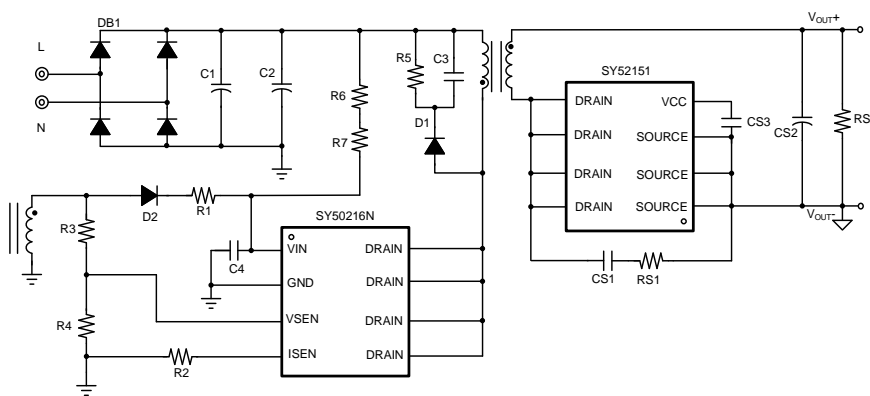
- Smart Turn off Technology
- Secondary-side Synchronous Rectifier Optimized for 5V~12V Systems
- Suitable for Discontinuous Mode (DCM), Critical Conduction Mode (CRM)
- Suitable for Primary Side Regulation(PSR), Secondary Side Regulation (SSR)
- RoHS Compliant and Halogen Free
- Compact Package: SO8

Applications

- AC/DC Adapters
- Battery Chargers
- Consumer Electronics
- Auxiliary Power Supplies



(a) Typical Application Circuit in High Side



(b) Typical Application Circuit in Low Side

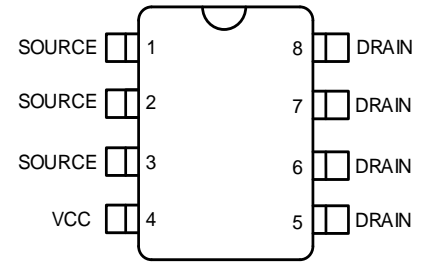
Figure 1. Typical Application Circuit

Ordering Information

Ordering Part Number	Package type	Top Mark
SY52151FAP	SO8 RoHS-Compliant and Halogen-Free	GHR <i>xyz</i>

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1,2,3	SOURCE	Source terminal of integrated SR MOS, also the analog GND
4	VCC	Output of internal LDO, power supply for control unit and drive circuit. Connect a 0.1 μ F or larger ceramic capacitor between VDD and SOURCE pin
5,6,7,8	DRAIN	DRAIN terminal of integrated SR MOSFET, also used for self-supply

Block Diagram

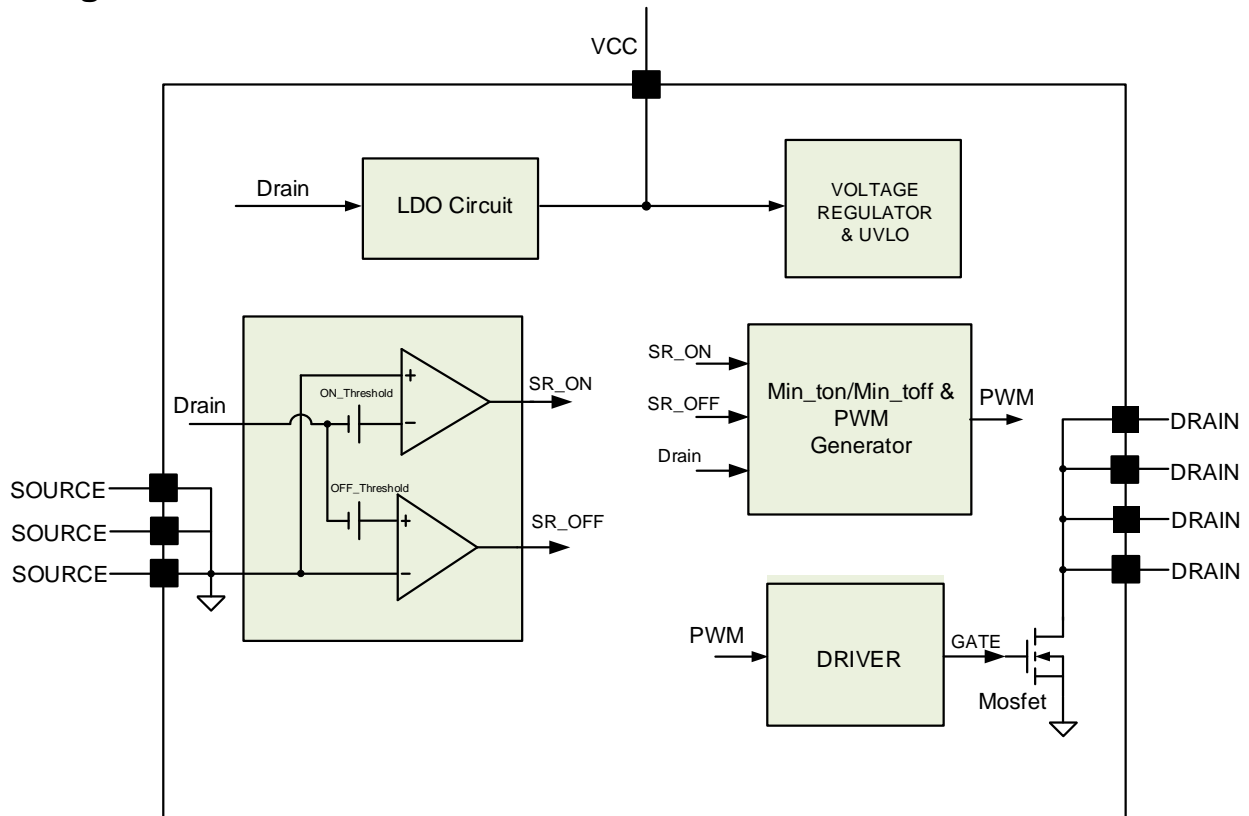


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter(Note 1)	Min	Max	Unit
VCC	-0.3	16	V
DRAIN	-1.5	40	
I _{VDD}		20	mA
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10 sec.)		260	
Storage Temperature	-65	150	
Human Body Model ESD, ANSI/ESDA/JEDEC JS-001-2017 ^(Note 2)	-2000	2000	V
Latch-up Test per JESD78E ^(Note 2)	-100	100	mA

Thermal Information

Parameter (Note 2)	Min	Max	Unit
θ_{JA} Junction-to-ambient Thermal Resistance		137	°C/W
θ_{JC} Junction-to-case Thermal Resistance		35	
PD Power Dissipation TA = 25°C		1.1	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VCC	4	7.35	V
Junction Temperature	-40	125	°C
Ambient Temperature	-40	105	

Electrical Characteristics

($V_{CC} = 10V$, $T_A = 25^\circ C$ unless otherwise specified)

Parameter		Symbol	Test conditions	Min	Typ	Max	Unit
VCC	On Threshold	V_{VCC_ON}		3.6	3.75	3.9	V
	VCC on Hysteresis	V_{VCC_HYS}		75	115	155	mV
	VCC Regulation Voltage	$V_{VCC_REG_VIN}$	$V_{DRAIN}=15V$, $I_{VCC}=2mA$	6.35	6.85	7.35	V
	Quiescent Current	I_Q			160	200	μA
DRAIN	On_threshold	V_{ON_TH}		-240	-190	-140	mV
	Initial Off_threshold (Note 4)	$V_{OFF_INITAIL}$		-45	-30	-15	mV
	Voltage threshold of Forced Turn off (Note 4)	$V_{OFF_TH_FORCE}$		5	20	35	mV
	Time threshold of Forced Turn off (Note 4)	$V_{OFF_TH_FORCE}$		28	40	52	ns
MOSFET	MOSFET Break down Voltage	$V_{DSS(BR)}$	$I_{DRAIN} > 1mA$	40			V
	MOSFET On-state Resistor	$R_{DS(ON)}$	$V_{VCC}=7V$		13	17	$m\Omega$
Blanking Time	Minimum ON Time	T_{ON_MIN}		900	1200	1500	ns
	Minimum OFF Time	T_{OFF_MIN}	$V_{DRAIN} > 2V$	1800	2200	2600	ns
	Maximum ON Time	T_{ON_MAX}		15	19	24	us
OTP	Thermal Shutdown Temperature (Note 4)	T_{SD}		150	160	170	$^\circ C$
	Hysteresis to Resume Operating (Note 4)	T_{OTP_HYS}		15	20	25	$^\circ C$

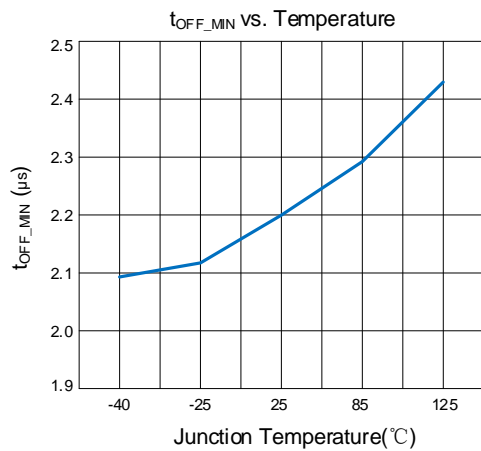
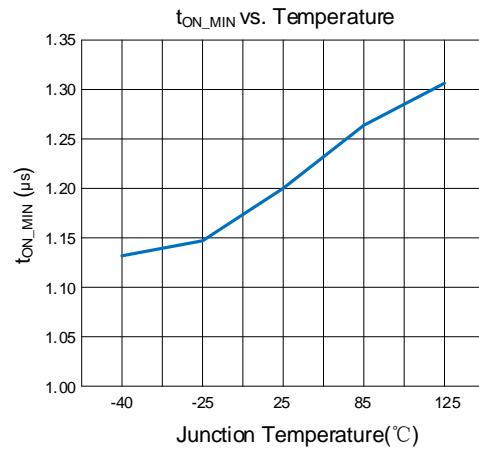
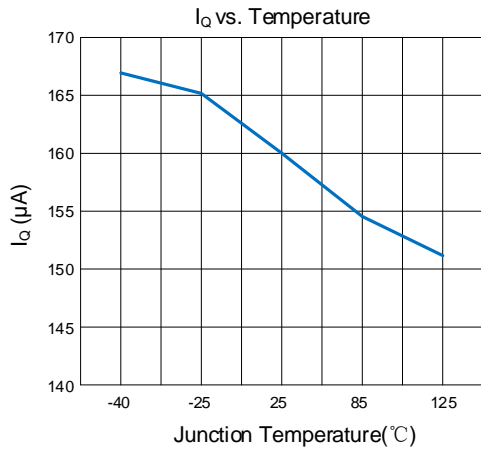
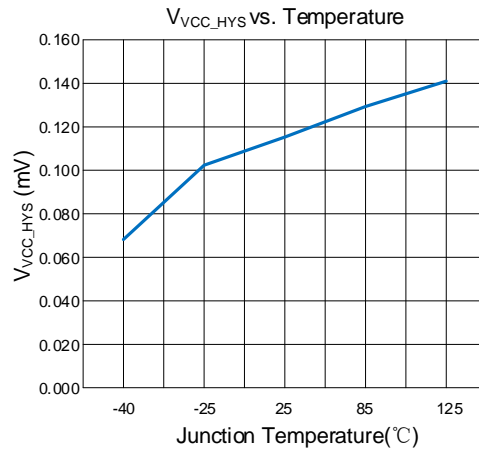
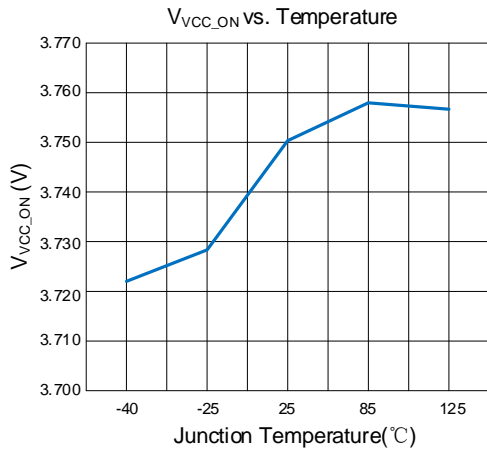
Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Meets JS-001-2017 and JESD78E.

Note 3: θ_{JA} is measured in the natural convection at $T_A = 25^\circ C$ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on “2x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal via to bottom layer ground plane.

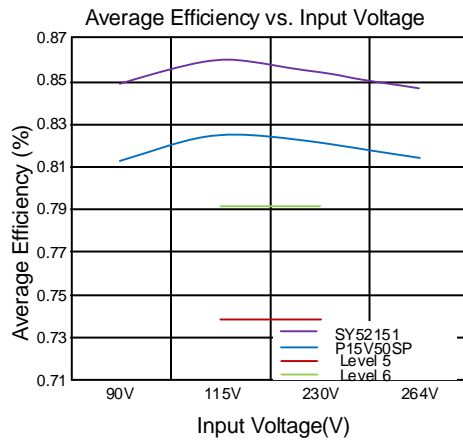
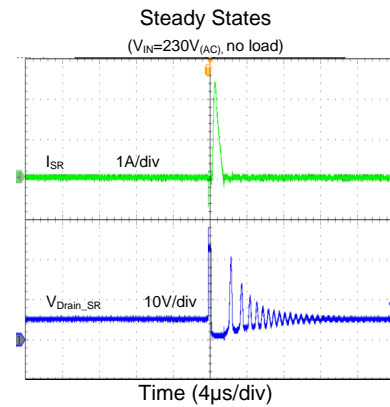
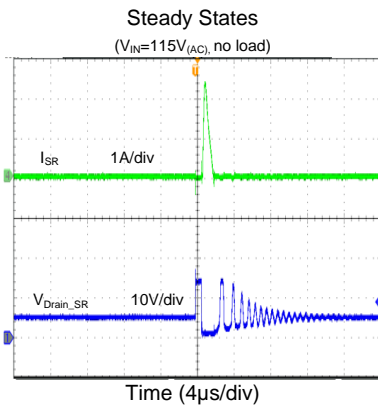
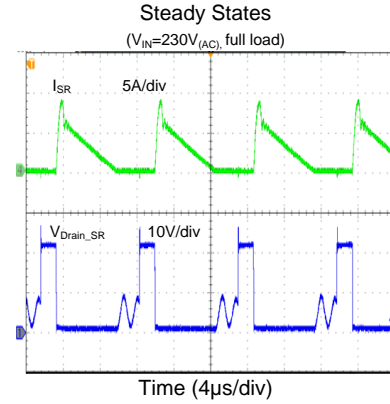
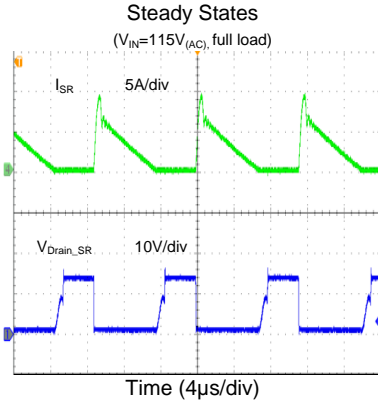
Note 4: Guaranteed by design.

Typical Characteristics



Typical Performance Characteristics

(Test condition: input voltage: 90Vac~264Vac; output spec: 5Vdc_2.1A; Ambient temperature: 25±5 °C; Ambient humidity: 65±25 %.)



Description

SR Turn On

When the primary MOSFET is turned off, V_{DRAIN} will be falling and down to V_{ON_THR} , then turn on the SR MOSFET after a short delay.

Accuracy Zero Current Turn off Strategy

The initial turn-off threshold $V_{OFF_INITIAL}$ of SR switcher is -30mV (typical value). When the Drain voltage on the SR is higher than the turn off threshold, the SR would turn off after a delay time.

The IC adopts a smart control strategy to achieve the SR accuracy zero current turn off by compensating the off threshold each switching period, which also make SR operating in high efficiency and reliability.

Min Ton & Min Toff

After switch-on of the SY52151, the input signal on the DRAIN pin will be blanked during the on blanking time T_{ON_BLANK} . This action eliminates the false switch-off due to high frequency ringing at the start of the secondary stroke. (See ON_BLANK in Fig.3).

After switch-off of the SY52151, the input signal on the DRAIN pin will be blanked during the off-blanking time. This action eliminates false switch-on due to high frequency ringing at the start of the secondary stroke. (See OFF_BLANK in Fig.3)

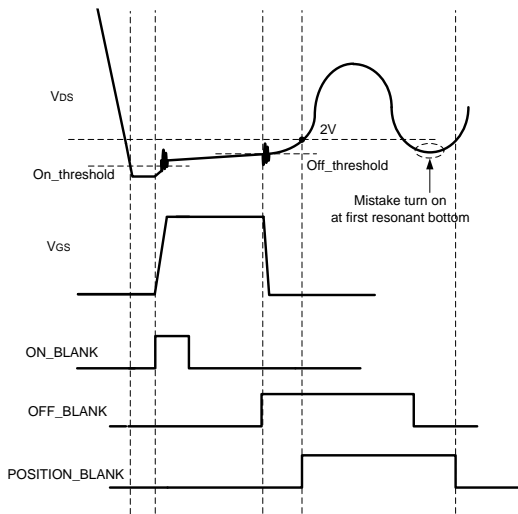


Fig.3 Timing Diagram of Min_ton & Min_toff

To prevent the SR false turn on after the resonant period which caused by primary magnetic inductor and primary equivalent cap, the off blanking time is not enough to accomplish. The position blanking time $T_{POSITION_BLANK}$ can work out. (See $POSITION_BLANK$ in Fig.3)

Self-Power Supply

When SR turns off, the voltage of DSEN will be pulled up. If the voltage of DSEN is higher than voltage of VCC, the charging current will flow to VCC from DSEN. As the voltage of DSEN exceed the Zener diode D2 breakdown voltage, the VCC voltage will be clamped. The charging current of T1 is limited to 30mA (typical value). If the voltage of DSEN is lower than voltage of VCC, the charging function will be shut down. As in Fig. 4.

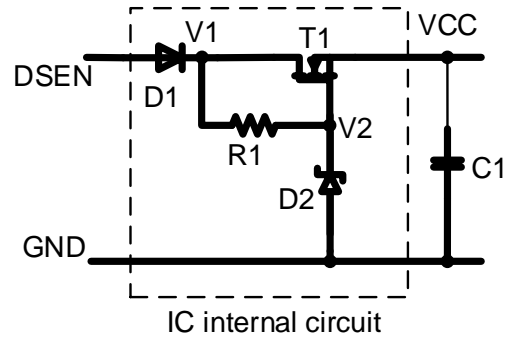


Fig. 4 Circuit Diagram of Self-power Supply

UVLO

The IC will leave the under-voltage lockout state and activate the synchronous rectifier circuit when the voltage on the VCC pin is above V_{VCC_ON} . When the voltage drops below V_{VCC_OFF} , the under-voltage lockout state will be entered and the SR driver output will be actively kept low. As in Fig. 5.

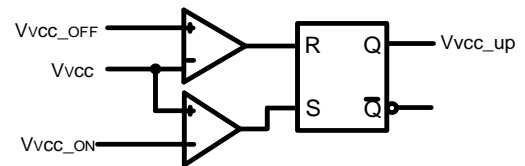


Fig.5 circuit diagram of UVLO

Typical Application Schematic

Typical application circuit information is displayed in a 15W Charger Flyback design. The charger circuit includes a primary side switcher (SY50216N), synchronous rectification switcher (SY52151).

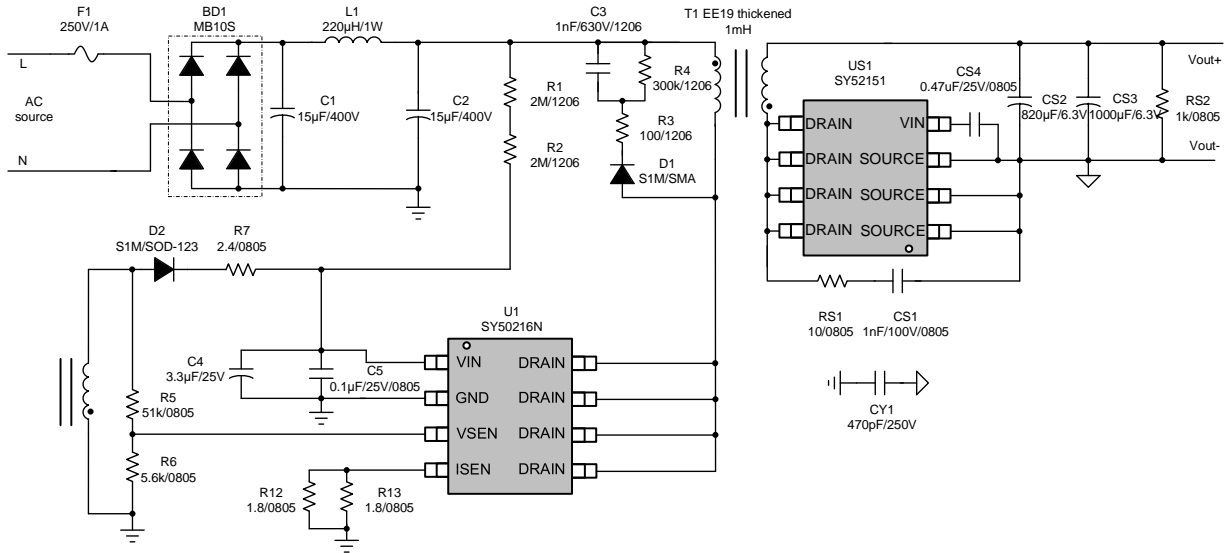


Fig. 6 15W Typical Application Circuit

Recommended BOM List

Designator	Description	Part Number	Manufacturer
RS1	10Ω/0805	0805W4J0100T5E	UNI-ROYAL
RS2	1kΩ/0805	0805W8J0102T5E	UNI-ROYAL
CS1	1nF/100V/ X7R,0805	CC0805KRX7R0BB102	YAGEO
CS2	820µF/16V	SPZ0JM821E09O00R	AISHI
CS3	1000µF/16V	ERS0JM102F16C32T	AISHI
CS4	0.47µF/25V/X7R,0805	CC0805KRX7R8BB474	YAGEO
US1	SY52151FAP/SO8	SY52151FAP	SILERGY

Design Procedure

External Components Selection

The recommended value and voltage rating for CS1 in the most applications are: 0.47uF/25V.

Circuit Parameter Selection

- The secondary side diode freewheeling time should be longer than 1.6us at no-load.
- To prevent the primary and secondary switch conducting at the same time when the circuit operates in Continuous Current Mode, the shut down time of primary switch should be larger than 24uS.

Layout Design

The following PCB layout guidelines for optimal performance and thermal dissipation:

- To achieve better EMI and Efficiency performance, the output connector should be connected to the output cap first, then to the SR Power pin.
- The circuit loop of all switching circuit should be kept

small: secondary power loop, secondary RC snubber circuit loop and IC power supply loop.

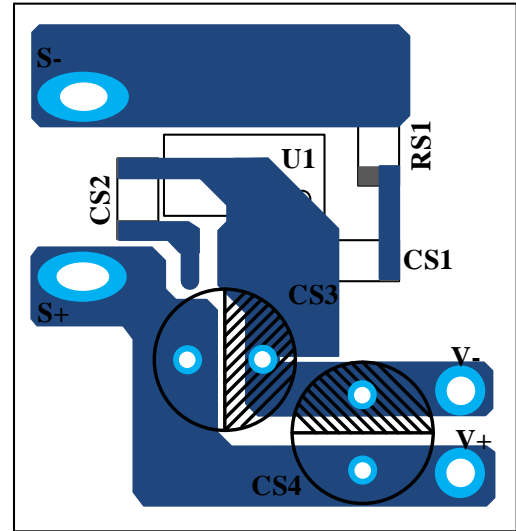
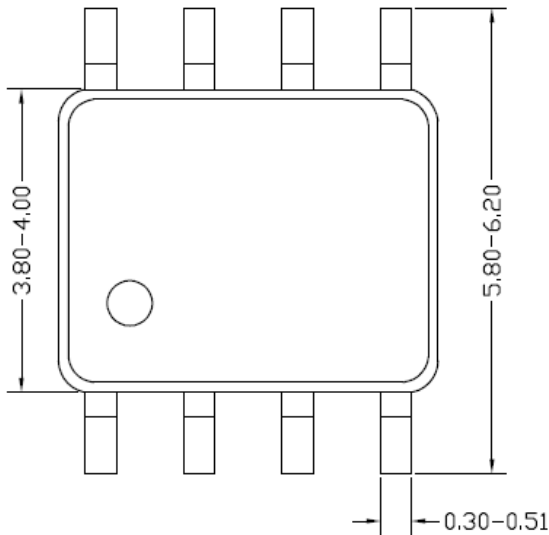
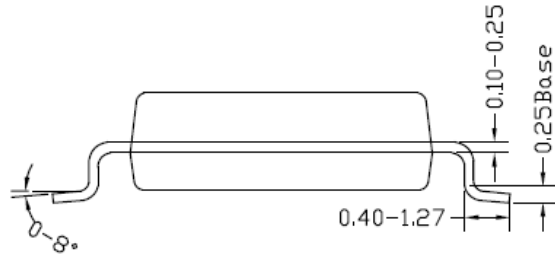


Fig.7 Layout Example

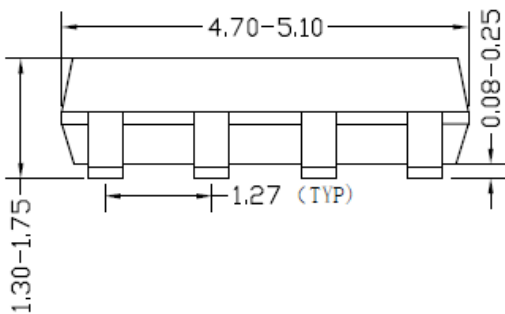
SO8 Package outline & PCB layout design



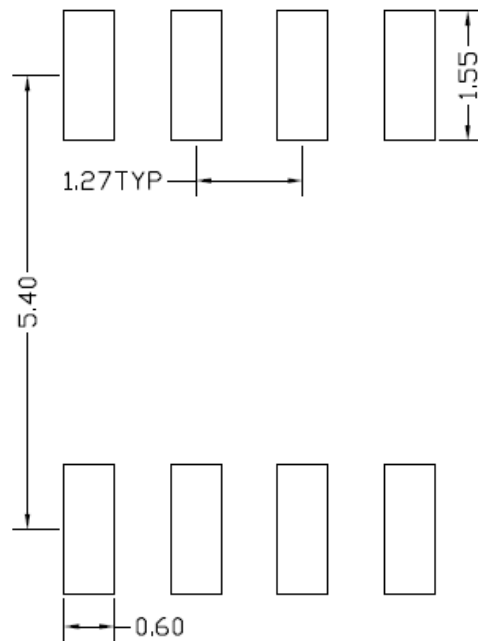
Top view



Side view



Front view



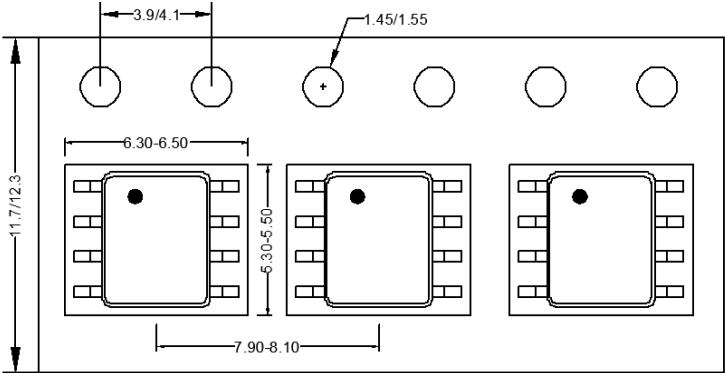
Recommended Pad Layout

(Reference only)

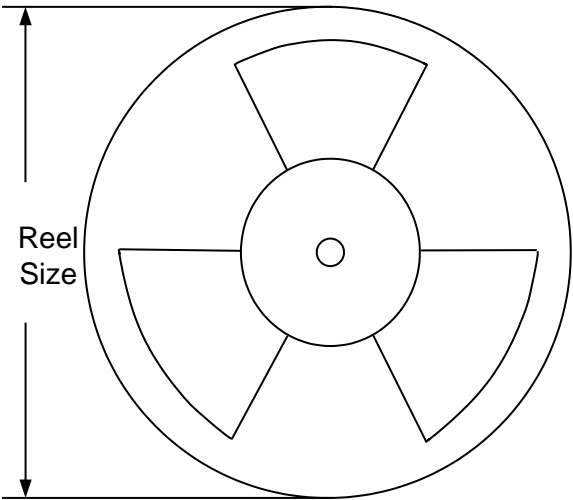
Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

1. Taping orientation for packages (SO8)



2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8	12	8	13"	400	400	2500

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
April 26, 2024	Revision 1.0	Initial Release

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