SQ40222

2.9V-5.5V Input, 20A, Dual Phase Capable, 1.7/2.5/5MHz, Scalable Step Down Regulator with I²C Interface

General Description

The SQ40222 is a high-frequency synchronous step-down DC-DC regulator capable of delivering 20A continuous current to the load, over the input range from 2.9V to 5.5V. The output voltage is adjustable from 0.34V to 1.272V.

It uses a proprietary ripple-based constant on-time architecture with phase locked loop. The SQ40222 can achieve very high loop bandwidth to support fast load transient response within ~500ns. Multi-phase operation allows multiple SQ40222 regulators to run out-of-phase, which increases maximum load current to 40A.

The operating frequency is selectable through I²C between 1.7MHz, 2.5MHz and 5MHz. The high switching frequency provides very compact solution size with small inductor and capacitors. The internal voltage reference provides ±1% accuracy over junction temperature from -40℃ to 125℃. The differential sense pins allow output feedback remote sensing.

The SQ40222 supports cycle-by-cycle current limit, input undervoltage lockout, output undervoltage protection and thermal shutdown, providing safe operation under all operating conditions.

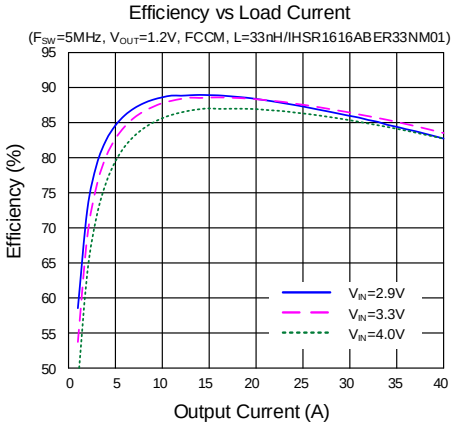
The device is available in a QFN3×4-16 package.

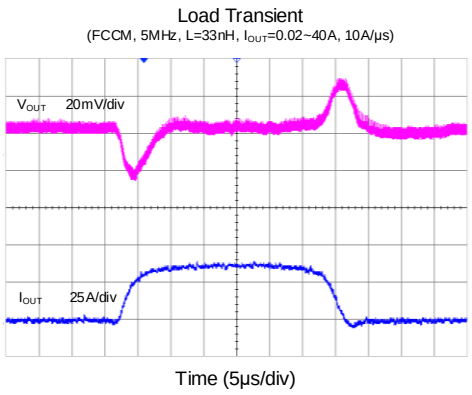
Key Features

- Wide Input Voltage Range from 2.9V to 5.5V
- Single or Dual Phase Operation
- Low $R_{DS(ON)}$ for Internal High-side and Synchronous MOSFETs
- Differential Remote Sense
- Fast Transient Response
  - I²C Programmable Output Voltage from 0.34V to 1.272V
  - Programmable Switching Frequency: 1.7MHz, 2.5MHz and 5MHz
- MTP Memory for Power-On Configuration
- Internal Soft-start
- Reliable Build-in Protections:
  - Automatic Recovery for:
    - Input Undervoltage (UVLO)
    - Output Undervoltage (UVP)
    - Output Short-Circuit (SCP)
    - Overtemperature (OTP)
  - Cycle-by-cycle Valley and Peak Current Limit (OCP)
  - Cycle-by-cycle Reverse Current Limit
- Compact Package: QFN3×4-16
- MSL Rating: MSL3

Applications

- Wireless Cards
- Optical Modules
- Mobile Computing
- DC-DC Modules





Typical Applications

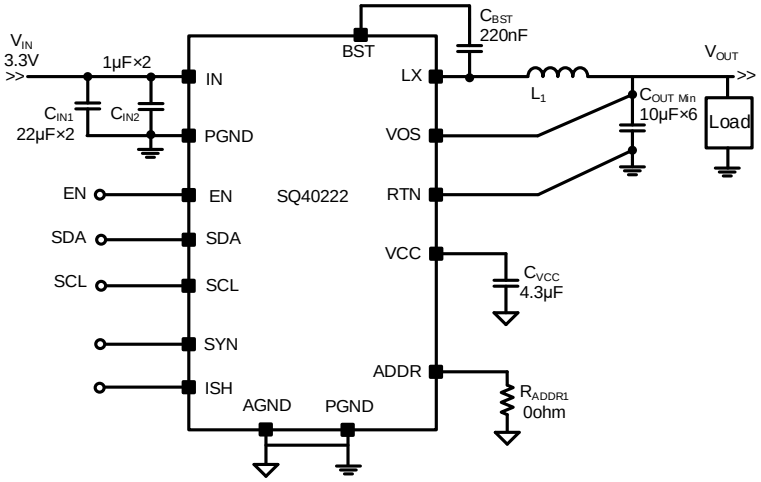


Figure 1. Single-Phase Application

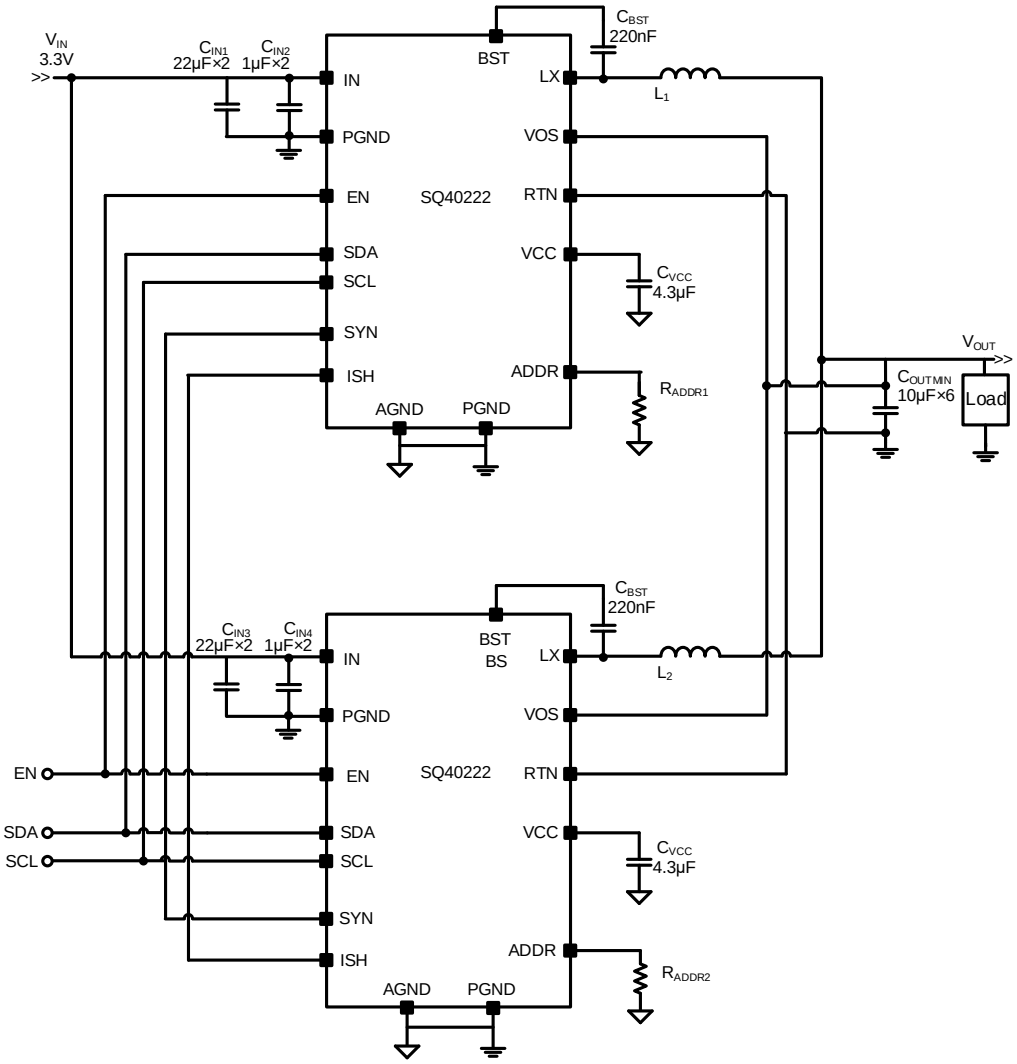


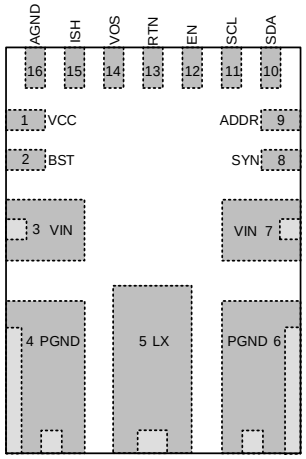
Figure 2. Two-Phase Application

Ordering Information

Ordering Part Number	Package Type	Top Mark
SQ40222QLQ	QFN3×4-16 RoHS-Compliant and Halogen-Free	**GRL*xyz***

x = year code, y = week code, z = lot number code

Pin-Out (Top View)



(QFN3×4-16)

Pin Description

Pin Name	Pin Number	Pin Description
VCC	1	Internal LDO output, power supply for the power MOSFET gate drive circuit. Decouple this pin to power ground with at least a 4.3μF ceramic capacitor.
BST	2	Bootstrap pin for the high-side gate driver supply. Connect this pin to the LX node using a 220nF ceramic capacitor.
VIN	3, 7	Input supply pin for the power and control circuit. Place a decoupling 1μF ceramic capacitor close to each VIN pin.
PGND	4, 6	Power GND pin.
LX	5	Switch pin connected to the internal MOSFETs. Connect the external inductor between this pin and the output capacitors.
SYN	8	Clock synchronization pin. For multiphase-phase application, the SYN pin of both devices should be connected together with a short trace. The peripheral device will synchronize its switching frequency with the Master device generating clock, to obtain a 180 degree phase shift. For single-phase application, this pin should be floating, to select the internal clock.
ADDR	9	Pin to set I²C Device address. Connect a resistor from this pin to GND to program the device address. 0 Ohm sets the address to 0x31; 49.9kOhm sets it to 0x32; 200kOhm sets it to 0x33. When R1 is not populated, the device address is set to 0x34. Dual Phase Operation: There are two dual phase combinations (0x31&0x32 and 0x33&0x34) for using 4 chips as two dual-phase channels on one board. When using the 0x31 and 0x32 combination, the device configured for address 0x31 operates as the master chip. When using 0x33 and 0x34 combination, the device configured for address 0x33 operates as the master chip. The DVS command will be synchronized to the peripheral device in the same group when a command is sent to the master device.
SDA	10	I²C data pin. Connect a pull-up resistor between this pin and the I/O power rail.
SCL	11	I²C clock pin. Connect a pull-up resistor between this pin and the I/O power rail.
EN	12	Enable pin of the device. Pull this pin low to shut down the device, or pull this pin high to enable the device. Do not leave floating.
RTN	13	Negative input of the remote sense amplifier.
VOS	14	Positive input of the remote sense amplifier.
ISH	15	Current sharing pin for multi-phase operation. Tie the ISH pins of all phases together for current sharing. For single phase operation, this pin should be left floating.
AGND	16	Analog GND supply pin for the control circuit. AGND and PGND pin should tie together on Evaluation Board.

Block Diagram

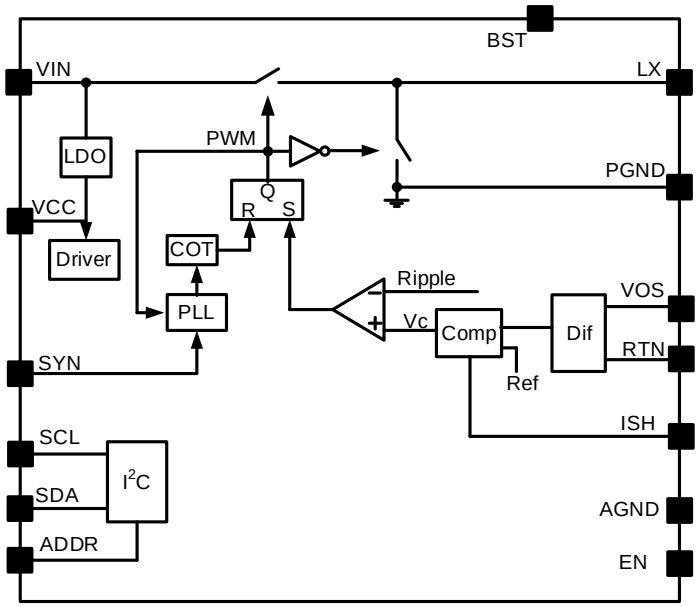


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VIN to GND (**Note 2**)	-0.3	6	V
EN, SDA, SCL, ADDR to GND	-0.3	6	
VCC, SYN, ISH, VOS to GND	-0.3	4	
RTN to GND	-0.3	0.3	
LX to GND (**Note 3**)	-0.3	VIN+0.3	
BST	LX-0.3	LX+4	
Junction Temperature Range	-40	150	°C
Lead Temperature (Soldering, 10 sec.)		260	
Storage Temperature Range	-65	150	
ESD Susceptibility			
HBM (Human Body Model)	±2000		V
CDM (Charged Device Model)	±750		

Thermal Information

Parameter (Note 4)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	21.6	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	5	
P_D Power Dissipation T_A = 25°C	4.6	W

Recommended Operating Conditions

Parameter (Note 5)	Min	Max	Unit
Input Voltage	2.9	5.5	V
Junction Temperature	-40	125	°C
Ambient Temperature	-40	105	

Electrical Characteristics

(V_{IN}=3.3V, V_{OUT}=0.8V, T_J = 25°C, unless otherwise specified. (**Note 6**)).

Parameter		Symbol	Test Conditions	Min	Typ.	Max	Unit
Input Supply	VIN Voltage Range	V_{IN}		2.9	3.3	5.5	V
	UVLO Rising Threshold	V_{UVLOR}	VIN Rising, redo soft-start	2.6	2.7	2.8	V
		V_{PORR}	VIN Rising, enable I^2C	2.5	2.6	2.7	V
	UVLO Falling Threshold	V_{UVLOF}	VIN Falling, stop switching	2.3	2.4	2.5	V
		V_{PORF}	VIN Falling, disable I^2C	2.2	2.3	2.4	V
	Shutdown Current	I_{SD}	EN Pin Pull high, “Reg0x01”[6]=0		0.5		mA
			EN Pin Pull low, Vin=5.5V		10		μA
	Input OVP Threshold	V_{INOV}		5.65	5.8	5.95	V
	Input OVP Hysteresis	$V_{INOVHYS}$			120		mV
	VCC Output Voltage	V_{VCC}			3.3		V
Power Stage	VOUT Voltage Range	V_{OUT}	$V_{OUT}=V_{FB}$	0.34		0.848	V
			$V_{OUT}=1.5\times V_{FB}$	0.51		1.272	V
	VOUT Step Size	V_{STEP}	$V_{OUT}=V_{FB}$		4		mV
			$V_{OUT}=1.5\times V_{FB}$		6		mV
	Output Accuracy		V_{OUT}=1V, T_J = -40°C to 125°C	-1		1	%
		V_{ERROR}	V_{OUT}< 0.6V $V_{OUT}=V_{FB}$, T_J = -40°C to 125°C	-6		6	mV
		V_{ERROR}	V_{OUT}< 0.9V $V_{OUT}=1.5\times V_{FB}$, T_J = -40°C to 125°C	-9		9	mV
	DVS Slew Rate Accuracy		VOUT=VFB : 2.5mv/μs VOUT=1.5×VFB : 3.75mv/μs TJ = 25°C, “Reg0x01”[7]=0	-10		10	%
			VOUT=VFB : 2.5mv/μs VOUT=1.5×VFB : 3.75mv/μs TJ = -40°C to 125°C “Reg0x01”[7]=0	-20		20	%
			VOUT=VFB : 10mv/μs VOUT=1.5×VFB : 15mv/μs TJ = 25°C, “Reg0x01”[7]=1	-10		10	%
			VOUT=VFB : 10mv/μs VOUT=1.5×VFB : 15mv/μs TJ = -40°C to 125°C “Reg0x01”[7]=1	-20		20	%
	Top FET R_{ON}	$R_{DS(ON)\_T}$			1.9		mΩ
	Bottom FET R_{ON}	$R_{DS(ON)\_B}$			1.2		mΩ
	Soft-Start Time	t_{SS}	Vout from 0% to 100%		1.2		ms
	Switching Frequency	F_{SW}	Fsw set 5MHz, “Reg0x01”[4:3]=00	4.5	5	5.5	MHz
			Fsw set 2.5MHz, “Reg0x01”[4:3]=01	2.25	2.5	2.75	MHz
			Fsw set 1.7MHz, “Reg0x01”[4:3]=10/11	1.5	1.7	1.9	MHz
	Current Sharing Accuracy	I_{match}				1	A
	Current Sharing Range	I_{SH}		-5		25	A
	Min ON Time	$t_{ON,MIN}$	V_{IN}=5.5V, V_{OUT} =0.34V		25		ns
	Output Discharge Resistance	R_{DIS}			115		Ω
Protection	High-Side Switch Positive Current Limit	I_{PLMT}	Vin=3.3V, L_{wire}≈100nH, T_J = 25°C		28		A

				Vin=3.3V, L_{wire}≈100nH, T_J= -40°C to 125°C	24	28	31	A
		Low-Side Switch Positive Current Limit	I_{VLMT}	Vin=3.3V, L_{wire}≈100nH, T_J = 25°C		28		A
				Vin=3.3V, L_{wire}≈100nH, T_J= -40°C to 125°C	21	24	27	A
			I_{VLMT_FDB}	Vin=3.3V, L_{wire}≈100nH		18		A
		Low-Side Switch Negative Current Limit	I_{NVLMT}	Vin=3.3V, L_{wire}≈100nH, T_J = 25°C		-7		A
		Thermal Shutdown Threshold	T_{SD}	Junction Temperature		155		°C
		Thermal Shutdown Hysteresis	T_{HYS}			20		°C
		Thermal Warning Threshold	T_{WN}	Junction Temperature		110		°C
		Thermal Warning Hysteresis	T_{WNHYS}			20		°C
		Output Under Voltage Threshold	V_{TH_UVP}		75	80	85	$\%V_{SET}$
		Output Short Circuit Protection Threshold	V_{TH_SCP}		35	40	45	$\%V_{SET}$
IO PINs	EN	EN Logic Level Low					0.4	V
		EN Logic Level High			1.2			V
	SCL, SDA, SYN	Low-Level Input Voltage					0.4	V
		High-Level Input Voltage			1.2			V
	I^2C Interface	I^2C Frequency Capability	F_{I2C}				3.4	MHz

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The PVIN pin can tolerate transient voltages up to 6.5V for a duration of up to 10ns. These transients can occur during normal operation of the device.

Note 3: The SW pin can tolerate transient voltages up to 9V for a duration of 6ns and -1V for a duration of 4ns. These transients can occur during normal operation of the device.

Note 4: Package thermal resistance is measured in the natural convection at T_A=25˚C on an 8cm×8cm size six-layer Silergy Evaluation Board.

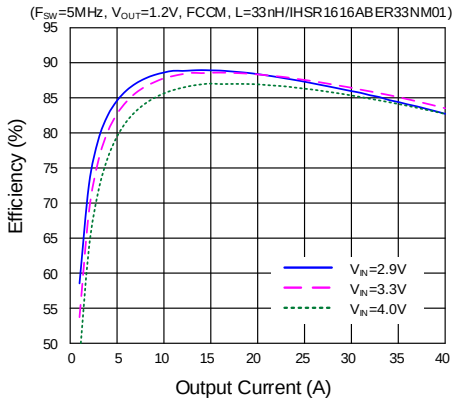
Note 5: The device is not guaranteed to function outside its operating conditions.

Note 6: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25 ˚C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

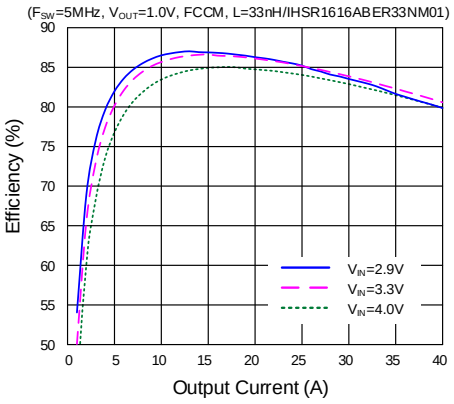
Typical Performance Characteristics

(T_A=25˚C, V_{IN}=3.3V, V_{OUT}=0.8V, L=33nH, C_{OUT}=22μF×6, f_{SW}=5MHz, unless otherwise noted)

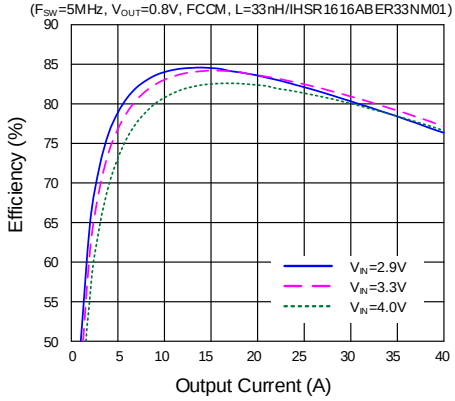
Efficiency vs Load Current
(F_{SW}=5MHz, V_{OUT}=1.2V, FCCM, L=33nH/IHSR1616ABER33NM01)



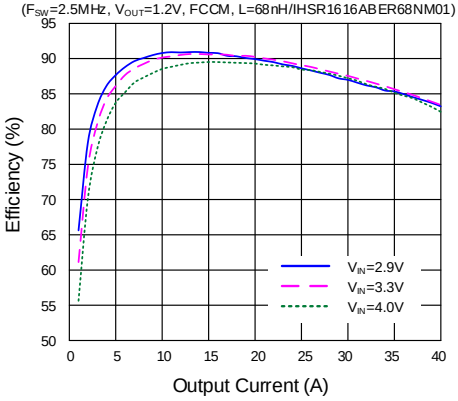
Efficiency vs Load Current
(F_{SW}=5MHz, V_{OUT}=1.0V, FCCM, L=33nH/IHSR1616ABER33NM01)



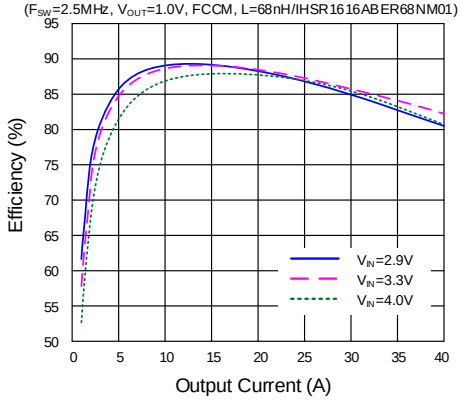
Efficiency vs Load Current
(F_{SW}=5MHz, V_{OUT}=0.8V, FCCM, L=33nH/IHSR1616ABER33NM01)



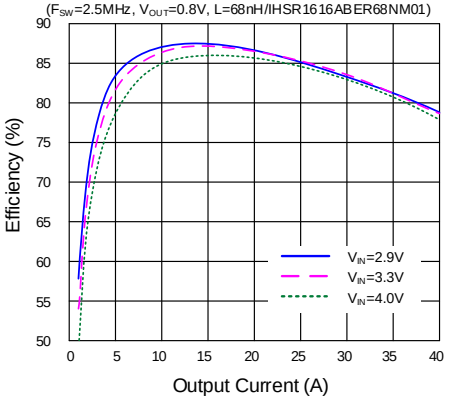
Efficiency vs Load Current
(F_{SW}=2.5MHz, V_{OUT}=1.2V, FCCM, L=68nH/IHSR1616ABER68NM01)



Efficiency vs Load Current
(F_{SW}=2.5MHz, V_{OUT}=1.0V, FCCM, L=68nH/IHSR1616ABER68NM01)

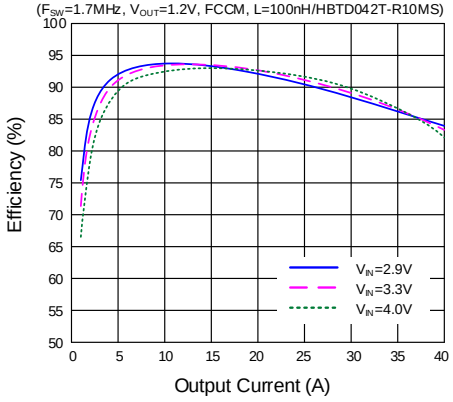


Efficiency vs Load Current
(F_{SW}=2.5MHz, V_{OUT}=0.8V, L=68nH/IHSR1616ABER68NM01)



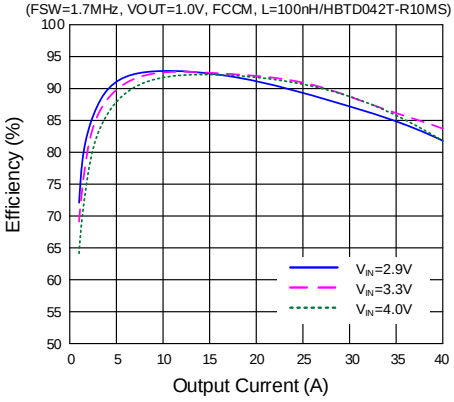
Efficiency vs Load Current

(F_{SW}=1.7MHz, V_{OUT}=1.2V, FCCM, L=100nH/HBTD042T-R10MS)



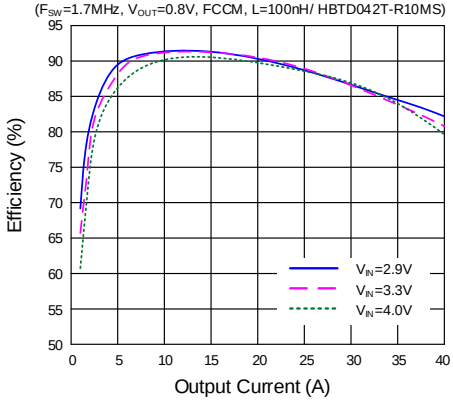
Efficiency vs Load Current

(FSW=1.7MHz, VOUT=1.0V, FCCM, L=100nH/HBTD042T-R10MS)



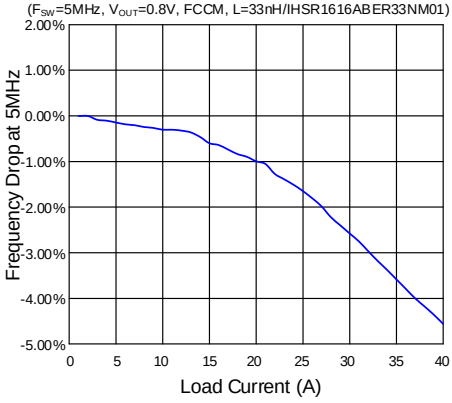
Efficiency vs Load Current

(F_{SW}=1.7MHz, V_{OUT}=0.8V, FCCM, L=100nH/ HBTD042T-R10MS)



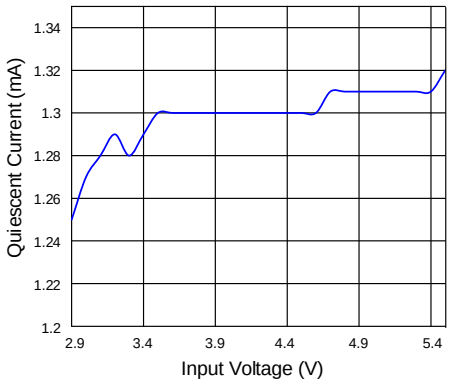
Frequency vs Load Current

(F_{SW}=5MHz, V_{OUT}=0.8V, FCCM, L=33nH/IHSR1616ABER33NM01)



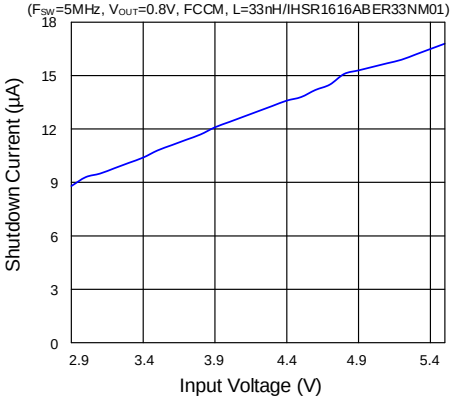
Quiescent Current

(F_{SW}=5MHz, V_{OUT}=0.8V, FCCM, L=33nH/ IHSR1616ABER33NM01)



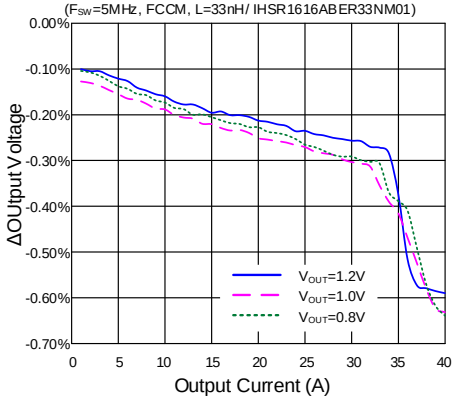
Shutdown Current

(F_{SW}=5MHz, V_{OUT}=0.8V, FCCM, L=33nH/IHSR1616ABER33NM01)



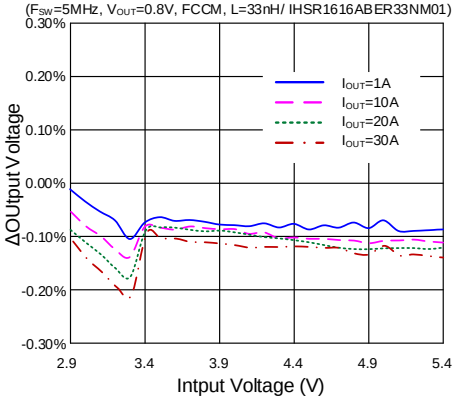
Load Regulation

(F_{SW}=5MHz, FCCM, L=33nH/ IHSR1616ABER33NM01)



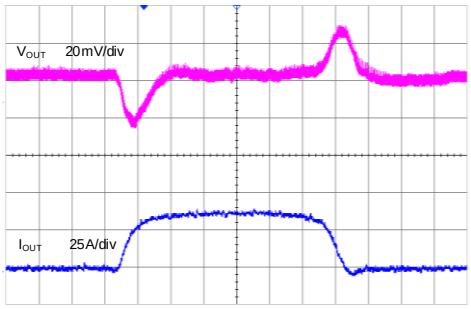
LIne Regulation

(F_{SW}=5MHz, V_{OUT}=0.8V, FCCM, L=33nH/ IHSR1616ABER33NM01)



Load Transient

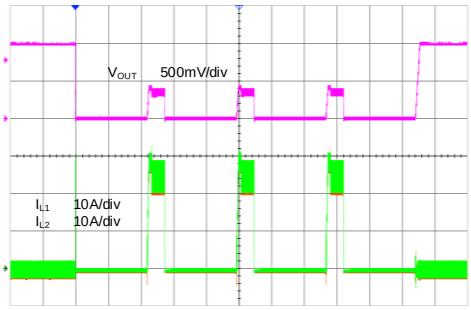
(FCCM, 5MHz, L=33nH, I_{OUT}=0.02~40A, 10A/μs)



Time (5μs/div)

Short Circuit Protection

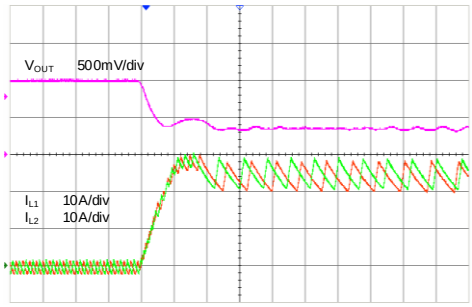
(I_{OUT}=0A~short, L=wire(33nH))



Time (10ms/div)

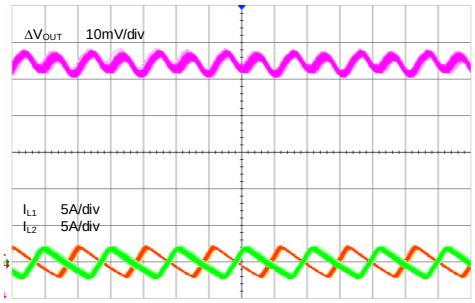
Zoom-in Short Circuit Protection

(I_{OUT}=0A~short, L=wire(33nH))



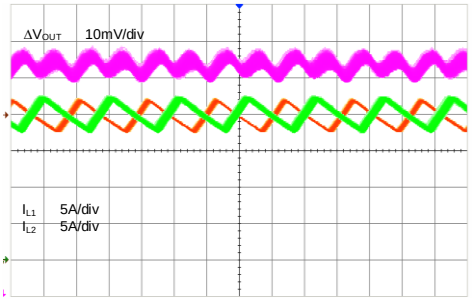
Time (1μs/div)

Current Balance & Output Ripple
(V_{IN}=3.3V, V_{OUT}=1V, I_{OUT}=0A)



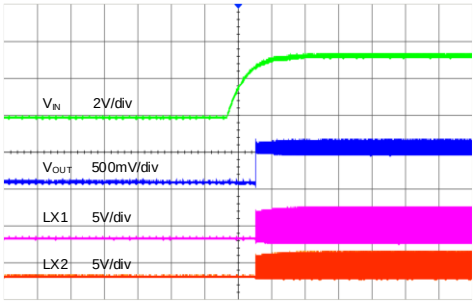
Time (100ns/div)

Current Balance & Output Ripple
(V_{IN}=3.3V, V_{OUT}=1V, I_{OUT}=40A)



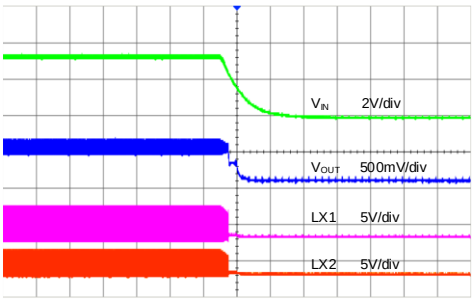
Time (100ns/div)

Startup from VIN



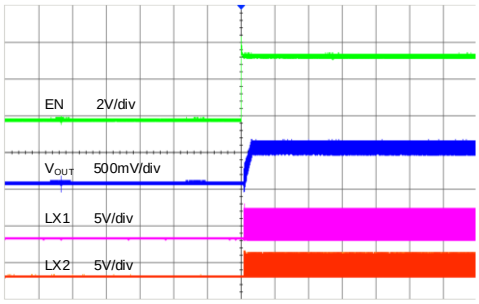
Time (5ms/div)

Shutdown from VIN



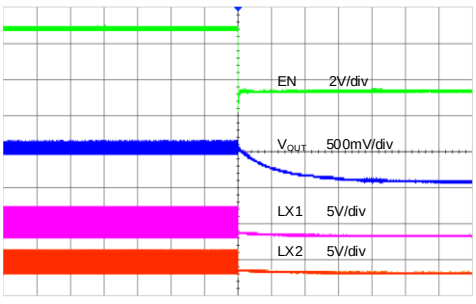
Time (5ms/div)

Startup from EN Pin



Time (5ms/div)

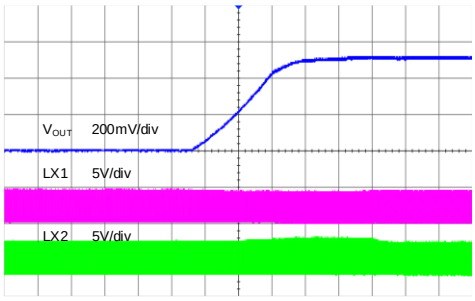
Shutdown from EN Pin



Time (5ms/div)

Dynamic Voltage Scaling

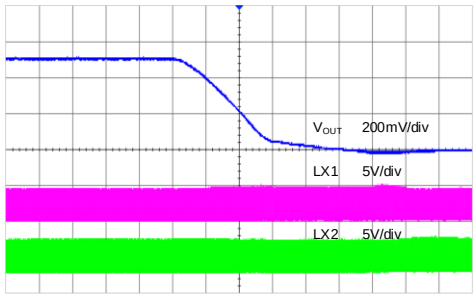
(DVS_SlewRate=10mV/μs, Reg 0x01 [1]=0, V_{OUT}=0.34V→0.848V)



Time (20μs/div)

Dynamic Voltage Scaling

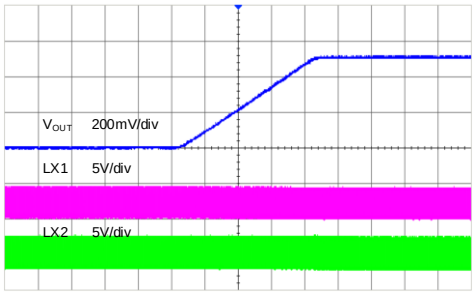
(DVS_SlewRate=10mV/μs, Reg 0x01 [1]=0, V_{OUT}= 0.848V→0.34V)



Time (20μs/div)

Dynamic Voltage Scaling

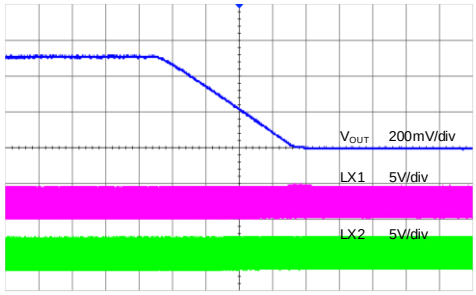
(DVS_SlewRate=2.5mV/μs, Reg 0x01 [1]=0, V_{OUT}=0.34V→0.848V)



Time (50μs/div)

Dynamic Voltage Scaling

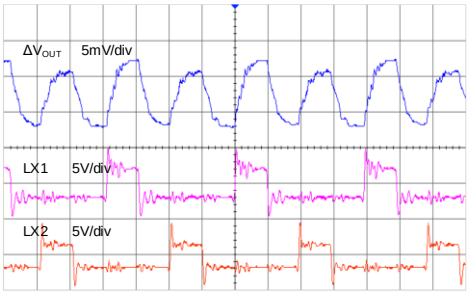
(DVS_SlewRate=2.5mV/μs, Reg 0x01 [1]=0, V_{OUT}=0.848V→0.34V)



Time (50μs/div)

Output Ripple

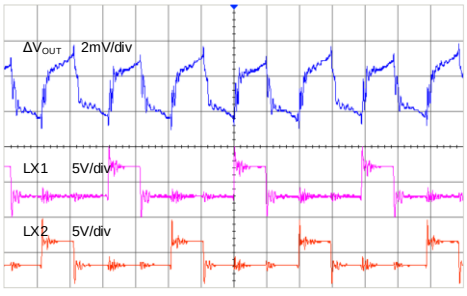
(F_{SW}=5MHz, V_{OUT}=0.848V, FCCM, L=33nH/IHSR1616ABER33NM01, Load=20A)



Time (50ns/div)

Output Ripple

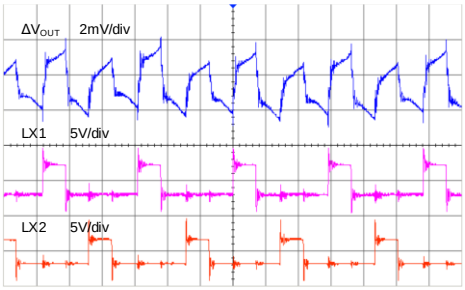
(F_{SW}=2.5MHz, V_{OUT}=0.848V, FCCM, L=68nH/IHSR1616ABER68NM01, Load=20A)



Time (100ns/div)

Output Ripple

(F_{SW}=1.7MHz, V_{OUT}=0.848V, FCCM, L=100nH/HBTD042T-R10MS Load=20A)



Time (200ns/div)

Detailed Description

Ripple-Based Constant On-Time Architecture

The SQ40222 is a constant on-time controlled step-down DC-DC regulator. An internal triangular ripple is generated to mimic the inductor current. The output feedback and reference voltage generate a control voltage. When the ripple drops below the control voltage, the top MOSFET is turned on for a fixed on-time. The on-time (t_{ON}) is internally calculated as $(V_{OUT}/V_{IN})\times(1/f_{SW})$ to operate the regulator at the desired switching frequency over the input and output voltage ranges.

SQ40222 utilizes a high bandwidth error amplifier and a fast comparator to minimize the control loop PWM delay for high frequency operation.

When multiple SQ40222s are paralleled, connect all the ISH pin together to achieve current sharing. Current flowing through the low side MOSFET is sensed during the low-side on time and hold at a capacitor during the low side off time. The ISH signal is the current sense of the master channel and referenced to the slave channel. Each slave compares its current sense to the ISH pin and adjusts its duty-cycle to track the master current. In steady state, each slave current tracks the master current.

Multi-Phase Auto Configuration

When the EN pin is pulled high and VIN reaches the POR voltage (2.6V typically), the device will be enabled and the MTP settings are loaded. Immediately after, the device will check its I²C address set by external ADDR pin. If its address is 0x31 or 0x33, the device is configured as master, otherwise the part will be slave.

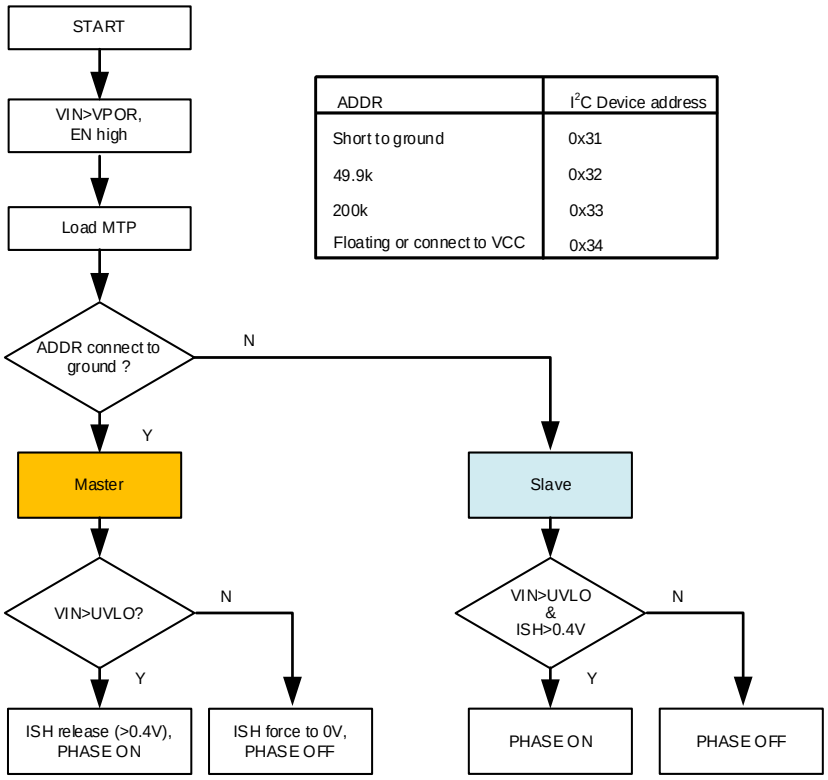


Figure 4. Master/Slave Auto Detection

Interleaving

For interleaving application, the SYN pins of both devices are connected together. The master device's output clock is received by slave device from SYN connection. An inverter buffer in the slave device provides a 180-degree phase shift. A phase lock loop in each part will lock onto SYN's phase. Since the PLL loop response is purposely designed to be much slower than the main control loop, the PWM loses tracking with external clock during a load transient, the transient response still behaves like original COT control.

Dynamic Voltage Scaling (DVS) function

For Optical modules, PC supplies and other high-current applications, dynamic voltage scaling function is frequently used for power management. This device can support the DVS function by sending I²C commands to the master device.

DVS and EN on/off should be written to both master and slave devices at the same time, otherwise the different reference voltages for the two devices will make the current flow to the device with a lower reference, and also increase the output ripple.

The 0x01 and 0x02 registers are designed as common registers. When writing to the 0x01 and 0x02 registers of the master device in the group whose address is 0x31 (or 0x33), the corresponding slave device whose address is 0x32 (or 0x34) will also change its 0x01 and 0x02 register values at the same time.

For example, when writing to I²C address 0x31 a value of 0x41h to register 0x02 to set master device voltage to 0.6V, the slave device whose address is 0x32 on the same I²C bus, will change its 0x02 register value to 0x41h at the same time.

Differential Remote Sense (VOS, RTN)

The SQ40222 provides differential remote sense capability through VOS and RTN pins. This pair of pins should be routed to directly sense the voltage at the load, thus compensating the DC voltage drop along the PCB traces which carry high current.

Minimum On Time

When SQ40222 is configured to operate with high input voltage and low output voltage, the PWM duty cycle becomes very low and minimum on-time threshold is reached. Under this scenario, the switching frequency, fsw, is automatically reduced to maintain regulation.

Linear Regulator (VCC Pin)

The VCC pin supplies internal power MOSFET drivers and other analog circuitry. The VCC pin is fed by an internal linear regulator, which produces 3.3V by default. For correct operation a low ESR 4.3μF ceramic capacitor should be connected between VCC and GND.

External Bootstrap Capacitor (C_{BST})

Proper operation requires a 0.22μF low ESR ceramic capacitor to be connected between BST and LX pins. This bootstrap capacitor provides the gate driver supply voltage for the high-side power MOSFET. The C_{BST} voltage is refreshed by VCC when LSFET is on.

Enable Control and Power Sequence

When EN pin is pulled low, the power stage and most of the internal circuitry are disabled. When EN toggles from low to high, the logic circuitry is active and the device is ready to accept I²C commands. Under this condition, the device can start and stop operation according to the EN bit ("Register 0x01" [6]) value. The logic truth table is shown in Table 1.

Table 1. Enable Control

EN pin	EN bit	Status
0	X	Disable
1	0	Disable
1	1	Enable

When Vin reaches POR(2.6V typically) and EN is high, I²C and service will be activated, and detect if the part is configured as master or slave. Master phase will pull ISH down to 0V when Vin is under UVLO (2.7V typically) and keep the buck off. Once Vin reaches UVLO, the voltage of ISH pin will be released to a normal voltage (indicating the average current of the master phase), typically >0.3V, and enter soft start. The slave will detect both Vin voltage and ISH voltage, and when V_{ISH} goes above 0.3V the phase will be activated and start to switch.

When Vin drops under UVLO, the master will shut down, and pull ISH voltage to 0V. Once slave detects that the ISH voltage is less than 0.3V, the part will shut down immediately.

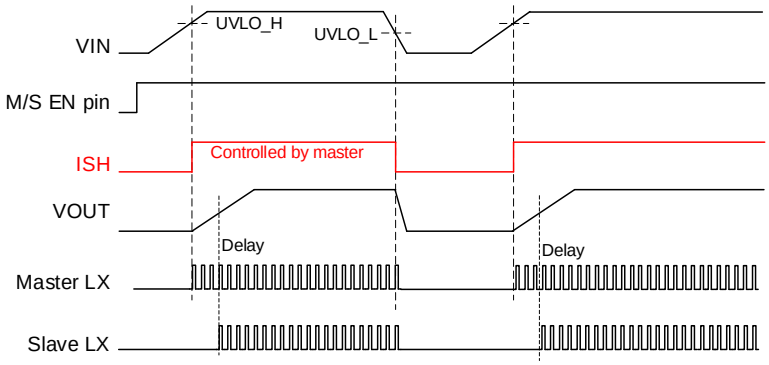


Figure 5. VIN Start Up and Shut Down Sequence

Protection Features

The SQ40222 offers integrated input overvoltage (OVP), output undervoltage (UVP), output short circuit (SCP) protections, as well as thermal warning and thermal shutdown protection. Only the master device has following protections, the protection of slave is disabled. The slave is only controlled by detecting ISH voltage which is sent from master.

Table 2. Protection Features

Protection	Threshold	Deglitch Time	Operation
Thermal shutdown	Rising: 155°C Falling: 135°C	-	Shutdown when temperature rises above155°C Restart when temperature falls below 135°C Record to FLT_TEMP_SD bit (“Register 0x05” [5]).
Thermal warning	Rising: 110°C Falling: 90°C	-	Warning when temperature rises above 110°C Remove when temperature falls below 90°C Record to FLT_TEMP_DIE bit (“Register0x05” [4]).
Output UVP	80%*V_{set}	170μs	Hiccup mode auto-recovery. Record to FLT_VO_UVP bit (“Register0x05” [3]).
Output SCP	40%*V_{set}	10μs	Hiccup mode auto recovery. Record to FLT_VO_SCP bit (“Register 0x05” [7]).
Input OVP	5.8V	4μs	Shutdown when PVIN or AVIN>5.8V, Restart when PVIN and AVIN<5.6V Record to FLT_VIN_OV bit (“Register 0x05” [2]).

Note: Hiccup mode consists of turn-off for a duration of 16 soft-start time intervals, followed by turn-on for a duration of 4 soft-start intervals, repeatedly.

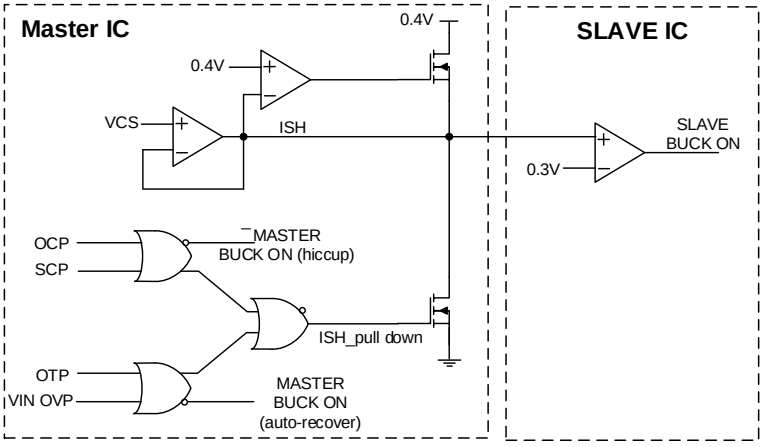


Figure 6. Protection Logic for Master/Slave

Thermal Warning and Thermal Shutdown

The SQ40222 provides thermal warning function and thermal shutdown protection. If the junction temperature is higher than 110°C, the thermal warning [FLT_TEMP_DIE] bit will be set to 1. The bit can be reset to 0 after I²C read, when the temperature drops below 90°C. The thermal warning function is activated when the EN pin is pulled high.

As the temperature goes higher, the device goes into thermal shutdown when the junction temperature exceeds 155°C. In this mode, the HSFET and LSFET are turned off, and the thermal shutdown [FLT_TEMP_SD] bit will be set to 1. When the junction temperature falls below 135°C, the device will be re-enabled automatically, and the [FLT_TEMP_SD] bit will be reset to 0 after I²C read.

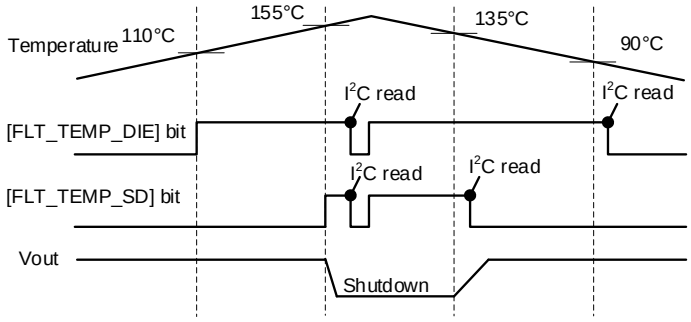


Figure 7. Thermal Shutdown and Thermal Warning Conditions

Cycle-by-Cycle Current Limit

The SQ40222 integrates a total of three current limits to prevent device damage by limiting the maximum and minimum inductor current under all operating conditions.

During HSFET on time, when I_{PLMT} is reached and detected, HSFET is turned off and LSFET is turned on, even if the on-time timer has not expired.

The SQ40222 also implements a negative current limit I_{NLMT}. During LSFET on-time, when I_{NLMT} is reached and detected, LSFET is turned off and HSFET is turned on, regardless of the command from the control loop, to prevent excessive negative inductor current.

A third current limit, I_{VLMT} is implemented as a prerequisite for the next HSFET turn on event. During LSFET on-time, the inductor current must fall below I_{VLMT} before the control loop is allowed to turn on HSFET. This sets a maximum limit to the starting point of inductor current when it ramps up (HSFET is on), and helps to limit the peak inductor current under extreme operating conditions scenarios. In order to reduce power consumption, the current limit threshold I_{VLMT} will be reduced to I_{VLMT_FDB} when inductor current reaches I_{PLMT} three times in a row. For example, when the device operates at 5MHz switching frequency, with very low duty cycle, I_{PLMT} is reached but not detected due to the short HSFET on time, which is lower than peak current detection blanking time.

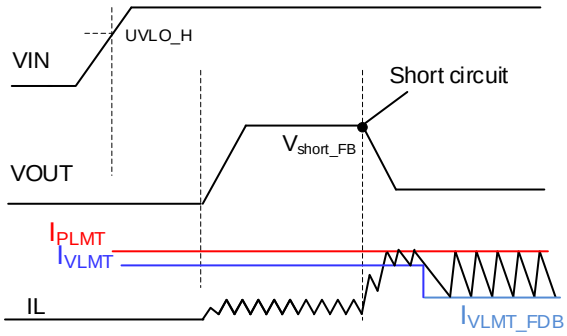


Figure 8. Cycle-by-Cycle Current Limit

Undervoltage Protection

Similar to short circuit protection, the device also includes an undervoltage protection function. When the output voltage drops below 80% of the target voltage for a duration of 170μs, the regulator enters hiccup mode. The restarting pattern will continue until the overload condition is removed. The UVP fault detection is disabled during the normal power up, shutdown and Dynamic Voltage Scaling (DVS).

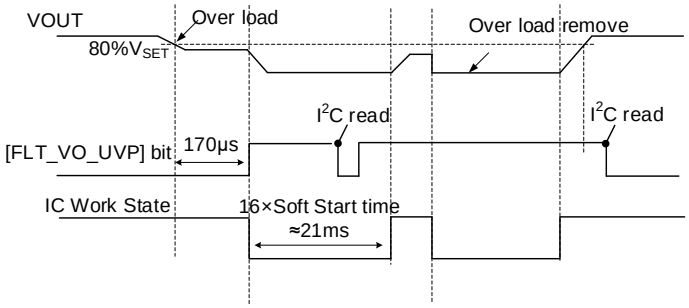


Figure 9. Short Circuit Protection Condition

Short-Circuit Protection

In a short-circuit condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to fall. As soon as the output voltage falls lower than 40% of the target voltage for a duration of 10μs, the regulator will enter hiccup mode. After the hiccup mode off time, the device initiates a soft start and tries to recover from short-circuit. The device operates in this mode until the short-circuit condition is removed.

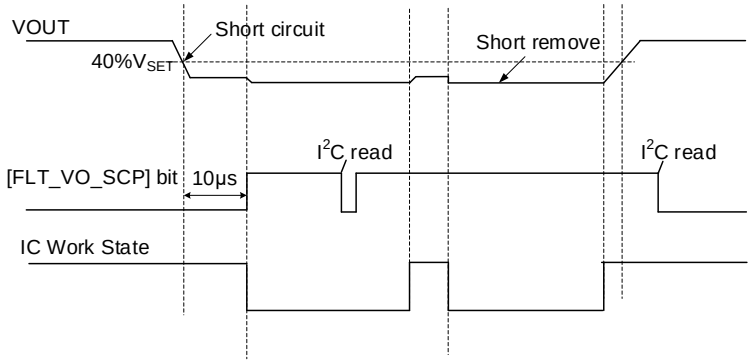


Figure 10. Short Circuit Protection Condition

Input Overvoltage Protection

The SQ40222 provides input OVP function, used to protect the device from high-voltage stress. When VIN exceeds 5.8V, the regulator is turned off. When VIN decreases below 5.6V, the regulator restarts. The input OVP fault detection is activated when EN pin is pulled high.

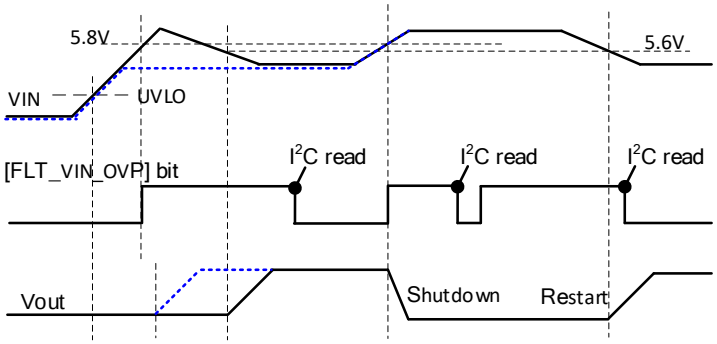


Figure 11. Input Overvoltage Logic for Master/Slave

Application Details

Input Capacitor Selection

Input filter capacitors are needed to reduce the ripple voltage on VIN pin caused by the switching current. X5R or X7R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability and high RMS current ratings over a wide temperature and voltage range. When the VIN pin is supplied by long routing with high parasitic inductance, to prevent device damage due to inductive voltage ringing, some bulk capacitance in parallel with ceramic capacitors is considered helpful. These bulk capacitors can be electrolytic, tantalum or polymer capacitors.

The max RMS ripple current (equation 1) occurs at D=0.5. For optimal operation, choose the input capacitor with an RMS current rating greater than half of the maximum load current.

$$I_{\text{cin\_RMS}} = I_{\text{out}} \times \sqrt{D(1-D)} \qquad \text{Equation 1}$$

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using Equation 2, and the worst-case occurs at D=0.5.

$$V_{cin\_ripple} = \frac{D(1-D)I_{\text{out}}}{f_s \times C_{\text{in}}} \qquad \text{Equation 2}$$

Two 22μF in parallel with two 1μF capacitors are sufficient in most applications. Place the ceramic input capacitors as close to the VIN and GND pins as possible.

Inductor Selection

The inductor selection is a trade-off between efficiency, size and transient performance for a given application. A lower inductance helps reduce the inductor size and enhance transient response, but it increases the inductor ripple current and output voltage ripple. A low DC resistance (DCR) inductor usually reduces DC losses and increases efficiency. For the same size inductance, higher inductor values tend to have higher DCR and slower transient response. Follow the steps below for choosing a suitable inductor.

Select an inductor ripple current ΔI_L equal to 20% ~ 40% of the desired full load current to get an inductor value range, as described in Equation 3.

$$L_o = \frac{V_{out} \times (V_{in} - V_{out})}{V_{in} \times f_{sw} \times \Delta I_L} \qquad \text{Equation 3}$$

As an example, for a typical application with 3.3V V_{IN}, 1V V_O, 20A full load current for each phase, operating at 5MHz, using a target inductor ripple current ΔI_L of 20% or 4A, the approximate inductance value is 35nH. Using the same method, 65nH is the inductance value for 2.5MHz respectively.

Select the nearest standard inductor value, and choose the inductor with saturation current higher than the I_{PEAK}:

$$I_{peak} = I_{out\_\max} + \frac{\Delta I_L}{2} \qquad \text{Equation 4}$$

Select the inductor with relatively low DCR which meets the value, size and cost requirements.

Output Capacitor Selection

The output ripple with 5MHz interleaved switching frequency is different from a conventional low frequency buck regulator. As the Equivalent Series Inductance (ESL) at 5MHz is much larger than that at 1.7MHz, the output ripple is dominated by ESL caused square wave. Using several small sized capacitors with low ESL, connected in parallel, is recommended for low output ripple. Reverse package ceramic capacitors feature much lower ESL. One such example is the Murata LLL series. The following figure provides two output capacitor solutions.

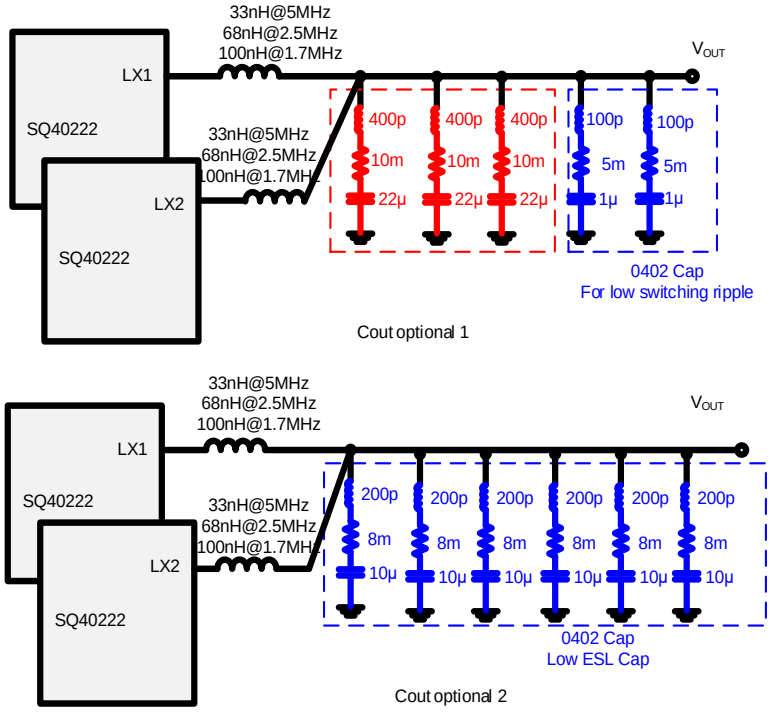


Figure 12. Output Capacitor Solution for 5MHz Application

The total output capacitor ripple can be calculated using Equation 5

Equation 5

$$v_{OUT}(t) = v_{ESR}(t) + v_{ESL}(t) + v_{COUT}(t)$$

$$0 \le t \le D \cdot T_{SW} \ (On\text{-}time\ Phase)$$

$$v_{ESR}(t) = R_{ESR}\left(\frac{\Delta I_L \cdot t}{D \cdot T_{SW}} - \frac{\Delta I_L}{2}\right) \quad v_{ESL}(t) = \frac{L_{ESL} \cdot \Delta I_L}{D \cdot T_{SW}} \quad v_{COUT}(t) = \frac{\Delta I_L \cdot t^2}{2C_{OUT} \cdot D \cdot T_{SW}} - \frac{\Delta I_L \cdot t}{2C_{OUT}} \quad 0 \le t \le D \cdot T_{SW}$$

$$D \cdot T_{SW} \le t \le T_{SW} \ (Off\text{-}time\ Phase)$$

$$v_{ESR}(t) = R_{ESR}\left[\frac{\Delta I_L}{2} - \frac{\Delta I_L \cdot (t - D \cdot T_{SW})}{(1-D) \cdot T_{SW}}\right] \quad v_{ESL}(t) = \frac{L_{ESL} \cdot \Delta I_L}{(1-D) \cdot T_{SW}} \quad v_{COUT}(t) = \frac{\Delta I_L \cdot (t - D \cdot T_{SW})}{2C_{OUT}} - \frac{\Delta I_L \cdot (t - D \cdot T_{SW})^2}{2C_{OUT} \cdot (1-D) \cdot T_{SW}} \quad D \cdot T_{SW} \le t \le T_{SW}$$

PCB Layout Recommendations

The SQ40222 is a high frequency switching regulator and proper PCB layout is critical for stable operation. For best results, refer to Figure 13 and follow the guidelines below.

A six-layer PCB has its layers named layer 1 to layer 6, from top to bottom layer. Layer 2 should be a complete GND copper plane for reduced switching path and noise immunity. Layer 6 should be used as a signal layer with Layer 5 a complete GND copper plane. The insulation thickness between layer 1 and layer 2, layer 3 and layer4, layer 5 and layer 6 should be minimized to reduce input loop parasitic inductance and noise immunity. 75μm is recommended for 1oz copper.

Place VIN copper islands on layer 1 (top) and layer 3&4 (mid) to form a sandwich structure with the inner GND plane, to reduce parasitic impedance from the input MLCC to the SQ40222. The VIN copper should be symmetrical for SQ40222 VIN pins on both-sides, which can help reduce EMI.

Place as many PGND vias as possible underneath the package and close to the C_{IN} and C_{OUT} capacitors' pads to minimize both parasitic impedance and thermal resistance.

Place low ESL input capacitors on the layer 1 as close as possible to the PVIN and PGND pins to reduce the parasitic PCB inductance, which can adversely affect operation.

The VOS and RTN lines are used to sense the output voltage and should be routed directly from the load. Keep the VOS and RTN traces away from switching nodes or high-speed digital signals. Use similar vias for both traces to compensate for the delay.

Avoid right-angle bends in a trace and try to route them at least with two 45° corners to minimize any VOS/RTN impedance change. Differential traces should be routed as close as possible to get a high coupling factor.

Place the BST cap and VCC decoupling cap as close to the SQ40222 pins as possible. Reduce the number of vias for the BST driving path. It's recommended to use a bootstrap cap of 0.22μF up to 1μF.

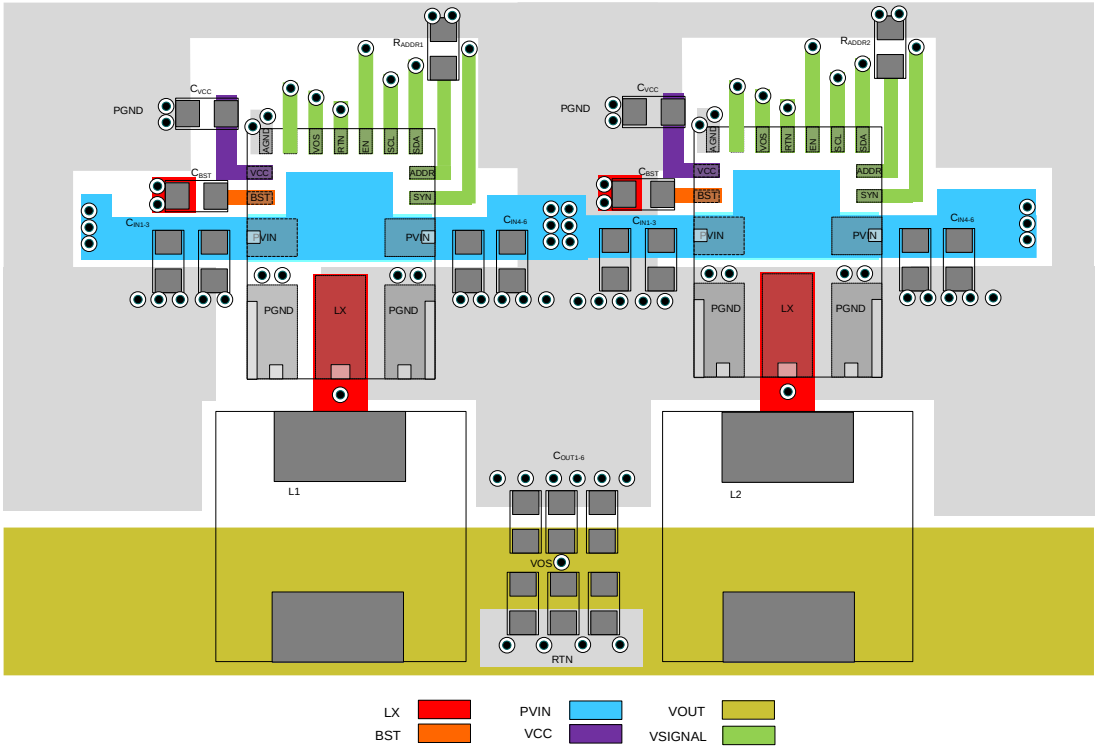


Figure 13. Recommended PCB Layout (Top Layer View)

Typical Application

The schematic diagram of the SQ40222 regulator with 40A load current is shown in Figure 14.

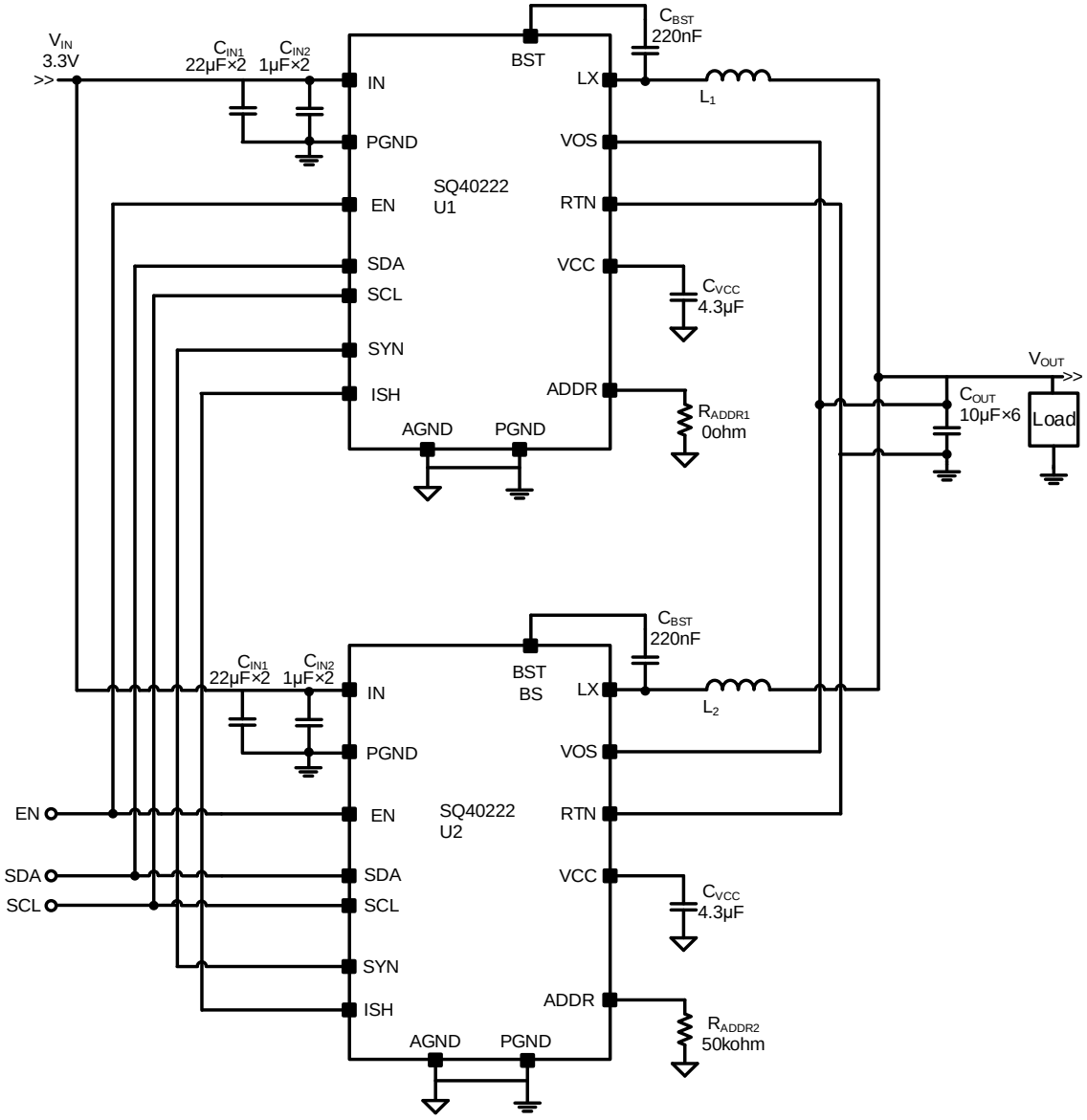


Figure 14. Two-phase Application Schematic

The output voltage set point is 0.46 V and the input voltage ranges from 2.9V to 5.5V. The switching frequency is set to 1.7 MHz using an I²C command. The soft-start time is 2ms. The relevant power stage components are listed in Table 3.

Table 3. Bill of Materials (V_{IN} = 2.9V to 5.5V, V_{OUT} = 0.46V, I_{OUT} =40A, F_{SW} = 1.7MHz)

REF DES	DESCRIPTION	VENDOR	PART NUMBER	QUANTITY
C_{IN1}	CAP, CERM, 22μF, 6.3V, ±20%, X5R, 0402	Murata	GRM158R60J226ME01DA	2*2phase
C_{IN2}	CAP, CERM, 0.1μF, 6.3V, ±10%, X6S, 0201	TDK	C0603X6S0J104K030BC	2*2phase
C_{VCC}	CAP, CERM, 4.3μF, 4V, ±20%, X5R, 0204	Samsung	CLL6A435MR4NLNC	1*2phase
C_{BST}	CAP, CERM, 220nF, 16V, ±10%, X7R, 0402	TDK	C1005X7R1C224K050BC	1*2phase
$L_{1@5MHz}$	IND, 33nH, 37A, 1.15mΩ, 4mm×4mm	VISHAY	IHSR1616ABER33NM01	1*2phase
$L_{1@2.5MHz}$ (option1)	IND, 65nH, 30A, 0.3mΩ, 4mm×4mm	SUNLORD	WPZ04044S165NKT	1*2phase
$L_{1@2.5MHz}$ (option2)	IND, 68nH, ±20%, 30A, 3.2mΩ, 4mm×4mm*1.15m	VISHAY	IHSR1616ABER68NM01	1*2phase
$L_{1@1.7MHz}$	IND, 100nH, ±20%, 34A, 1.3mΩ, 4.1mm×4.1mm*2mm	CYNTEC	HBTD042T-R10MS	1*2phase
C_{O1}	CAP, CERM, 10μF, 4V, ±20%, X6S, 0402	Murata	GRM155C80G106ME44D	6
R_1	RES, 0Ω, 1%, 0.063W, 0402	YAGEO	RC0402FR-070RL	1
R_2	RES, 49.9kΩ, 1%, 0.063W, 0402	YAGEO	RC0402FR-0749K9L	1
U_1	Synchronous Buck Regulator	Silergy	SQ40222QLQ	1*2phase

I²C Compatible Interface

The SQ40222 features an I²C interface that allows the HOST to set the desired parameters and read out fault conditions. The I²C interface supports clock speed up to 3.4Mbps and uses standard I²C commands. The I²C Device address is programmed by ADDR pin. The SQ40222 always operates as a peripheral device, and is addressed using a 7-bit address followed by an 8th bit, which indicates whether the transaction is a read or write operation.

The I²C interface is fully functional after VIN goes above V_{PORR} threshold.

Table 4. I²C Device Address Configuration

ADDR Pin	I²C Device address
0ohm to GND	0x31
49.9kohm to GND	0x32
200kohm to GND	0x33
Floating or connect to VCC	0x34

START and STOP Conditions

The START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition. The I²C master always generates the START and STOP conditions.

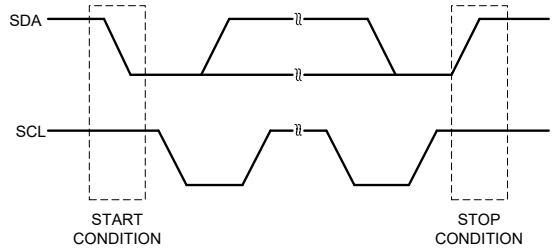


Figure 15. I²C START and STOP Conditions

Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

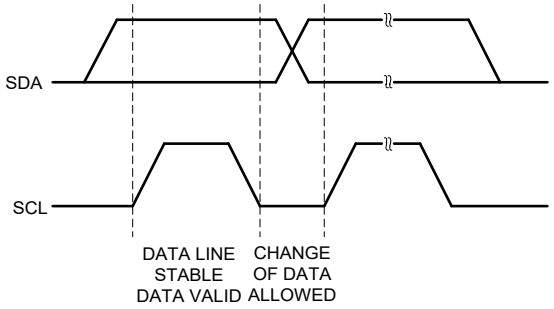


Figure 16. I²C Data Validity Condition

Acknowledge

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the master sends 7 address bits and an R/$\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the peripheral to acknowledge receipt of register addresses and data.

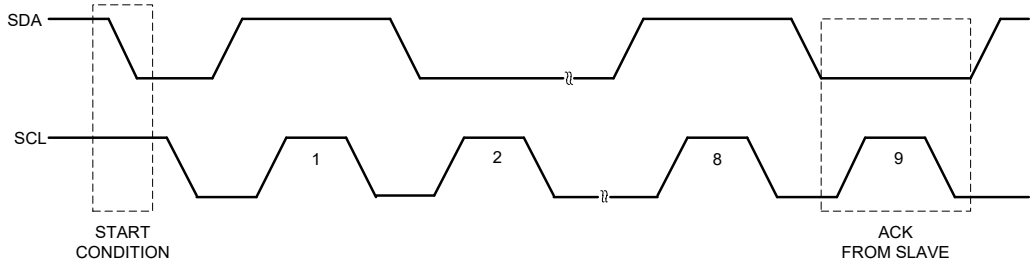


Figure 17. I²C Acknowledge Condition

Data Transactions

All transactions start with a control byte sent from the I²C host device. The control byte begins with a START condition, followed by 7-bits of the peripheral address for the SQ40222 (this address can be changed if necessary), followed by the 8th bit, R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for write or 1 for read. If any peripheral devices on the I²C bus recognize their address, they will acknowledge by pulling the SDA line low for the ninth clock cycle. If no devices exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge (NACK) condition. Once the control byte is sent, and the SQ40222 acknowledges it, the 2nd byte sent by the host must be a register address byte. The register address byte tells the SQ40222 which register the host will write or read. Once SQ40222 receives a register address byte it responds with an acknowledge (ACK).

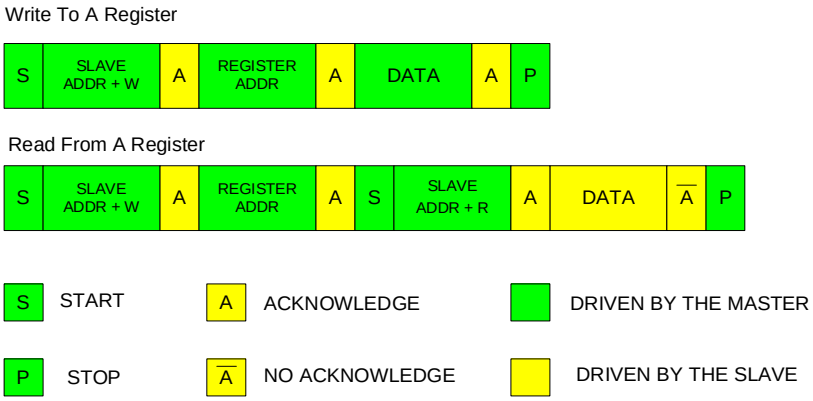


Figure 18. Data Transfer Format in Standard/Fast Mode

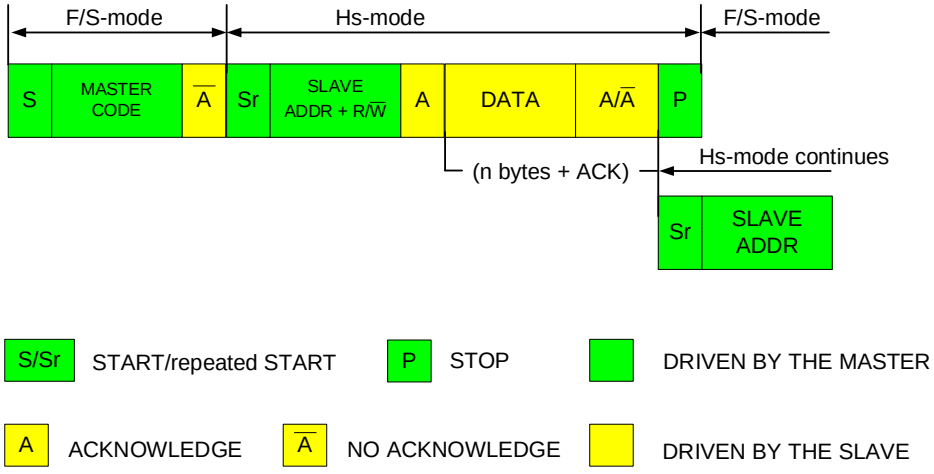


Figure 19. Data Transfer Format in Hs-Mode

I²C Interface Timing Diagram

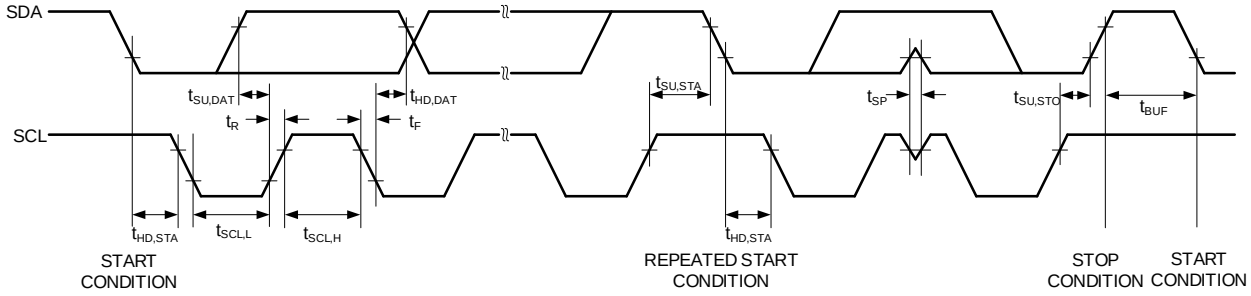


Table 5. I²C Specifications

Characteristics	Symbol	Units	Standard Mode		Fast Mode		High-Speed Mode	
			Min	Max	Min	Max	Min	Max
SCL Clock Frequency	f_{SCL}	kHz	0	100	0	400	0	3400
Hold Time (repeated) START Condition. (After this period, the first clock pulse is generated.)	$t_{HD;STA}$	µs	4		0.6		0.16	
LOW Period of the SCL Clock	t_{LOW}	µs	4.7		1.3		0.16	
HIGH Period of the SCL Clock	t_{HIGH}	µs	4		0.6		0.06	
Set-up Time for a Repeated START Condition	$t_{SU;STA}$	µs	4.7		0.6		0.16	
DATA in Hold Time	$t_{HD;DAT}$	ns	0	900	0	900	0	70
DATA out Hold Time	$t_{HD;DAT}$	ns		900		900		70
Data set-up Time	$t_{SU;DAT}$	ns	250		100		10	
Rise Time of both SDA and SCL Signals	t_r	ns		1000	5	300	5	40
Fall Time of both SDA and SCL Signals	t_f	ns		300	5	300	5	40
Set-up Time for STOP Condition	$t_{SU;STO}$	µs	4		0.6		0.16	
Bus Free Time between STOP and START Conditions	t_{BUF}	µs	4.7		1.3			
Capacitive Load for Each Bus Line	C_b	pF		400		400		100

Register Map

Table 6 Register Map

Address	Register
0x00	MTP_CTRL
0x01	Function Setting
0x02	REF_CTRL
0x05	FLT_RECORD

Register Settings

MTP_CTRL (Address=0x00, default=00h)				
Bits	**Default**	**Name**	**R/W**	**Description**
7	0	MTP_R_EN	R/W	MTP read enable 0 disable 1 enable, MTP data can be read by I^2C This bit will auto reset to '0' when MTP read is finished
6	0	MTP_W_EN	R/W	MTP write enable 0 disable 1 enable This bit will auto reset to '0' when MTP write is finished
5	0	MTP EN	R/W	MTP write and read enable 0=MTP read/write disable, MTP block <1μA 1=MTP read/write enable, MTP block consume When programming "Reg 0x00" [5] = 1 to enable MTP, wait at least 100μs to enable MTP read or write bit. 260μA~360μA when no R/W request from MTP
4:0	000	Reserved	R/W	-

FUNCTION_SETTING (Address=0x01, default=3Ah)				
Bits	**Default**	**Name**	**R/W**	**Description**
7	0	FB_RATIO	R/W	Feedback ratio 0 VOUT=VFB 1 VOUT=1.5*VFB This bit is forbidden changing when "Reg 0x01" [6]=1.
6	0	ENABLE	R/W	Enable control 0 Disable 1 Enable
5	1	DISCHARGE	R/W	Discharge control 0 Disable discharge 1 Auto discharge
4:3	11	FRE_CTRL	R/W	Switching frequency setting 00=5MHz 01=2.5MHz 10=1.7MHz 11=1.7MHz
2	0	Reserved	R/W	
1	1	DVS_SR	R/W	DVS slew rate select When 0x01 bit[7]=0, VOUT=VFB 0=10mV/μs 1=2.5mV/μs When 0x01 bit[7]=1, VOUT=1.5*VFB 0=15mV/μs 1=3.75mV/μs
0	0	VCC_CTRL	R/W	VCC voltage control 0=3.3V 1=3.0V

VO_CTRL (Address=0x02, default=1Eh)				
Bits	**Default**	**Name**	**R/W**	**Description**
7	0	-	R/W	
6:0	0011110	VO_CTRL	R/W	When “Reg0x01”[7]=0, Feedback Reference Voltage range is 0.34V~1.272V, LSB = 4mV VO_CTRL = 340mV + DAC_DC_CTRL×4mV Ex: REF =0.46V = 340mV + 30×4mV

FLT_RECORD (Address=0x05, default=00h)				
Bits	**Default**	**Name**	**R/W**	**Description**
7	0	FLT_VO_SCP	R	Output Short Current (SCP) 0=No fault 1=Fault
6	0	Reserved	R	
5	0	FLT_TEMP_SD	R	Over temperature shutdown (155℃) 0=No fault 1=Fault, greater than threshold
4	0	FLT_TEMP_DIE	R	Thermal warning (110℃) 0= No fault 1=Fault, greater than threshold
3	0	FLT_VO_UVP	R	Output Under Voltage (UVP) 0= No fault 1=Fault
2	0	FLT_VIN_OVP	R	Input Over Voltage (OVP) 0=No fault 1=Fault
1	0	Reserved	R	
0	0	FLT_BOOT	R	1=MTP data load fail 0=MTP data load is finished

Output Voltage Setting

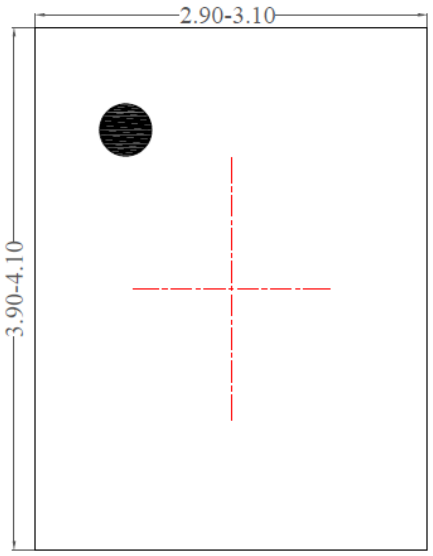
The output voltage can be programmed by writing to the 7-bit register VO_CTRL. The feedback divider can be programmed by FB_RATIO. The corresponding output voltage setting is shown below.

Table 7. Output Voltage Setting

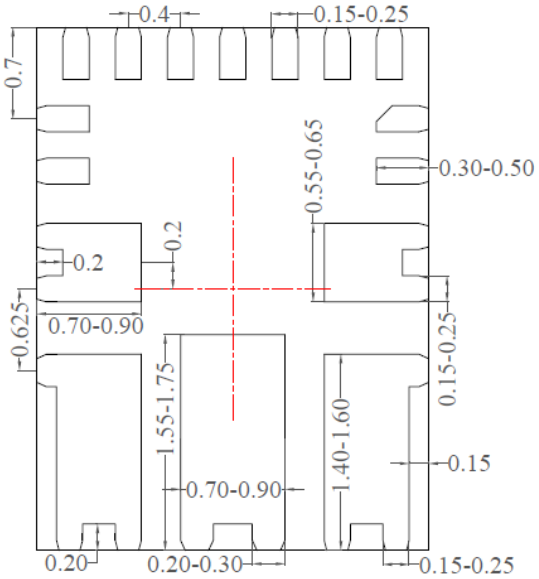
	$V_{OUT}=V_{FB}$	$V_{OUT}=1.5*V_{FB}$		$V_{OUT}=V_{FB}$	$V_{OUT}=1.5*V_{FB}$
DAC code Bit[6-0]	V_{OUT} (V)	V_{OUT} (V)	DAC code Bit[6-0]	V_{OUT} (V)	V_{OUT} (V)
0000000	0.34	0.51	1000000	0.596	0.894
0000001	0.344	0.516	1000001	0.6	0.9
0000010	0.348	0.522	1000010	0.604	0.906
0000011	0.352	0.528	1000011	0.608	0.912
0000100	0.356	0.534	1000100	0.612	0.918
0000101	0.36	0.54	1000101	0.616	0.924
0000110	0.364	0.546	1000110	0.62	0.93
0000111	0.368	0.552	1000111	0.624	0.936
0001000	0.372	0.558	1001000	0.628	0.942
0001001	0.376	0.564	1001001	0.632	0.948
0001010	0.38	0.57	1001010	0.636	0.954
0001011	0.384	0.576	1001011	0.64	0.96
0001100	0.388	0.582	1001100	0.644	0.966
0001101	0.392	0.588	1001101	0.648	0.972
0001110	0.396	0.594	1001110	0.652	0.978
0001111	0.4	0.6	1001111	0.656	0.984
0010000	0.404	0.606	1010000	0.66	0.99
0010001	0.408	0.612	1010001	0.664	0.996
0010010	0.412	0.618	1010010	0.668	1.002
0010011	0.416	0.624	1010011	0.672	1.008
0010100	0.42	0.63	1010100	0.676	1.014
0010101	0.424	0.636	1010101	0.68	1.02
0010110	0.428	0.642	1010110	0.684	1.026
0010111	0.432	0.648	1010111	0.688	1.032
0011000	0.436	0.654	1011000	0.692	1.038
0011001	0.44	0.66	1011001	0.696	1.044
0011010	0.444	0.666	1011010	0.7	1.05
0011011	0.448	0.672	1011011	0.704	1.056
0011100	0.452	0.678	1011100	0.708	1.062
0011101	0.456	0.684	1011101	0.712	1.068
0011110	0.46(Default)	0.69	1011110	0.716	1.074
0011111	0.464	0.696	1011111	0.72	1.08
0100000	0.468	0.702	1100000	0.724	1.086
0100001	0.472	0.708	1100001	0.728	1.092
0100010	0.476	0.714	1100010	0.732	1.098
0100011	0.48	0.72	1100011	0.736	1.104
0100100	0.484	0.726	1100100	0.74	1.11
0100101	0.488	0.732	1100101	0.744	1.116

0100110	0.492	0.738	1100110	0.748	1.122
0100111	0.496	0.744	1100111	0.752	1.128
0101000	0.5	0.75	1101000	0.756	1.134
0101001	0.504	0.756	1101001	0.76	1.14
0101010	0.508	0.762	1101010	0.764	1.146
0101011	0.512	0.768	1101011	0.768	1.152
0101100	0.516	0.774	1101100	0.772	1.158
0101101	0.52	0.78	1101101	0.776	1.164
0101110	0.524	0.786	1101110	0.78	1.17
0101111	0.528	0.792	1101111	0.784	1.176
0110000	0.532	0.798	1110000	0.788	1.182
0110001	0.536	0.804	1110001	0.792	1.188
0110010	0.54	0.81	1110010	0.796	1.194
0110011	0.544	0.816	1110011	0.8	1.2
0110100	0.548	0.822	1110100	0.804	1.206
0110101	0.552	0.828	1110101	0.808	1.212
0110110	0.556	0.834	1110110	0.812	1.218
0110111	0.56	0.84	1110111	0.816	1.224
0111000	0.564	0.846	1111000	0.82	1.23
0111001	0.568	0.852	1111001	0.824	1.236
0111010	0.572	0.858	1111010	0.828	1.242
0111011	0.576	0.864	1111011	0.832	1.248
0111100	0.58	0.87	1111100	0.836	1.254
0111101	0.584	0.876	1111101	0.84	1.26
0111110	0.588	0.882	1111110	0.844	1.266
0111111	0.592	0.888	1111111	0.848	1.272

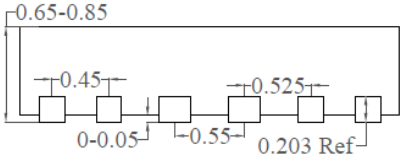
QFN3×4-16 Package Outline Drawing



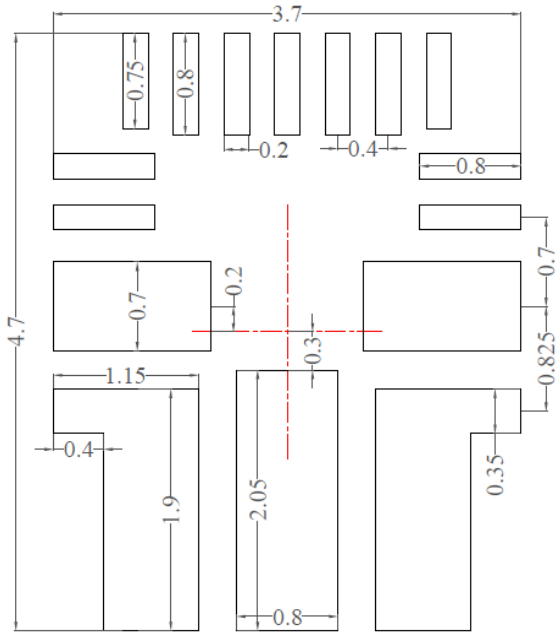
Top View



Bottom View



Side View



Recommended PCB layout
(Reference Only)

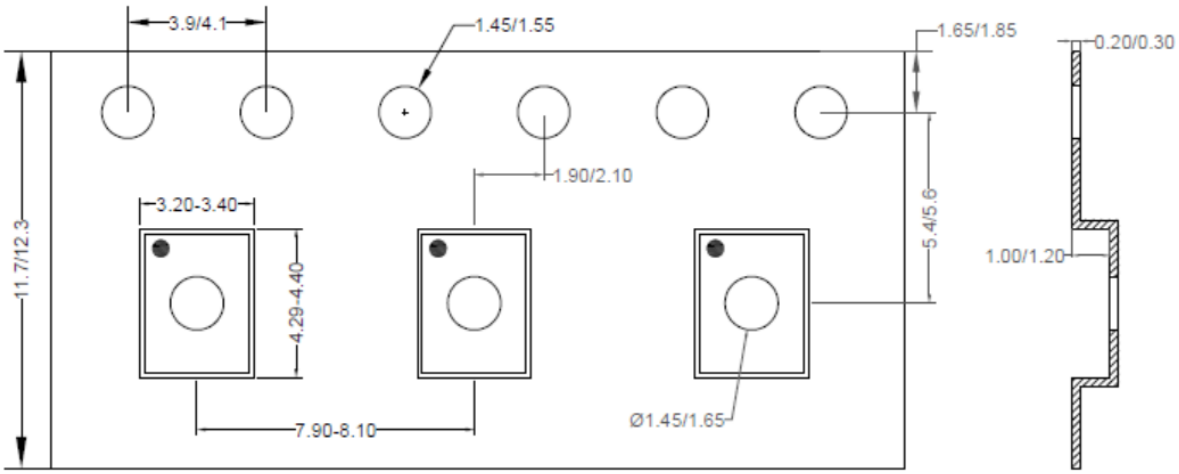
Notes:

1. All dimensions in millimeter and exclude mold flash & metal burr.
2. Center of PCB refers the chip body Center.

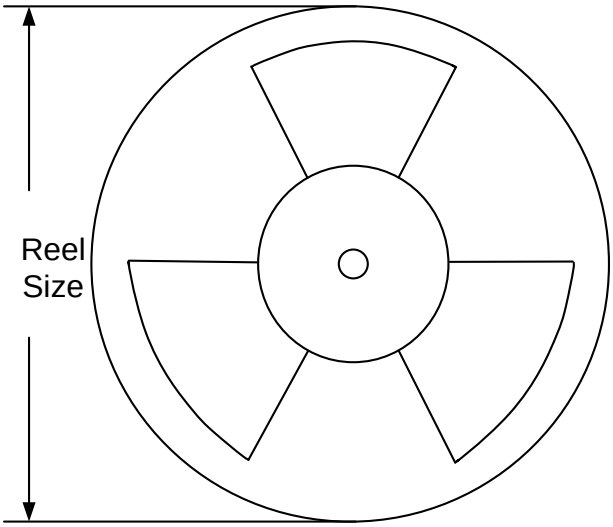
Taping and Reel Specification

Tape Dimensions and Pin 1 Orientation

QFN3×4



Reel Dimensions



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
QFN3x4	12	8	13"	400	400	5000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
Mar.10, 2026	Revision 1.0	Initial release.	-

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