SQ38576B

PWM/PFM Mode SSR Flyback Switcher

General Description

The SQ38576B is a secondary side regulation (SSR) flyback switcher featuring pulse width modulation and pulse frequency modulation (PWM/PFM) operation. It integrates a 1000V power MOSFET within a DIP7 package. Integrated high voltage (HV) startup minimizes no-load loss. The pseudo fixed frequency control strategy avoids sub-harmonic oscillation problems under continuous conduction mode (CCM). For high average efficiency, the SQ38576B will enter frequency fold back mode when load decreases. It will enter burst mode under light load conditions. It features switching frequency modulation to reduce electromagnetic interference (EMI) noise, and soft-start to reduce current and voltage stress on the power device during V_{IN} start up.

The SQ38576B provides reliable protections for overload (OLP), VCC overvoltage (OVP), and over temperature (OTP).

The SQ38576B is available in a compact DIP7 package.

Features

- Secondary Side Regulation
- Integrated 1000V Power MOSFET
- HV Startup
- 60kHz Rated Switching Frequency
- Pseudo Fixed Frequency Control to Eliminate Slope Compensation for CCM (Duty Cycle > 50%)
- Frequency Fold Back Control for High Average Efficiency
- Burst Mode Control for High Light-Load Efficiency
- 25kHz Minimum Switching Frequency to Eliminate Audible Noise
- Frequency Modulation to Reduce EMI Noise
- Internal Soft-Start Process
- OLP, VCC OVP, OTP Protections
- Compact DIP7 Package

Applications

- Smart Power Meter
- Home Appliances
- AC/DC Power Supply

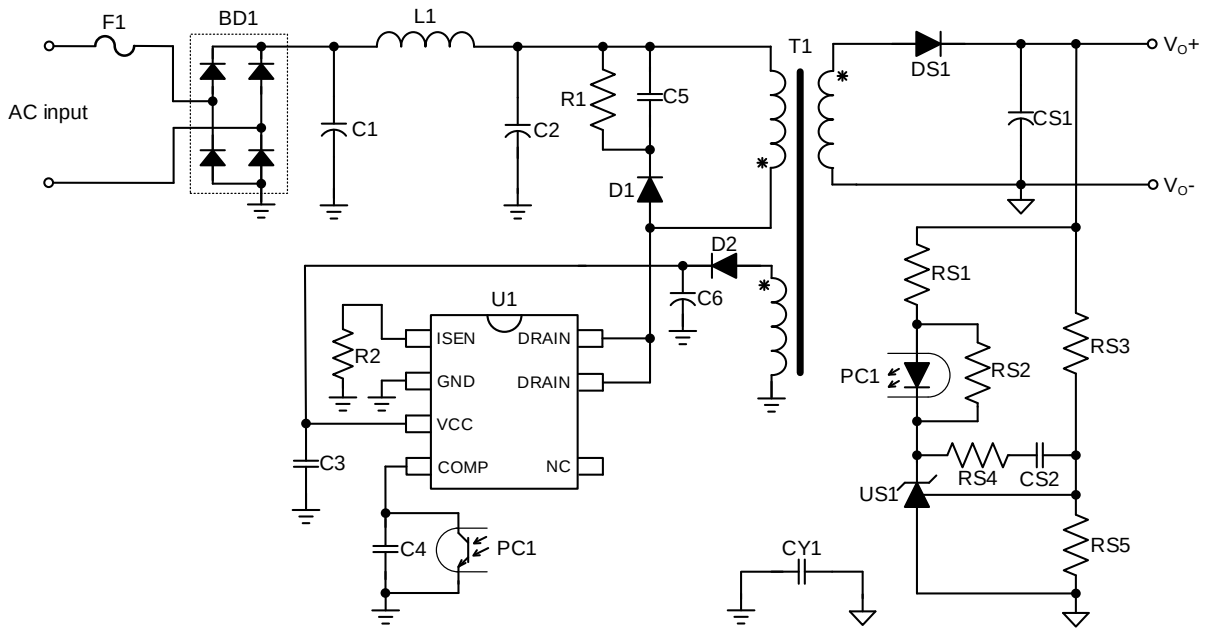


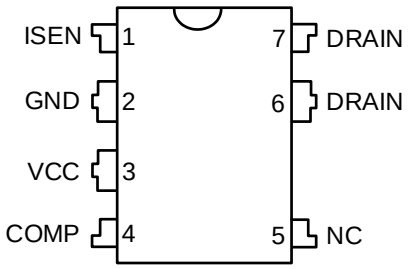
Figure 1. Typical Application Circuit

Ordering Information

Ordering Part Number	Package Type	Top Mark
SQ38576BFIB	DIP7 RoHS-Compliant and Halogen-Free	AARY***xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	ISEN	Primary current sense pin
2	GND	Ground pin
3	VCC	IC supply pin
4	COMP	Output feedback pin. Connect directly to an opto-coupler
5	NC	Not connected
6,7	DRAIN	DRAIN terminal of internal power MOSFET, HV startup

Block Diagram

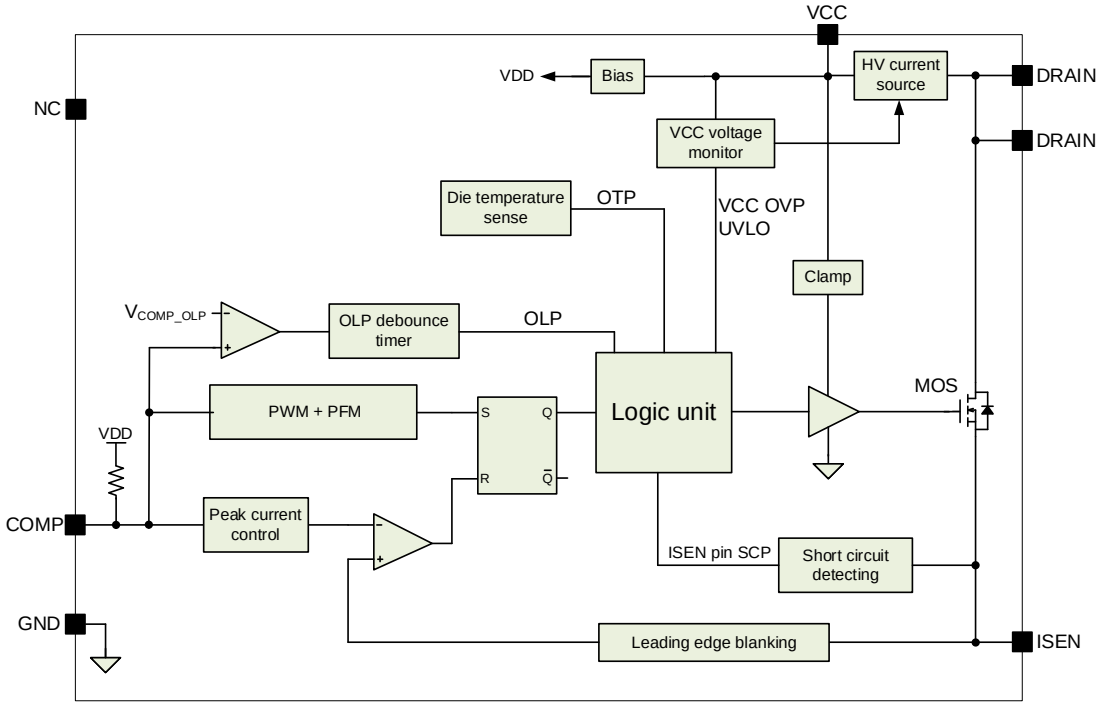


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
DRAIN	-0.3	1000	V
VCC	-0.3	29.5	
ISEN	-0.3	3.6	
COMP	-0.3	3.6	
Junction Temperature, Operating	-45	150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature	-60	150	

Thermal Information

Parameter (Note 2)	Min	Max	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance		110	°C/W
θ_{JC} Junction-to-Case Thermal Resistance		30	
P_D Power Dissipation T_A = 25°C		1.1	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VCC	10	26	V
Junction Temperature	-40	125	°C
Ambient Temperature	-40	105	

Electrical Characteristics

(V_{VCC} = 12V, T_j = -40°C~125°C unless otherwise specified (Note 4))

Parameter		Symbol	Test conditions	Min	Typ	Max	Unit
DRAIN	BV of Power MOS	V_{DS_BV}	V_{COMP} = 0V, I_{DRAIN} = 250μA	1000			V
	On Resistance of Power MOS	R_{DSON}	I_{DRAIN} = 50mA		8	10.5	Ω
	Leakage Current	I_{DRAIN_LK}	V_{DRAIN} = 1000V_{DC}, V_{COMP} = 0V	21	37	53	μA
	HV Current Source	I_{HV}	V_{DRAIN} = 100V_{DC}, V_{VCC} = 5V	0.7	1.2	1.7	mA
VCC	Startup Current	I_{CC_ST}	V_{VCC} = V_{VCC_ON}-0.5V		3	5	μA
	Turn-On Threshold	V_{VCC_ON}	V_{VCC} rising up	13.6	14.6	15.6	V
	Stop Switching Threshold	V_{VCC_MIN}	V_{VCC} falling down	8.2	8.8	9.4	V
	Turn-Off Threshold	V_{VCC_OFF}	V_{VCC} falling down	6.9	7.5	8.1	V
	OVP Threshold	V_{VCC_OVP}	V_{VCC} rising up	27	28	29	V
	Current Sink to Clamp VCC	I_{VCC_SINK}	V_{VCC} = V_{VCC_OVP}	4	5.7	7.5	mA
	Operating Current	I_{VCC_OPRT}	V_{COMP} = 1.4V (Note 5)		1.6		mA
	Quiescent Current	I_{VCC_Q}	V_{COMP} = 0V	340	450	560	μA
	Discharge Current after Protections are Triggered	I_{VCC_FAULT}		85	115	145	μA
ISEN	Maximum Peak Current Limit	V_{ISEN_MAX}		0.44	0.49	0.54	V
	Minimum Peak Current Limit	V_{ISEN_MIN}	(Note 5)		180		mV
	Leading Edge Blanking Time	T_{ISEN_LEB}	(Note 5)		400		ns
	Blanking Time for Pin Short Detection	$T_{ISENSCP\_BLK}$	(Note 5)		3		μs
	Pin Short Threshold	V_{ISEN_SCP}	(Note 5)		50		mV
COMP	Internal Pull up Voltage	V_{COMP_HIGH}		2.2	2.5	2.7	V
	Internal Pull up Resistor	R_{COMP}		17	21	25	kΩ
	PFM Start Threshold	$V_{COMP\_PFM\_STT}$	V_{COMP} falling down (Note 5)		1.2		V
	PFM Stop Threshold	$V_{COMP\_PFM\_STP}$	V_{COMP} falling down (Note 5)		0.9		V
	Threshold to Enter Sleep Mode	V_{COMP_ENSLP}	V_{COMP} falling down (Note 5)		410		mV
	Threshold to Exit Sleep Mode	V_{COMP_EXSLP}	V_{COMP} rising up (Note 5)		460		mV
	OLP Threshold	V_{COMP_OLP}	V_{COMP} rising up (Note 5)		2		V
	OLP Debounce Time	T_{OLP_DBT}		50	70	90	ms
Switching Frequency	Rated Switching Frequency	F_{SW_RATE}	V_{COMP} = 1.4V	55	60	65	kHz
	Maximum On-Time	T_{ON_MAX}		9.5	14	19	μs
	Minimum Switching Frequency	F_{SW_MIN}	V_{COMP} = 0.6V	18	25	33	kHz
Switching Frequency	Frequency Modulation Amplitude	$F_{SW\_MOD\_AMP}$	(Note 5)		±7		%
	Frequency Modulation Period	T_{FSW_MOD}	(Note 5)		4		ms
Soft-Start Process	Soft-Start Time	T_{SS}	(Note 5)		8		ms

Internal OTP	Thermal Shutdown Threshold	T_{OTP}	(Note 5)		150		°C
	Hysteresis to Resume Operation	T_{HYS}	(Note 5)		20		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Chip mounted on low effective single layer PCB.

Note 3: The device is not guaranteed to function outside its operating conditions.

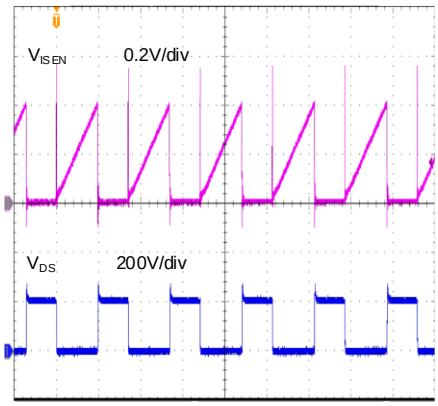
Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \approx T_J = 25°C$. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

Typical Performance Characteristics

Steady

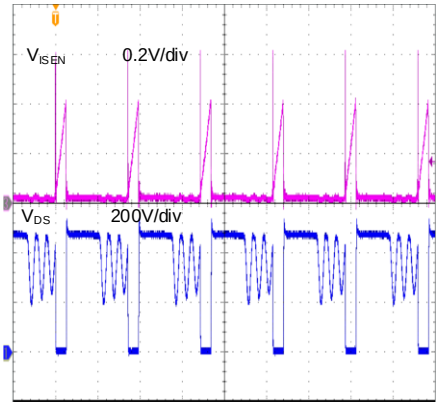
(V_{IN}=90V, V_O=12V, I_O=0.9A)



Time (10µs/div)

Steady

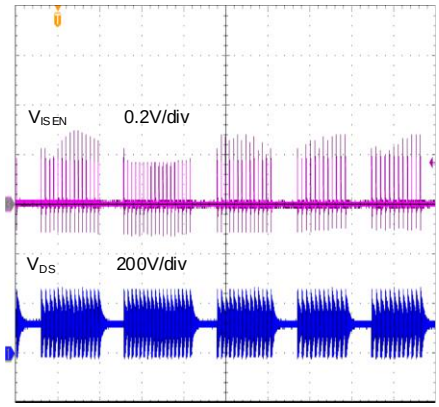
(V_{IN}=264V, V_O=12V, I_O=0.9A)



Time (10µs/div)

Steady

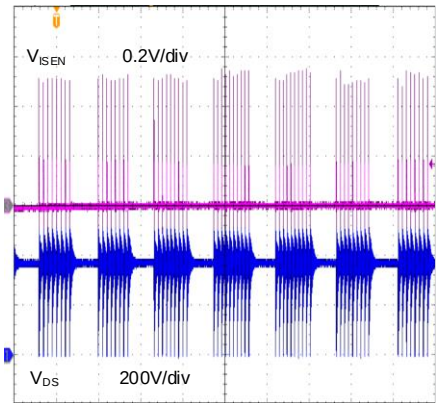
(V_{IN}=90V, V_O=12V, I_O=50mA)



Time (400µs/div)

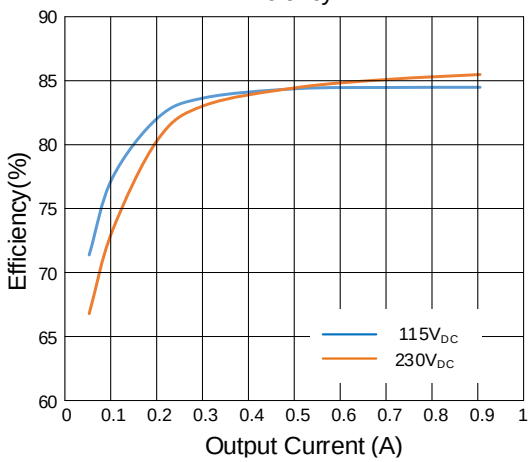
Steady

(V_{IN}=264V, V_O=12V, I_O=50mA)



Time (400µs/div)

Efficiency



Functional Description

High Voltage Startup

The SQ38576B integrates a high voltage startup circuit internally connected to the DRAIN pin. A current source I_{HV} is used to charge the VCC pin capacitor. When VCC pin voltage is charged to the V_{VCC_ON} threshold, the current source will be turned off.

Pseudo Fixed Frequency Control

The SQ38576B uses a Silergy proprietary pseudo fixed frequency control to avoid sub-harmonic oscillation when the converter operates under continuous conduction mode (CCM) and at a duty cycle of greater than 50%. Sub-harmonic oscillation is an inherent issue for peak current control. Traditionally, slope compensation is used to avoid this issue. The SQ38576B does not require slope compensation to prevent sub-harmonic oscillation, thus simplifying the design.

Frequency Fold Back Control

The SQ38576B uses frequency foldback control to improve medium and light load efficiency. As the load is reduced, the COMP pin voltage is also reduced. When COMP pin voltage drops below 1.2V, the device begins to decrease its switching frequency. A minimum switching frequency of 25kHz is reached when COMP pin voltage drops to 0.9V. The minimum switching frequency is maintained to 25kHz for minimized audible noise. The frequency foldback curve is shown in Figure 3.

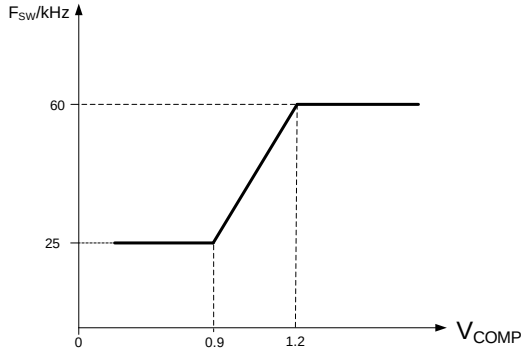


Figure 3. Switching Frequency Control Curve

Burst Mode

The SQ38576B uses burst mode control under very light load or no-load conditions. Under very low load when the COMP pin voltage drops below V_{COMP_ENSLP} (0.41V typ.), the device enters sleep mode, where switching stops and most parts of internal control circuitry are shut down to save energy. As there is no switching, the output voltage will gradually drop. In this state, COMP pin voltage increases until reaching the threshold V_{COMP_EXSLP} (0.46V typ.), when the device wakes up and resumes normal operation. This control architecture helps maintain high efficiency during light load operation. During burst mode, a slightly larger output voltage ripple is expected.

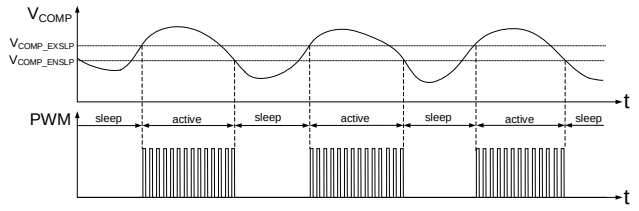


Figure 4. Burst Operating Mode Timing

Internal Soft Start Process

The SQ38576B integrates a soft-start process to achieve monotonic output voltage rise, and to keep the peak current of the power MOSFET within the safe operating area (SOA). The device gradually increases COMP pin voltage while the peak current and switching frequency gradually increase.

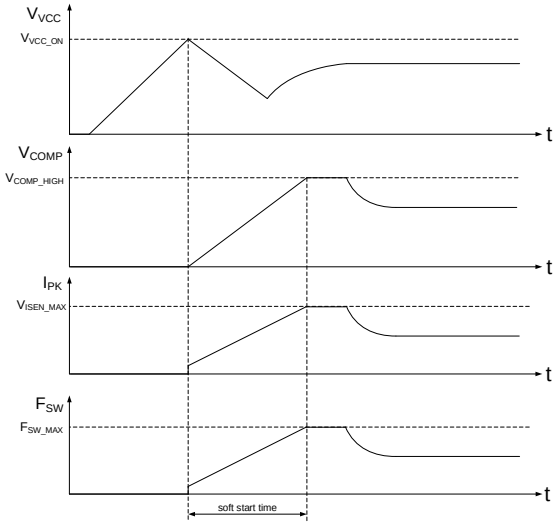


Figure 5. Soft-Start Process Timing

VCC OVP

Under abnormal conditions, such as opto-coupler open circuit or failure, the output voltage will increase along with VCC (VCC is supplied by the auxiliary winding). To avoid the device damage caused by a VCC pin overvoltage condition, switching stops as soon as VCC voltage exceeds the OVP threshold V_{VCC_OVP} and the device enters auto-recovery mode. Before V_{VCC} reaches threshold V_{VCC_OVP}, a current sink I_{VCC_SINK} (5.7mA typ.) on the VCC pin will try to clamp VCC pin voltage. As soon as the OVP condition is detected, a timer is enabled. When the auto-recovery timer elapses, the device will attempt to resume normal operation.

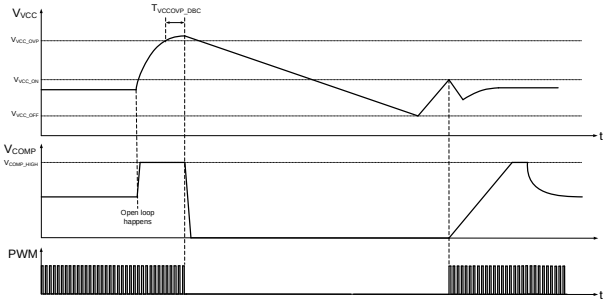


Figure 6. VCC OVP Timing

OLP

During overload conditions, the COMP pin voltage will be pulled up to high level, and peak current and switching frequency will reach maximum value. When the COMP pin voltage rises above the OLP threshold V_{COMP_OLP}, a timer is enabled. If COMP pin voltage is continuously higher than the OLP threshold until the timer elapses, OLP is triggered, the device stops switching and enters auto-recovery mode by initiating a soft-start sequence. The device stays in auto-recovery mode until the condition is resolved.

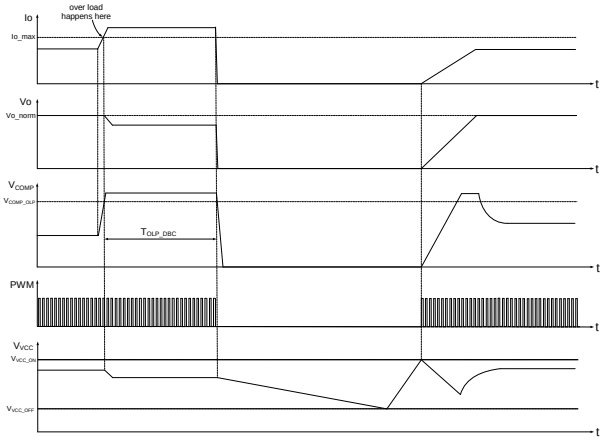


Figure 7. OLP Timing

Output SCP

When an output short-circuit occurs, output voltage drops to nearly zero and auxiliary winding voltage is also nearly zero, so auxiliary winding supply for the VCC pin cannot be maintained. VCC pin voltage will begin to drop. When VCC drops below threshold V_{VCC_MIN}, the SQ38576B will stop switching, and the VCC pin voltage will further drop from V_{VCC_MIN} to V_{VCC_OFF} with a small pulldown current I_{VCC_FAULT} (115uA typ.). This process slows the auto-recovery speed, and the output short-circuit power loss is minimized.

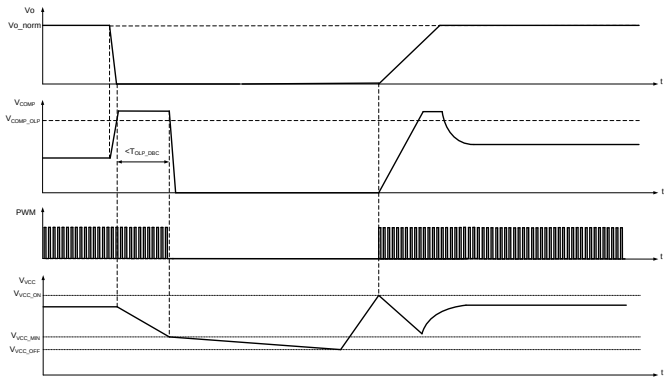


Figure 8. Output SCP Timing

ISEN Pin Short-Circuit Protection

The SQ38576B will check whether the ISEN pin is shorted to GND during the first switching cycle during VIN startup. When the primary side power MOS is turned on, a blanking time $T_{ISENSCP\_BLK}$ (3μs typ.) is used. After this blanking time elapses, the device will compare ISEN pin voltage to internal threshold V_{ISEN_SCP} (50mV typ.). If ISEN pin voltage is lower than this threshold, it triggers the ISEN pin shorted to GND fault, the device will stop switching and enter auto-recovery mode.

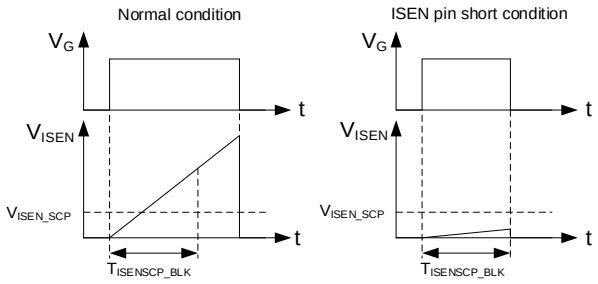


Figure 9. ISEN Pin Short Detection Timing

Internal OTP

The SQ38576B monitors die temperature under normal operating mode. Once die temperature rises above the internal OTP threshold, the device will stop switching and enter auto-recovery mode. When the die temperature drops below threshold T_{OTP} - T_{HYS}, the device will resume normal operation.

Power Supply Design Guide

Bus Capacitor Calculation

Generally, bulk capacitor C_{BUS} is selected according to the following guidelines:

- 1–2μF per watt of input power
- $C_{BUS\_MIN} = (1.0 \cdot P_{IN})uF$
- $C_{BUS\_MAX} = (2.0 \cdot P_{IN})uF$

To be more accurate, the bus capacitor can be selected according to predefined voltage ripple $\triangle V_{BUS}$ on the bus capacitor under minimum AC input voltage and full load

conditions, as shown in Figure 10.

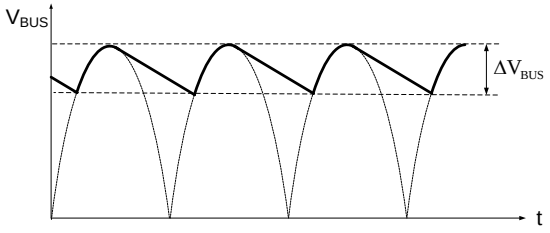


Figure 10. Voltage Ripple on BUS Capacitor

When voltage ripple $\triangle V_{BUS}$ is selected, the bus capacitor can be calculated as follows:

$$C_{BUS} = \frac{P_O}{\eta \cdot \pi \cdot f_{AC} \cdot \Delta V_{BUS}} \cdot \frac{\arcsin(1 - \frac{\Delta V_{BUS}}{\sqrt{2} \cdot V_{IN\_MIN}}) + \frac{\pi}{2}}{2\sqrt{2} \cdot V_{IN\_MIN} - \Delta V_{BUS}}$$

Where P_O is the rated output power, $\triangle V_{BUS}$ is the predefined voltage ripple on the bus capacitor, η is converter efficiency, f_{AC} is the frequency of AC input voltage, and V_{IN_MIN} is the minimum AC input voltage

Transformer Design

Primary/Secondary Turns Ratio: N_{PS}

Maximum allowed N_{PS} is limited by the voltage stress of primary power MOSFET:

$$N_{PS} \le \frac{V_{MOS\_BR} \cdot K_{DR} - \sqrt{2} \cdot V_{IN\_MAX} - \Delta V_{SN}}{V_{O\_MAX}}$$

Where V_{MOS_BR} is the primary MOSFET breakdown voltage, K_{DR} is the MOSFET V_{DS} de-rating factor, ΔV_{SN} is the voltage spike generated when the primary MOS is turned off, and V_{O_MAX} is the maximum output voltage.

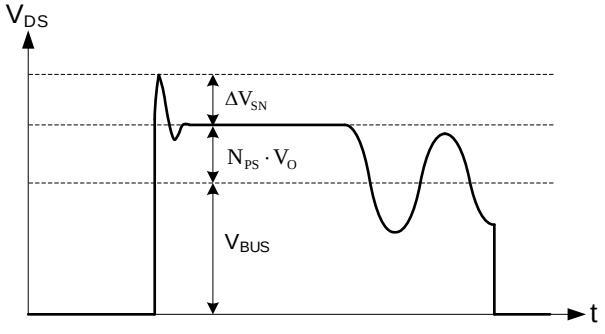


Figure 11. Primary MOS DRAIN Waveform

Primary Inductance: L_M

Primary inductance of the transformer is related to the primary current ripple. Generally, primary side current ripple is defined as shown in Figure 12, and the current ripple factor is defined as follows:

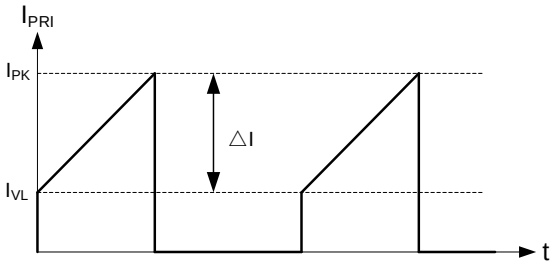


Figure 12. Primary Current Ripple under CCM

$$K_{RP} = \frac{0.5 \cdot \Delta I}{I_{PK} - 0.5 \cdot \Delta I}$$

- K_{RP}<1: CCM
- K_{RP} = 1: BCM

Generally, to optimize transformer size and efficiency for universal input applications under low input and full load conditions, CCM operating is selected. Under high input condition and full load conditions, QR mode is selected.

Based on design experience, under lowest input and full load conditions, it is recommended to choose K_{RP} between 0.3–0.9 for optimized performance. Once K_{RP} is selected, primary inductance of transformer is calculated as follows:

$$L_M = \frac{V_{BUS\_MIN}^{\ 2} \cdot D_{MAX}^{\ 2} \cdot \eta}{2 \cdot P_O \cdot f_{SW} \cdot K_{RP}}$$

Where f_{SW} is the rated CCM switching frequency, P_O is the rated output power, η is converter efficiency, D_{MAX} is the maximum duty cycle at V_{BUS_MIN} and rated output power, and D_{MAX} is calculated as follows:

$$D_{MAX} = \frac{N_{PS} \cdot V_O}{V_{BUS\_MIN} + N_{PS} \cdot V_O}$$

Turns of Primary Winding

(a) Select the magnetic core type and identify the effective cross-sectional area A_E

(b) Preset the maximum magnetic flux density B_{MAX} at minimum bus voltage and full load condition:

B_{MAX}=0.2T~0.3T

(c) Calculate maximum primary peak current I_{PK} at rated output power:

$$I_{PK} = \frac{V_O \cdot I_O \cdot (1 + K_{RP})}{V_{BUS\_MIN} \cdot D_{MAX} \cdot \eta}$$

(d) Calculate primary turns N_P

$$N_P = \frac{L_M \cdot I_{PK}}{B_{MAX} \cdot A_E}$$

Where A_E is the effective cross-sectional area of the core

Turns of Secondary Winding: N_S

$$N_S = \frac{N_P}{N_{PS}}$$

Turns of Auxiliary Winding: N_A

VCC pin voltage V_{CC_AUX} should be predefined before calculating auxiliary turns. Generally, VCC pin voltage should be guaranteed to exceed 12V under minimum output voltage, and auxiliary turns are calculated as follows:

$$N_A = \frac{V_{CC\_AUX} \cdot N_S}{V_O}$$

The worst case of VCC pin voltage is under minimum output voltage and null load condition. Auxiliary winding turns should be fine-tuned according to actual VCC pin voltage under such a case.

Peak Current Sense Resistor Calculation

Under minimum AC input voltage conditions, maximum output current (OCP point) is reached when bus voltage is at maximum value and primary peak current reaches the ISEN pin maximum set point. Under the OCP point, primary peak current is calculated as follows:

$$D_{OCP} = \frac{N_{PS} \cdot V_O}{\sqrt{2} \cdot V_{IN\_MIN} + N_{PS} \cdot V_O}$$

$$I_{PK\_MAX} = \frac{P_O \cdot K_{OCP}}{\sqrt{2} \cdot V_{IN\_MIN} \cdot D_{OCP} \cdot \eta} + \frac{\sqrt{2} \cdot V_{IN\_MIN} \cdot D_{OCP}}{2 \cdot L_M \cdot f_{SW}}$$

Where K_{OCP} is the OCP proportion; K_{OCP} is generally set to 120%–150%.

$$K_{OCP} = \frac{I_{O\_OCP}}{I_O}$$

After the maximum primary peak current has been calculated, the peak current sense resistor R_{ISEN} can be easily derived as follows:

$$R_{ISEN} = \frac{V_{ISEN\_MAX}}{I_{PK\_MAX}}$$

Where V_{ISEN_MAX} is the ISEN pin current sense limit voltage (typical = 0.49V).

Note: The current sense resistor must be fined tuned according to the converter's required actual OCP point. If the OCP point is higher than the target level, R_{ISEN} should be selected slightly larger. If the OCP point is lower than the target level, R_{ISEN} should be selected slightly smaller.

Secondary Rectifier Diode Selection

The secondary rectifier diode reverse voltage will reach the maximum level under the conditions of maximum bus voltage and maximum output voltage. The maximum diode reverse voltage is calculated follows:

$$V_{DR\_MAX} = \frac{\sqrt{2} \cdot V_{IN\_MAX}}{N_{PS}} + V_{O\_MAX} + V_{SPIKE}$$

Where V_{IN_MAX} is the maximum AC input voltage, N_{PS} is the primary/secondary turns ratio of the transformer, V_{O_MAX} is the maximum output voltage, and V_{SPIKE} is the voltage spike generated when the primary MOS is turned on.

The maximum peak current of the SR MOS is calculated as follows:

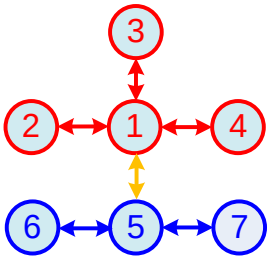
$$I_{D\_MAX} = I_{PK\_MAX} \cdot N_{PS}$$

Where I_{PK_MAX} is the maximum primary peak current at V_{BUS_MIN} and the OCP point.

Recommended PCB Layout

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

- To achieve better EMI performance and reduce line frequency ripple, connect the output of the bridge rectifier first to the bus line capacitor, then to the switching circuit.
- Keep the circuit loop of all switching circuits small: primary power loop, secondary loop and auxiliary power loop.
- Connect the bias supply trace to the bias supply capacitor first, and then to the GND pin. Place the bias supply capacitor as close as possible to the IC.
- Keep the switching loop formed by the source pin, current sense resistor, and GND pin as small as possible.
- Connect the primary ground as follows:



  - Ground ①: Ground of bus capacitor
  - Ground ②: Ground of current sense resistor.
  - Ground ③: Ground node of auxiliary winding
  - Ground ④: Ground of primary side Y capacitor
  - Ground ⑤: Ground pin of SQ38576B
  - Ground ⑥: Ground of VCC pin bypass capacitor C3
  - Ground ⑦: Ground of receiver of opto-coupler

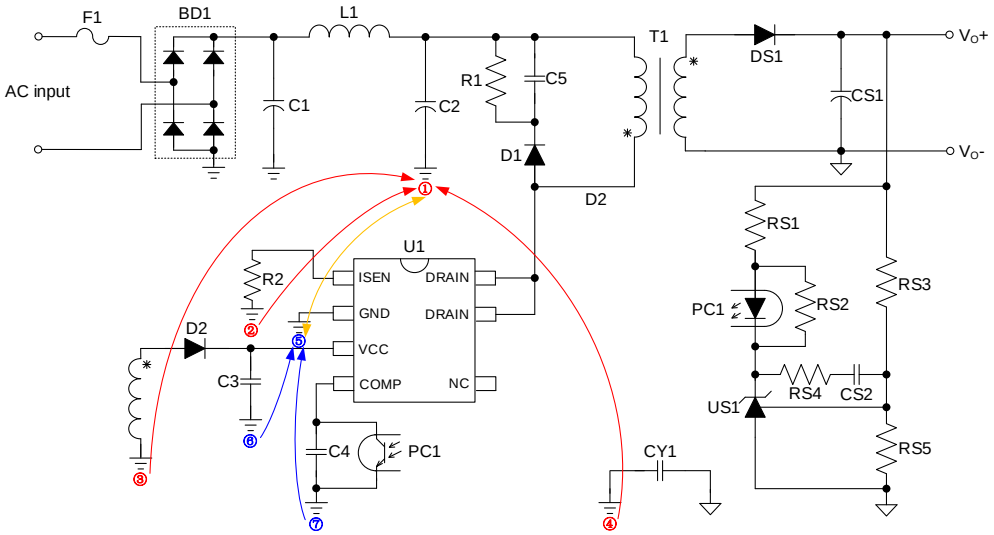


Figure 13. Suggested PCB Layout

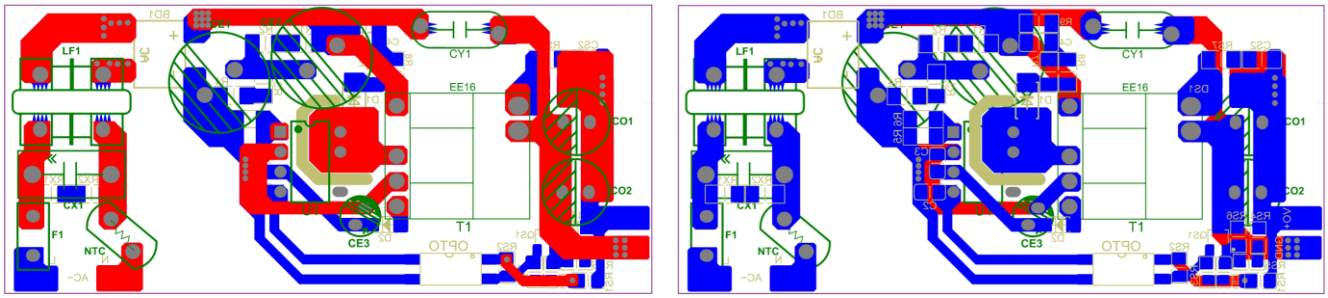


Figure 14. Suggested PCB Layout

Typical Application Schematic

Figure 15 shows a typical application circuit in an 11W auxiliary power supply design.

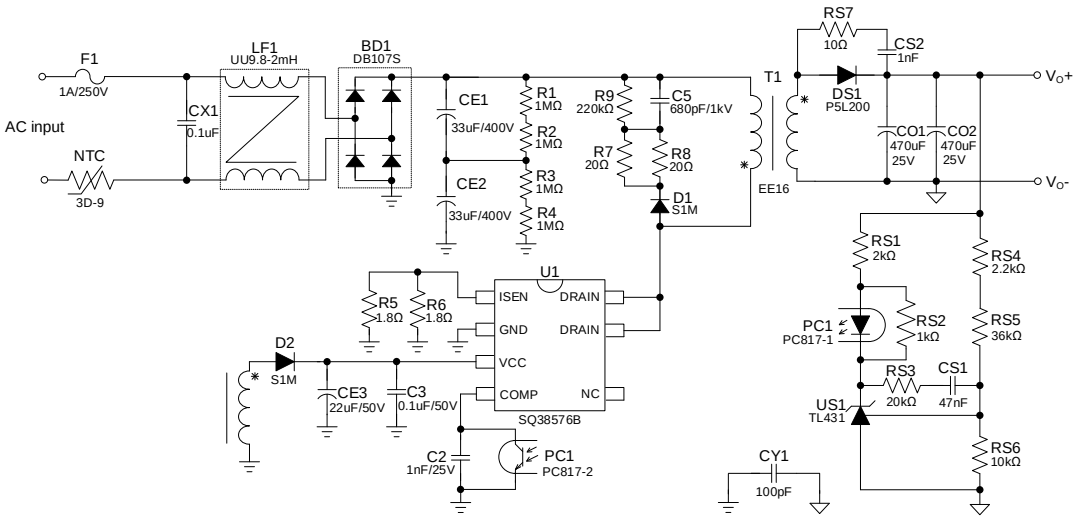


Figure 15. 11W Auxiliary Power Supply Application Circuit

Recommended BOM List

Designator	Description	Part Number	Manufacturer
F1	Fuse, 1A/250V	T1A 250V	jdtfuse
NTC	Thermistor	3D-9	RUILON
CX1	0.1uF/275V, X cap	MP21004K27C3X6LC	SRD
LF1	Common mode choke	UU9.8-2mH	SR
BD1	Full bridge rectifier	DB107S	MDD
CE1, CE2	Electrolytic capacitor, 33μF/400V	EGW2GM330K200T	AiSHi
CE3	Electrolytic capacitor, 22μF/50V	ERE1HM220D11OT	AiSHi
R1,R2,R3,R4	SMD resistor, 1MΩ, 1206	1206W4J0105T5E	UNI-ROYAL
R5,R6	SMD resistor, 1.8Ω, 1206	1206W4F1801T5E	UNI-ROYAL
R7,R8	SMD resistor, 20Ω, 1206	1206W4J0200T5E	UNI-ROYAL
R9	SMD resistor, 220kΩ, 1206	1206W4J0224T5E	UNI-ROYAL
C2	SMD capacitor, 1nF/25V, 0805	0805B102K500NT	FH
C3	SMD capacitor, 0.1uF/50V, 0805	0805B104K500NT	FH
C5	SMD capacitor, 680pF/1000V, 1206	CC1206JKNPOCBN681	YAGEO
D1	Diode, 1A/1000V, SMA	S1M	DIODES
D2	Diode, 1A/1000V, SOD-123F	S1M	DIODES
U1	FLYBACK switcher, DIP7	SQ38576BFIB	Silergy
T1	Transformer	EE16/6.5, L_M = 2mH	/
PC1	Opto-coupler	PC817	Sharp
CY1	Y cap, 100pF/Y1/400V	CY1101KE1IEB45W2A2	Dersonic
RS1	SMD resistor, 2kΩ, 0805	0805W8J0202T5E	UNI-ROYAL
RS2	SMD resistor, 1kΩ, 0805	0805W8J0102T5E	UNI-ROYAL

RS3	SMD resistor, 20kΩ, 0805	0805W8J0203T5E	UNI-ROYAL
RS4	SMD resistor, 2.2kΩ, 0805	0805W8F2201T5E	UNI-ROYAL
RS5	SMD resistor, 36kΩ, 0805	0805W8J0363T5E	UNI-ROYAL
RS6	SMD resistor, 10kΩ, 0805	0805W8F1002T5E	UNI-ROYAL
RS7	SMD resistor, 10Ω, 1206	1206W4J0100T5E	UNI-ROYAL
CS1	SMD capacitor, 47nF/25V, 0805	0805B473K500NT	FH
CS2	SMD capacitor, 1nF/500V, 1206	CC1206KRX7RBBB102	FH
CO1,CO2	Electrolytic capacitor, 470uF/25V	ERZ1EM471G13OT	AiSHi
DS1	Diode	P5L200	PFC
US1	Shunt voltage reference	TL431	HKT

11W Power Supply Design Example

A design example of typical application is shown below step by step.

Input/output specifications

Parameter	Symbol	Value
Input voltage range	V_{IN}	90~380Vac
AC input frequency	f_{AC}	50Hz
Rated output voltage	V_O	12V
Rated output current	I_O	0.9A
OCP proportion	K_{OCP}	130%

Preset parameters

Parameter	Symbol	Value
Break down voltage of power MOS	$V_{MOS,BR}$	1000V
V_{DS} de-rating factor of power MOS	K_{DR}	85%
Voltage spike on power MOS during turn off instant	ΔV_{SN}	150V
Converter efficiency	η	82%
Primary current ripple factor	K_{RP}	0.65
Voltage ripple on BUS capacitor	ΔV_{BUS}	55
Transformer effective cross-sectional area (EE16/6.5)	A_E	25 mm^2
Max flux density of magnetic core at rated output power	B_{MAX}	0.29T
Voltage spike on secondary rectifier diode	V_{SPIKE}	10V

1. BUS Capacitor Selection

Voltage ripple on BUS capacitor is set to: ΔV_{BUS}=55V

$$C_{BUS}=\frac{P_O}{\eta\cdot\pi\cdot f_{AC}\cdot\Delta V_{BUS}}\cdot\frac{\arcsin(1-\frac{\Delta V_{BUS}}{\sqrt{2}\cdot V_{IN\_MIN}})+\frac{\pi}{2}}{2\sqrt{2}\cdot V_{IN\_MIN}-\Delta V_{BUS}}=\frac{10.8}{82\%\times 3.14\times 50\times 55}\cdot\frac{\arcsin(1-\frac{55}{\sqrt{2}\times 90})+\frac{\pi}{2}}{2\sqrt{2}\times 90-55}=16.61uF$$

Select BUS capacitor: $C_{BUS}=16.5uF$

Minimum BUS voltage:

$$V_{BUS\_MIN}=\sqrt{2}\cdot V_{IN\_MIN}-\Delta V_{BUS}=\sqrt{2}\times 90-55=72.3V$$

2. Transformer Design

(a) Calculate primary/secondary turns ratio N_{PS}:

$$N_{PS} \le \frac{V_{MOS\_BR} \cdot K_{DR} - \sqrt{2}V_{IN\_MAX} - \Delta V_{SN}}{V_{O\_MAX}} = \frac{1000 \times 85\% - \sqrt{2} \cdot 380 - 150}{12} = 13.55$$

N_{PS} is selected as $N_{PS} = 10$

(b) Calculate maximum duty cycle D_{MAX} at minimum bus voltage and rated output power condition:

$$D_{MAX} = \frac{N_{PS} \cdot V_O}{V_{BUS\_MIN} + N_{PS} \cdot V_O} = \frac{10 \times 12}{72.3 + 10 \times 12} = 62.4\%$$

(c) Calculate primary inductance L_M:

$$L_M = \frac{V_{BUS\_MIN}^{\ 2} \cdot D_{MAX}^{\ 2} \cdot \eta}{2 \cdot P_O \cdot f_{SW} \cdot K_{RP}} = \frac{72.3^2 \times 62.4\%^2 \times 82\%}{2 \times 10.8 \times 60k \times 0.65} = 1.98mH$$

Select $L_M = 2mH$

(d) Calculate primary peak current at minimum bus voltage and rated output power condition:

$$I_{PK} = \frac{P_O}{V_{BUS\_MIN} \cdot D_{MAX} \cdot \eta} + \frac{V_{BUS\_MIN} \cdot D_{MAX}}{2 \cdot L_M \cdot f_{SW}} = \frac{10.8}{72.3 \times 62.4\% \times 82\%} + \frac{72.3 \times 62.4\%}{2 \times 2m \times 60k} = 0.48A$$

(e) Calculate primary winding turns N_P:

Transformer core effective cross-sectional area: $A_E = 25 \cdot 10^{-6} m^2$

Maximum allowed flux density at rated output power: $B_{MAX} = 0.29T$

$$N_P = \frac{L_M \cdot I_{PK}}{B_{MAX} \cdot A_E} = \frac{2m \times 0.48}{0.29 \times 25 \times 10^{-6}} = 132.4$$

Select primary winding turns N_P = 130

(f) Calculate secondary winding turns N_S:

$$N_S = \frac{N_P}{N_{PS}} = \frac{130}{10} = 13$$

Select secondary turns N_S = 13

(g) Calculate auxiliary winding turns N_A:

VCC supply voltage from auxiliary winding is set to $V_{CC(AUX)}$ = 12V

$$N_A = \frac{V_{CC\_AUX} \cdot N_S}{V_O} = \frac{12 \times 13}{12} = 13$$

Select auxiliary winding turns N_A = 13

Note: Auxiliary winding turns should be fine-tuned according to actual VCC pin voltage under no-load condition

(h) If another transformer core type is selected, then re-calculate using steps e through g.

3. Current Sense Resistor Calculation

(a) Calculate duty cycle under minimum input voltage (minimum bus voltage) D_{OCP}:

$$D_{OCP} = \frac{N_{PS} \cdot V_O}{\sqrt{2} \cdot V_{IN\_MIN} + N_{PS} \cdot V_O} = \frac{10 \times 12}{\sqrt{2} \times 90 + 10 \times 12} = 48.5\%$$

(b) Calculate primary side peak current at OCP point I_{PK_MAX}:

$$I_{PK\_MAX} = \frac{P_O \cdot K_{OCP}}{\sqrt{2} \cdot V_{IN\_MIN} \cdot D_{OCP} \cdot \eta} + \frac{\sqrt{2} \cdot V_{IN\_MIN} \cdot D_{OCP}}{2 \cdot L_M \cdot f_{SW}} = \frac{10.8 \times 130\%}{\sqrt{2} \times 90 \times 48.5\% \times 82\%} + \frac{\sqrt{2} \times 90 \times 48.5\%}{2 \times 2m \times 60k} = 0.535A$$

(c) Calculate current sense resistor R_{ISEN}:

$$R_{ISEN} = \frac{V_{ISEN\_MAX}}{I_{PK\_MAX}} = \frac{0.49}{0.535} = 0.916\Omega$$

Note: ISEN pin current sense resistor R_{ISEN} should be fine-tuned according to the actual OCP point.

4. Secondary Rectifier Diode Selection

(a) Maximum reverse voltage calculation:

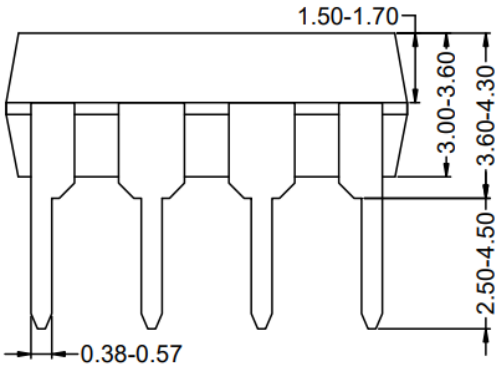
$$V_{BR\_MAX} = \frac{\sqrt{2} \cdot V_{IN\_MAX}}{N_{PS}} + V_O + V_{SPIKE} = \frac{\sqrt{2} \times 380}{10} + 12 + 10 = 75.73V$$

Considering voltage derating, secondary rectifier diode with 100V rating is recommended.

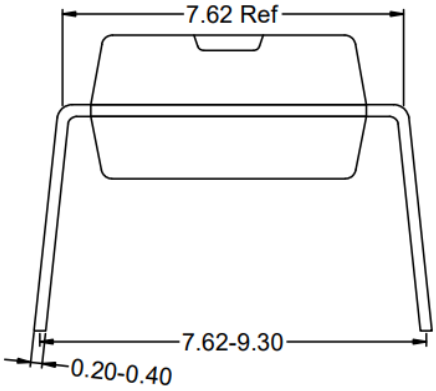
(b) Maximum instantaneous SR MOS current:

$$I_{F\_MAX} = N_{PS} \cdot I_{PK\_MAX} = 10 \times 0.535 = 5.35A$$

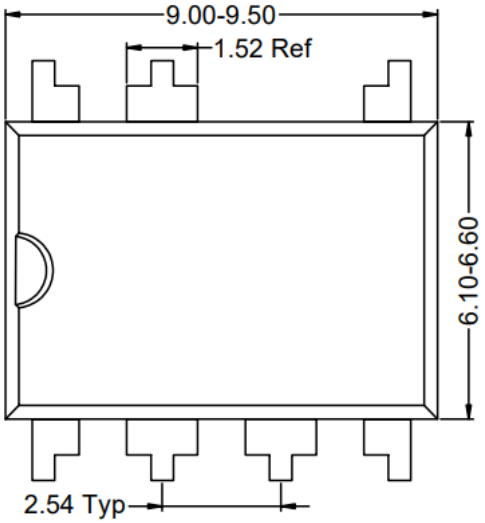
DIP7 Package Outline Drawing



Side view A



Side view B

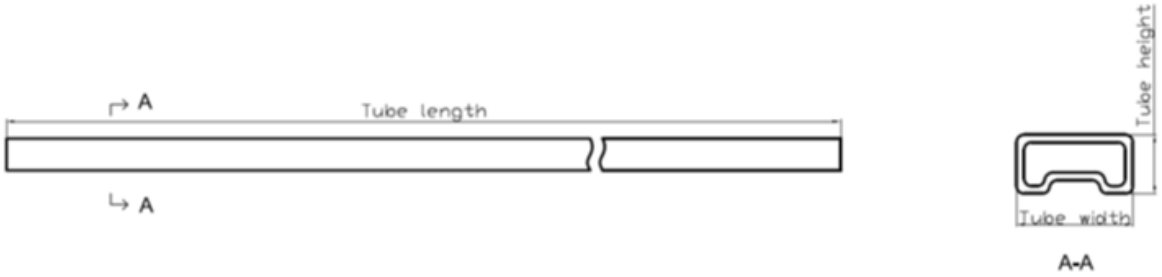


Top view

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

Taping Specification

DIP7 Taping orientation



Package Type	Tube Length (mm)	Tube Width (mm)	Tube Height (mm)	Qty per Tube (pcs)	Qty per Box
DIP7	520+/-10	11.7+/-2	10.7+/-0.5	50	2000

Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
December 29,2025	Revision 1.0	Initial Release

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