SQ58621

Low Power Audio Codec

General Description

The SQ58621 is a low power mono audio codec. It features two analog differential inputs with two programmable gain amplifiers and a mixer for the microphone. The device includes two differential output line drivers and one single-ended output. The SQ58621 is available as a I²S controller(I²S master) or target(I²S slave) device. The controller generates SCLK and LRCLK for the target for data transmission.

The high-resolution sigma-delta audio ADC converts analog signals to digital and transmits them to the host SOC via I²S or TDM serial data formats. The audio DAC converts the I²S or TDM serial data from the host SOC to analog outputs. An integrated analog direct path transmits the microphone input to the outputs with a high drive strength line driver. The SQ58621 is available in a compact QFN4×4-24 package.

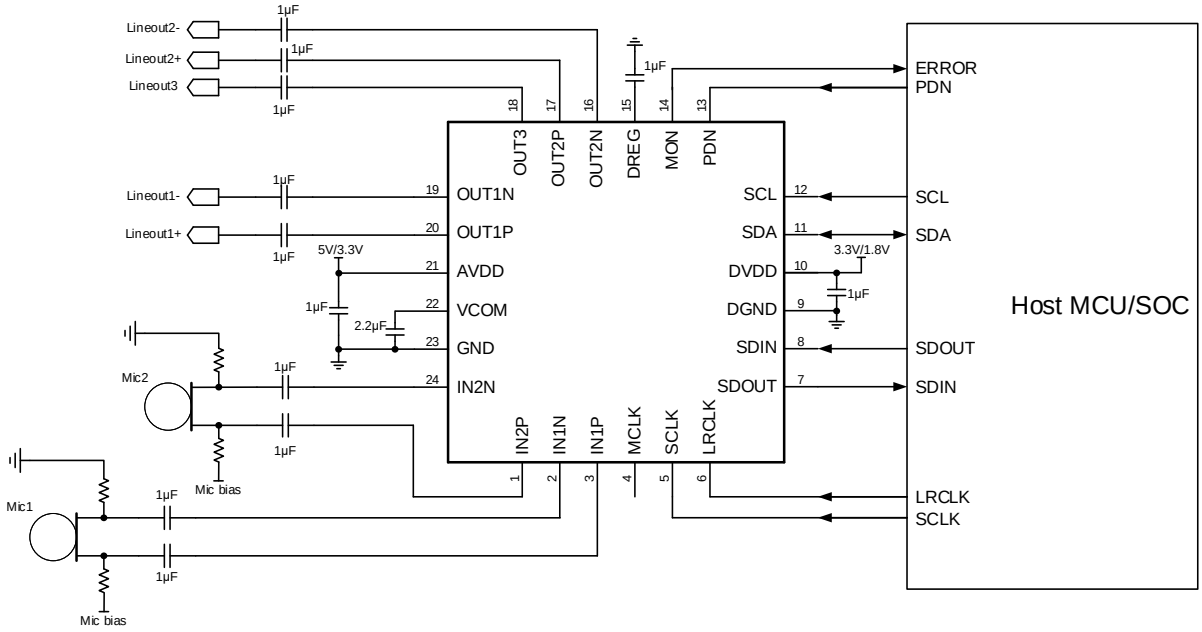
Features

- Power Supplies:
  - 3.3V or 5V Analog Supply
  - 1.8V or 3.3V Digital IO Interface
- Audio DAC:
  - Digital Volume: +12 to -115dB, 0.5dB Per Step, Mute
  - Digital Filters: Sharp/Slow Roll-Off Filter
  - 2 Fully Differential Outputs and 1 Single-Ended Output
  - Differential Voltage Output: 5.8V_{pp} at 3.3V AVDD, 8.7V_{pp} at 5V AVDD
  - 107dB SNR, -83dB THD+N with Fully Differential Output
- Audio ADC:
  - 2 Fully Differential Inputs
  - Input PGA: -18 to +27dB, 3dB Per Step
  - Input Mixer
  - Digital Filters: Narrow Band Voice Filter, Wide Band Voice Filter, Full Band Voice Filter and 2 Optional Bi-Quad Filters
  - Differential Voltage Input: 4.5V_{pp} at 3.3V AVDD, 6.8V_{pp} at 5V AVDD
  - Digital Volume: +24 to -103dB, 0.5dB Per Step, Mute
  - 99dB SNR, -91dB THD+N
- Mic Direct Path Line Driver:
  - Mic Direct Path Boost Gain: 0 to +9dB, 3dB Per Step
  - 2 Fully-Differential Outputs
  - Differential Voltage Output: 5.8V_{pp} at 3.3V AVDD, 8.7V_{pp} at 5V AVDD
  - 108dB SNR, -96dB THD+N with Fully-Differential Output
- Audio Interface:
  - Supports Controller and Target Mode
  - Format: I²S, Left-/Right-Justified, TDM with 4/8/16 Slots
  - Supports Sampling Rates from 8 kHz to 96 kHz
  - Input/output Data Length: 16-bit, 20-bit, 24-bit, 32-bit
  - Slot Width: 16-bit, 24-bit, 32-bit
- I²C Control
- MSL Rating: MSL3
- Package Size: QFN4×4-24

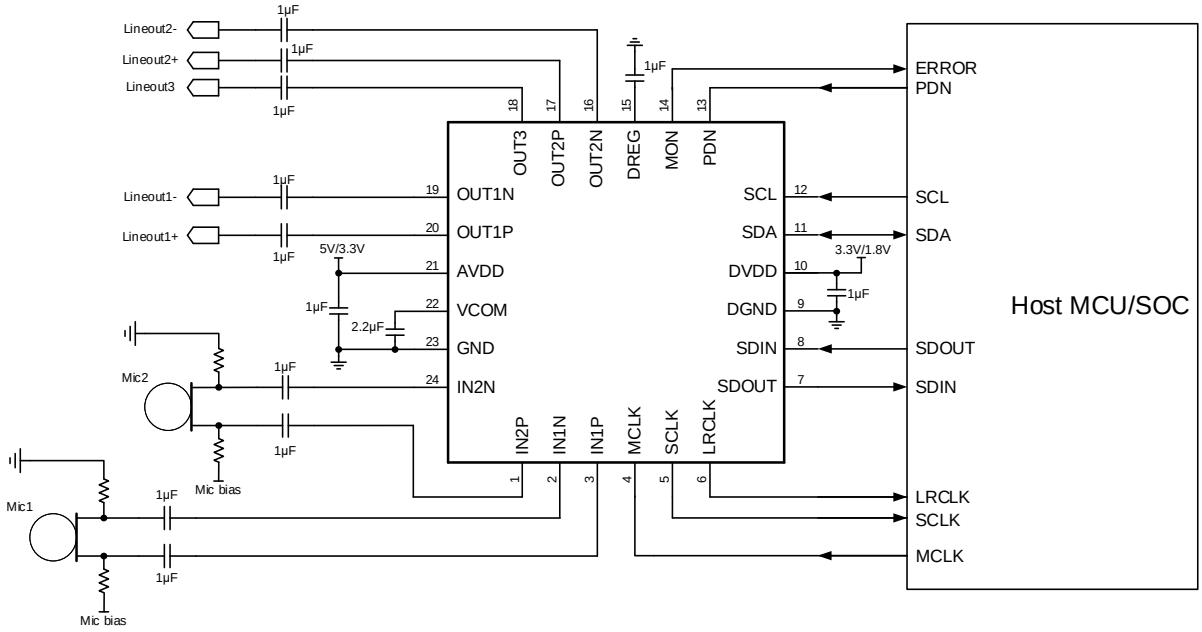
Applications

- IP Network Camera
- Video Conference System

Typical Application



(1) Target Mode



(2) Controller Mode with External Clock

Figure 1. Typical Application Circuit

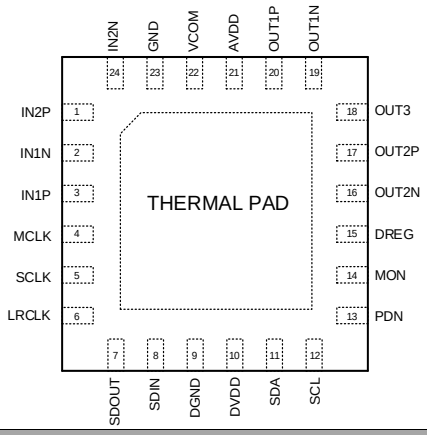
Ordering Information

Ordering Part Number	Package Type	Top Mark
SQ58621QCQ	QFN4×4-24 RoHS Compliant and Halogen Free	***AAOGxyz***

Device code: AAOG

x=year code, y=week code, z= lot number code

Pinout (Top View)

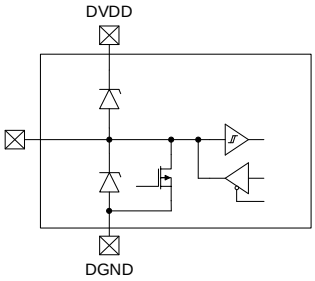
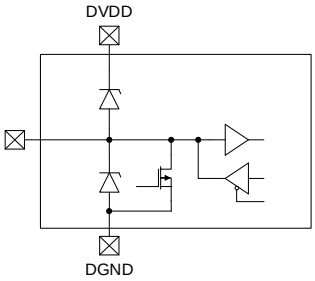
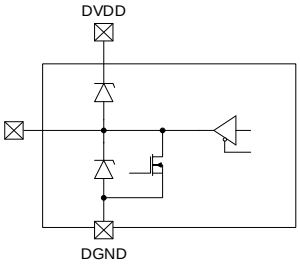
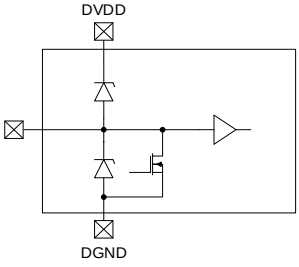
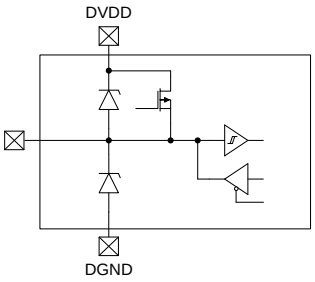


Pin Name	Pin Number	Type (Note 1)	Termination (Note 2)	Description
IN2P	1	AI		Analog input 2 positive.
IN1N	2	AI		Analog input 1 negative.
IN1P	3	AI		Analog input 1 positive.
MCLK	4	DI	Pull down	Master clock input. Only used in controller mode. In controller mode, connect it to an external clock. In target mode, leave it open or connect to GND.
SCLK	5	DIO	Pull down	Audio serial data bus bit clock. In controller mode it is the output bit clock. In target mode it is the input bit clock.
LRCLK	6	DIO	Pull down	Audio serial data bus frame clock. In controller mode it is the output frame clock. In target mode it is the input frame clock.
SDOUT	7	DO	Pull down	Audio serial data output.
SDIN	8	DI	Pull down	Audio serial data input.
DGND	9	P		Digital power ground.
DVDD	10	P		Digital power supply. Connect a 1μF capacitor between DVDD and GND.
SDA	11	DIO	Pull high	I^2C serial clock.
SCL	12	DI	Pull high	I^2C serial data.
PDN	13	DI	Pull down	Shutdown pin, input with active low.
MON	14	DIO	Pull down	Multi-function pin. During startup: Input to select controller or target mode. Pulled up for controller mode and pulled down for target mode. After startup, the mode will be latched. After startup: Can be configured to monitor the pin, including error status and SDOUT. This pin will be high when an error appears.
DREG	15	P		Regulator for the digital core decoupling pin. This pin must not be connected to external load.
OUT2N	16	AO		Channel 2 negative output.
OUT2P	17	AO		Channel 2 positive output.
OUT3	18	AO		Channel 3 output (single-ended).
OUT1N	19	AO		Channel 1 negative output.
OUT1P	20	AO		Channel 1 positive output.
AVDD	21	P		Analog power supply. Connect a 1μF capacitor between AVDD and GND.
VCOM	22	P		Analog output common voltage. Connect a 2.2μF(Note 3) capacitor between AVDD and GND. This pin must not be connected to external load.
AGND	23	P		Analog power ground.

IN2N	24	AI		Analog input 2 negative.

Note 1: Type: A = analog; D = digital; P = power/ground/decoupling; I = input; O = output; IO = inout
Note 2: All pull-highs and pull-downs are weak.
Note 3: The recommended VCOM decoupling capacitance is 2.2μF. Larger capacitance is prefered for high DAC OUT3 PSRR performance.

Digital IO Equivalent Circuits

Pin No.	Pin Name	Equivalent Circuit	IO Type
4 5	MCLK SCLK		Bidirectional IO with pulldown (109kΩ)
6 14	LRCLK MON		Bidirectional IO with pulldown (51kΩ)
7	SDOUT		Output with pulldown (51kΩ)
8	SDIN		Input with pulldown (51kΩ)
11	SDA		Bidirectional IO with pullup (135kΩ)

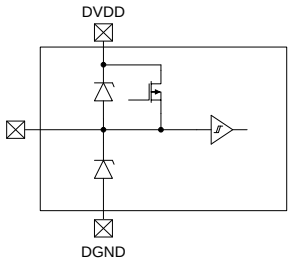
12	SCL		Input with pullup (135kΩ)

Figure 2. Digital IO Equivalent Circuits

Block Diagram

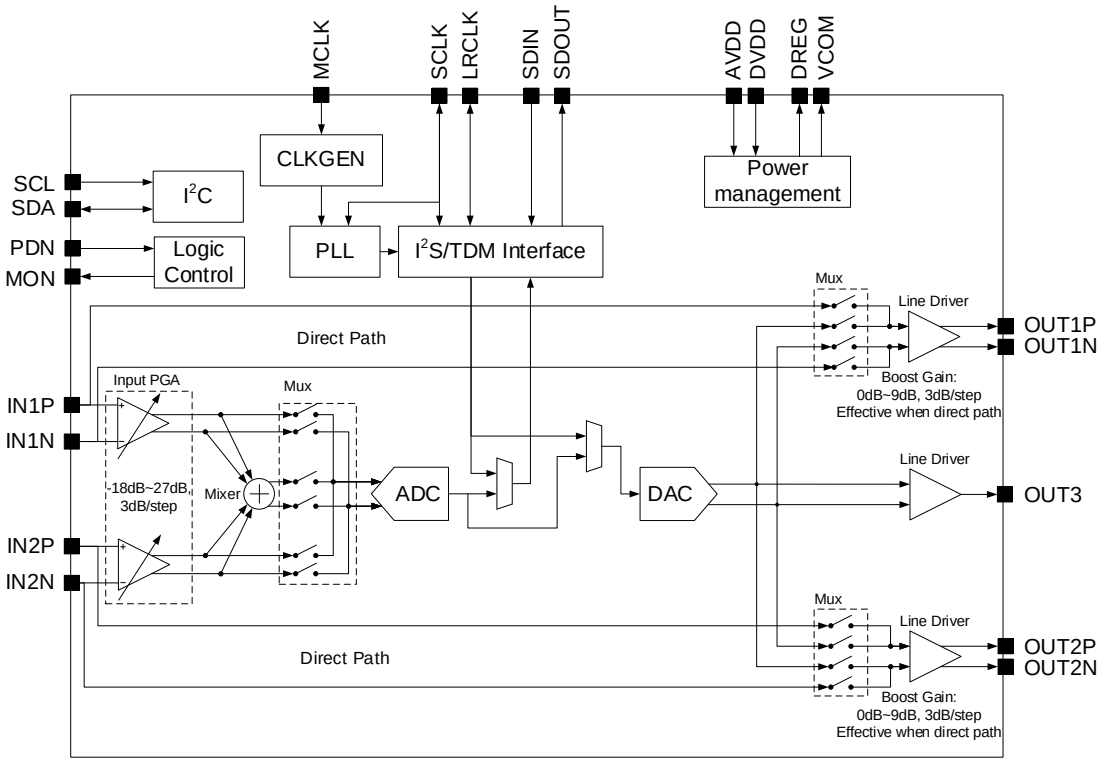


Figure 3. Block Diagram

Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Analog Power Supply	AVDD	AVDD to AGND	-0.3		5.7	V
Digital Power Supply	DVDD	DVDD to DGND	-0.3		3.9	V
Ground Pin Voltage	GND	AGND, DGND	-0.3		0.3	V
INP, INN			-0.3		AVDD	V
Digital Input		SDA, SCL, MCLK, LRCLK, SCLK, SDIN, PDN	-0.3		DVDD+0.3	V
Digital Output		LRCLK, SCLK, SDOUT, MON	-0.3		DVDD+0.3	V
Regulator for Digital Core	DREG		-0.3		2	V
Storage Temperature	T_{stg}		-55		150	°C
Electrostatic Discharge	HBM (Human Body Model)		±2000			V
	CDM (Charge Device Model)		±750			

Thermal Information (Note 2)

Parameter	Value	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	28	°C/W
θ_{JB} Junction-to-board Thermal Resistance	10.3	
$\theta_{JC\ TOP}$ Junction-to-case (top) Thermal Resistance	26	
$\theta_{JC\ BOT}$ Junction-to-case (bot) Thermal Resistance	2.5	

Recommended Operating Conditions

Parameter(Note 3)	Symbol	Conditions	Min	Typ	Max	Unit
Analog Power Supply	AVDD		3	3.3/5	5.5	V
Digital Power Supply	DVDD		1.62	1.8/3.3	3.6	V
Ambient Temperature	T_{amb}		-40		85	°C

Electrical Characteristics (Note 4)

T_A=-40~85°C, Typical values are at T_A=25°C, AVDD=DVDD=3.3 V, f=1kHz, f_s= 48kHz, 24-bit audio data (unless otherwise noted)(Note 5)

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Power Supply	Analog Quiescent Current	I_{AVDD}	ADC and DAC enable with zero input, 1 OUT enable(Note 6)		18.5	24	mA
			ADC and DAC enable with zero input, 3 OUT enable		22	27	mA
			Shutdown mode(PDN=Low)		0.6	1.5	μA
			ADC and DAC enable with zero input, 1 OUT enable, AVDD=5V (Note 6)		22	28	mA
			ADC and DAC enable with zero input, 3 OUT enable, AVDD=5V		25	31	mA
			Shutdown mode(PDN=Low), AVDD=5V		0.8	2	μA
	Digital Quiescent Current	I_{DVDD}	ADC and DAC enable with zero input		11.5	17	μA
			Shutdown mode(PDN=Low)		0.05	1	μA
			ADC and DAC enable with zero input, DVDD= 1.8V		4	8	μA
			Shutdown mode(PDN=Low), DVDD= 1.8V		0.02	0.5	μA
Input and Output Logic	Input Logic Level, High	V_{iH}	SDA, SCL, MCLK, RCLK,SCLK, SDIN, MON, PDN	0.7			DVDD
	Input Logic Level, Low	V_{iL}	SDA, SCL, MCLK, RCLK,SCLK, SDIN, MON, PDN			0.2	
	Output Logic Level, High	V_{oH}	SCLK, LRCLK, SDOUT, MON, SDA; I_{OH}=3mA	0.8			
	Output Logic Level, Low	V_{oL}	SCLK, LRCLK, SDOUT, MON, SDA; I_{OL}=3mA			0.1	
ADC	Differential Full Scale Input Voltage (0dBFS)		Input PGA gain=0dB, 20~20kHz	4.4	4.5	4.7	V_{pp}
			Input PGA gain=0dB, 20~20kHz, AVDD=5V	6.6	6.8	7	
	Noise(Note 6)		No input, A-weighted		-100		dBFS
			No input, CCIR-1k		-90		
			No input, A-weighted, AVDD=5V		-100		
			No input, CCIR-1k, AVDD=5V		-91		
	Signal-to-Noise Ratio(Note 6)	SNR	reference to -1dBFS, A-weighted		99		dB
			reference to -1dBFS, CCIR-1k		89		
			reference to -1dBFS, A-eighted, AVDD=5V		99		
			reference to -1dBFS, CCIR-1k, AVDD=5V		90		
	Dynamic Range(Note 6)	DR	-60dBFS, A-weighted		100		dB
	Total Harmonic Distortion and Noise(Note 6)	THD+N	-1dBFS		-91		dB
	Power Supply Rejection Ratio(Note 5)	PSRR	217Hz 100mV_{pp} signal applied to AVDD		66		dB
			1kHz 100mV_{pp} signal applied to AVDD		66		
Voice Filter (Narrow Band) (Note 6)	Pass Band					0.08	f_s
	Pass Band Ripple				±0.05		dB
	Stop Band			0.21			f_s
	Stop Band Attenuation				-78		dB
	Group Delay				36		$1/f_s$
Voice Filter (Wide Band) (Note 6)	Passband					0.16	f_s
	Pass Band Ripple				±0.05		dB
	Stop Band			0.285			f_s
	Stop Band Attenuation				-78		dB
	Group Delay Time				36		$1/f_s$
Voice Filter (Full Band) (Note 6)	Passband					0.454	f_s
	Pass Band Ripple				±0.05		dB
	Stop Band			0.58			f_s

	Stop Band Attenuation				-82		dB
	Group Delay Time				36		$1/f_s$
DAC with Output Line Driver	Differential Full Scale Output Voltage(0dBFS)		0dBFS input, 20~20kHz	5.7	5.8	5.9	V_{pp}
			0dBFS input, 20~20kHz, AVDD=5V	8.5	8.7	8.9	V_{pp}
	Noise(Note 6)		No input, A-weighted, OUT1 and OUT2		8		μV
			No input, CCIR-1k, OUT1 and OUT2		12		μV
			No input, A-weighted, AVDD=5V, OUT1 and OUT2		12		μV
			No input, CCIR-1k, AVDD=5V, OUT1 and OUT2		16		μV
			No input, A-weighted, OUT3		13		μV
			No input, CCIR-1k, OUT3		32		μV
			No input, A-weighted, AVDD=5V, OUT3		15		μV
			No input, CCIR-1k, AVDD=5V, OUT3		37		μV
	Signal-to-Noise Ratio(Note 6)	SNR	reference to -1dBFS, A-weighted, OUT1 and OUT2		107		dB
			reference to -1dBFS, CCIR-1k, OUT1 and OUT2		103		dB
			reference to -1dBFS, A-weighted, AVDD=5V, OUT1 and OUT2		107		dB
			reference to -1dBFS, CCIR-1k, AVDD=5V, OUT1 and OUT2		104		dB
			reference to -1dBFS, A-weighted,OUT3		97		dB
			reference to -1dBFS, CCIR-1k, OUT3		89		dB
			reference to -1dBFS, A-weighted, AVDD=5V, OUT3		99		dB
			reference to -1dBFS, CCIR-1k, AVDD=5V, OUT3		91		dB
	Dynamic Range (Note 6)	DR	-60dBFS, A-weighted, OUT1 and OUT2		108		dB
			-60dBFS, A-weighted, OUT3		98		dB
	Total Harmonic Distortion and Noise (Note 6)	THD+N	-1dBFS, no load, OUT1 and OUT2		-83		dB
			-1dBFS, 600Ω load, output capacitor = 10μF, OUT1 and OUT2		-81		dB
			-1dBFS, 10kΩ load, output capacitor = 1μF, OUT1 and OUT2		-81		dB
			-1dBFS, 30kΩ load, outputcapacitor = 1μF, OUT1 and OUT2		-82		dB
			-1dBFS, no load, OUT3		-57		dB
			-1dBFS, 600Ω load, output capacitor = 10μF, OUT3		-57		dB
			-1dBFS, 10kΩ load, output capacitor = 1μF, OUT3		-57		dB
			-1dBFS, 30kΩ load, output capacitor = 1μF, OUT3		-57		dB
	Power Supply Rejection Ratio (Note 6)	PSRR	217Hz 100mV$_{pp}$ signal applied to AVDD, OUT1 and OUT2		91		dB
			1kHz 100mV$_{pp}$ signal applied to AVDD, OUT1 and OUT2		89		dB
			217Hz 100mV$_{pp}$ signal applied to AVDD, C_{VCOM}=10μF, OUT3		48		dB
			1kHz 100mV$_{pp}$ signal applied to AVDD, C_{VCOM}=10μF, OUT3		60		dB
			217Hz 100mV$_{pp}$ signal applied to		38		dB

			AVDD, C_{VCOM}=2.2μF, OUT3				
			1kHz 100mV_{pp} signal applied to AVDD, C_{VCOM}=2.2μF, OUT3		51		
DAC Sharp Roll-off Filter (Note 6)	Passband					0.454	fs
	Stop Band			0.546			fs
	Pass Band Ripple				±0.001 8		dB
	Stop Band Attenuation				-75		dB
	Group Delay Time				78		1/fs
DAC Slow Roll-off Filter (Note 6)	Passband					0.328	fs
	Stop Band			0.673			fs
	Pass Band Ripple				±0.001		dB
	Stop Band Attenuation				-112		dB
	Group Delay Time				37		1/fs
Mic Direct Path from Input to Output Line Driver (Note 6)	Differential Full Scale Output Voltage		20~20kHz		5.6		V_{pp}
			20~20kHz, AVDD=5V		8.6		
	Noise		No input, A-weighted		7		μV
			No input, CCIR-1k		11		
			No input, A-weighted, AVDD=5V		7		
			No input, CCIR-1k, AVDD=5V		11		
	Signal-to-Noise Ratio	SNR	Reference to -1dB full-scale, A-weighted		108		dB
	Dynamic Range	DR	-60dB, A-weighted		109		dB
	Total Harmonic Distortion and Noise	THD+N	-1dB full-scale, no load		-96		dB
			-1dB full-scale, 600Ω load output capacitor = 10μF		-77		
			-1dB full-scale, 10kΩ load output capacitor = 1μF		-78		
			-1dB full-scale, 30kΩ load output capacitor = 1μF		-95		
	Power Supply Rejection Ratio	PSRR	217Hz 100mV_{pp} signal applied to AVDD		88		dB
			1kHz 100mV_{pp} signal applied to AVDD		91		dB
	Frequency Response		20~20kHz, refer to 1kHz input	-0.08		+0.01	dB
LDO, DREG	Regulator Voltage for Digital Core	V_{DREG}		1.62	1.8	1.98	V
	DREG Overcurrent Protection				30		mA
	Ramp Time from PDN Pull High(Note 6)		With a 1μF decoupling capacitor		500		μs
VCOM	Analog Output Common Voltage	VCOM			AVDD/ 2		V
	Ramp Time from PDN Pull High(Note 6)		With a 2.2μF decoupling capacitor		2.5		ms

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a four-layer Silergy evaluation board.

Note 3: Deviation from the nominal operation voltage may result in performance degradation.

Note 4: The device is not guaranteed to function outside its operating conditions.

Note 5: Unless otherwise stated, limits are 100% production tested under pulsed load conditions. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 6: Guaranteed by design or statistical correlation and not production tested.

I²C Timing Requirements

Parameter	Symbol	Conditions	Min	Max	Unit
SCL Frequency	f_{SCL}	No wait states		400	kHz
SCL and SDA Rise Time	t_r			300	ns
SCL and SDA Fall Time	t_f			300	ns
SCL High Duration Time	t_{WH}		0.6		μs
SCL Low Duration Time	t_{WL}		1.3		μs
SDA to SCL Setup Time	t_{S1}		250		ns
SCL to SDA Hold Time	t_{h1}		0		ns
Free Time between Stop and Start Condition	t_{buf}		1.3		μs
SCL to Start Condition	t_{S2}		0.6		μs
Start Condition to SCL Hold Time	t_{h2}		0.6		μs
SCL to Stop Condition	t_{S3}		0.6		μs

Note: A device must internally provide a hold time of at least t_f for the SDA signal to bridge the undefined region of the falling edge of SCL.

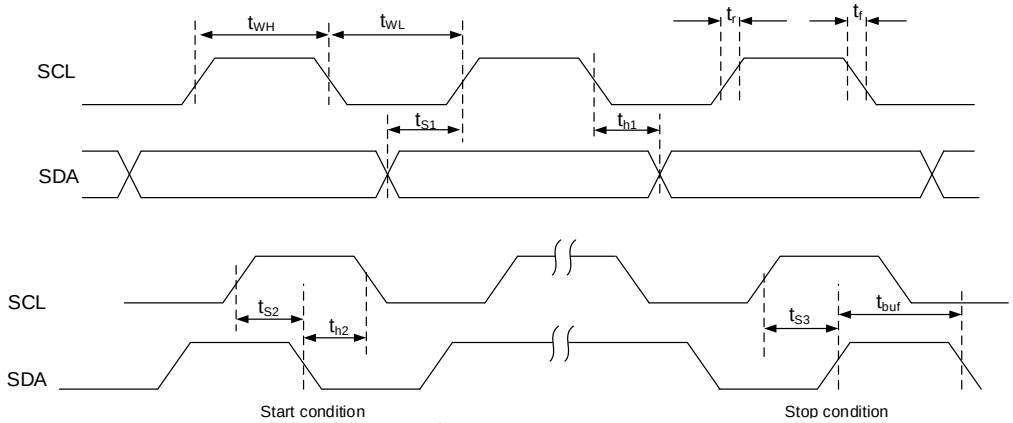


Figure 4. I²C Timing Diagram

Serial Audio Ports

System Clock	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
In Target Mode	LRCLK Input Clock	f_{LRCLK} or f_s		8		96	kHz
	SCLK Frequency	f_{SCLK}		1.024		24.576	MHz
	SCLK Duty Cycle			40	50	60	%
	LRCLK Duty Cycle			40	50	60	%
	LRCLK to SCLK Rising Edge Setup Time	t_{S4}		10			ns
	LRCLK from SCLK Rising Edge Hold Time	t_{h3}		10			ns
	SDIN to SCLK Rising Edge Setup Time	t_{S5}		10			ns
	SDIN from SCLK Rising Time Hold Time	t_{h4}		10			ns
	LRCLK Edge with Respect to the Falling Edge of SCLK	t_{edge}		-1/4		1/4	SCLK period
	Rise/Fall Time for SCLK/LRCLK	t_{rs} /t_{fs}			1/8		SCLK period
In Controller Mode	MCLK or OSC_IN Input Clock	f_{sys}		1.024	12.288	24.576	MHz
	Duty Cycle			40	50	60	%

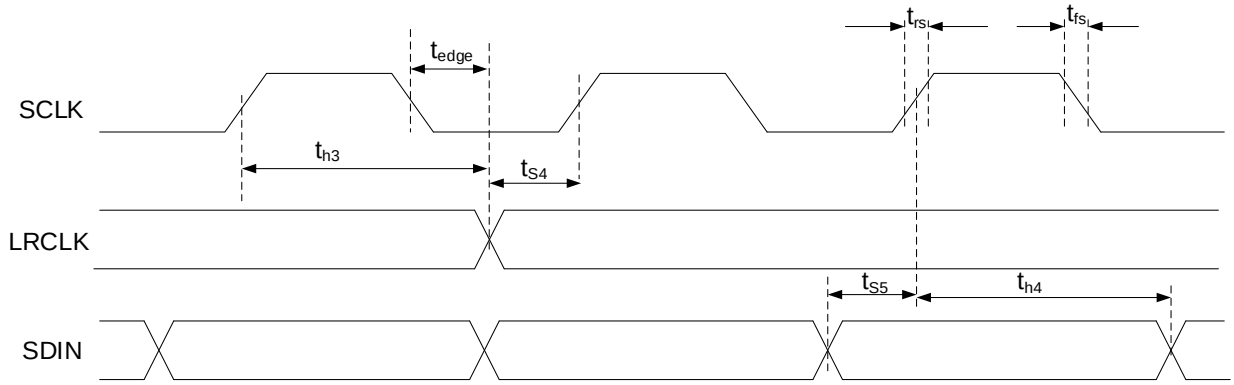


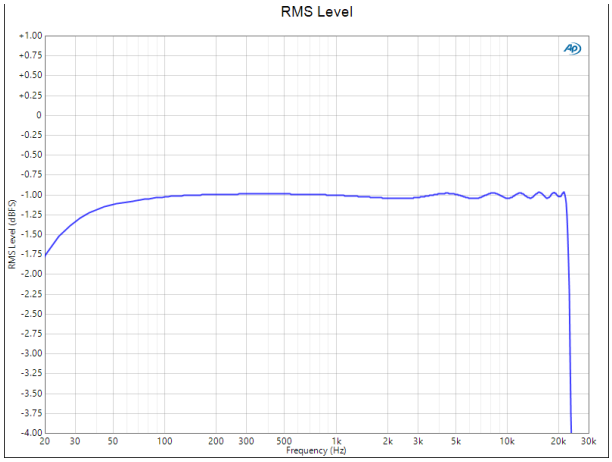
Figure 5. I²S Timing Diagram

Typical Performance Characteristics

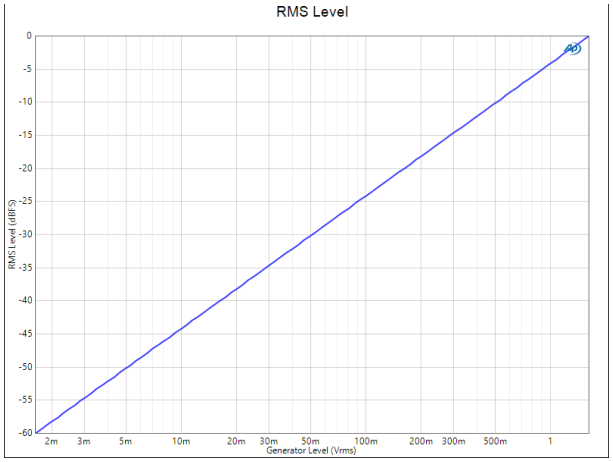
T_A=25°C, AVDD=3.3V, DVDD=3.3 V, f=1kHz, f_S= 48kHz, 32-bit slot width, 24-bit data length, I²S standard mode, IN and OUT blocking capacitor is 1μF, VCOM decoupling capacitor is 2.2μF, DREG decoupling capacitor is 1μF, full scale input as 0dB, frequency response, FFT and THD+N vs. frequency are tested at -1dB signal input, THD+N vs. output is tested at 1kHz (unless otherwise noted)

ADC Performance

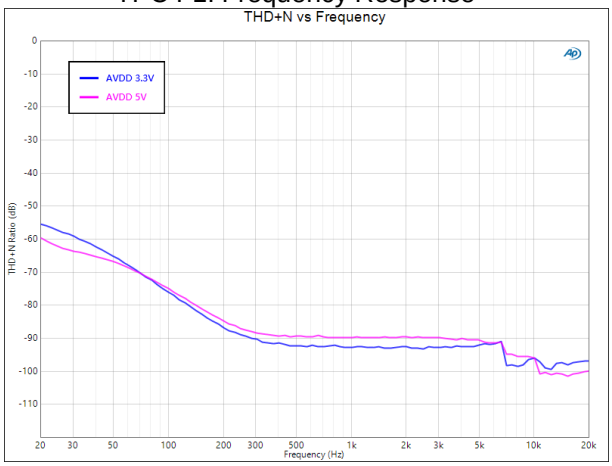
Full band filter unless otherwise noted.



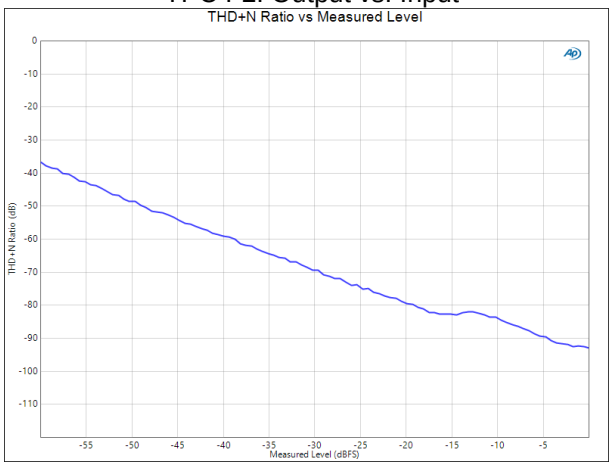
TPC F1. Frequency Response



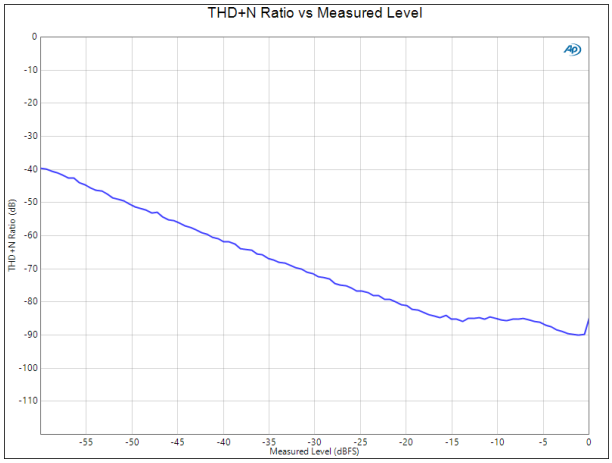
TPC F2. Output vs. Input



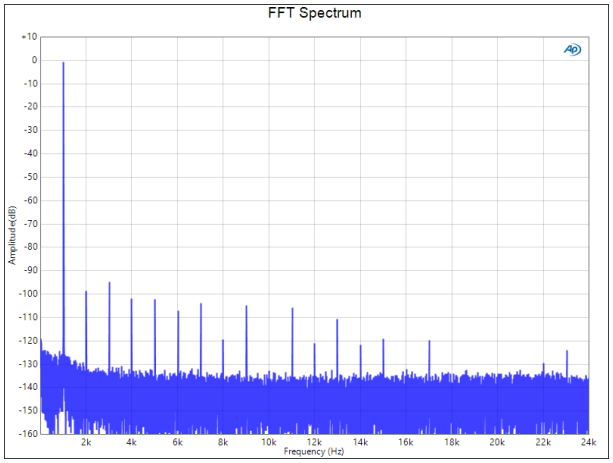
TPC F3. THD+N vs. Frequency



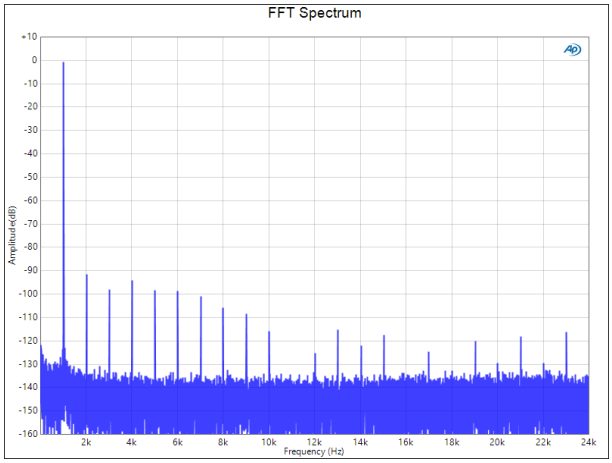
TPC F4. THD+N vs. Output
AVDD=3.3V



TPC F5. THD+N vs. Output
AVDD=5V

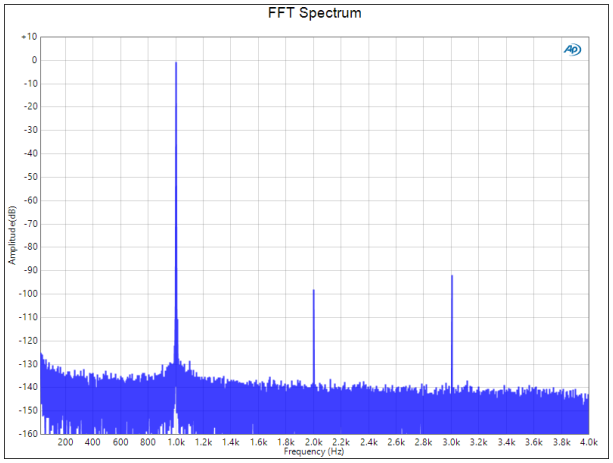


TPC F6. FFT Spectrum
AVDD=3.3V



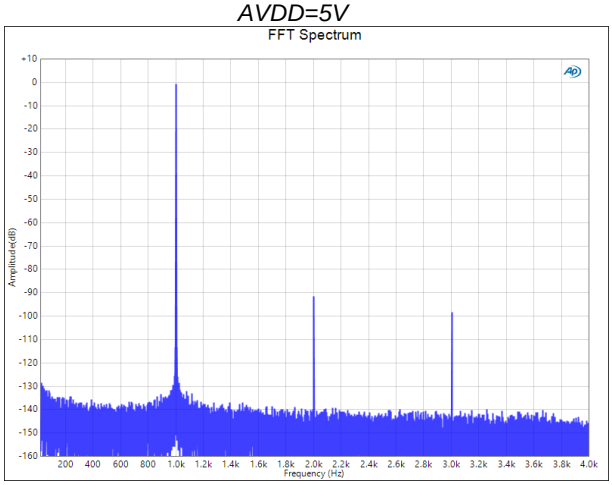
TPC F7. FFT Spectrum

AVDD=5V



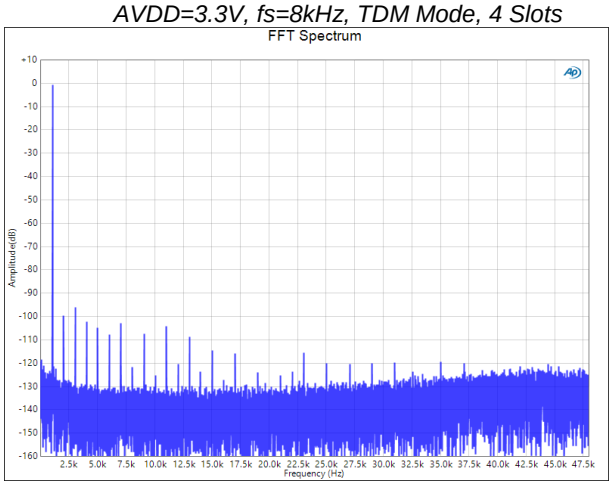
TPC F8. FFT Spectrum

AVDD=3.3V, fs=8kHz, TDM Mode, 4 Slots



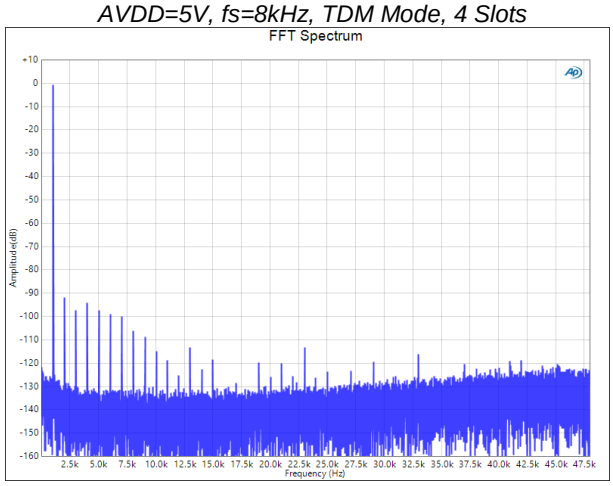
TPC F9. FFT Spectrum

AVDD=5V, fs=8kHz, TDM Mode, 4 Slots



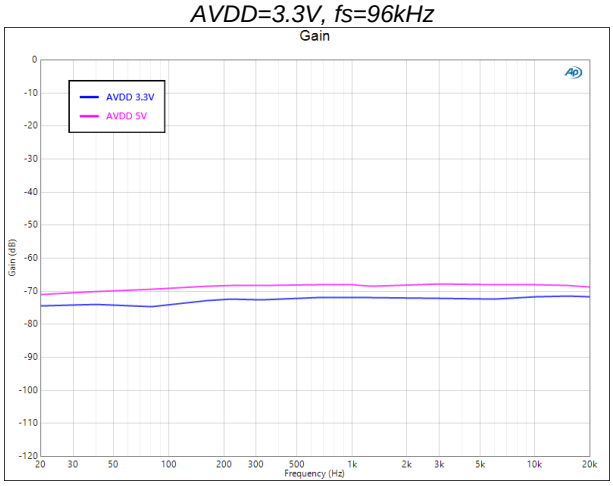
TPC F10. FFT Spectrum

AVDD=3.3V, fs=96kHz



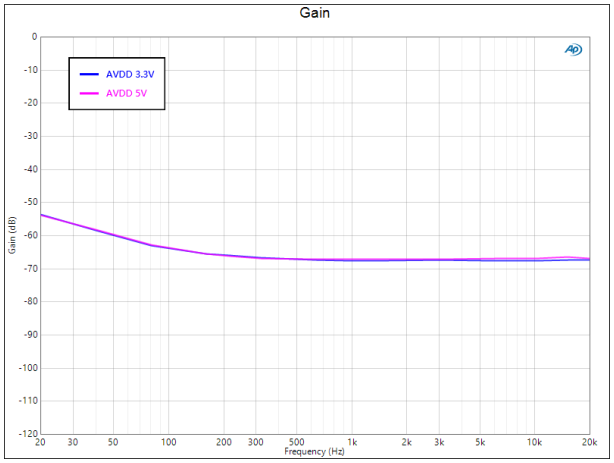
TPC F11. FFT Spectrum

AVDD=5V, fs=96kHz



TPC F12. PSRR

Inject 100mVpp sine wave to AVDD

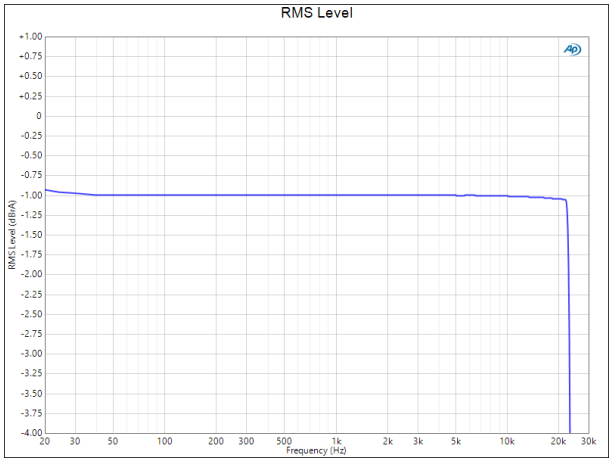


TPC F13. CMRR

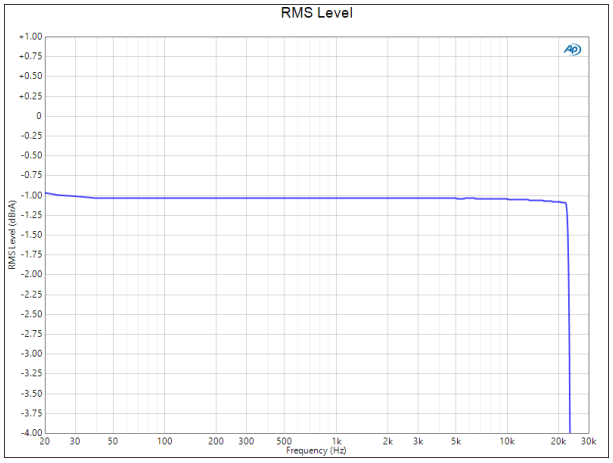
Input 100mVpp common mode sine wave to INP and INN

DAC Performance

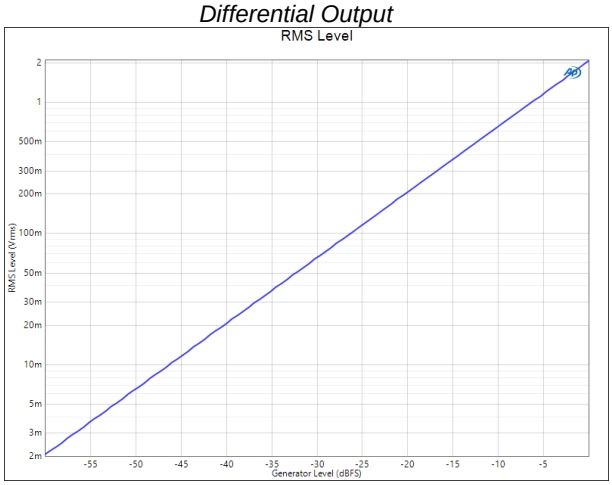
Sharp roll-off filter unless otherwise noted.



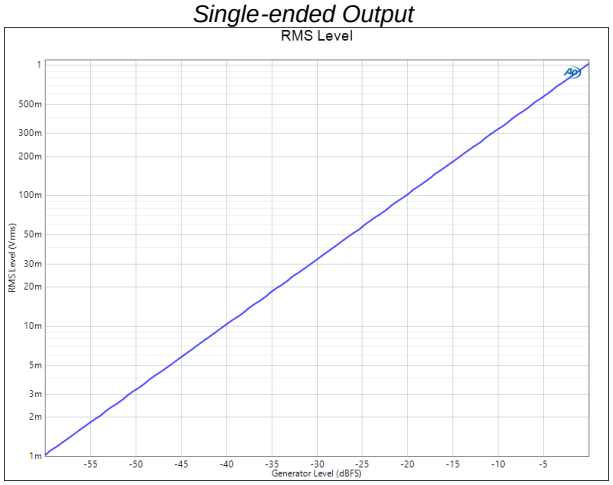
TPC F14. Frequency Response
Differential Output



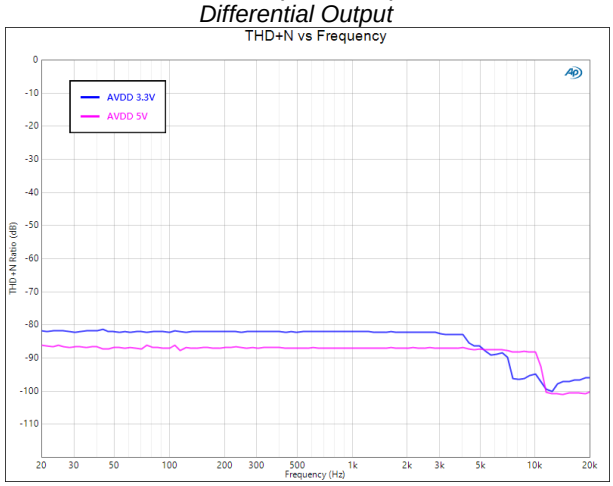
TPC F15. Frequency Response
Single-ended Output



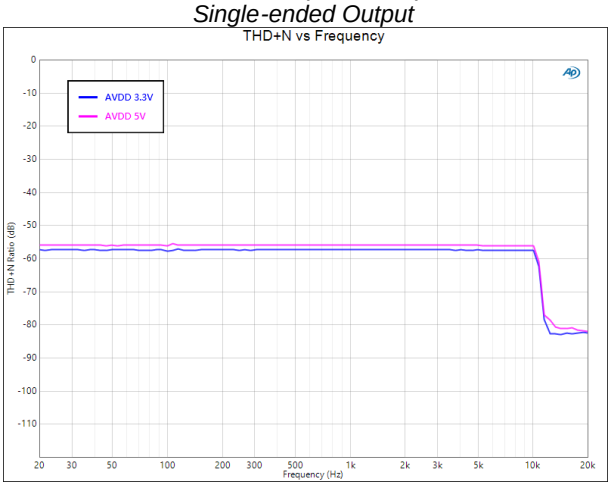
TPC F16. Output vs. Input
Differential Output



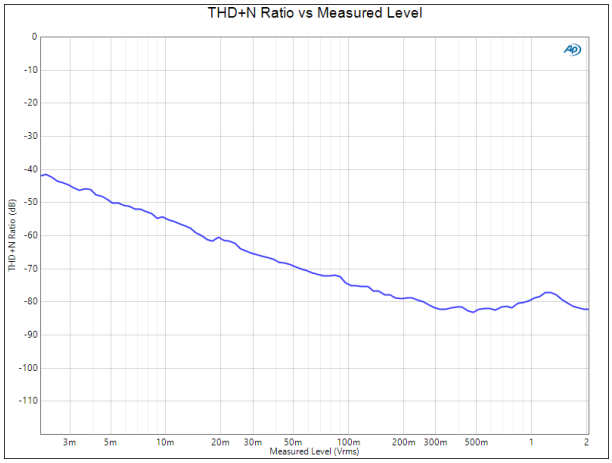
TPC F17. Output vs. Input
Single-ended Output



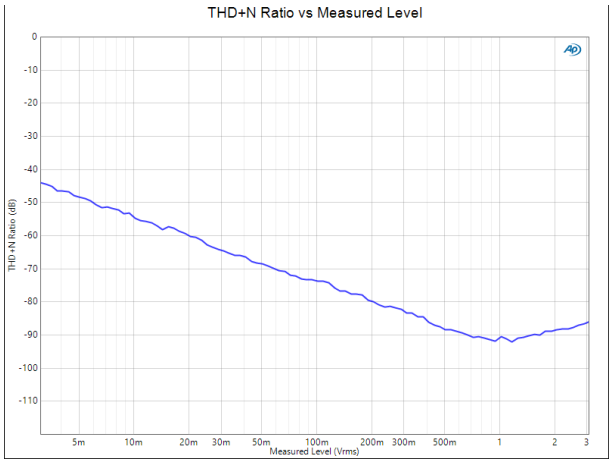
TPC F18. THD+N vs. Frequency
Differential Output



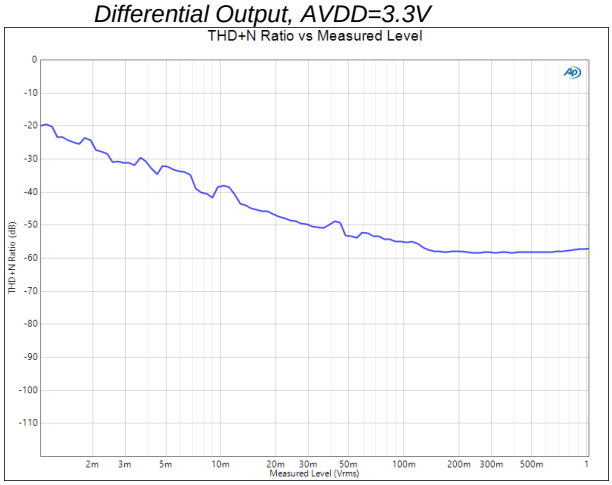
TPC F19. THD+N vs. Frequency
Single-ended Output



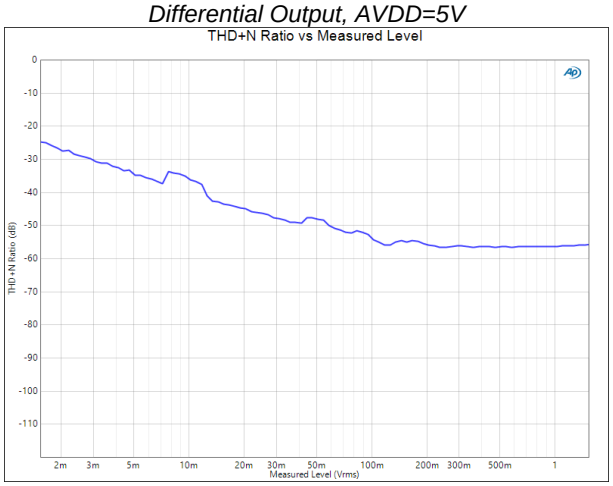
TPC F20. THD+N vs. Output
Differential Output, AVDD=3.3V



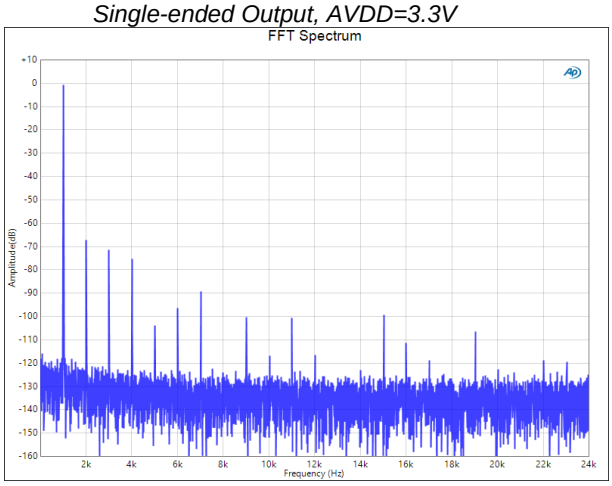
TPC F21. THD+N vs. Output
Differential Output, AVDD=5V



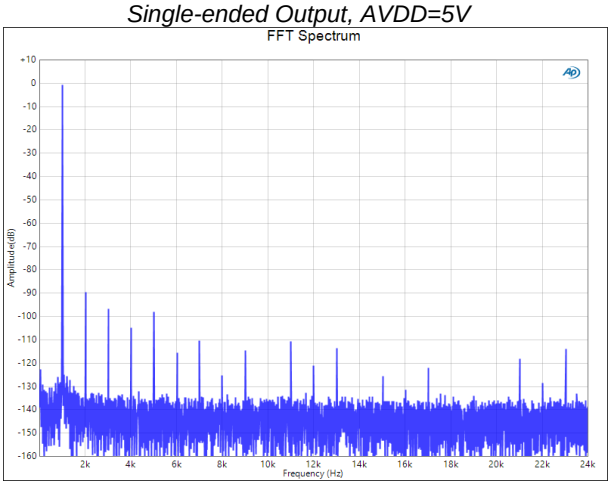
TPC F22. THD+N vs. Output
Single-ended Output, AVDD=3.3V



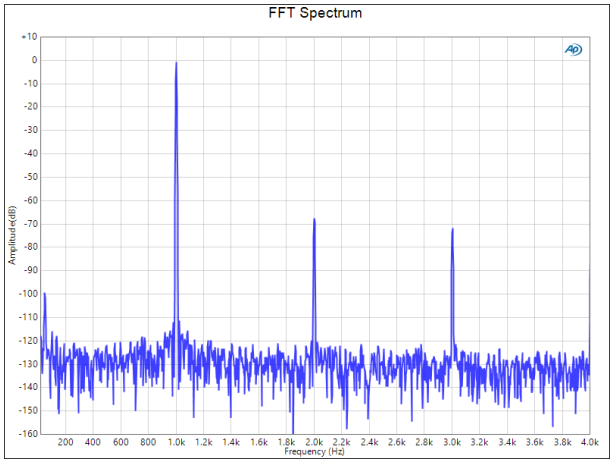
TPC F23. THD+N vs. Output
Single-ended Output, AVDD=5V



TPC F24. FFT Spectrum
Differential Output, AVDD=3.3V

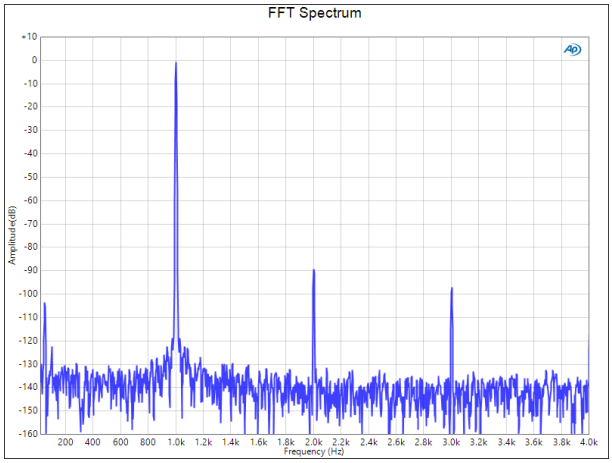


TPC F25. FFT Spectrum
Differential Output, AVDD=5V



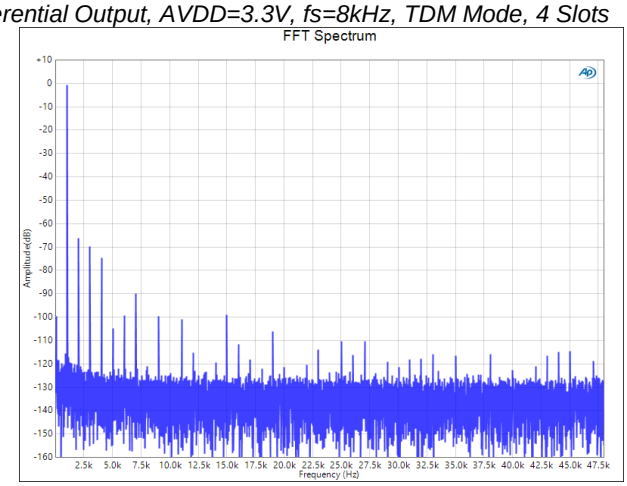
TPC F26. FFT Spectrum

Differential Output, AVDD=3.3V, fs=8kHz, TDM Mode, 4 Slots



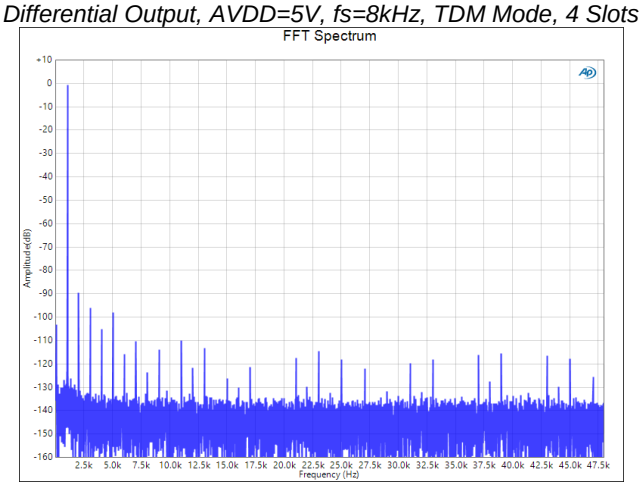
TPC F27. FFT Spectrum

Differential Output, AVDD=5V, fs=8kHz, TDM Mode, 4 Slots



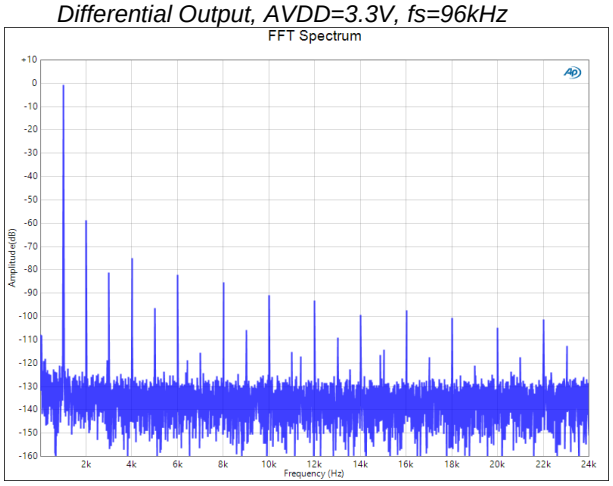
TPC F28. FFT Spectrum

Differential Output, AVDD=3.3V, fs=96kHz



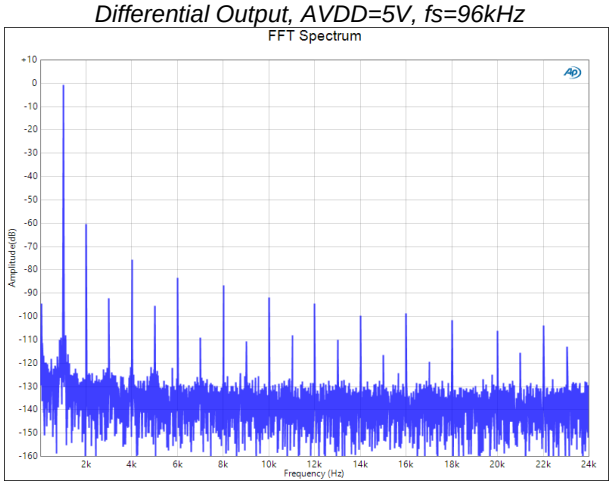
TPC F29. FFT Spectrum

Differential Output, AVDD=5V, fs=96kHz



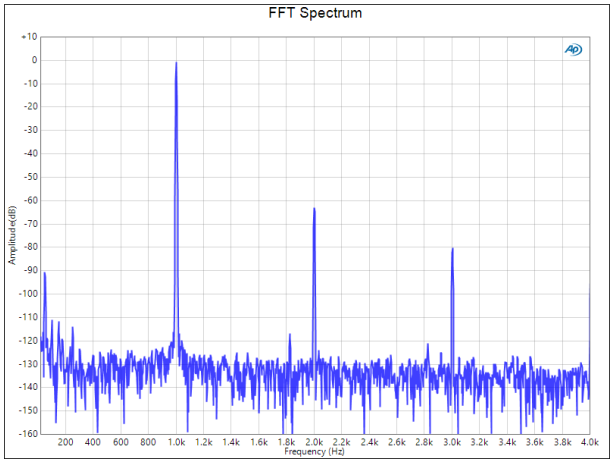
TPC F30. FFT Spectrum

Single-ended Output, AVDD=3.3V



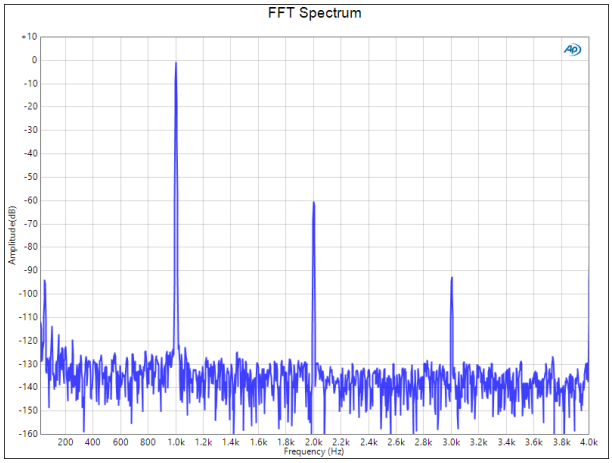
TPC F31. FFT Spectrum

Single-ended Output, AVDD=5V



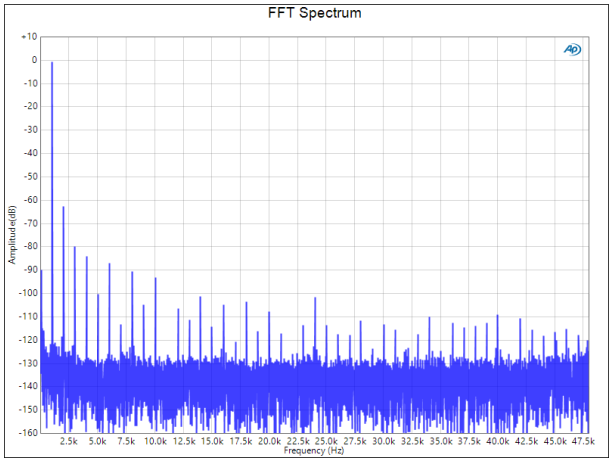
TPC F32. FFT Spectrum

Single-ended Output, AVDD=3.3V, fs=8kHz, TDM Mode, 4 Slots



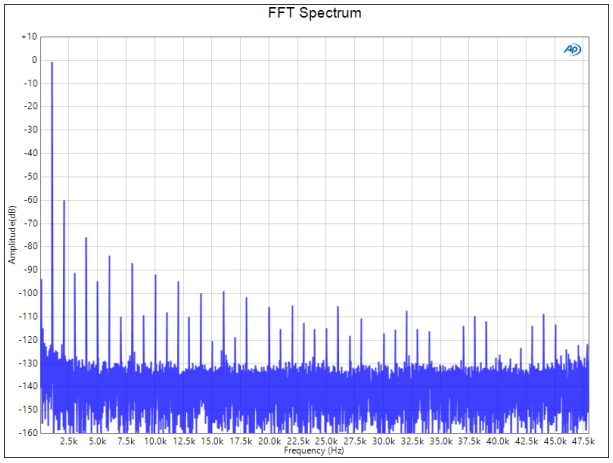
TPC F33. FFT Spectrum

Single-ended Output, AVDD=5V, fs=8kHz, TDM Mode, 4 Slots



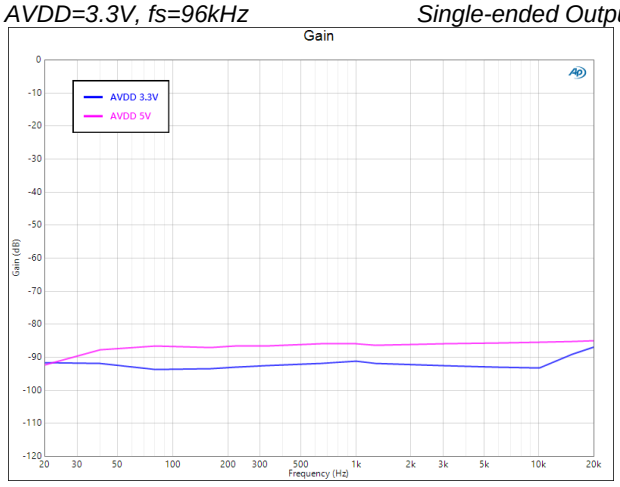
TPC F34. FFT Spectrum

Single-ended Output, AVDD=3.3V, fs=96kHz



TPC F35. FFT Spectrum

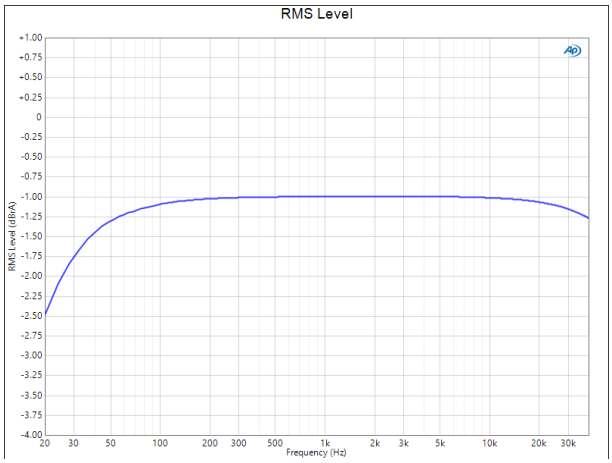
Single-ended Output, AVDD=5V, fs=96kHz



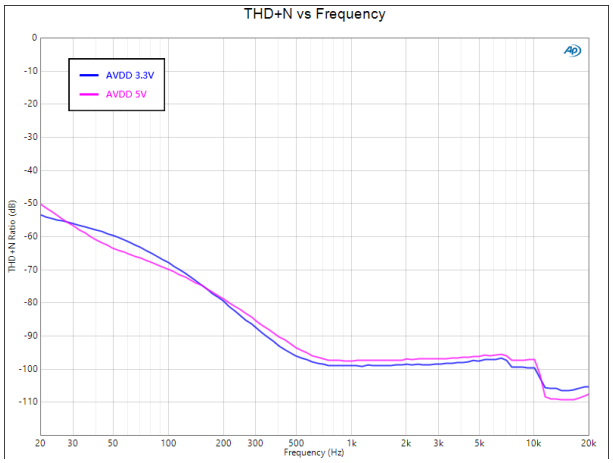
TPC F36. PSRR

Differential Output, Inject 100mVpp sine wave to AVDD

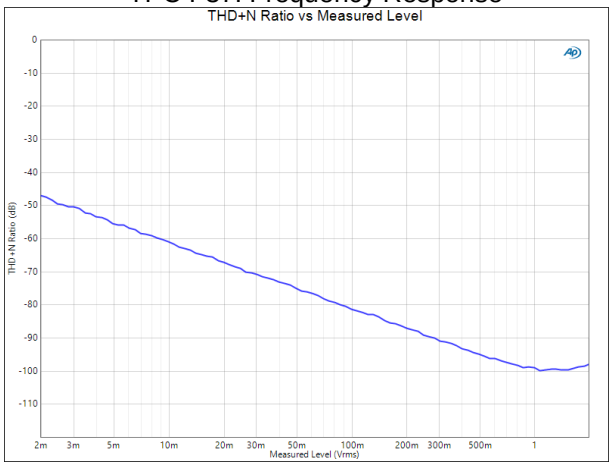
Direct Path Performance



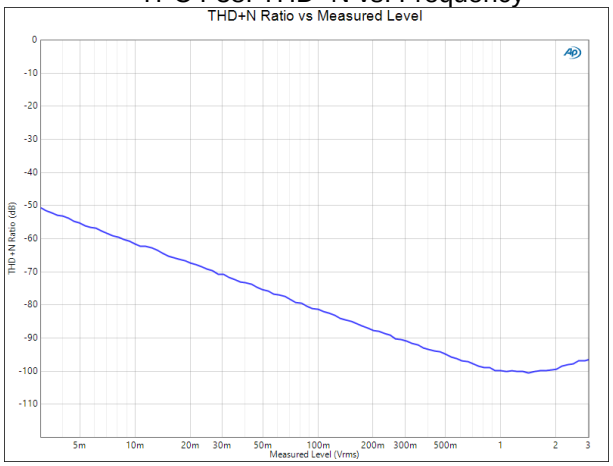
TPC F37. Frequency Response



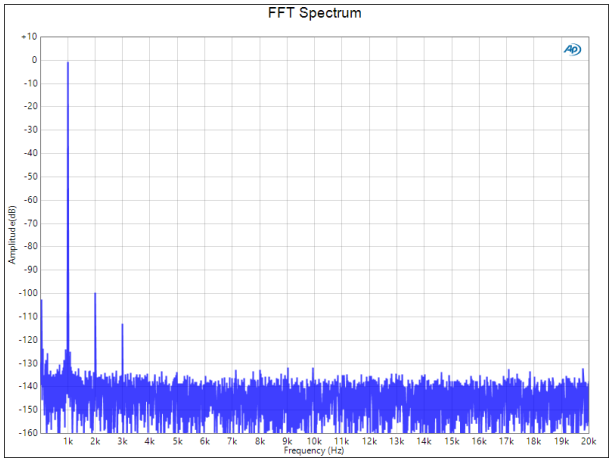
TPC F38. THD+N vs. Frequency



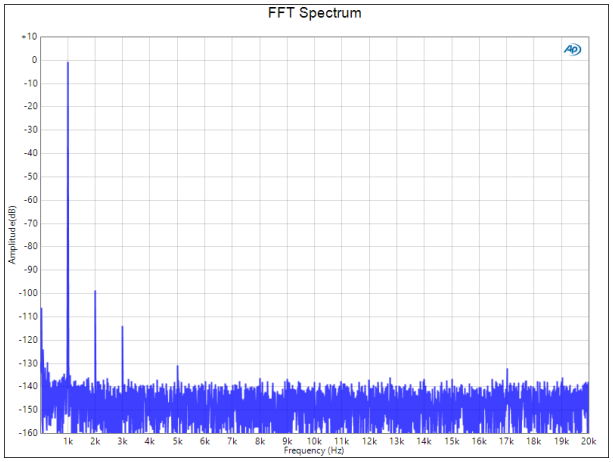
TPC F39. THD+N vs. Output
AVDD=3.3V



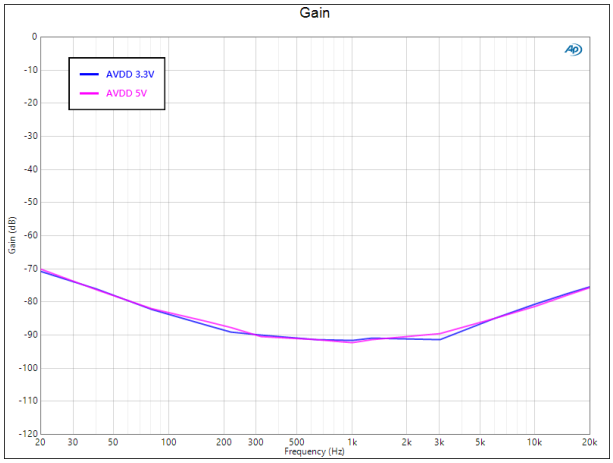
TPC F40. THD+N vs. Output
AVDD=5V



TPC F41. FFT Spectrum
AVDD=3.3V



TPC F42. FFT Spectrum
AVDD=5V

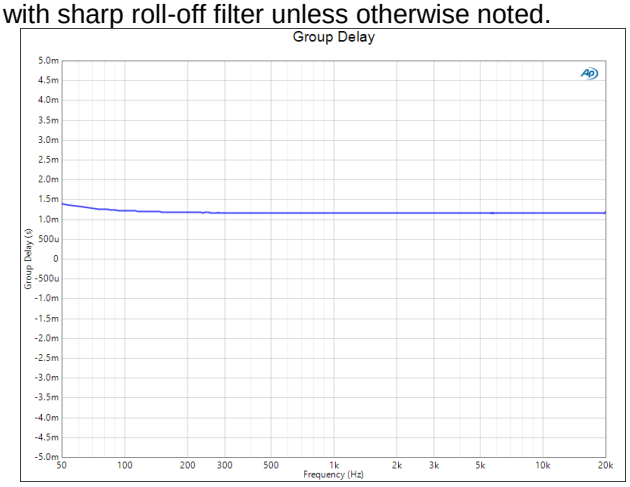


TPC F43. PSRR

Inject 100mVpp sine wave to AVDD

Other Characteristics

ADC with full band filter and DAC with sharp roll-off filter unless otherwise noted.



TPC F44. Group Delay
ADC to DAC Path

Detailed Description and Theory of Operation

Power Supply

The SQ58621 requires an external power supply for AVDD to power the entire system and for DVDD to power the digital I/O interfaces. An integrated low-dropout (LDO) regulator generates DREG for the digital core power supply. Note that DREG can only be used internally and must not be connected to external loads. The SQ58621 features DREG current limit protection, which activates if DREG is shorted to the power supply or GND. Set 0x49[3:2] bits to change the DREG current limit threshold. Connect 1μF capacitors between AVDD, DVDD, DREG, and GND for decoupling.

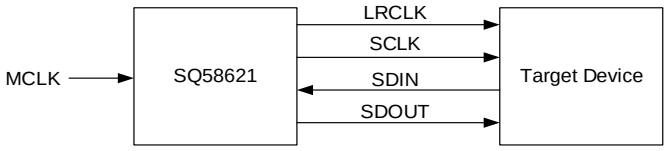
The VCOM analog output common voltage is derived from the resistor divider of AVDD, making VCOM equal to AVDD/2. Connect a 2.2μF capacitor between VCOM and GND for noise filtering.

Audio Serial Data Interface

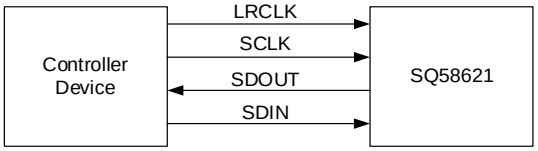
Controller and Target Mode

The SQ58621 can function as an I²S controller(master) or target(slave) device. When PDN transitions from low to high, the SQ58621 will change from shutdown to normal operation. During PDN activation or AVDD/DVDD startup, the MON pin defines the SQ58621 as either a controller or target mode. Once set, this mode is latched regardless of subsequent MON changes until the next power up event. Register 0x04[3] indicates the current mode of the SQ58621.

In controller mode, the SQ58621 receives an external controller clock on the MCLK pin and internally generates the I²S clock, outputting it on the LRCLK and SCLK pins for the target device. In target mode, the SQ58621 only accepts I²S clock from the controller device on the LRCLK and SCLK pins, eliminating the need for the controller clock. Thus, the MCLK pin can be left open or connected to GND. To disable MCLK error processing, write 0x05 to register 0x33 (0x33[3] mclk_stop_error_en and 0x33[1] mclk_error_en).



(a) Controller Mode



(b) Target Mode

Figure 6. Controller Device and Target Device Connection

In controller mode, the SQ58621 accepts an external clock on the MCLK pin, ranging from 1.024MHz to 24.576MHz, at a multiple of the sampling frequency, to generate the system clock.

Table 1. MCLK Frequency Setting

Address	Access	Default	Description
0x03[3,0]	RW	4'h0	MCLK frequency selection: 4'h0: 1.024MHz 4'h1: 1.536MHz 4'h2: 2.048MHz 4'h3: 2.304MHz 4'h4: 3.072MHz 4'h5: 4.096MHz 4'h6: 4.068MHz 4'h7: 6.144MHz 4'h8: 8.192MHz 4'h9: 9.216MHz 4'hA: 12.288MHz 4'hB: 16.384MHz

			4'hC: 18.432MHz 4'hD: 24.576MHz Others: NA

Audio Serial Data Format

The SQ58621 supports flexible data transfer formats, including I²S and TDM. In TDM format, it supports 4, 8, or 16 slots. The device can accept serial data using 16, 20, 24, or 32 bits. The SQ58621 also supports LRCLK shift left, invert in left-justified and right-justified modes, and SCLK invert. All audio serial data formats can be configured using registers 0x05~0x06.

Table 2. Audio Serial Data Format Setting

Address	Bit	Label	Access	Default	Description
0x05[6,0]	6	serial_data_stream_mode	RW	1'b0	1'b0: I²S mode 1'b1: TDM mode
	5:4	serial_data_stream_format	RW	2'b00	2'b00: I²S standard 2'b01: Left-justified 2'b10: Right-justified 2'b11: Reserved
	3:2	serial_data_stream_data_length	RW	2'b01	2'b00: 32-bit 2'b01: 24-bit 2'b10: 20-bit 2'b11: 16-bit
	1:0	serial_data_stream_slot_width	RW	2'b00	2'b00: 32-bit 2'b01: 24-bit 2'b10: 16-bit 2'b11: Reserved
0x06[4,0]	4:3	serial_data_stream_slot_sel	RW	2'b00	2'b00: TDM – 4 slots 2'b01: TDM – 8 slots 2'b10: TDM – 16 slots
	2	serial_data_lrclk_shift	RW	1'b0	Only effective in left-justified and right-justified modes 1'b0: Not shift left LRCLK 1'b1: Shift left LRCLK by one bit
	1	serial_data_lrclk_invert	RW	1'b0	Only effective in left-justified and right-justified modes 1'b0: Not invert LRCLK 1'b1: Invert LRCLK
	0	serial_data_sclk_invert	RW	1'b0	1'b0: Not invert SCLK 1'b1: Invert SCLK

Normal I²S Mode

In normal I²S mode, SCLK functions as the bit clock for data transmission, while LRCLK determines the data frame. The data is written MSB first. Input data (SDIN) is valid on the rising edge of SCLK, and output data (SDOUT) is valid on the falling edge of SCLK. The DSP masks unused trailing data bit positions.

The SQ58621 supports I²S standard, left-justified, and right-justified formats in normal I²S mode. The serial audio port settings are programmed in registers 0x03~0x06.

In I²S the MSB of channel 1 is valid on the second rising edge of SCLK after the falling edge of the audio frame clock (LRCLK). Similarly, the MSB of channel 2 is valid on the second rising edge of SCLK after the rising edge of LRCLK.

In left-justified and right-justified formats, LRCLK defines the start of the audio data. The rising edge of LRCLK initiates the data transfer, starting with the channel 1 data slot, followed by the channel 2 data slot. Each data bit is valid on the rising edge of the serial clock (SCLK). In left-justified mode, the MSB of the slot is valid on the first rising edge of SCLK. In right-justified mode, the MSB of the slot is valid on the [slot width - data length]th rising edge of SCLK.

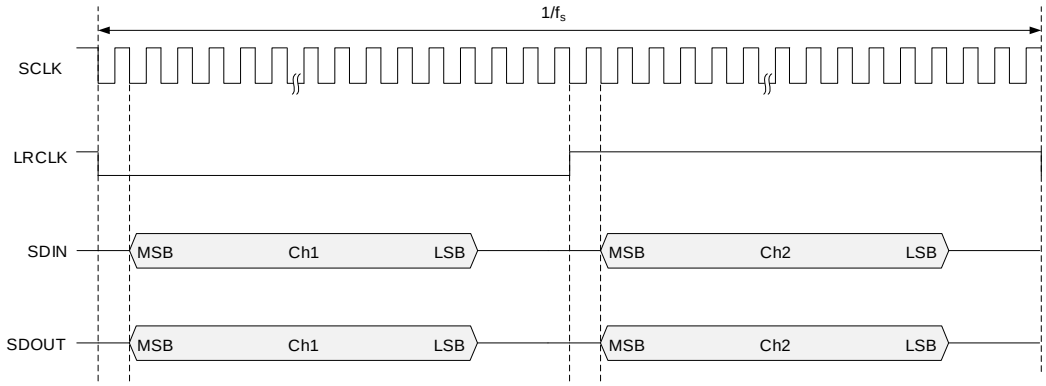


Figure 7. I²S Standard Data Format

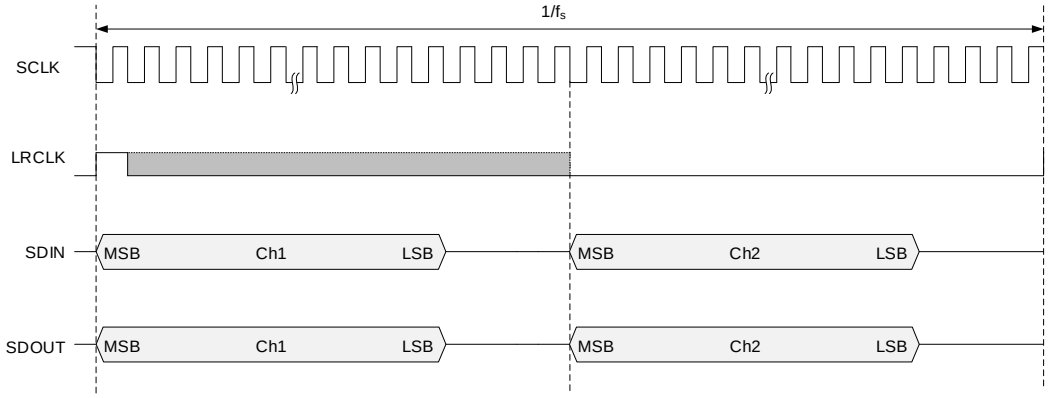


Figure 8. Left-Justified Data Format

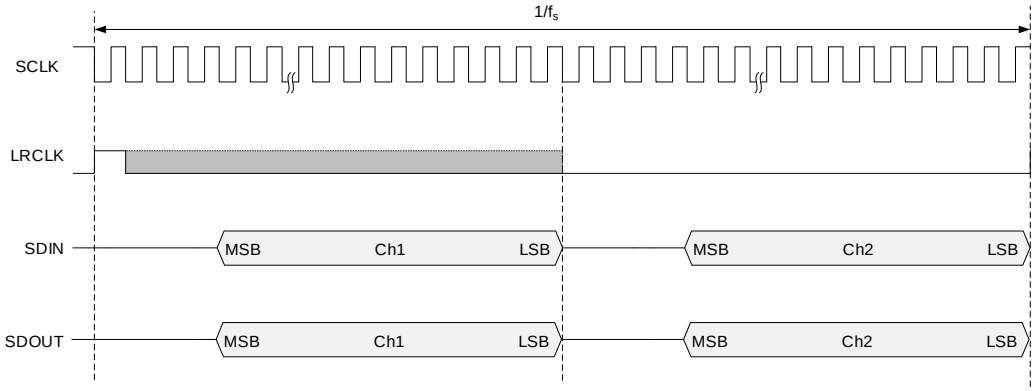


Figure 9. Right-Justified Data Format

TDM Mode

In TDM (time-division multiplexing) mode, embeds audio data in a single data stream. Channels are sequentially embedded in the data stream, beginning with channel 1, followed by channel 2, channel 3, and so on. The SQ58621 can be configured for a single 4-channel, 8-channel, or 16-channel data stream. The interface supports 16-bit, 20-bit, 24-bit, and 32-bit serial data signals. Data is written MSB first. Input data (SDIN) is valid on the rising edge of the clock, and output data (SDOUT) is valid on the falling edge of the clock. The DSP masks unused trailing data bit positions.

The SQ58621 supports I²S standard, left-justified, and right-justified formats in TDM mode. In TDM mode, regardless of the specific format, LRCLK defines the start of the audio data.

- In I²S standard format, the falling edge of LRCLK initiates data transfer, starting with the channel 1 data slot, followed by channel 2, channel 3, and so on.
- In left-justified and right-justified formats, the rising edge of LRCLK initiates data transfer in the same channel sequence.

Each data bit is sampled on the rising edge of the serial clock (SCLK) and output on the falling edge of SCLK. The key differences are as follows:

- In I2S standard mode, the MSB of the slot is valid on the second rising edge of SCLK.
- In left-justified mode, the MSB of the slot is valid on the first rising edge of SCLK.
- In right-justified mode, the MSB of the slot is valid on the [slot width - data length]th rising edge of SCLK.

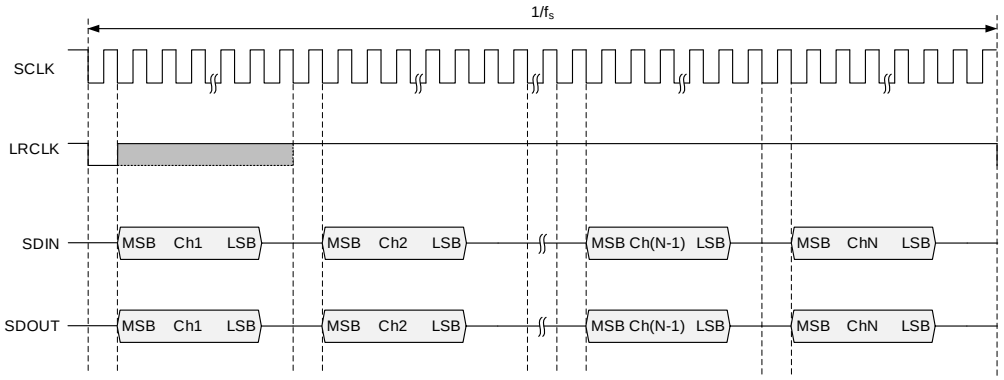


Figure 10. TDM Mode (I²S Standard)

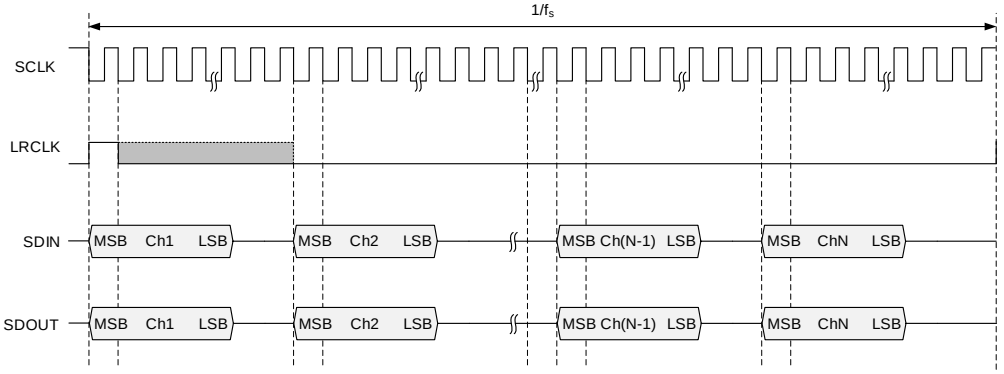


Figure 11. TDM Mode (Left-Justified)

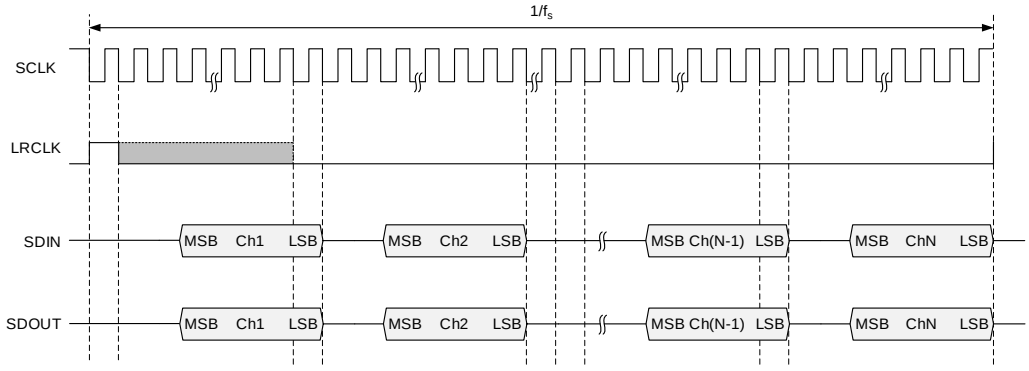


Figure 12. TDM Mode (Right-Justified)

SCLK Invert

The SQ58621 supports SCLK invert for both normal I²S mode and TDM mode. If this function is enabled, the clock can be inverted for internal data recognition.

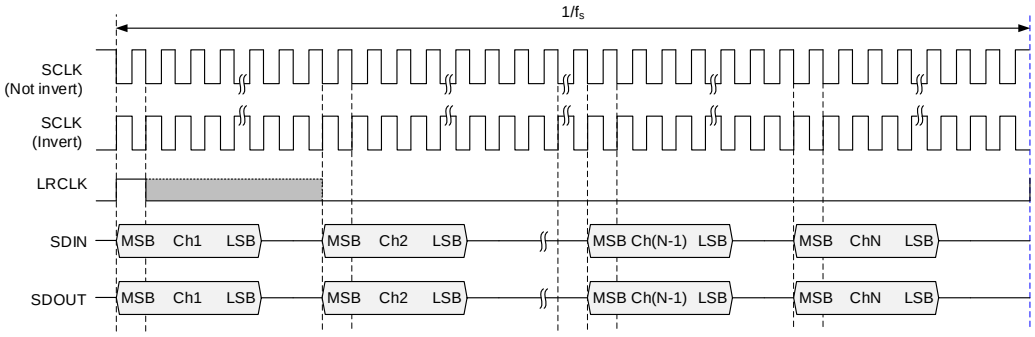


Figure 13. SCLK Invert

LRCLK Clock Invert

The SQ58621 can support LRCLK invert for both normal I²S mode and TDM mode, but it can only be used in left-justified and right-justified formats. If this function is enabled, the clock can be inverted for internal data recognition.

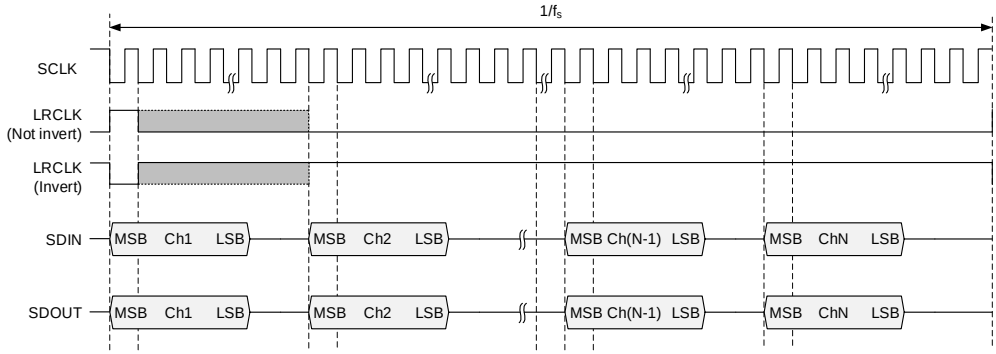


Figure 14. LRCLK Invert

LRCLK Shift Left

The SQ58621 also supports LRCLK shift left for normal I²S mode and TDM mode, but this function is applicable only in left-justified and right-justified formats. When enabled, the frame clock will be shifted left by one clock bit.

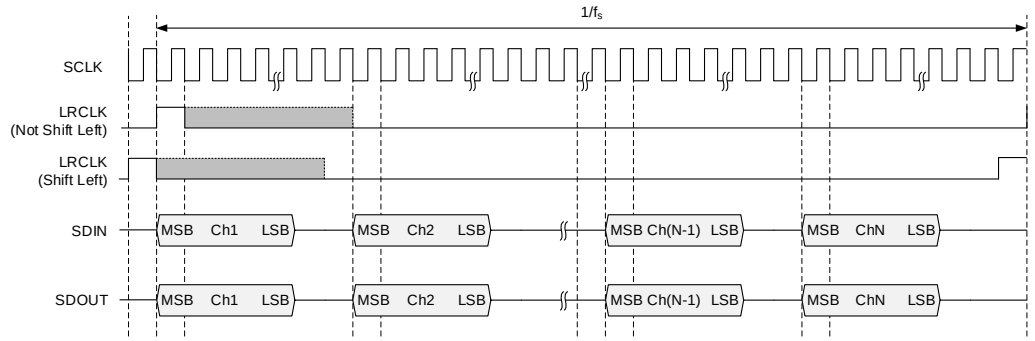


Figure 15. LRCLK Shift Left

Clock, Auto Detection, and PLL

The SQ58621 requires configuration to match the clock from an external device or generate the necessary clock output. In controller mode, after setting the MCLK frequency, the SQ58621 can generate LRCLK and SCLK as needed. First, set f_{LRCLK} or fs to either a 48kHz base or a 44.1kHz base using register 0x03[6]. In target mode, the LRCLK base setting can be skipped.

Table 3. LRCLK Base Setting

Address	Access	Default	Description
0x03[6]	RW	1'b0	Set fs base in controller mode, skipped in target mode 1'b0: 48k(fs=8kHz, 16kHz, 32kHz, 48kHz, 96kHz) 1'b1: 44.1k(fs=44.1kHz, 88.2kHz)

In target mode, the SQ58621 can automatically detect the LRCLK clock from an external device or configure the LRCLK clock manually. If 0x04[7] is set as 1'b0, the SQ58621 detects LRCLK automatically, and 0x04[2,0] indicates the real-time clock input on the LRCLK pin.

In controller mode, the SQ58621 can only configure the LRCLK clock manually. When 0x04[7] is set as 1'b1, the SQ58621, in either controller or target mode, can configure LRCLK as required. After setting the LRCLK base and configuring LRCLK, the SQ58621 can properly receive an external LRCLK clock or generate an internal LRCLK clock.

Table 4. LRCLK Clock Setting

Address	Bit	Label	Access	Default	Description		
0x04	7	fs_rate_cfg_en	RW	1'b1	In target mode: 1'b0: Detect fs rate automatically 1'b1: Configure fs rate manually In controller mode: 1'b0/1'b1: Configure fs rate manually		
	6:4	fs_rate_cfg	RW	3'b011	Sampling rate configuration		
					fs_rate_cfg	48kHz base	44.1kHz base
					3'b000	8kHz	
					3'b001	16kHz	
					3'b010	32kHz	
					3'b011	48kHz	44.1kHz
					3'b100	96kHz	88.2kHz
					Others	NA	NA
	3	sysclk_mode_sel	R	1'b0	Indicate SQ58621 status: 1'b1: Controller mode 1'b0: Target mode		
	2:0	auto_detected_fs_rate	R	3'b011	Auto-detected sampling rate		
					fs_rate_cfg	48kHz base	44.1kHz base
					3'b000	8kHz	
					3'b001	16kHz	
					3'b010	32kHz	
					3'b011	48kHz	44.1kHz
					3'b100	96kHz	88.2kHz
					Others	NA	NA

During data transmission, the ‘serial_data_stream_slot_width’ refers to the number of sampling bits for one channel in an LRCLK cycle, while the ‘serial_data_stream_data_length’ refers to the quantization accuracy of audio data for one channel in an LRCLK cycle. Both parameters represent the number of SCLK cycles. For complete audio data transmission, the slot width must not be less than the data length.

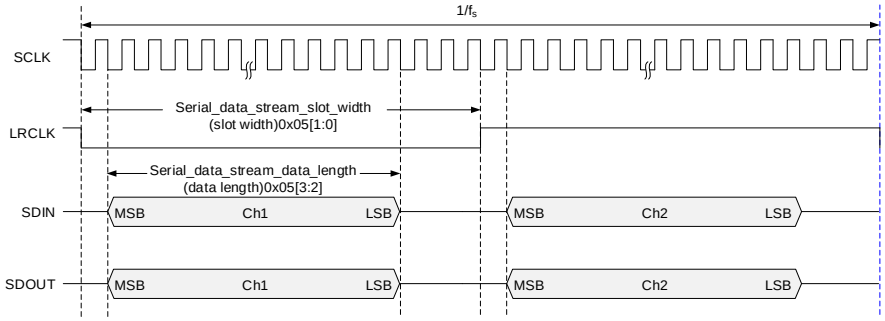


Figure 16. Slot Width and Data Length

The digital audio processor supports all the sample rates and SCLK rates defined in the clock control register. The sample rate can be set manually or auto-detected by the SQ58621.

$$\text{SCLK rate} = f_s \times \text{serial\_data\_stream\_slot\_width} \times \text{slots}$$

The PLL can be set manually or automatically by the DAP through 0x38~0x3A.

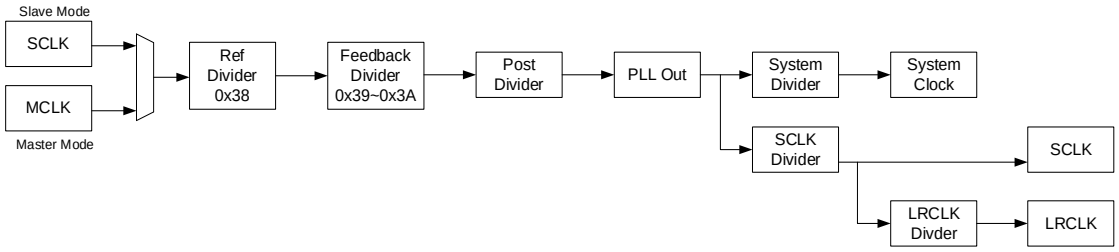


Figure 17. Audio Clock Generation

The device features robust clock error handing using a built-in trimmed oscillator clock to quickly detect changes or errors. Once the system detects a clock change or error, it will mute the audio and then force to PLL to limp mode by using the internal oscillator as a reference clock. Once the clock error dissapears, the system reverts to normal operation.

Input and Output MUX

The SQ58621 features two analog differential inputs, two differential outputs, and one single-ended output. Additionally, the SQ58621 has serial data input (SDIN) and serial data output (SDOUT).

For analog outputs, configure register 0x0B to set the output from either the DAC or the mic direct path. Note that OUT3 can only output DAC data.

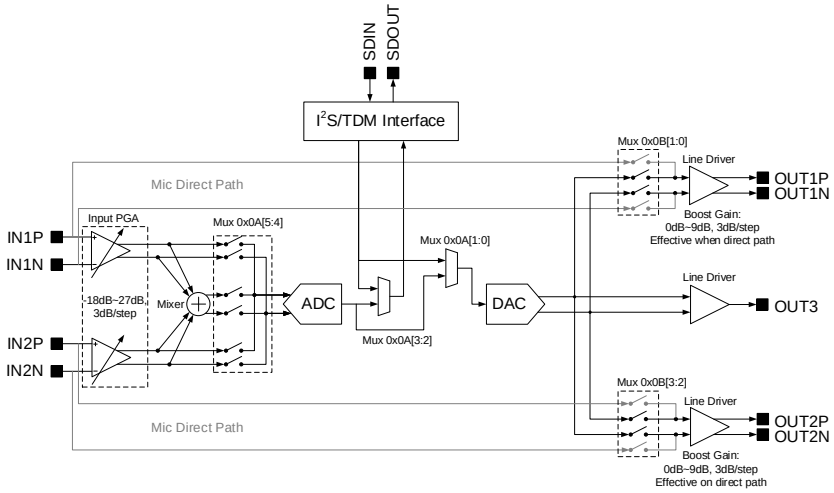


Figure 18. Input and Output MUX

Input PGA

The SQ58621 integrates an analog programmable gain amplifier (PGA) before the ADC. Depending on the input signal, configure registers 0x08~0x09 to set the appropriate gain to maximize the dynamic range. The input PGA offers a wide gain range from -18dB to 27dB in 3dB steps.

- To enable IN1 PGA, set 0x08[4], and to unmute IN1 PGA, set 0x4F[3].
- To enable IN2 PGA, set 0x09[4], and to unmute IN2 PGA, set 0x4F[2].

Adjust the PGA gain using 0x08[3:0] for IN1 and 0x09[3:0] for IN2.

Table 5. IN PGA Gain

0x08[3:0]	IN1 PGA Gain/dB	0x09[3:0]	IN2 PGA Gain/dB
4'hF	27	4'hF	27
4'hE	24	4'hE	24
4'hD	21	4'hD	21
4'hC	18	4'hC	18
4'hB	15	4'hB	15
4'hA	12	4'hA	12
4'h9	9	4'h9	9
4'h8	6	4'h8	6
4'h7	3	4'h7	3
4'h6	0	4'h6	0
4'h5	-3	4'h5	-3
4'h4	-6	4'h4	-6
4'h3	-9	4'h3	-9
4'h2	-12	4'h2	-12
4'h1	-15	4'h1	-15
4'h0	-18	4'h0	-18

When the mic direct path is disabled, the total input impedance is equal to $2R_{G1}$. When the mic direct path is enabled, the total input impedance is equal to $2R_{G1}$ and $2R_{G2}$ in parallel. The IN2 PGA structure and input impedance are identical to IN1.

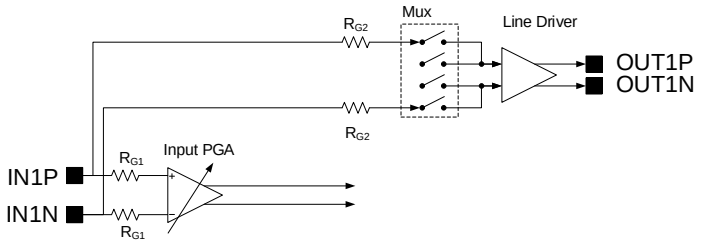


Figure 19. IN1 Structure

Table 6. Input PGA Gain and Impedance

IN1 PGA Gain/dB	Total R_{IN}/Ω	
	Mic Direct Path Disabled	Mic Direct Path Enabled
27	4000	3800
24	5554	5176
21	7662	6960
18	10476	9207
15	14157	11934
12	18846	15101
9	24617	18594

6	31431	22235
3	39092	25814
0	47244	29134
-3	55427	32052
-6	63173	34498
-9	70110	36468
-12	76019	38005
-15	80843	39173
-18	84646	40045

ADC Block

DC Filter

The ADC supports a fixed DC filter to remove harmonic content below 2Hz in the AC signal. Configure 0x0D [2] to enable or disable the DC filter.

Voice Filter

By configuring 0x0D [4:3], the voice filter of the ADC can be set to full band, wide band, or narrow band, with the stop band width decreasing successively.

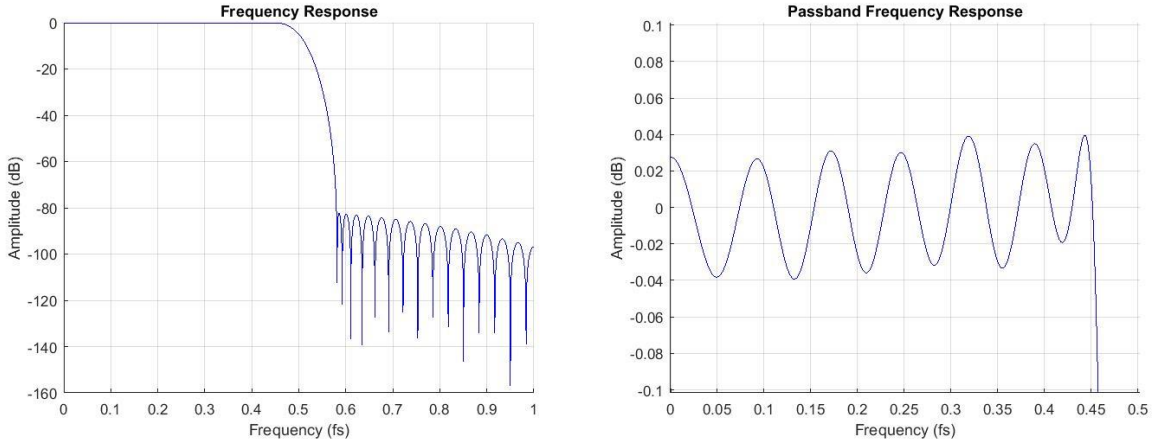


Figure 20. Full Band Filter Performance

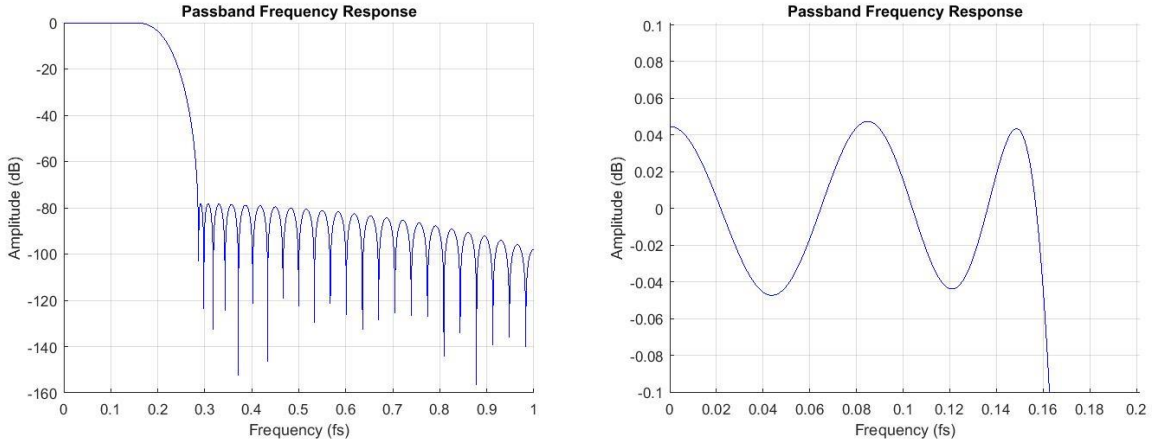


Figure 21. Wide Band Filter Performance

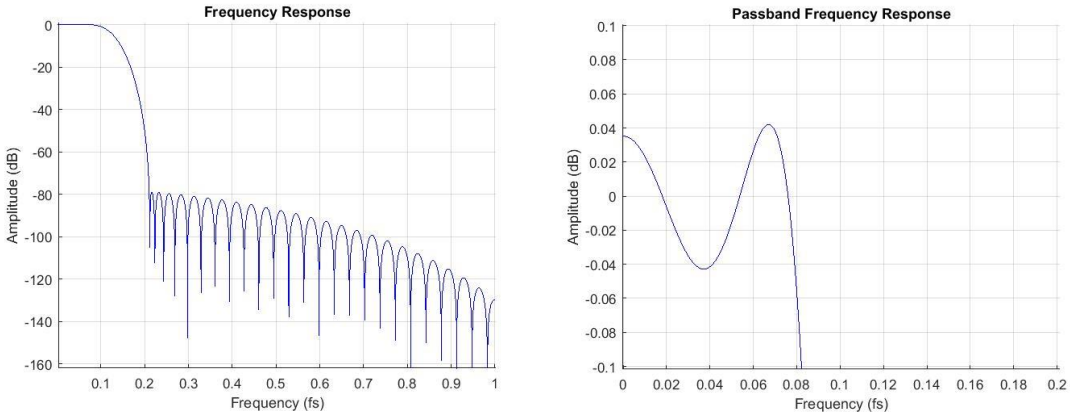


Figure 22. Narrow Band Filter Performance

Bi-Quad Structure

The SQ58621 has two Bi-Quad filters linked in series for each channel. These filters are configured using registers 0x0E~0x2B. Bi-Quad filters can be set to various filter types and combined with voice filters to form a bandpass filter.

Each Bi-quad has a 2nd IIR filter structure with three coefficients on the direct path (b0, b1, b2) and two coefficients on the feedback path (a1, a2), as shown in the diagram.

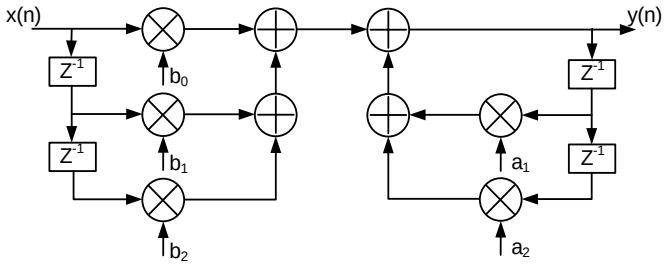


Figure 23. Bi-Quad Filter Structure

Digital Volume

The SQ58621 allows ADC volume configuration through register 0x2C. The ADC volume range is from -103dB to +24dB, adjustable in 0.5dB steps. Refer to Table 7 for the detailed volume settings.

Table 7. Digital Volume Setting

0x2C	Volume	0x2C	Volume	0x2C	Volume	0x2C	Volume	0x2C	Volume	0x2C	Volume
0xFF	24dB	0xD4	2.5dB	0xA9	-19dB	0x7E	-40.5dB	0x53	-62dB	0x28	-83.5dB
0xFE	23.5dB	0xD3	2dB	0xA8	-19.5dB	0x7D	-41dB	0x52	-62.5dB	0x27	-84dB
0xFD	23dB	0xD2	1.5dB	0xA7	-20dB	0x7C	-41.5dB	0x51	-63dB	0x26	-84.5dB
0xFC	22.5dB	0xD1	1dB	0xA6	-20.5dB	0x7B	-42dB	0x50	-63.5dB	0x25	-85dB
0xFB	22dB	0xD0	0.5dB	0xA5	-21dB	0x7A	-42.5dB	0x4F	-64dB	0x24	-85.5dB
0xFA	21.5dB	0xCF	0dB	0xA4	-21.5dB	0x79	-43dB	0x4E	-64.5dB	0x23	-86dB
0xF9	21dB	0xCE	-0.5dB	0xA3	-22dB	0x78	-43.5dB	0x4D	-65dB	0x22	-86.5dB
0xF8	20.5dB	0xCD	-1dB	0xA2	-22.5dB	0x77	-44dB	0x4C	-65.5dB	0x21	-87dB
0xF7	20dB	0xCC	-1.5dB	0xA1	-23dB	0x76	-44.5dB	0x4B	-66dB	0x20	-87.5dB
0xF6	19.5dB	0xCB	-2dB	0xA0	-23.5dB	0x75	-45dB	0x4A	-66.5dB	0x1F	-88dB
0xF5	19dB	0xCA	-2.5dB	0x9F	-24dB	0x74	-45.5dB	0x49	-67dB	0x1E	-88.5dB
0xF4	18.5dB	0xC9	-3dB	0x9E	-24.5dB	0x73	-46dB	0x48	-67.5dB	0x1D	-89dB
0xF3	18dB	0xC8	-3.5dB	0x9D	-25dB	0x72	-46.5dB	0x47	-68dB	0x1C	-89.5dB
0xF2	17.5dB	0xC7	-4dB	0x9C	-25.5dB	0x71	-47dB	0x46	-68.5dB	0x1B	-90dB
0xF1	17dB	0xC6	-4.5dB	0x9B	-26dB	0x70	-47.5dB	0x45	-69dB	0x1A	-90.5dB
0xF0	16.5dB	0xC5	-5dB	0x9A	-26.5dB	0x6F	-48dB	0x44	-69.5dB	0x19	-91dB
0xEF	16dB	0xC4	-5.5dB	0x99	-27dB	0x6E	-48.5dB	0x43	-70dB	0x18	-91.5dB

0xEE	15.5dB	0xC3	-6dB	0x98	-27.5dB	0x6D	-49dB	0x42	-70.5dB	0x17	-92dB
0xED	15dB	0xC2	-6.5dB	0x97	-28dB	0x6C	-49.5dB	0x41	-71dB	0x16	-92.5dB
0xEC	14.5dB	0xC1	-7dB	0x96	-28.5dB	0x6B	-50dB	0x40	-71.5dB	0x15	-93dB
0xEB	14dB	0xC0	-7.5dB	0x95	-29dB	0x6A	-50.5dB	0x3F	-72dB	0x14	-93.5dB
0xEA	13.5dB	0xBF	-8dB	0x94	-29.5dB	0x69	-51dB	0x3E	-72.5dB	0x13	-94dB
0xE9	13dB	0xBE	-8.5dB	0x93	-30dB	0x68	-51.5dB	0x3D	-73dB	0x12	-94.5dB
0xE8	12.5dB	0xBD	-9dB	0x92	-30.5dB	0x67	-52dB	0x3C	-73.5dB	0x11	-95dB
0xE7	12dB	0xBC	-9.5dB	0x91	-31dB	0x66	-52.5dB	0x3B	-74dB	0x10	-95.5dB
0xE6	11.5dB	0xBB	-10dB	0x90	-31.5dB	0x65	-53dB	0x3A	-74.5dB	0x0F	-96dB
0xE5	11dB	0xBA	-10.5dB	0x8F	-32dB	0x64	-53.5dB	0x39	-75dB	0x0E	-96.5dB
0xE4	10.5dB	0xB9	-11dB	0x8E	-32.5dB	0x63	-54dB	0x38	-75.5dB	0x0D	-97dB
0xE3	10dB	0xB8	-11.5dB	0x8D	-33dB	0x62	-54.5dB	0x37	-76dB	0x0C	-97.5dB
0xE2	9.5dB	0xB7	-12dB	0x8C	-33.5dB	0x61	-55dB	0x36	-76.5dB	0x0B	-98dB
0xE1	9dB	0xB6	-12.5dB	0x8B	-34dB	0x60	-55.5dB	0x35	-77dB	0x0A	-98.5dB
0xE0	8.5dB	0xB5	-13dB	0x8A	-34.5dB	0x5F	-56dB	0x34	-77.5dB	0x09	-99dB
0xDF	8dB	0xB4	-13.5dB	0x89	-35dB	0x5E	-56.5dB	0x33	-78dB	0x08	-99.5dB
0xDE	7.5dB	0xB3	-14dB	0x88	-35.5dB	0x5D	-57dB	0x32	-78.5dB	0x07	-100dB
0xDD	7dB	0xB2	-14.5dB	0x87	-36dB	0x5C	-57.5dB	0x31	-79dB	0x06	-100.5dB
0xDC	6.5dB	0xB1	-15dB	0x86	-36.5dB	0x5B	-58dB	0x30	-79.5dB	0x05	-101dB
0xDB	6dB	0xB0	-15.5dB	0x85	-37dB	0x5A	-58.5dB	0x2F	-80dB	0x04	-101.5dB
0xDA	5.5dB	0xAF	-16dB	0x84	-37.5dB	0x59	-59dB	0x2E	-80.5dB	0x03	-102dB
0xD9	5dB	0xAE	-16.5dB	0x83	-38dB	0x58	-59.5dB	0x2D	-81dB	0x02	-102.5dB
0xD8	4.5dB	0xAD	-17dB	0x82	-38.5dB	0x57	-60dB	0x2C	-81.5dB	0x01	-103dB
0xD7	4dB	0xAC	-17.5dB	0x81	-39dB	0x56	-60.5dB	0x2B	-82dB	0x00	MUTE
0xD6	3.5dB	0xAB	-18dB	0x80	-39.5dB	0x55	-61dB	0x2A	-82.5dB		
0xD5	3dB	0xAA	-18.5dB	0x7F	-40dB	0x54	-61.5dB	0x29	-83dB		

DAC Block

DAC Filter

The user can select either a sharp roll-off band or a slow roll-off band filter by configuring 0x0D[5]. The sharp roll-off band filter has a faster attenuation slope from the pass band to the stop band compared to the slow roll-off filter.

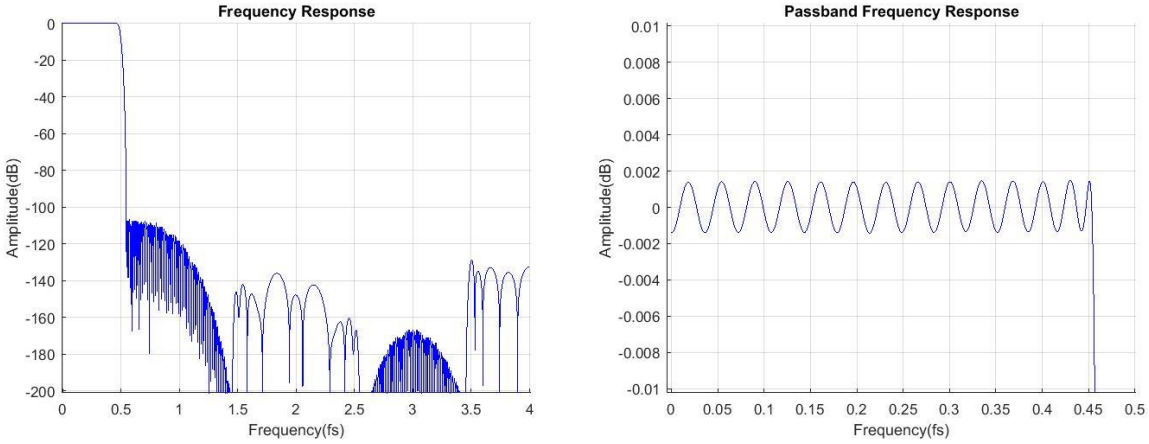


Figure 24. Sharp Roll-Off Filter Performance

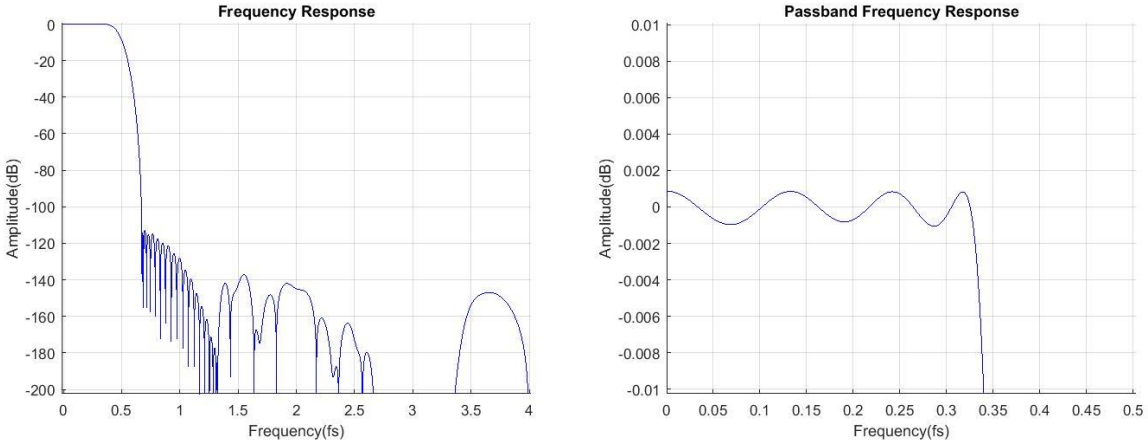


Figure 25. Slow Roll-Off Filter Performance

Digital Volume

The SQ58621 allows DAC volume configuration through register 0x2D. The DAC volume range is from -115dB to +12dB, adjustable in 0.5dB steps. Refer to Table 8 for the detailed volume settings.

Table 8. Digital Volume Setting

0x2D	Volume	0x2D	Volume	0x2D	Volume	0x2D	Volume	0x2D	Volume	0x2D	Volume
0xFF	12dB	0xD4	-9.5dB	0xA9	-31dB	0x7E	-52.5dB	0x53	-74dB	0x28	-95.5dB
0xFE	11.5dB	0xD3	-10dB	0xA8	-31.5dB	0x7D	-53dB	0x52	-74.5dB	0x27	-96dB
0xFD	11dB	0xD2	-10.5dB	0xA7	-32dB	0x7C	-53.5dB	0x51	-75dB	0x26	-96.5dB
0xFC	10.5dB	0xD1	-11dB	0xA6	-32.5dB	0x7B	-54dB	0x50	-75.5dB	0x25	-97dB
0xFB	10dB	0xD0	-11.5dB	0xA5	-33dB	0x7A	-54.5dB	0x4F	-76dB	0x24	-97.5dB
0xFA	9.5dB	0xCF	-12dB	0xA4	-33.5dB	0x79	-55dB	0x4E	-76.5dB	0x23	-98dB
0xF9	9dB	0xCE	-12.5dB	0xA3	-34dB	0x78	-55.5dB	0x4D	-77dB	0x22	-98.5dB
0xF8	8.5dB	0xCD	-13dB	0xA2	-34.5dB	0x77	-56dB	0x4C	-77.5dB	0x21	-99dB
0xF7	8dB	0xCC	-13.5dB	0xA1	-35dB	0x76	-56.5dB	0x4B	-78dB	0x20	-99.5dB
0xF6	7.5dB	0xCB	-14dB	0xA0	-35.5dB	0x75	-57dB	0x4A	-78.5dB	0x1F	-100dB
0xF5	7dB	0xCA	-14.5dB	0x9F	-36dB	0x74	-57.5dB	0x49	-79dB	0x1E	-100.5dB
0xF4	6.5dB	0xC9	-15dB	0x9E	-36.5dB	0x73	-58dB	0x48	-79.5dB	0x1D	-101dB
0xF3	6dB	0xC8	-15.5dB	0x9D	-37dB	0x72	-58.5dB	0x47	-80dB	0x1C	-101.5dB
0xF2	5.5dB	0xC7	-16dB	0x9C	-37.5dB	0x71	-59dB	0x46	-80.5dB	0x1B	-102dB
0xF1	5dB	0xC6	-16.5dB	0x9B	-38dB	0x70	-59.5dB	0x45	-81dB	0x1A	-102.5dB
0xF0	4.5dB	0xC5	-17dB	0x9A	-38.5dB	0x6F	-60dB	0x44	-81.5dB	0x19	-103dB
0xEF	4dB	0xC4	-17.5dB	0x99	-39dB	0x6E	-60.5dB	0x43	-82dB	0x18	-103.5dB
0xEE	3.5dB	0xC3	-18dB	0x98	-39.5dB	0x6D	-61dB	0x42	-82.5dB	0x17	-104dB
0xED	3dB	0xC2	-18.5dB	0x97	-40dB	0x6C	-61.5dB	0x41	-83dB	0x16	-104.5dB
0xEC	2.5dB	0xC1	-19dB	0x96	-40.5dB	0x6B	-62dB	0x40	-83.5dB	0x15	-105dB
0xEB	2dB	0xC0	-19.5dB	0x95	-41dB	0x6A	-62.5dB	0x3F	-84dB	0x14	-105.5dB
0xEA	1.5dB	0xBF	-20dB	0x94	-41.5dB	0x69	-63dB	0x3E	-84.5dB	0x13	-106dB
0xE9	1dB	0xBE	-20.5dB	0x93	-42dB	0x68	-63.5dB	0x3D	-85dB	0x12	-106.5dB
0xE8	0.5dB	0xBD	-21dB	0x92	-42.5dB	0x67	-64dB	0x3C	-85.5dB	0x11	-107dB
0xE7	0dB	0xBC	-21.5dB	0x91	-43dB	0x66	-64.5dB	0x3B	-86dB	0x10	-107.5dB
0xE6	-0.5dB	0xBB	-22dB	0x90	-43.5dB	0x65	-65dB	0x3A	-86.5dB	0x0F	-108dB
0xE5	-1dB	0xBA	-22.5dB	0x8F	-44dB	0x64	-65.5dB	0x39	-87dB	0x0E	-108.5dB
0xE4	-1.5dB	0xB9	-23dB	0x8E	-44.5dB	0x63	-66dB	0x38	-87.5dB	0x0D	-109dB
0xE3	-2dB	0xB8	-23.5dB	0x8D	-45dB	0x62	-66.5dB	0x37	-88dB	0x0C	-109.5dB
0xE2	-2.5dB	0xB7	-24dB	0x8C	-45.5dB	0x61	-67dB	0x36	-88.5dB	0x0B	-110dB

0xE1	-3dB	0xB6	-24.5dB	0x8B	-46dB	0x60	-67.5dB	0x35	-89dB	0x0A	-110.5dB
0xE0	-3.5dB	0xB5	-25dB	0x8A	-46.5dB	0x5F	-68dB	0x34	-89.5dB	0x09	-111dB
0xDF	-4dB	0xB4	-25.5dB	0x89	-47dB	0x5E	-68.5dB	0x33	-90dB	0x08	-111.5dB
0xDE	-4.5dB	0xB3	-26dB	0x88	-47.5dB	0x5D	-69dB	0x32	-90.5dB	0x07	-112dB
0xDD	-5dB	0xB2	-26.5dB	0x87	-48dB	0x5C	-69.5dB	0x31	-91dB	0x06	-112.5dB
0xDC	-5.5dB	0xB1	-27dB	0x86	-48.5dB	0x5B	-70dB	0x30	-91.5dB	0x05	-113dB
0xDB	-6dB	0xB0	-27.5dB	0x85	-49dB	0x5A	-70.5dB	0x2F	-92dB	0x04	-113.5dB
0xDA	-6.5dB	0xAF	-28dB	0x84	-49.5dB	0x59	-71dB	0x2E	-92.5dB	0x03	-114dB
0xD9	-7dB	0xAE	-28.5dB	0x83	-50dB	0x58	-71.5dB	0x2D	-93dB	0x02	-114.5dB
0xD8	-7.5dB	0xAD	-29dB	0x82	-50.5dB	0x57	-72dB	0x2C	-93.5dB	0x01	-115dB
0xD7	-8dB	0xAC	-29.5dB	0x81	-51dB	0x56	-72.5dB	0x2B	-94dB	0x00	MUTE
0xD6	-8.5dB	0xAB	-30dB	0x80	-51.5dB	0x55	-73dB	0x2A	-94.5dB		
0xD5	-9dB	0xAA	-30.5dB	0x7F	-52dB	0x54	-73.5dB	0x29	-95dB		

Output Current Limit

The SQ58621 includes an output stage current limit function. The output stage current is sensed and compared with a reference current (i_{ref}). If the output current exceeds i_{ref}, it will be limited to i_{ref}. This features protects the DAC output stage by limiting the output current in case of an accidental short.

The limited output current can be selected using register 0x4C[4:3] for the current limit ratio and 0x4C[2:1] for the current limit base. The output stage current limit function can be enabled through register 0x4C[7], which is disabled by default.

Line Driver

Boost Gain

To compensate for signal attenuation and drive strength for long-distance transmission from the microphone to the head unit, the SQ58621 integrates an output line driver with a 0~9dB boost gain.

Table 9. Line Driver Boost Gain

0x0C[5:3]	Line Driver 1 Boost Gain	0x0C[2:0]	Line Driver 2 Boost Gain
3'd0	-40dB	3'd0	-40dB
3'd1	0dB	3'd1	0dB
3'd2	3dB	3'd2	3dB
3'd3	6dB	3'd3	6dB
3'd4	9dB	3'd4	9dB
Others	NA	Others	NA

When the output line driver is used for DAC output, the gain is fixed at 0dB, regardless of any gain settings, ensuring that the DAC output is not affected.

I²C Bus Interface

The SQ58621 features a bidirectional I²C interface compatible with the I²C bus protocol, supporting 100kHz and 400kHz data transfer rates for writing and reading operations. The device does not support multi-controller bus configurations or wait state insertion. The I²C control is used to program the device registers and read the device status. Refer to the following figures for detailed write and read transfer operations.

The SQ58621 has a 7-bit target address, defaulting to 0x4C, which can be read from register 0xF7[6,0]. After powering up the device, the I²C target address change can be enabled by writing the value F9A5A5A5 to registers 0xF8~0xFB. Subsequently, the I²C target address can be changed to any value from 0x00 to 0x7F by writing to register 0xF7[6,0]. The I²C target address resets to 0x4C after the device powers down.

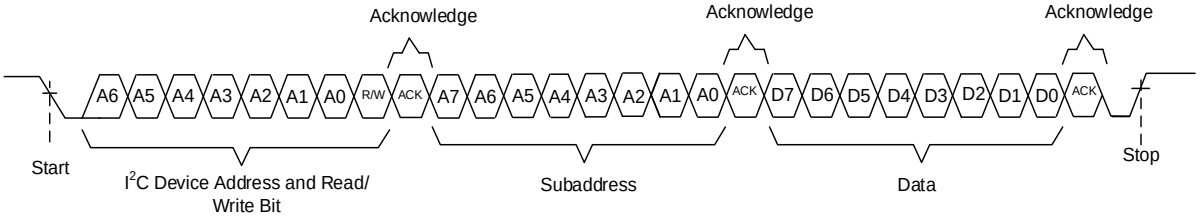


Figure 26. Write Transfer

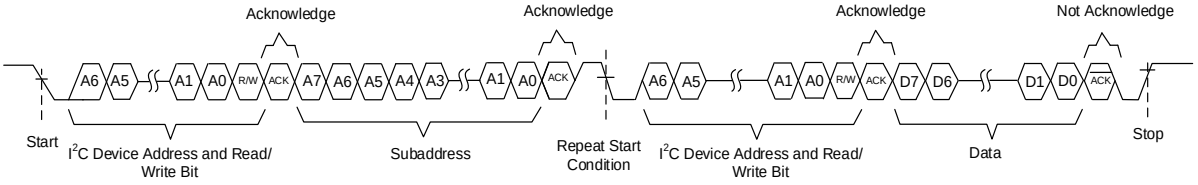


Figure 27. Read Transfer

IO Control

PDN

PDN is the shutdown control pin for the SQ58621. When PDN is pulled up, the internal LDO activates, powering the SQ58621 and making the I²C ready for use. However, when PDN is pulled down, the entire device shuts down, the internal LDO is disabled, and the I²C is inaccessible.

Monitor

MON is a multiple-function pin. During startup, MON is an input pin to set the controller/target mode. When MON is pulled up, the SQ58621 is in controller mode, and when MON is pulled down, it is in target mode. After startup, the status of the SQ58621 will be latched up. By configuring 0x2F, MON can be set as an output pin for error out or SDOUT. As error out, MON is high when an error occurs. Through 0x34[3:2], choose the error displayed on MON.

Mute and Fade

The SQ58621 can mute or unmute the ADC and DAC blocks by configuring 0x2E[5] and 0x2E[1], respectively. During the mute/unmute or volume change process, the SQ58621 supports digital fade for smooth volume adjustment, allowing for audio fade-in and fade-out effects. The digital fade function for the ADC and DAC can be enabled or disabled independently through 0x31[1:0].

$$\text{fade time} = \text{fade step} \times \text{fade speed}$$

$$\text{fade step} = \Delta\text{volume}/0.5\text{dB}$$

For example, if the DAC digital volume is currently 0dB and changes to -10dB, the change in volume (Δvolume) is calculated as:

$$\Delta\text{volume} = 0\text{dB} - (-10\text{dB}) = 10\text{dB}$$

With a fade step size of 0.5dB, the number of fade steps required is:

$$\text{fade steps} = 10\ \text{dB}/0.5\text{dB} = 20$$

The fade speed can be set using 0x31[3:2] and is dependent on the sampling frequency (f_S).

Table 10. Fade Speed Setting

0x31[3:2]	Fade Speed	Unit
00	$2/f_S$	per step
01	$4/f_S$	per step
10	$8/f_S$	per step
11	$16/f_S$	per step

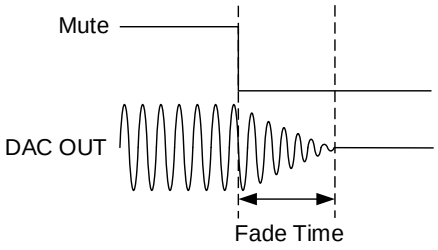


Figure 28. Fade Process Example

Amute is an automatic mute process. When 0x36[4:1] is configured, the following conditions will trigger Amute: MCLK halt, asynchronous detection, zero detection, DAC disable command, and DAC SRAM error. Upon triggering Amute, the analog output is set to VCOM to avoid noise.

Detection

SQ58621 detection includes SDIN zero input detection, SRAM ecc multiple bites error detection, clock error detection(includes SCLK stop error, SCLK error, LRCLK error and MCLK stop error). After setting MON as error out, SQ58621 should choose what displays on monitor pin. When 0x34[2] enabled, SDIN zero input detection result will display on monitor pin. When 0x32[3] enabled, errorout(includes ADC SRAM ecc multi error, DAC SRAM ecc multi error, SCLK stop error, SCLK error, LRCLK error and MCLK stop error) will display on monitor pin. Or read 0x52 and 0x53 to get the detection results. In target mode, MCLK stop error needs to be ignored, disabled 0x33[3] and it won't display on monitor pin, also on 0x53[4]. If 0x33[2] is disabled, SCLK error won't display on monitor pin, also on 0x53[5]. Among these detection, SCLK error and MCLK stop error detection results will remain on monitor pin and 0x53 though the two kinds of error disappear, so it's necessary to write 1'b1 to 0x32[1] to update detection results.

Table 11. Error Status Clear

Address	Bit	Label	Access	Default	Description
0x32	7:1	N/A	R	7'h00	Reserved
	0	fault_clr	WO	1'b0	Write 1'b1 to clear the fault flag, and the fault_clr register value will return to 1'b0 automatically

Table 12. Error Display Selection

Address	Bit	Label	Access	Default	Description
0x33	7:4	N/A	R	4'h0	Reserved
	3	mclk_stop_err_en	RW	1'b1	MCLK stop error displays on 0x53[4] and error out, MCLK stop error results in amute_cfg_0 1'b0: Disable 1'b1: Enable
	2	sclk_err_en	RW	1'b1	SCLK error displays on 0x53[5] and error out, SCLK error results in amute_cfg_1 1'b0: Disable 1'b1: Enable
	1	mclk_err_en	RW	1'b1	MCLK stop error results in amute_cfg_1 1'b0: Disable 1'b1: Enable
	0	bist_fail_shutdwn_en	RW	1'b1	1'b0: Disable bist fail shutdown 1'b1: Enable bist fail shutdown

Table 13. Error Flag Setting

Address	Bit	Label	Access	Default	Description
0x34	7:4	N/A	R	3'b000	Reserved
	3	errout_en	RW	1'b0	Include SRAM error, SCLK error, MCLK error 1'b0: Disable error display on error flag signal 1'b1: Enable error display on error flag signal
	2	zero_out_en	RW	1'b1	1'b0: Disable zero flag display on error flag signal 1'b1: Enable zero flag display on error flag signal

	1	sram_err_mute_en	RW	1'b1	1'b0: Disable SRAM error to mute DAC dsp 1'b1: Enable SRAM error to mute DAC dsp
	0	ecc_err_mute_en	RW	1'b0	1'b0: Disable SRAM ecc error to mute DAC dsp 1'b1: Enable SRAM ecc error to mute DAC dsp

Table 14. Zero Input Indicator Register

Address	Bit	Label	Access	Default	Description
0x52	7:1	N/A	R	7'h00	Reserved
	0	zero_flag_clk_cross	R	1'b0	SDIN zero input detection result 1'b0: SDIN has input 1'b1: SDIN zero input

Table 15. Error Indicator Register

Address	Bit	Label	Access	Default	Description
0x53	7	dac_sram_ecc_mulit_err	R	1'b0	DAC sram ecc multi error
	6	adc_sram_ecc_multi_err	R	1'b0	ADC sram ecc multi error
	5	sclk_err_fault	R	1'b0	SCLK not stable error
	4	mclk_stop_err_fault	R	1'b0	MCLK stop error
	3:2	N/A	R	2'b00	Researved
	1	sclk_stop_err_flag	R	1'b0	SCLK stop error
	0	lrclk_err_fault	R	1'b0	LRCLK stop or not stable error

Zero Detection

If the SDIN input data remains at '0' for 20ms, the zero input will be detected. After the zero input is detected, the event can be signaled on the monitor pin when configured as error output. Once data is input into SDIN again, the error flag disappears immediately. Zero data detection is supported for 16, 20, 24, and 32-bit data widths.

SCLK Stop Error Detection

There is a window in the clock error detection block for counting SCLK. If the counted value is 0, it will report an SCLK stop error. In target mode, when the SCLK stop error appears, the reference clock will switch to the internal oscillator automatically, until SCLK recovers and the error disappears.

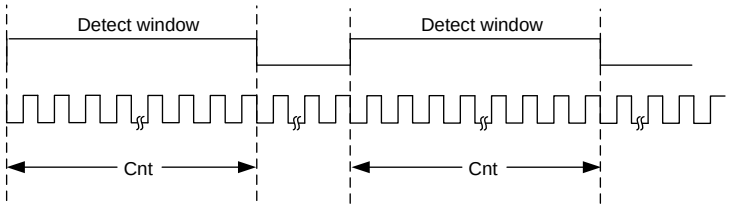


Figure 29. SCLK Stop Error Detection

SCLK Error Detection

The clock error detection block will count the SCLK pulses in each LRCLK frame. If Csn≠Csn+1 or Cs is out of range(meaning LRCLK is stop), an SCLK error is detected. In target mode, when an SCLK error occurs, the reference clock automatically switches to the internal OSC. Once the SCLK recovers and the error disappears, the reference clock switches back to SCLK. If an SCLK error occurs in target mode and the ADC or DAC are enabled from a disabled state via register 0x2E, both the ADC and DAC will produce no output.

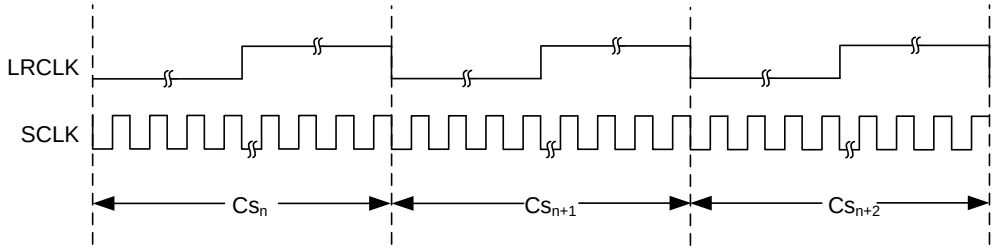


Figure 30. SCLK Error Detection

LRCLK Error Detection

The clock error detection block will count the oscillator clk pulses in each LRCLK frame. If Csn≠Csn+1 or Cs is out of range(meaning LRCLK is stop), an LRCLK error is detected .In target mode, when the LRCLK error appears, the reference clock will switch to the internal oscillator automatically, until LRCLK recovers and the error disappears.

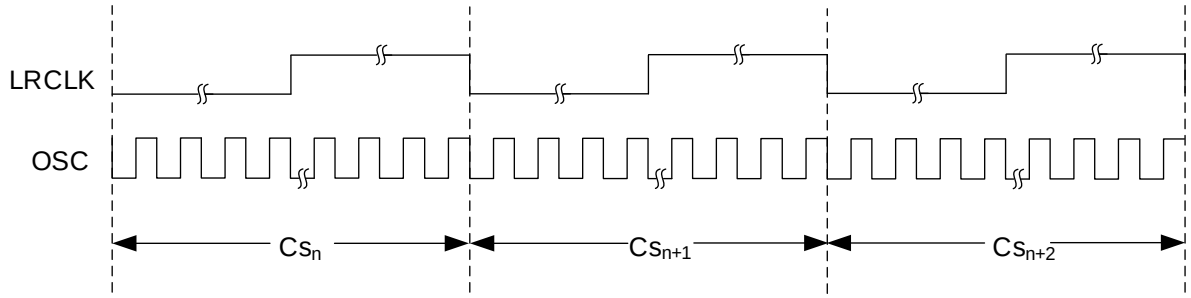


Figure 31 LRCLK Error Detection

MCLK Stop Error Detection

There is a window in the clock error detection block for counting MCLK. If the counted value is 0, it will report an MCLK stop error. In controller mode, when the MCLK stop error appears, the reference clock will switch to the internal oscillator automatically, until MCLK recovers and the error disappears.

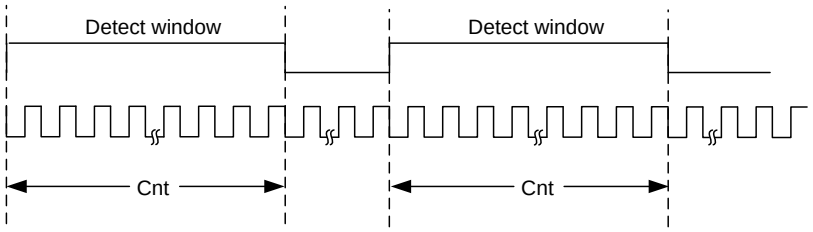


Figure 32. MCLK Stop Error Detection

SRAM Error

SRAM error detection is based on ECC (Error Correcting Code), an algorithm developed based on the published Single Error Correct-Double Error Detect (SECDED) algorithm using Hamming code. ECC provides automatic error detection and correction. In this design, six parity bits are added to the data word when writing to memory. These parity bits allow the detection of both single and double data errors when reading from memory. A single bit data error can be corrected, while a double bit error cannot be corrected and will be reported.

Power Up and Down Sequence

Recommended Power-Up Timing

The recommended power-up timing is shown in Figure 33:

1. Connect MON to DVDD through a 10kΩ resistor for controller mode or to GND for target mode.
2. Supply DVDD and AVDD; there are no timing constraints between these two supplies.
3. Once AVDD and DVDD reach their operating voltages, there are no timing constraints for pulling PDN high and providing the necessary clocks.
4. Wait at least 20ms, then download the initialization settings via I2C. After this, the SQ58621 will enter normal operation mode.

Recommended Power-Down Timing

The recommended power-down timing is shown in Figure 33:

1. Enter shutdown mode via I^2C.
2. After the fade process completes (fade time=fade step * fade speed, fade step = Δvolume/0.5dB), wait another 10ms, then pull down PDN and stop external clocks.

3. After at least 10ms, ramp down AVDD and DVDD.

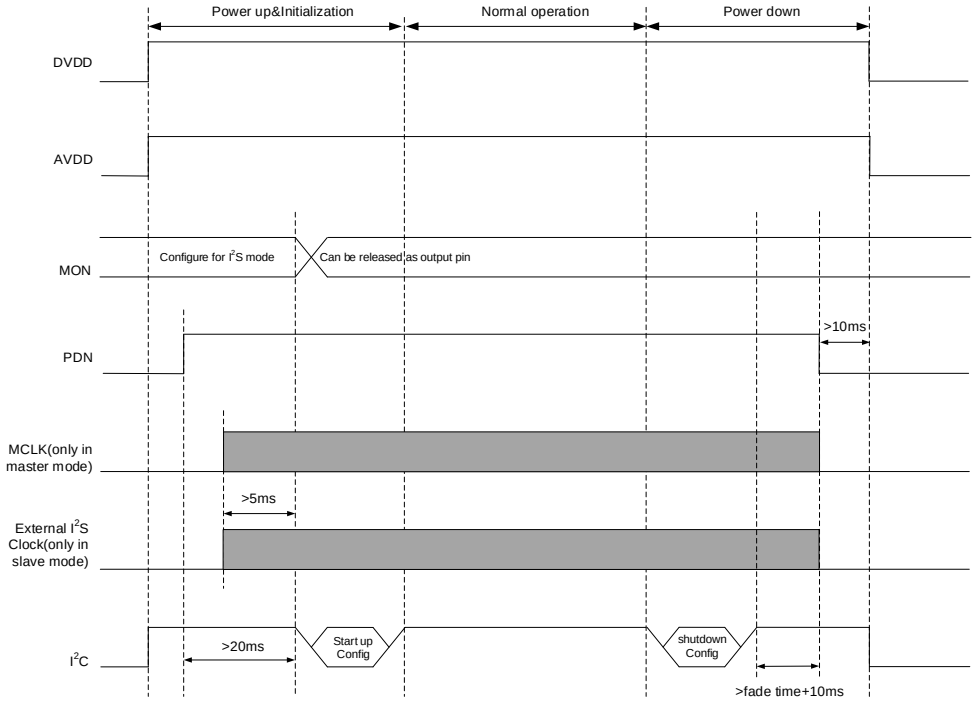


Figure 33. Recommended Power Up and Down Timing

Recommended Software Initialization

The recommended software initialization of emergency mode is as follows:

Emergency mode initialization *(Sequence number, Command, Target address, Register, Data, Annotation)*

1.	*Write 0x98 0x33 0x05*	*// Disable MCLK error and MCLK stop error processing in target mode (must be skipped in controller mode)*
2.	*Write 0x98 0x03 0x00*	*// Set fs base and MCLK/Crystal frequency in controller mode (can be skipped if in target mode)*
3.	*Write 0x98 0x04 0xB3*	*// Configure fs manually.*
4.	*Write 0x98 0x05 0x84*	*// I2S format (can be skipped if in default). 0x84: I2S standard mode, 24-bit data length, 32-bit slot length*
5.	*Write 0x98 0x06 0x00*	*// I2S format (can be skipped if in default).*
6.	*Write 0x98 0x07 0x00*	*// SDIN, SDOUT slot assign (can be skipped if in default), 0x00: SDIN Slot 1 to DAC, ADC to Slot 1 of SDOUT*
7.	*Write 0x98 0x0B 0x10*	*// Set line driver output mux. 0x10: OUT1 and OUT2 no outputs, DAC to OUT3*
8.	*Write 0x98 0x0A 0x20*	*// Set ADC input mux. 0x20: IN1 PGA to ADC.*
9.	*Write 0x98 0x08 0x16*	*// Enable IN1 PGA and set the PGA gain. 0x16: IN1PGA enabled, PGA gain 0dB*
10.	*Write 0x98 0x09 0x16*	*// Enable IN2 PGA and set the PGA gain. 0x16: IN1PGA enabled, PGA gain 0dB*
11.	*Write 0x98 0x4F 0x00*	*// Unmute IN PGA*
12.	*Wait 10us*	*// Delay 10μs*
13.	*Write 0x98 0x2E 0x11*	*// Enable and unmute ADC and DAC*

The recommended software initialization of non-emergency mode is as follows:

Non-emergency mode initialization *(Sequence number, Command, Target address, Register, Data, Annotation)*

1. Write 0x98 0x0B 0x05 // Set line driver output mux. 0x05: IN1 to OUT1, IN2 to OUT2, OUT3 no output.

2. Write 0x98 0x0C 0x09 // Set line driver gain, 0x09: Line driver 1 and line driver 2 gain 0dB.

When changing the operation mode from emergency mode to non-emergency mode or from non-emergency mode to emergency mode, change the blue marked commands of each sequence.

					3'b001	16kHz	
					3'b010	32kHz	
					3'b011	48kHz	44.1kHz
					3'b100	96kHz	88.2kHz
					Others	NA	NA
	3	sysclk_mode_sel	R	1'b0	Indicate SQ58621 status: 1'b1: Controller mode 1'b0: Target mode		
	2:0	auto_detected_fs_rate	R	3'b011	Auto detected sampling rate		
					fs_rate_cfg	48kHz base	44.1kHz base
					3'b000	8kHz	
					3'b001	16kHz	
					3'b010	32kHz	
					3'b011	48kHz	44.1kHz
					3'b100	96kHz	88.2kHz
					Others	NA	NA

Address	Bit	Label	Access	Default	Description
0x05	7	serial_data_stream_enable	RW	1'b1	1'b0: Disable serial data stream 1'b1: Enable serial data stream
	6	serial_data_stream_mode	RW	1'b0	1'b0: I^{2}S mode 1'b1: TDM mode
	5:4	serial_data_stream_format	RW	2'b00	2'b00: I^{2}S standard 2'b01: Left-justified 2'b10: Right-justified 2'b11: Reserved
	3:2	serial_data_stream_data_length	RW	2'b01	2'b00: 32-bit 2'b01: 24-bit 2'b10: 20-bit 2'b11: 16-bit
	1:0	serial_data_stream_slot_width	RW	2'b00	2'b00: 32-bit 2'b01: 24-bit 2'b10: 16-bit 2'b11: Reserved

Address	Bit	Label	Access	Default	Description
0x06	7:5	N/A	R	2'b00	Reserved
	4:3	serial_data_stream_slot_sel	RW	2'b00	2'b00: TDM – 4 slots 2'b01: TDM – 8 slots 2'b10: TDM – 16 slots
	2	serial_data_lrclk_shift (Note 2)	RW	1'b0	1'b0: Not shift left LRCLK 1'b1: Shift left LRCLK by one bit
	1	serial_data_lrclk_invert (Note 2)	RW	1'b0	1'b0: Not invert LRCLK 1'b1: Invert LRCLK
	0	serial_data_sclk_invert	RW	1'b0	1'b0: Not invert SCLK 1'b1: Invert SCLK

Address	Bit	Label	Access	Default	Description
0x07	7:6	i2s_sdin_selection	RW	2'b00	SDIN channel selection: 2'b00: Left channel only 2'b01: Right channel only 2'b10: 1/2(left + right)
	5:3	sdin_slot_assign	RW	3'b000	SDIN slot assignment: 3'b000: Slot 0,1 3'b001: Slot 2,3 3'b010: Slot 4,5 3'b011: Slot 6,7 3'b100: Slot 8,9

					3'b101: Slot 10,11 3'b110: Slot 12,13 3'b111: Slot 14,15
	2:0	sdout_slot_assign	RW	3'b000	SDOUT slot assignment: 3'b000: Slot 0,1 3'b001: Slot 2,3 3'b010: Slot 4,5 3'b011: Slot 6,7 3'b100: Slot 8,9 3'b101: Slot 10,11 3'b110: Slot 12,13 3'b111: Slot 14,15

Address	Bit	Label	Access	Default	Description	
0x08	7:5	NA	R	3'b000	Reserved	
	4	in1_pga_en	RW	1'b0	1'b0: Disable IN1 PGA 1'b1: Enable IN1 PGA	
	3:0	in1_pga_gain	RW	4'h0	Value	PGA gain
					4'h0	-18dB
					4'h1	-15dB
					4'h2	-12dB
					4'h3	-9dB
					4'h4	-6dB
					4'h5	-3dB
					4'h6	0dB
					4'h7	3dB
					4'h8	6dB
					4'h9	9dB
					4'hA	12dB
					4'hB	15dB
					4'hC	18dB
					4'hD	21dB
					4'hE	24dB
					4'hF	27dB

Address	Bit	Label	Access	Default	Description	
0x09	7:5	NA	R	3'b000	Reserved	
	4	in2_pga_en	RW	1'b0	1'b0: Disable IN2 PGA 1'b1: Enable IN2 PGA	
	3:0	in2_pga_gain	RW	4'h0	Value	PGA gain
					4'h0	-18dB
					4'h1	-15dB
					4'h2	-12dB
					4'h3	-9dB
					4'h4	-6dB
					4'h5	-3dB
					4'h6	0dB
					4'h7	3dB
					4'h8	6dB
					4'h9	9dB
					4'hA	12dB
					4'hB	15dB
					4'hC	18dB
					4'hD	21dB

					4'hE	24dB
					4'hF	27dB

Address	Bit	Label	Access	Default	Description
0x0A	7:6	NA	R	2'b00	Reserved
	5:4	adc_input_mux	RW	2'b00	ADC input selection: 2'b00: None to ADC input 2'b01: IN2 to ADC input 2'b10: IN1 to ADC input 2'b11: Mixer to ADC input
	3:2	i2s_output_mux	RW	2'b00	SDOUT output selection: 2'b00: ADC out to I2S out 2'b01: I^2S in to I2S out 2'b10: None to I2S out 2'b11: Reserved
	1:0	dac_input_mux	RW	2'b00	DAC input selection: 2'b00: I^2S in to DAC input 2'b01: ADC out to DAC input 2'b10: None to DAC input 2'b11: Reserved

Address	Bit	Label	Access	Default	Description
0x0B	7:5	NA	RW	3'b000	Reserved
	4	output_line_driver3_mux	RW	1'b0	OUT3 output selection: 1'b0: Vcom 1'b1: DAC output path
	3:2	output_line_driver2_mux	RW	2'b00	OUT2 output selection: 2'b00: Vcom 2'b01: Mic direct path(IN2 direct to OUT2) 2'b10: DAC output path 2'b11: Reserved
	1:0	output_line_driver1_mux	RW	2'b00	OUT1 output selection: 2'b00: Vcom 2'b01: Mic direct path(IN1 direct to OUT1) 2'b10: DAC output path 2'b11: Reserved

Address	Bit	Label	Access	Default	Description
0x0C (Note 3)	7:6	NA	R	2'b00	Reserved
	5:3	output_line_driver1_gain	RW	3'b000	3'b000: -40dB 3'b001: 0dB 3'b010: 3dB 3'b011: 6dB 3'b100: 9dB Others: NA
	2:0	output_line_driver2_gain	RW	3'b000	3'b000: -40dB 3'b001: 0dB 3'b010: 3dB 3'b011: 6dB 3'b100: 9dB Others: NA

Address	Bit	Label	Access	Default	Description
0x0D	7:6	N/A	R	2'b00	Reserved
	5	dac_filter_sel	RW	1'b0	1'b0: Sharp roll-off 1'b1: Slow roll-off
	4:3	adc_voice_filter_sel	RW	2'b00	2'b00: Full band 2'b01: Wide band 2'b10/2'b11: Narrow band

	2	adc_dc_disable	RW	1'b0	1'b0: Enable ADC dc removal filter and adc dc calculation 1'b1: Disable ADC dc removal filter and adc dc calculation
	1	adc_eq1_en	RW	1'b0	1'b0: Disable equalizer filter 1 1'b1: Enable equalizer filter 1
	0	adc_eq0_en	RW	1'b0	1'b0: Disable equalizer filter 0 1'b1: Enable equalizer filter 0

Address	Bit	Label	Access	Default	Description
0x0E	7:0	bq0_b0[23:16]	RW	8'h40	Parameters of the equalization filter
0x0F	7:0	bq0_b0[15:8]	RW	8'h00	Parameters of the equalization filter
0x10	7:0	bq0_b0[7:0]	RW	8'h00	Parameters of the equalization filter
0x11	7:0	bq0_b1[23:16]	RW	8'h00	Parameters of the equalization filter
0x12	7:0	bq0_b1[15:8]	RW	8'h00	Parameters of the equalization filter
0x13	7:0	bq0_b1[7:0]	RW	8'h00	Parameters of the equalization filter
0x14	7:0	bq0_b2[23:16]	RW	8'h00	Parameters of the equalization filter
0x15	7:0	bq0_b2[15:8]	RW	8'h00	Parameters of the equalization filter
0x16	7:0	bq0_b2[7:0]	RW	8'h00	Parameters of the equalization filter
0x17	7:0	bq0_a1[23:16]	RW	8'h00	Parameters of the equalization filter
0x18	7:0	bq0_a1[15:8]	RW	8'h00	Parameters of the equalization filter
0x19	7:0	bq0_a1[7:0]	RW	8'h00	Parameters of the equalization filter
0x1A	7:0	bq0_a2[23:16]	RW	8'h00	Parameters of the equalization filter
0x1B	7:0	bq0_a2[15:8]	RW	8'h00	Parameters of the equalization filter
0x1C	7:0	bq0_a2[7:0]	RW	8'h00	Parameters of the equalization filter
0x1D	7:0	bq1_b0[23:16]	RW	8'h40	Parameters of the equalization filter
0x1E	7:0	bq1_b0[15:8]	RW	8'h00	Parameters of the equalization filter
0x1F	7:0	bq1_b0[7:0]	RW	8'h00	Parameters of the equalization filter
0x20	7:0	bq1_b1[23:16]	RW	8'h00	Parameters of the equalization filter
0x21	7:0	bq1_b1[15:8]	RW	8'h00	Parameters of the equalization filter
0x22	7:0	bq1_b1[7:0]	RW	8'h00	Parameters of the equalization filter
0x23	7:0	bq1_b2[23:16]	RW	8'h00	Parameters of the equalization filter
0x24	7:0	bq1_b2[15:8]	RW	8'h00	Parameters of the equalization filter
0x25	7:0	bq1_b2[7:0]	RW	8'h00	Parameters of the equalization filter
0x26	7:0	bq1_a1[23:16]	RW	8'h00	Parameters of the equalization filter
0x27	7:0	bq1_a1[15:8]	RW	8'h00	Parameters of the equalization filter
0x28	7:0	bq1_a1[7:0]	RW	8'h00	Parameters of the equalization filter
0x29	7:0	bq1_a2[23:16]	RW	8'h00	Parameters of the equalization filter
0x2A	7:0	bq1_a2[15:8]	RW	8'h00	Parameters of the equalization filter
0x2B	7:0	bq1_a2[7:0]	RW	8'h00	Parameters of the equalization filter

Address	Bit	Label	Access	Default	Description
0x2C	7:0	adc_digital_vol	RW	8'hCF	0dB default, 0x00~0xFF(mute, -103dB to +24dB, …0.5dB step)

Address	Bit	Label	Access	Default	Description
0x2D	7:0	dac_digital_vol	RW	8'hE7	0dB default, 0x00~0xFF(mute, -115dB to +12dB, …0.5dB step)

Address	Bit	Label	Access	Default	Description
0x2E	7:6	N/A	R	2'b00	Reserved
	5	adc_mute	RW	1'b1	1'b0: Unmute ADC 1'b1: Mute ADC
	4	adc_enable	RW	1'b0	1'b0: Disable ADC

					1'b1: Enable ADC
	3:2	N/A	R	2'b00	Reserved
	1	dac_mute	RW	1'b1	1'b0: Unmute DAC 1'b1: Mute DAC
	0	dac_enable	RW	1'b0	1'b0: Disable DAC 1'b1: Enable DAC

Address	Bit	Label	Access	Default	Description
0x2F	7	monitor_out_en	RW	1'b0	1'b0: Set monitor pin as input pin 1'b1: Set monitor pin as output pin
	6:4	monitor_pin_cfg	RW	3'b000	3'b000: Error out(configure 0x34[3:2] to choose error presentation) 3'b001: SDOUT Others: NA
	3:0	N/A	RW	4'h0	Reserved

Address	Bit	Label	Access	Default	Description
0x30	7:1	N/A	R	7'h00	Reserved
	0	dac_out_invert	RW	1'b0	1'b0: DAC out normal 1'b1: DAC out inverted

Address	Bit	Label	Access	Default	Description
0x31	7:4	N/A	R	4'h0	Reserved
	3:2	dsp_fade_time_sel	RW	2'b01	Fade speed setting: 2'b00: 2/fs per step 2'b01: 4/fs per step 2'b10: 8/fs per step 2'b11: 16/fs per step
	1	adc_fade_en	RW	1'b1	1'b0: ADC digital volume fade disabled 1'b1: ADC digital volume fade enabled
	0	dac_fade_en	RW	1'b1	1'b0: DAC digital volume fade disabled 1'b1: DAC digital volume fade enabled

Address	Bit	Label	Access	Default	Description
0x32	7:1	N/A	R	7'h00	Reserved
	0	fault_clr	WO	1'b0	Write 1'b1 to clear the fault flag, and the fault_clr register value will return to 1'b0 automatically

Address	Bit	Label	Access	Default	Description
0x33	7:4	N/A	R	4'h0	Reserved
	3	mclk_stop_err_en	RW	1'b1	MCLK stop error displays on 0x53[4] and error out, MCLK stop error results in amute_cfg_0 1'b0: Disable 1'b1: Enable
	2	sclk_err_en	RW	1'b1	SCLK error displays on 0x53[5] and error out, SCLK error results in amute_cfg_1 1'b0: Disable 1'b1: Enable
	1	mclk_err_en	RW	1'b1	MCLK stop error results in amute_cfg_1 1'b0: Disable 1'b1: Enable
	0	bist_fail_shutdwn_en	RW	1'b1	1'b0: Disable bist fail shutdown 1'b1: Enable bist fail shutdown

Address	Bit	Label	Access	Default	Description
0x34	7:4	N/A	R	3'b000	Reserved
	3	errout_en	RW	1'b0	Include SRAM error, SCLK error, MCLK error 1'b0: Disable error display on error flag signal 1'b1: Enable error display on error flag signal

	2	zero_out_en	RW	1'b1	1'b0: Disable zero flag display on error flag signal 1'b1: Enable zero flag display on error flag signal
	1	sram_err_mute_en	RW	1'b1	1'b0: Disable SRAM error to mute DAC dsp 1'b1: Enable SRAM error to mute DAC dsp
	0	ecc_err_mute_en	RW	1'b0	1'b0: Disable SRAM ecc error to mute DAC dsp 1'b1: Enable SRAM ecc error to mute DAC dsp

Address	Bit	Label	Access	Default	Description
0x36	7:5	N/A	R	4'h0	Reserved
	4	amute_cfg_4	RW	1'b0	1'b0: Disable auto mute controlled by SRAM error 1'b1: Enable auto mute controlled by SRAM error
	3	amute_cfg_3	RW	1'b0	1'b0: Disable auto mute controlled by DAC disable command 1'b1: Enable auto mute controlled by DAC disable command
	2	amute_cfg_2	RW	1'b0	1'b0: Disable auto mute controlled by zero detect 1'b1: Enable auto mute controlled by zero detect
	1	amute_cfg_1	RW	1'b0	1'b0: Disable auto mute controlled by asynchronous detect 1'b1: Enable auto mute controlled by asynchronous detect
	0	amute_cfg_0	RW	1'b0	1'b0: Disable auto mute controlled by MCLK halt 1'b1: Enable auto mute controlled by MCLK halt

Address	Bit	Label	Access	Default	Description
0x37	7:1	N/A	R	7'h00	Reserved
	0	osc_pwd	RW	1'b0	1'b0: Enable OSC 1'b1: Disable OSC

Address	Bit	Label	Access	Default	Description
0x38	7:0	pll_prediv_pllc	RW	8'h03	pll_ref_divider

Address	Bit	Label	Access	Default	Description
0x39	7:3	N/A	R	5'h00	Reserved
	2:0	pll_fbdiv_pllc[10:8]	RW	3'b001	pll_feedback_divider pll_clk =input_clk*pll_feedback_divider/2*pll_ref_divider
0x3A	7:0	pll_fbdiv_pllc[7:0]	RW	8'h80	

Address	Bit	Label	Access	Default	Description
0x3E (Note 4)	7:5	N/A	R	3'b000	Reserved
	4	bist_ram1_skip	RW	1'b0	Write 1'b1 to skip ram1 check
	3	bist_ram2_skip	RW	1'b0	Write 1'b1 to skip ram2 check
	2	bist_ram3_skip	RW	1'b0	Write 1'b1 to skip ram3 check
	1	bist_mode	RW	1'b0	Bist check pattern select 1'b0: Full ram check with all pattern 1'b1: Zero in out only, without other pattern
	0	bist_en	RW	1'b0	1'b0: Disable bist 1'b1: Enable bist

Address	Bit	Label	Access	Default	Description
0x3F	7:1	N/A	R	7'h00	Reserved
	0	fastchg_force_high	RW	1'b0	1'b0: Disable VCOM into fast charge 1'b1: Enable VCOM into fast charge

Address	Bit	Label	Access	Default	Description
0x40	7:2	N/A	R	6'h00	Reserved
	1	i2c_dly_en	RW	1'b0	1'b0: Disable SDA 37ns later than SCL 1'b1: Enable SDA 37ns later than SCL
	0	i2c_sda_timeout_en	RW	1'b0	If SDA is low for 20ms, then make the device into I^2C idle status 1'b0: Disable I^2C timeout 1'b1: Enable I^2C timeout

Address	Bit	Label	Access	Default	Description
0x49	7:4	N/A	R	4'h0	Reserved
	3:2	ldo_ilimctrl	RW	2'b00	DREG current limit threshold 2'b00: 30mA 2'b01: 45mA 2'b10: 60mA 2'b11: 75mA
	1:0	N/A	R	2'b00	Reserved

Address	Bit	Label	Access	Default	Description
0x4C	7	drv_ilimit_en	RW	1'b0	1'b0: Disable line driver current limit 1'b1: Enable line driver current limit
	6:5	N/A	R	2'b01	Reserved
	4:3	drv_ilimit_cur_sel	RW	2'b01	Line driver current limit ratio 2'b00: ×2 2'b01: ×4 2'b10: ×6 2'b11: ×8
	2:1	drv_ilimit_sel_base	RW	2'b00	Line driver current limit base 2'b00: 25mA 2'b01,10: 33mA 2'b11: 66mA Line driver current limit= drv_ilimit_cur_sel*drv_ilimit_sel_base
	0	clk_hold_sel	RW	1'b1	1'b0: Disable DAC current to driver hold 1'b1: Enable DAC current to driver hold

Address	Bit	Label	Access	Default	Description
0x4E (Note 1)	7	N/A	R	1'b0	Reserved
	6	xtal_osc_en	RW	1'b0	1'b0: Disable XTAL circuit 1'b1: Enable XTAL circuit
	5:4	xtal_osc_ib	RW	2'b01	Set inverter current base: 2'b00: 10μA 2'b01: 20μA 2'b10: 40μA 2'b11: 80μA
	3:1	xtal_osc_iwork	RW	3'b011	Set inverter current ratio: 3'b000: m=3 3'b001: m=9 3'b010: m=15 3'b011: m=21 3'b100: m=33 3'b101: m=39 3'b110: m=45 3'b111: m=51 Inverter current=xtal_osc_ib*xtal_osc_iwork
	0	N/A	R	1'b0	Reserved

Address	Bit	Label	Access	Default	Description
0x4F	7:4	N/A	R	4'h0	Reserved
	3	rg_enmute_pgal	RW	1'b1	1'b0: Unmute IN1 PGA 1'b1: Mute IN1 PGA
	2	rg_enmute_pgar	RW	1'b1	1'b0: Unmute IN2 PGA 1'b1: Mute IN2 PGA
	1:0	N/A	R	2'b00	Reserved

Address	Bit	Label	Access	Default	Description
0x50	7:2	N/A	R	6'h00	Reserved

	1	rg_en_iref	RW	1'b1	1'b0: Disable current generator in ADC 1'b1: Enable current generator in ADC
	0	rg_en_refgen	RW	1'b1	1'b0: Disable ADC reference buffer 1'b1: Enable ADC reference buffer

Address	Bit	Label	Access	Default	Description
0x52	7:1	N/A	R	7'h00	Reserved
	0	zero_flag_clk_cross	R	1'b0	SDIN zero input detection result 1'b0: SDIN has input 1'b1: SDIN zero input

Address	Bit	Label	Access	Default	Description
0x53	7	dac_sram_ecc_mulit_err	R	1'b0	DAC sram ecc multi error
	6	adc_sram_ecc_multi_err	R	1'b0	ADC sram ecc multi error
	5	sclk_err_fault	R	1'b0	SCLK not stable error
	4	mclk_stop_err_fault	R	1'b0	MCLK stop error
	3:2	N/A	R	2'b00	Researved
	1	sclk_stop_err_flag	R	1'b0	SCLK stop error
	0	lrclk_err_fault	R	1'b0	LRCLK stop or not stable error

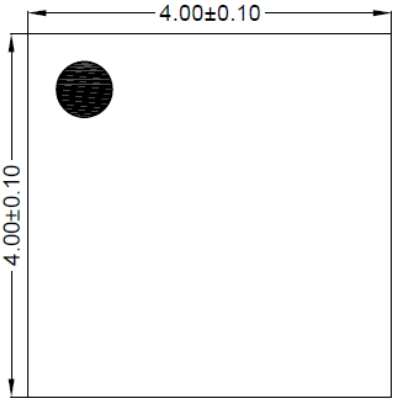
Address	Bit	Label	Access	Default	Description
0x59	7	adc_sram_ecc_multi_err	R	1'b0	ADC sram ecc multi error
	6	adc_sram_ecc_single_err	R	1'b0	ADC sram ecc single error
	5	dac_sram_ecc_mulit_err	R	1'b0	DAC sram ecc multi error
	4	dac_sram_ecc_single_err	R	1'b0	DAC sram ecc single error
	3:2	bist_fail_ram(Note 4)	R	2'b00	Bist fail sram information
	1	c_bist_fail(Note 4)	R	1'b0	Bist fail flag
	0	c_bist_done(Note 4)	R	1'b0	Bist done flag

Address	Bit	Label	Access	Default	Description
0xF7	7	N/A	R	1'b0	Reserved
	6:0	slave_addr	RW	7'h4C	I^2C address

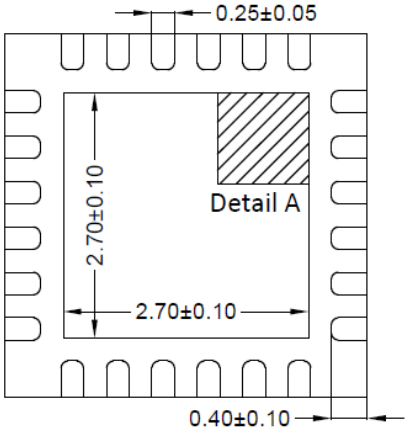
Address	Bit	Label	Access	Default	Description
0xF8~0xFB	31:0	i2c_dev_data_en	RW	32'h00000000	Write 32'hF9A5A5A5 to enable I^2C address change

Note 1: XTAL circuit only available in QFN28.
Note 2: Only effective in left-justified and right-justified.
Note 3: Only effective when direct path is used.
Note 4: Only for factory use.

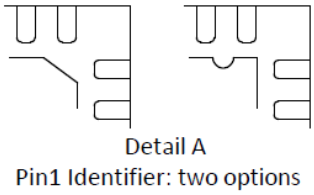
QFN4×4-24 Package Outline

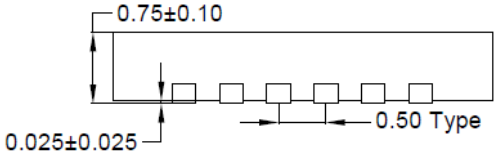


Top View

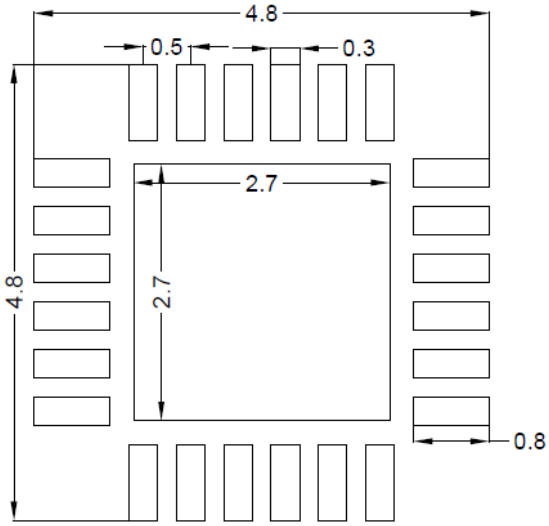


Bottom View





Front View

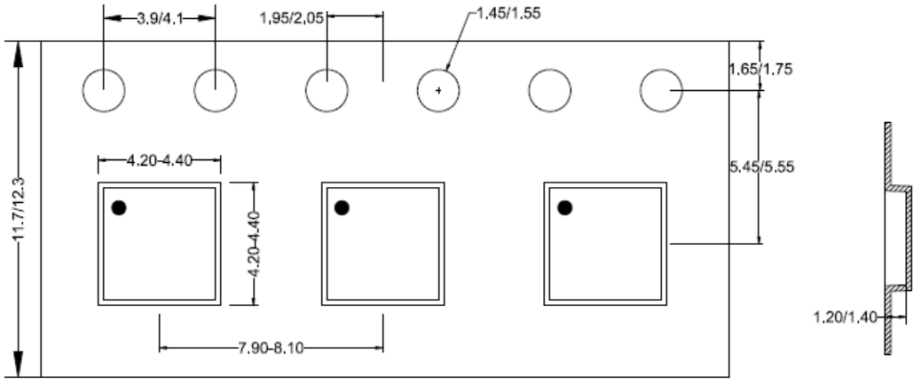


PCB Layout (Recommended)

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

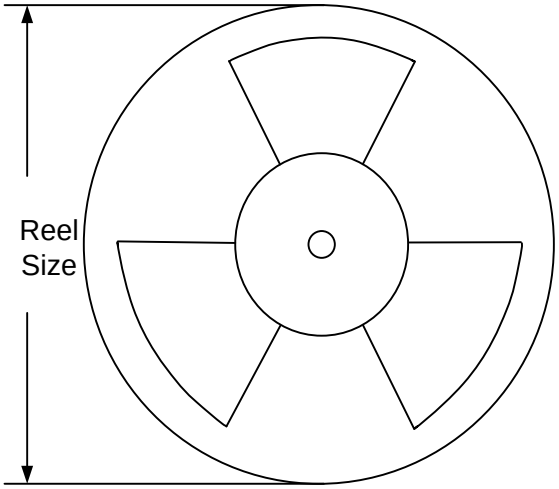
Tape and Reel Information

Tape Dimensions and Pin 1 Orientation



Feeding Direction

Reel Dimensions



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Trailer Length(mm)	Leader Length (mm)	Qty per Reel (pcs)
QFN4×4	12	8	13"	400	400	5000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warrantied. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
1.0	Jun. 14, 2025	Initial Release	

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. Applications. Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of a Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com