# SY20749

## Negative Charge Pump With Integrated Adjustable LDO

## General Description

The SY20749 is a charge pump with a wide input voltage range of 2.3V to 5.5V. It provides an unregulated negative voltage equal to VIN and features an adjustable negative linear voltage regulator between 0V and the negative input voltage, which can deliver a maximum of 200 mA to a load.

The SY20749 does not require an inductor and uses only four ceramic capacitors as external components. It is available in a compact QFN 1.4mm×1.8mm package, ensuring a small PCB size and low BOM cost.

## Features

- Wide Input Voltage Range: 2.3V to 5.5V
- Low Quiescent Current: 1.2mA
- Output Current: Up to 200mA
- No Inrush Current During Startup:
  - SY20749: 1.6A Charge Pump Current Limit (Typ.)
  - SY20749B: 0.8A Charge Pump Current Limit (Typ.)
- Overcurrent and Short-Circuit Protection
- Dual Output:
  - -1× Charge Pump
  - Regulated Output Between 0V and $-V_{IN}$
- Compact Package: QFN 1.4mm×1.8mm

## Applications

- Negative Rails for Analog Power
- Optical Applications Modules
- Power Supply for RF Amplifiers
- Power Source for Sensors in Portable Devices

## Typical Application

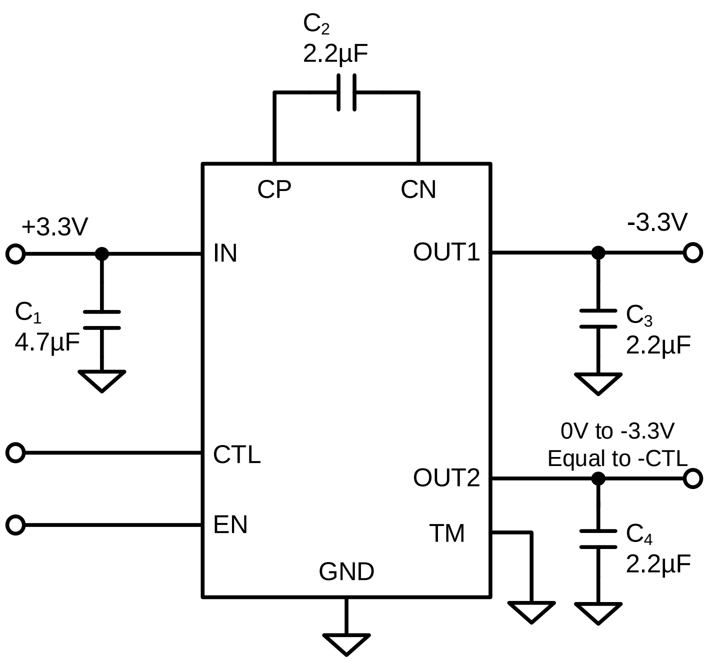



*Figure 1. Schematic Diagram*

## Ordering Information

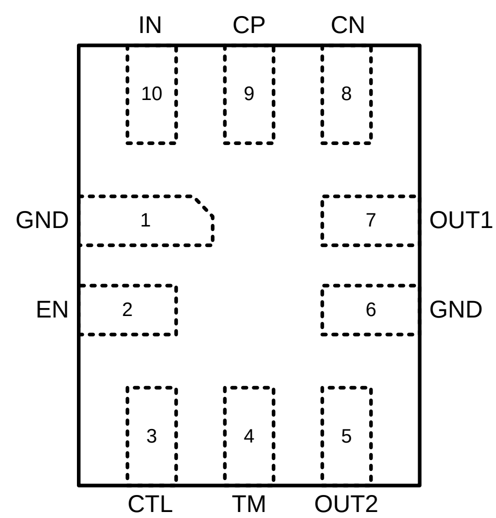
| Ordering Part Number | Details |
|---|---|
| SY20749**VLQ** | 1.6A Charge Pump Current Limit (Typ.) |
| SY20749**BVLQ** | 0.8A Charge Pump Current Limit (Typ.) |

## Package Information

| Part Number | Top Mark | Package type |
|---|---|---|
| SY20749**VLQ** | **6G*xyz*** | **QFN1.4×1.8-10** RoHS-Compliant, Halogen-Free |
| SY20749**BVLQ** | **y9*xyz*** | |

***x = year code, y = week code, z = lot number code***

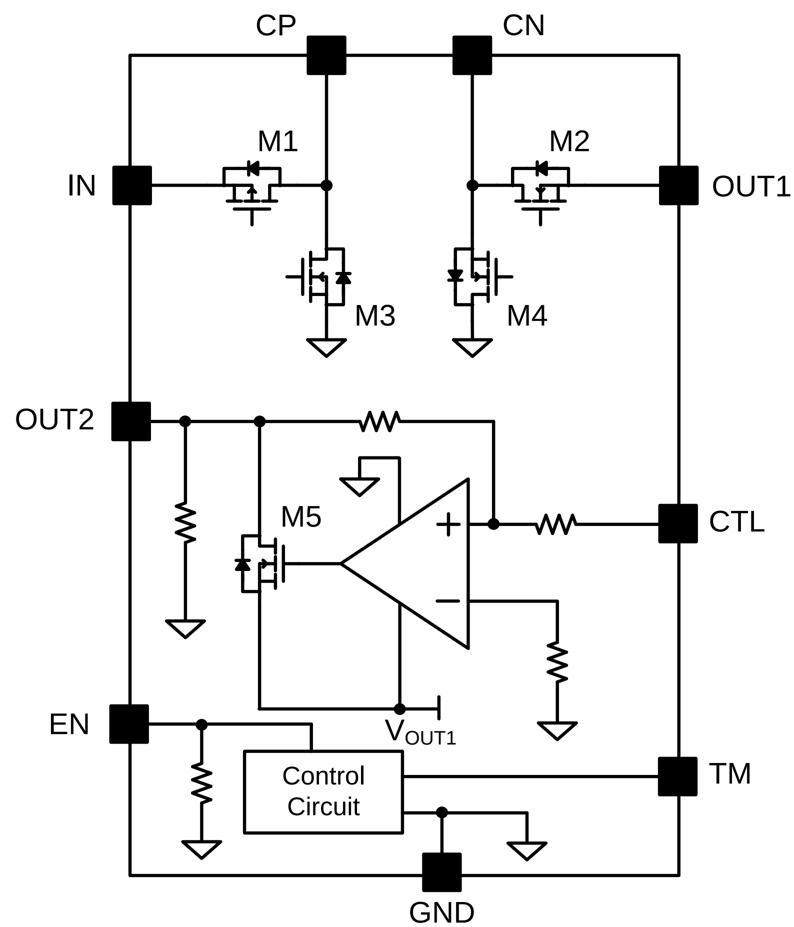
## Pinout (top view)




## Pin Description

| Pin Name | Pin Number | Pin Description |
|---|---|---|
| GND | 1 | Power ground. |
| EN | 2 | ON/OFF Control. Integrated 1MΩ pull-down resistor. |
| CTL | 3 | LDO analog control input voltage. Regulates the OUT2 LDO output to a value of -CTL. |
| TM | 4 | Test mode pin. This pin is for entering the device test mode. Connect to GND during normal operation. |
| OUT2 | 5 | Negative linear regulator output. A decoupling capacitor is required. The $V_{OUT2}$ follows the -$V_{CTL}$. |
| GND | 6 | Power ground. |
| OUT1 | 7 | Negative charge pump output. A decoupling capacitor is required. |
| CN | 8 | Negative terminal of the flying capacitor. |
| CP | 9 | Positive terminal of the flying capacitor. |
| IN | 10 | Power supply pin for the charge pump and internal control circuit. A 4.7μF ceramic capacitor to GND is recommended for decoupling. |

## Block Diagram




## Absolute Maximum Ratings

| Parameter (Note 1) | Min | Max | Unit |
|---|---|---|---|
| IN, EN, CTL, TM | -0.3 | 6.5 | V |
| CP | -0.3V/-0.7V(<100ns) | $V_{IN}$+0.3V/0.7V(<100ns) | |
| CN | $V_{OUT1}$-0.3V/-0.7V(<100ns) | 0.3V/1.5V(<4μs) | |
| OUT1 | -6.5 | 0.3 | |
| OUT2 | $V_{OUT1}$ | 0.3 | |
| Junction Temperature, Operating | -40 | 150 | °C |
| Lead Temperature (Soldering,10s) | | 260 | |
| Storage Temperature | -65 | 150 | |

## Thermal Information

| Parameter (Note 2) | Typ | Unit |
|---|---|---|
| $\theta_{JA}$ Junction-to-Ambient Thermal Resistance | 70 | °C/W |
| $\theta_{JC}$ Junction-to-Case Thermal Resistance | 45 | |
| $P_D$ Power Dissipation $T_A$ = 25°C | 1.4 | W |

## Recommended Operating Conditions

| Parameter (Note 3) | Min | Max | Unit |
|---|---|---|---|
| IN | 2.3 | 5.5 | V |
| CP | 0 | $V_{IN}$ | V |
| CN | $V_{OUT1}$ | 0 | V |
| OUT1 | $-V_{IN}$ | 0 | V |
| OUT2 | $V_{OUT1}$ | 0 | V |
| EN, CTL, TM | 0 | 5.5 | V |
| Junction Temperature | -40 | 125 | °C |

## Electrical Characteristics

(The specification in the following table applies over the –40˚C≤ $T_J$≤+125˚C. Unless otherwise noted, the typical values are for $T_A$ = 25°C, $V_{IN}$=3.3V. (Note 4))

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Voltage Range | $V_{IN}$ | | 2.3 | | 5.5 | V |
| Under Voltage Lockout Threshold | $V_{UVLO}$ | | | 2.2 | 2.3 | V |
| Under Voltage Lockout Threshold Hysteresis | $V_{UV\_HYS}$ | | | 200 | | mV |
| Shutdown Current | $I_{SHDN}$ | $V_{IN}$=3.3V, EN=0V | | 0.1 | 10 | μA |
| Quiescent Current | $I_Q$ | $V_{IN}$=3.3V, EN=2V, Null load | | 1.2 | | mA |
| Charge Pump Frequency | $f_{CP}$ | | 350 | 500 | 650 | kHz |
| Charge Pump Current Limit | $I_{CP}$ | SY20749VLQ | 1.27 | 1.6 | 1.88 | A |
| | | SY20749BVLQ | 0.4 | 0.75 | 1.1 | A |
| Charge Pump MOS Switch On Resistance | $R_{ON}$ | | | 0.12 | | Ω |
| EN Turn On Delay | td | $V_{IN}$=3.3V, EN=2V, Null load | 15 | 35 | 55 | μs |
| **Negative Linear Regulator** | | | | | | |
| Load Current Limit | $I_{LMT}$ | | 200 | 250 | 300 | mA |
| Output Accuracy | | $T_A$=25°C, $I_{OUT2}$=10mA, compare to $V_{CTL}$ | -1 | | 1 | % |
| | | -40°C <$T_J$<125°C, $V_{IN}$=3.3V, CTL=1V, $I_{OUT2}$=10mA, compare to $V_{CTL}$ | -2 | | 2 | % |
| Output Offset | $V_{OS}$ | $V_{IN}$=3.3V, CTL=1V, $I_{OUT2}$=10mA | -20 | | 20 | mV |
| Drop Out Voltage | $V_{DO}$ | $V_{IN}$=2.5V, $I_{OUT2}$=60mA | 30 | 50 | 70 | mV |
| | | $V_{IN}$=3.3V, $I_{OUT2}$=60mA | 15 | 35 | 55 | mV |
| Load Regulation (Note 5) | | $V_{OUT1}$=-3.3V, CTL=1V | | 0.005 | 0.01 | %/mA |
| PSRR (Note 5) | | 100Hz, $C_{OUT1}$=100pF $C_{OUT2}$=1μF, $I_{OUT2}$=10mA | | 60 | | dB |
| | | 50kHz, $C_{OUT1}$=100pF $C_{OUT2}$=1μF, $I_{OUT2}$=10mA | | 50 | | dB |
| | | 300kHz, $C_{OUT1}$=100pF $C_{OUT2}$=1μF, $I_{OUT2}$=10mA | | 40 | | dB |
| Soft-Start Slew Rate | SR | | | 5 | | V/ms |
| EN Logic Low Voltage | $V_{IL}$ | $V_{IN}$=3.3V | | | 0.4 | V |
| EN Logic High Voltage | $V_{IH}$ | | 1.5 | | | V |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Discharge Resistor | $R_{DIS1}$ | $V_{EN}$=0V, $V_{OUT1}$ Rail | | 150 | | Ω |
| | $R_{DIS2}$ | $V_{EN}$=0V, $V_{OUT2}$ Rail | | 150 | | Ω |
| EN Input Current | $I_{EN\_LKG}$ | $V_{EN}$=2V | | 2 | | μA |
| | | $V_{EN}$=0V | | 0 | | μA |
| Thermal Shutdown Threshold (Note 5) | $T_{TSD}$ | | | 150 | | °C |
| Thermal Shutdown Hysteresis (Note 5) | $T_{HYS}$ | | | 20 | | °C |
| OUT1 Voltage | $V_{OUT1}$ | | | -1 | | $V_{IN}$ |
| Output Ripple (Note 5) | $V_{RIPPLE1}$ | $V_{IN}$=3.3V, $V_{OUT1}$= -3.3V, $C_{FLY}$=$C_{OUT1}$=4.7μF, $I_{OUT1}$=60mA | | 50 | | mV |
| | $V_{RIPPLE2}$ | $V_{IN}$=3.3V, $V_{OUT2}$= -2.5V, $C_{OUT2}$=1μF, $I_{OUT2}$=60mA | | 1 | | mV |

**Note 1**: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2**: $\theta_{JA}$ is measured with natural convection at $T_A$ = 25°C on a Silergy EVB test board.

**Note 3:** The device is not guaranteed to function outside its operating conditions.

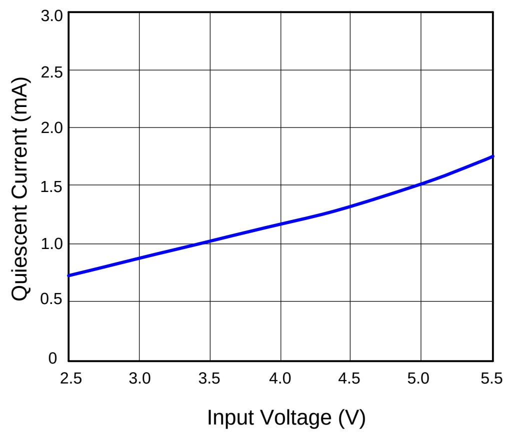
**Note 4:** Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$= 25°C. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

**Note 5:** Guaranteed by design.

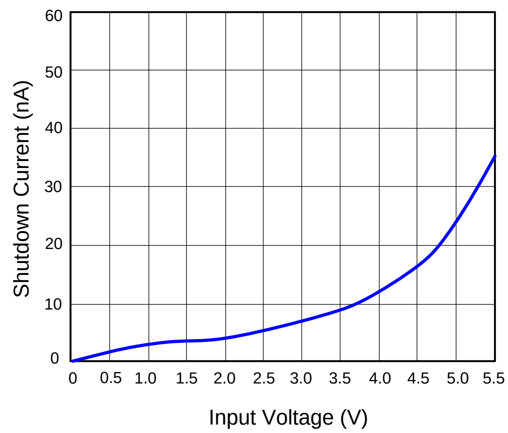
## Typical Performance Characteristics

(Unless otherwise noted, the typical values are for $T_A$ = 25°C, $V_{IN}$=3.3V.)

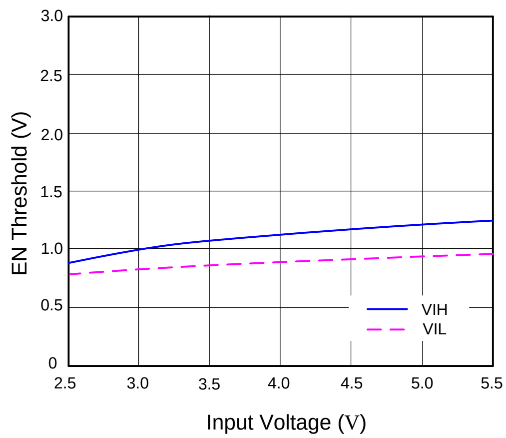
Quiescent Current vs. Input Voltage



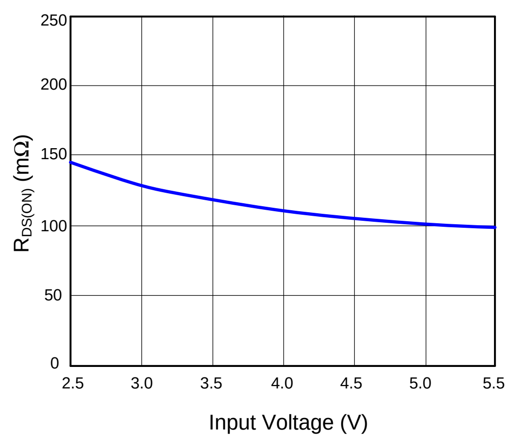

Shutdown Current vs. Input Voltage




EN Threshold vs. Input Voltage

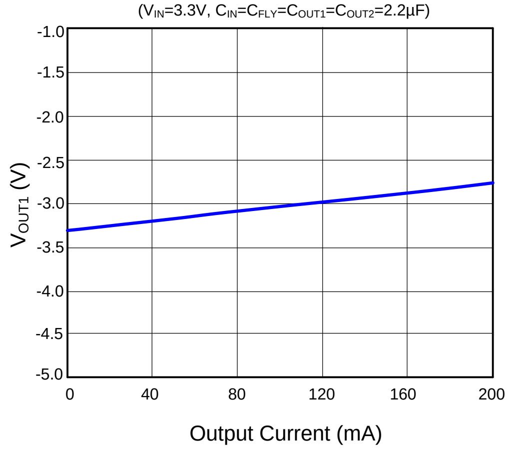



$R_{DS(ON)}$ vs. Input Voltage



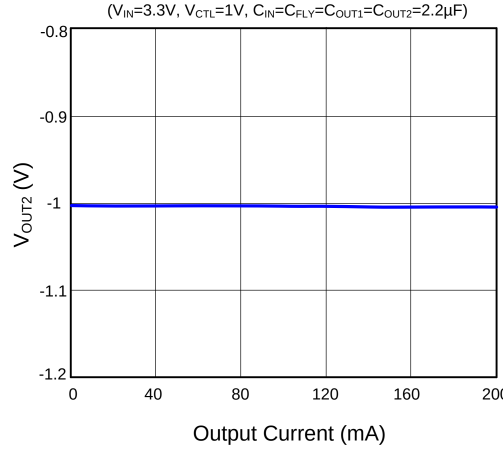

VOUT1 Load Regulation

($V_{IN}$=3.3V, $C_{IN}$=$C_{FLY}$=$C_{OUT1}$=$C_{OUT2}$=2.2μF)

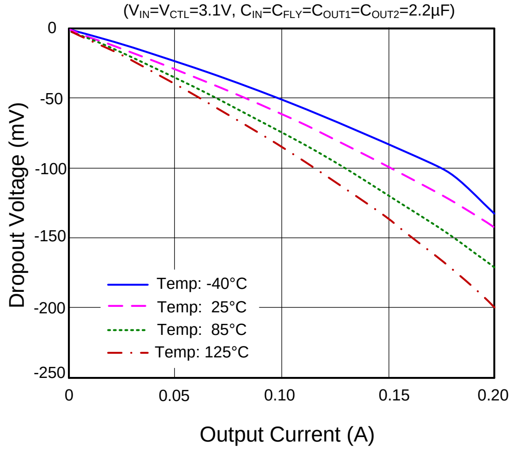



VOUT2 Load Regulation

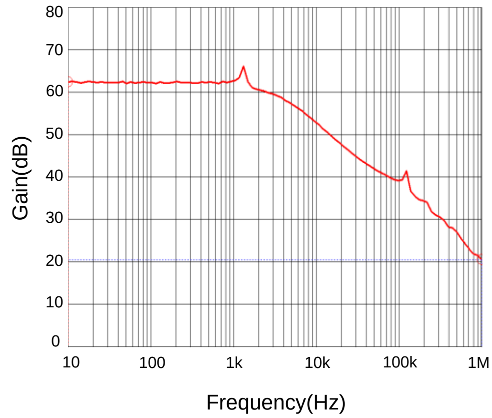
($V_{IN}$=3.3V, $V_{CTL}$=1V, $C_{IN}$=$C_{FLY}$=$C_{OUT1}$=$C_{OUT2}$=2.2μF)



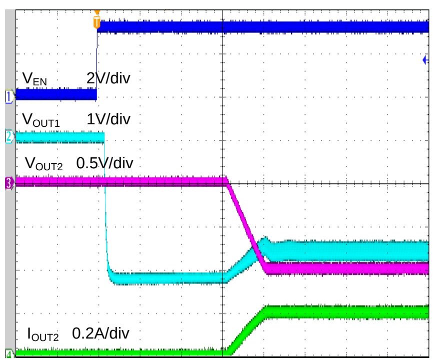
Dropout Voltage vs. Output Current
($V_{IN}$=$V_{CTL}$=3.1V, $C_{IN}$=$C_{FLY}$=$C_{OUT1}$=$C_{OUT2}$=2.2µF)




PSRR
($V_{IN}$=3.3V, $V_{CTL}$=1V, $C_{IN}$=$C_{FLY}$=$C_{OUT1}$=$C_{OUT2}$=2.2µF, $I_{OUT2}$=10mA )

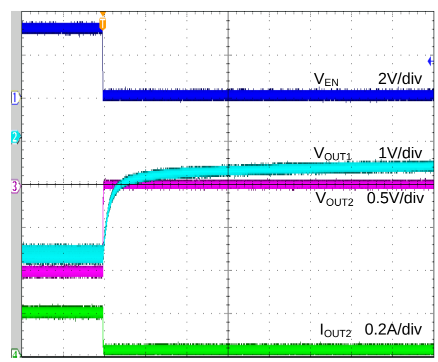



Startup from EN
($V_{IN}$=3.3V, CTL=1V, $C_{IN}$=$C_{OUT1}$=$C_{OUT2}$=$C_{FLY}$=2.2µF, 5Ω Load)



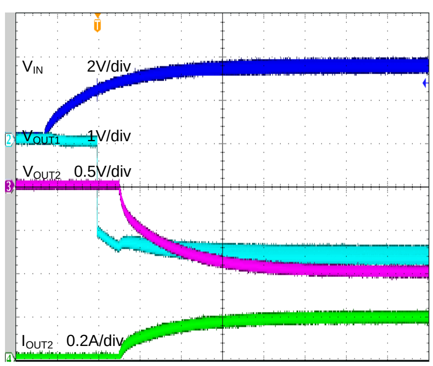

Time (200µs/div)

Shutdown from EN
($V_{IN}$=3.3V, CTL=1V, $C_{IN}$=$C_{OUT1}$=$C_{OUT2}$=$C_{FLY}$=2.2µF, 5Ω Load)



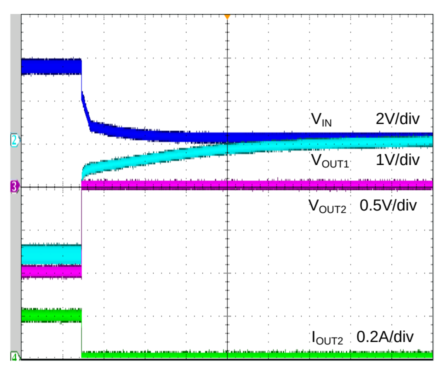

Time (2ms/div)

Startup from $V_{IN}$
($V_{IN}$=3.3V, CTL=1V, $C_{IN}$=$C_{OUT1}$=$C_{OUT2}$=$C_{FLY}$=2.2µF, 5Ω Load)




Time (20ms/div)

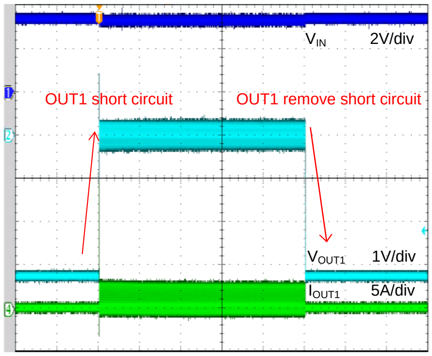
Shutdown from $V_{IN}$
($V_{IN}$=3.3V, CTL=1V, $C_{IN}$=$C_{OUT1}$=$C_{OUT2}$=$C_{FLY}$=2.2µF, 5Ω Load)




Time (200ms/div)

OUT1 Short Circuit Response

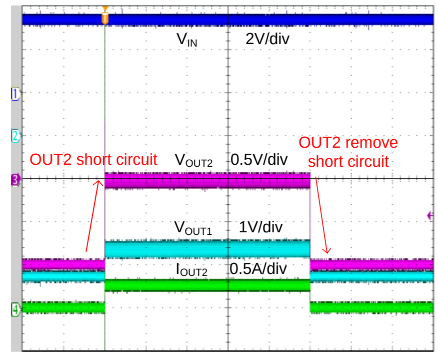
($V_{IN}$=3.3V, CTL=0V, $C_{IN}$=$C_{OUT1}$=$C_{OUT2}$=$C_{FLY}$=2.2µF)




Time (10ms/div)

OUT2 Short Circuit Response

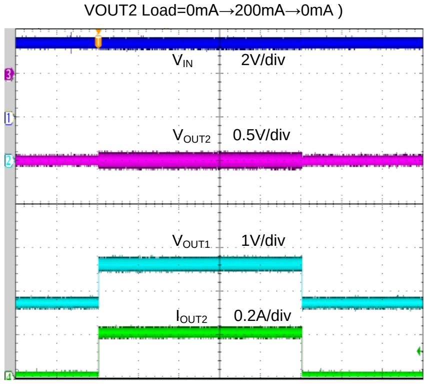
($V_{IN}$=3.3V, CTL=1V, $C_{IN}$=$C_{OUT1}$=$C_{OUT2}$=$C_{FLY}$=2.2µF)




Time (10ms/div)

Load Transient

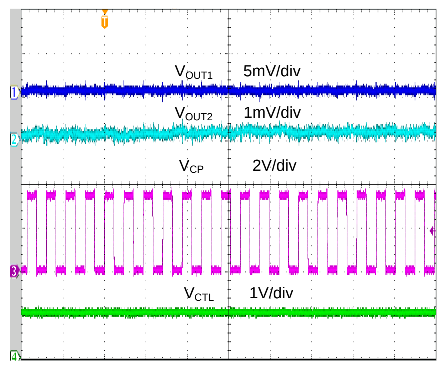
($V_{IN}$=3.3V, CTL=1V, $C_{IN}$=$C_{OUT1}$=$C_{OUT2}$=$C_{FLY}$=2.2µF,
VOUT2 Load=0mA→200mA→0mA )




Time (10ms/div)

Steady State 1

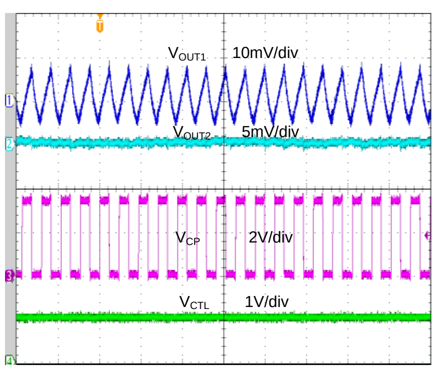
($V_{IN}$=3.3V,CTL=1V, $C_{IN}$=$C_{OUT1}$=$C_{OUT2}$=$C_{FLY}$=2.2µF, $I_{OUT2}$=0mA)




Time (4µs/div)

Steady State 2

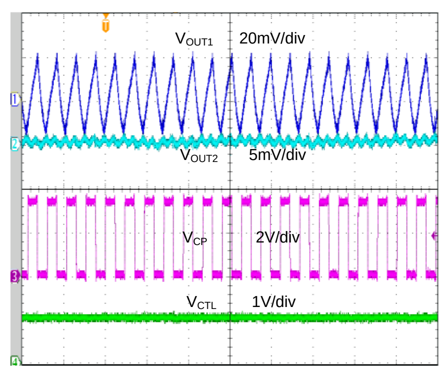
($V_{IN}$=3.3V,CTL=1V,$C_{IN}$=$C_{OUT1}$=$C_{OUT2}$=$C_{FLY}$=2.2µF,$I_{OUT2}$=20mA)




Time (4µs/div)

Steady State 3

($V_{IN}$=3.3V,CTL=1V,$C_{IN}$=$C_{OUT1}$=$C_{OUT2}$=$C_{FLY}$=2.2µF,$I_{OUT2}$=60mA)




Time (4µs/div)

## Operation

The SY20749 is an integrated monolithic device that functions as a negative voltage charge pump and includes an adjustable negative linearl voltage regulator. It is designed to accept input voltages ranging between 2.3V and 5.5V. The device offers an unregulated output voltage inverse of the supplied input voltage. The integrated LDO can deliver a regulated output voltage that falls within the range of 0V to the negative equivalent of the input voltage.

No additional inductors are needed, simplifying the design and allowing for a more compact layout. The built-in soft-start circuitry minimizes the inrush current during the initial power-up phase.

**Negative Charge Pump**

The SY20749 uses a switched-capacitor charge pump mechanism to generate an unregulated negative voltage corresponding to the negative of the input voltage. An internal oscillator within the control circuitry produces the driving signal for the charge pump. The oscillator frequency, responsible for the charge pump switching, is set at approximately 500kHz.

If the absolute value of the output voltage ($V_{OUT1}$) falls below 1V, the device interprets this as an overcurrent situation. In response, the SY20749 reduces the oscillator frequency to one-third of its original value, thereby implementing a fold-back current limiting mechanism.

A diode is present between the OUT1 and GND pins. When the voltage at $V_{OUT1}$ exceeds 0.3V, this diode becomes conductive, allowing the voltage at $V_{OUT1}$ to discharge.

The LDO dropout voltage based on the worst process corners is listed below and is guaranteed by design.

| $V_{IN}$=3.1V, 120mA | | |
|---|---|---|
| | $V_{OUT1}$ | $V_{OUT2}$ |
| $T_J$=85˚C | -2.85V | -2.73V |
| $T_J$=125˚C | -2.81V | -2.67V |

| $V_{IN}$=3.1V, 160mA | | |
|---|---|---|
| | $V_{OUT1}$ | $V_{OUT2}$ |
| $T_J$=85˚C | -2.76V | -2.59V |
| $T_J$=125˚C | -2.71V | -2.51V |

**Negative Linear Regulator**

The SY20749 features an integrated negative linear regulator powered by the output of the negative charge pump. This regulator is characterized by a low dropout voltage, a low quiescent supply current, and minimal output noise, providing linear regulation. Its output ranges from 0V to $V_{OUT1}$ voltage.

The regulator features an internal feedback loop that adjusts the output voltage to match the inverse of the voltage applied to the CTL pin, providing a straightforward interface for use with a digital-to-analog converter (DAC).

The Power Supply Rejection Ratio (PSRR) of the linear regulator is specially designed to complement the charge pump functionality, ensuring that the negative linear regulator exhibits a low output ripple.

**Overcurrent Protection**

The current supplied by the charge pump is internally limited within the device, incorporating safeguards to protect against both overload and over-temperature conditions. The peak charge pump input current for the SY20749VLQ is limited to 1.6A within the recommended input voltage range.

For the SY20749BVLQ, the peak charge pump input current is limited to 0.75A when the input voltage is higher than 3V. To improve load capacity at low input voltage, the SY20749BVLQ's current limit increases to 1.6A when the input voltage is lower than 3V. Additionally, it decreases to 0.75A when the OUT1 voltage is higher than -1V, if the input voltage is lower than 3V.

**Thermal Shutdown Protection**

If the overcurrent condition persists for a long time, the junction temperature may exceed 150°C, and overtemperature protection will shut down the part. Once the chip temperature drops below 130°C, the part will restart

**Undervoltage Lockout**

When the input voltage is higher than the undervoltage lockout (UVLO) threshold, typically set at 2.2V, the SY20749 can be enabled by applying a voltage level higher than 1.2V to the EN (enable) pin. If the EN pin is left unconnected (floating) or pulled down to the ground, the SY20749 will be disabled. Note that there is an internal 1MΩ resistor connected from the EN pin to the ground.

When the device is disabled, it automatically enters an output discharge mode. In this mode, an internal discharge MOSFET is engaged, providing a resistive path to discharge the output capacitor.

## Equivalent Output Resistance

The equivalent output resistance of the SY20749 is influenced by the frequency of the charge pump operation and flying capacitor. The equation is shown below:

$$R_O = \frac{1}{f \times C_{FLY}} + 8 \times R_{ON}$$

$R_{ON}$ is the on-resistance of each switch MOSFET in charge pump.

The OUT1 voltage (charge pump output) is influenced by $I_O$ and $R_O$. The equation is below:

$$V_{OUT1} = -(V_{IN} - I_O \times R_O)$$

## Soft-Start

The integrated linear regulator within the SY20749 features a built-in soft-start function that gradually increases the output voltage at a regulated rate to prevent overshoot at start-up. By default, the soft-start slew rate is internally configured to a value of 5V/ms.

## Supply Input Capacitor

A 4.7µF or larger input ceramic capacitor is strongly recommended to be placed close to the device. Without the input capacitor, an output short can cause ringing on the input. It could destroy the internal circuitry when the input transient exceeds the absolute maximum supply voltage, even for a short duration.

## Output Filter Capacitor

1µF-10µF output ceramic capacitors ($C_{OUT1}$ and $C_{OUT2}$) should be placed close to the device and output connector to reduce voltage drop during load transients. Higher values of output capacitors can be used to further improve load transient response and reduce noise.

## Flying Capacitor Selection

Considering the impact of the fly capacitor on output resistance and the voltage at OUT1, it is advisable to use a larger flying capacitor for higher output currents. Additionally, it is recommended that the flying capacitor be placed close to both the input capacitor ($C_{IN}$) and the output capacitor ($C_{OUT1}$).

## Output Voltage Setting

The linear regulator tracks the voltage at the CTL pin, regulating the output to the negative value of the CTL voltage ($V_{OUT2}$ = -$V_{CTL}$). The CTL pin acts as an analog input and can be directly connected to a DAC's output. The application circuit is shown in Figure 2.

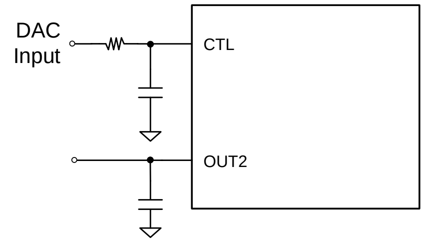



*Figure 2. Output Voltage Setting*

## PCB Layout Guide

For optimal regulation, noise suppression, transient response, and heat management, the following PCB layout guidelines are recommended:

- Place high-current paths, such as the ground (GND), input (IN), and charge pump (CP and CN) connections, as close to the device as possible, using short, straight, and wide traces.
- Position the input capacitor near the IN and GND pins.
- Place the ground connection of the output capacitor adjacent to the device ground pins.

Figure 3 provides a recommended layout for the PCB.

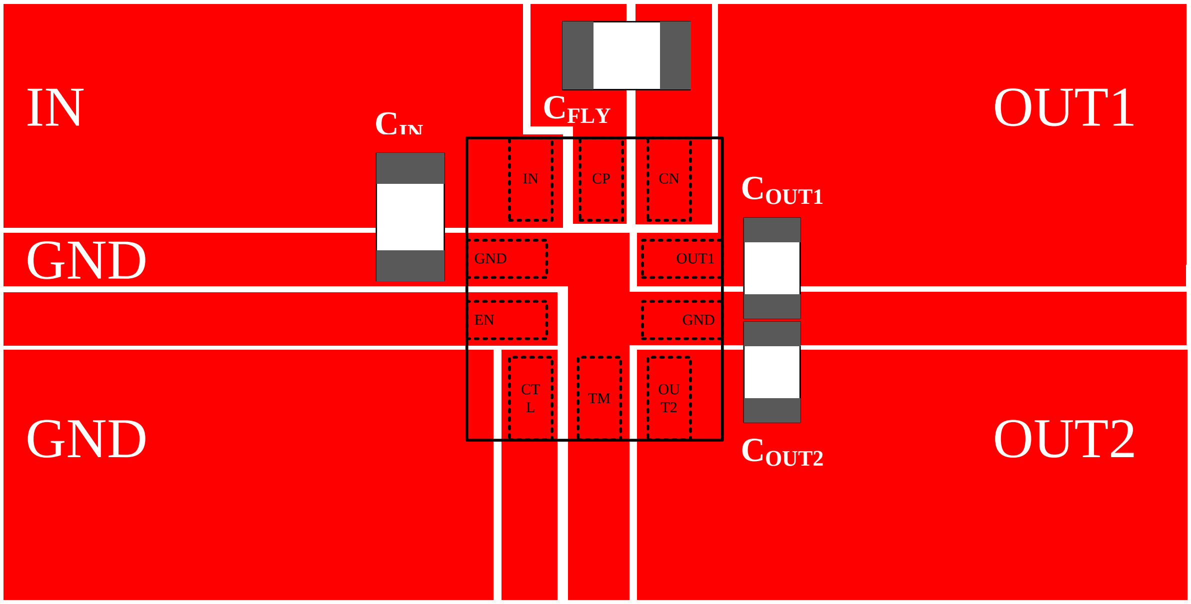
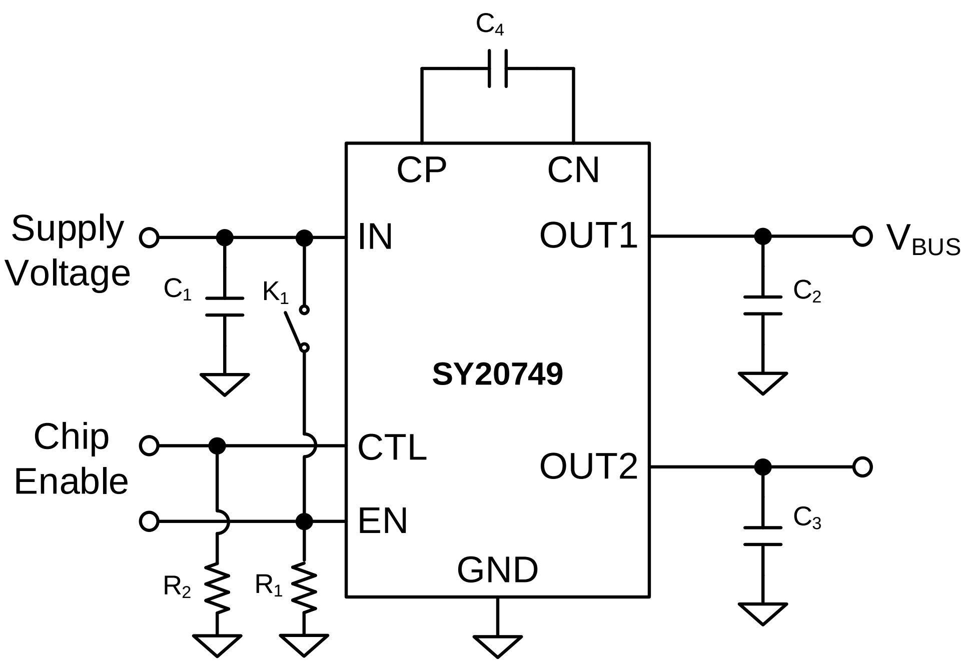



*Figure 3. PCB Layout Suggestion*

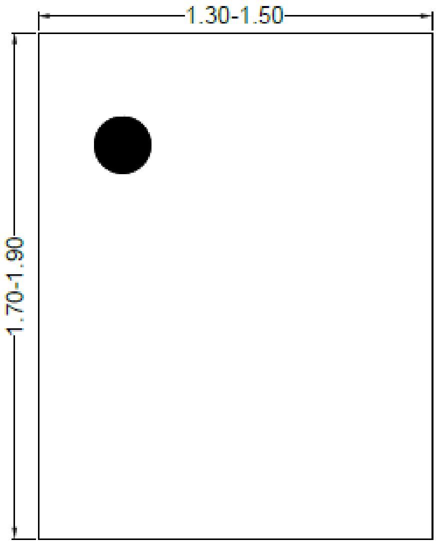
## Schematic



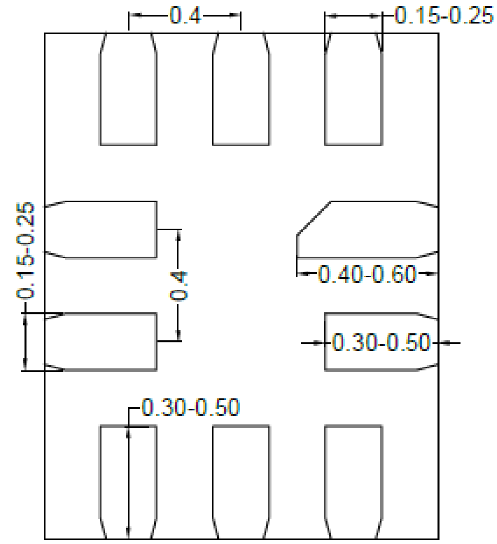
## BOM List

| Reference Designator | Description | Part Number | Manufacturer |
|---|---|---|---|
| $C_1$ | 4.7μF/16V, 0603 | GRM185R61C475KE11D | Murata |
| $C_2$ | 2.2μF/16V, 0603 | GRM188R61C225KE15D | Murata |
| $C_3$ | 2.2μF/16V, 0603 | GRM188R61C225KE15D | Murata |
| $C_4$ | 2.2μF/16V, 0603 | GRM188R61C225KE15D | Murata |
| $R_1$ | 1MΩ, 0603 | RC0603FR-071ML | YAGEO |
| $R_2$ | 1MΩ, 0603 | RC0603FR-071ML | YAGEO |

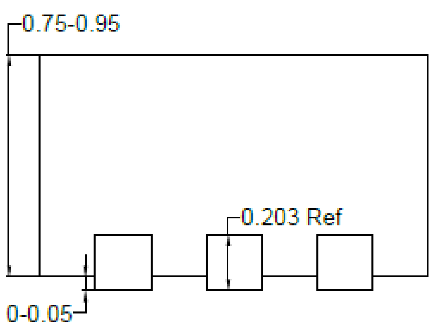
## QFN1.4×1.8-10 Package Outline Drawing



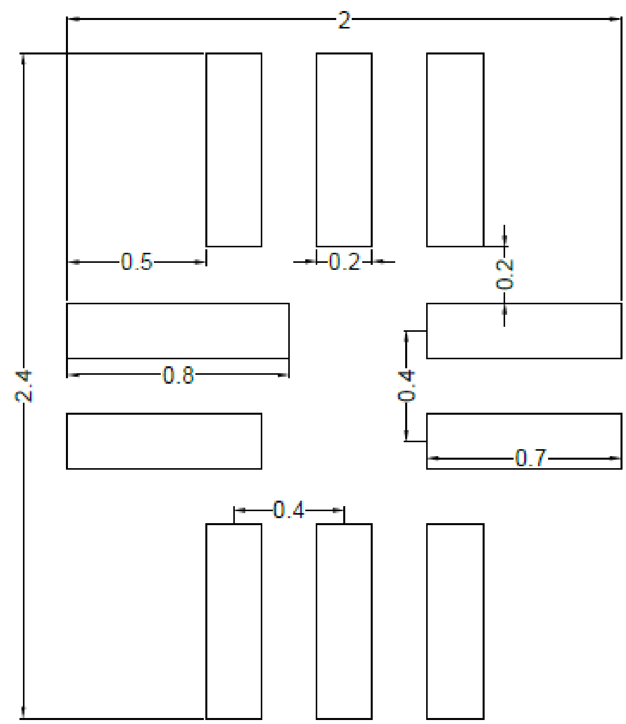

**Top View**




**Bottom View**




**Front View**

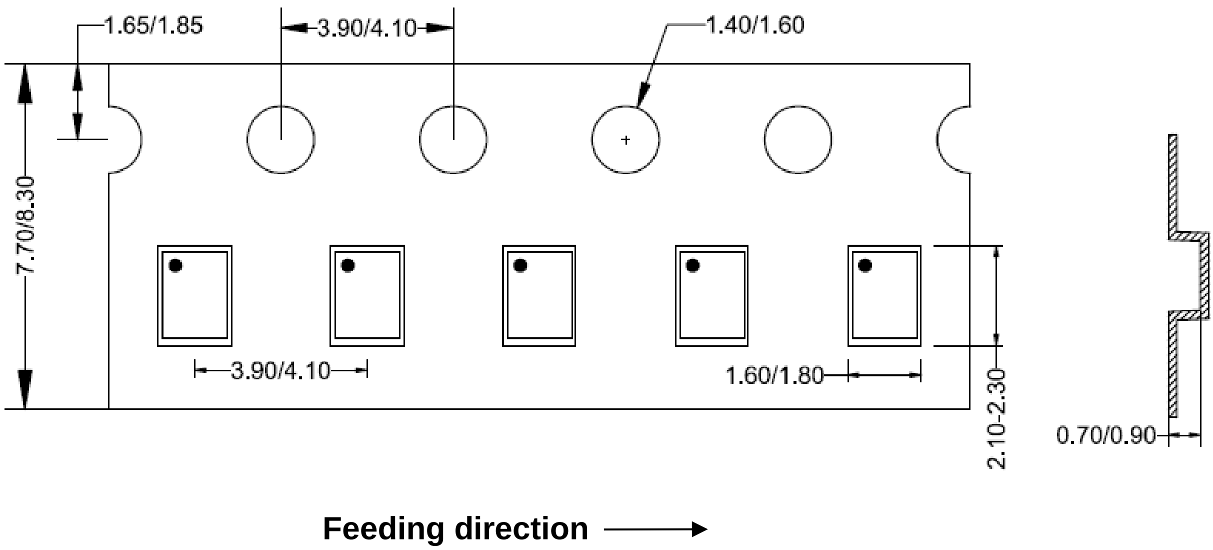



**Recommended PCB Layout (Reference Only)**

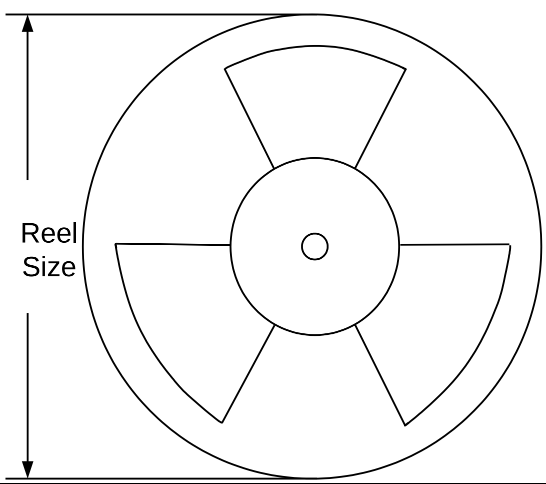
*Note: All dimensions are in millimeters and exclude mold flash and metal burr.*

# Tape and Reel Information

## QFN1.4×1.8 Tape Dimensions and Pin 1 Orientation




## Reel Dimensions




| Package type | Tape width (mm) | Pocket pitch (mm) | Reel size (Inch) | Trailer length (mm) | Leader length (mm) | Qty per reel |
|---|---|---|---|---|---|---|
| QFN1.4×1.8 | 8 | 4 | 7" | 400 | 160 | 3000 |

# Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warrantied. Please make sure that you have the latest revision.

| Date | Revision | Change |
|---|---|---|
| June 14, 2024 | Revision 1.0 | Added SY20749B specification. |
| Nov.09, 2022 | Revision 0.9A | Added Tape & Reel Specification (page12) |
| Dec.30, 2020 | Revision 0.9 | Initial Release |

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