SY72025

High Current Over Voltage Protection Switch with High Current Bi-directional DC/DC Regulator and Capacitance Measurement

General Description

SY72025 is a power management IC for the applications of power backup in Solid-State Driver or other backup power supplies which can achieve backup power storage and release functions. The energy is transferred bi-directionally between the BUS side and the energy storage side with high efficiency by bi-directional DC/DC regulator. Fast transient response and excellent stability are achieved by the quasi-fixed frequency constant off time control strategy.

A reverse blocking switch is integrated at the input side to prevent from energy leaking when the input power source is removed. The reverse blocking switch also has the programmable current limit function with the program range from 1.2A to 6.2A. Three different BUS over voltage protection (OVP) thresholds are selectable by OVP pin for the applications with different kind of input power source.

I^2C interface is internally integrated in SY72025 to reduce the amount of external components. Control parameters such as input current limit, switching frequency, and boost peak current limit can be programmed by I^2C.

Storage capacitance measurement is integrated inside of SY72025. The measurement results are stored in internal read only data registers for MCU reading by I^2C interface.

SY72025 along with QFN4×4-25 package provides compact PCB layout to save circuit area for the increase of SSD memory capacity.

Ordering Information

SY72025□(□□□)

Package Code

Optional Spec Code

Ordering Number	Package Type	Note
SY72025RGQ	QFN4×4-25	

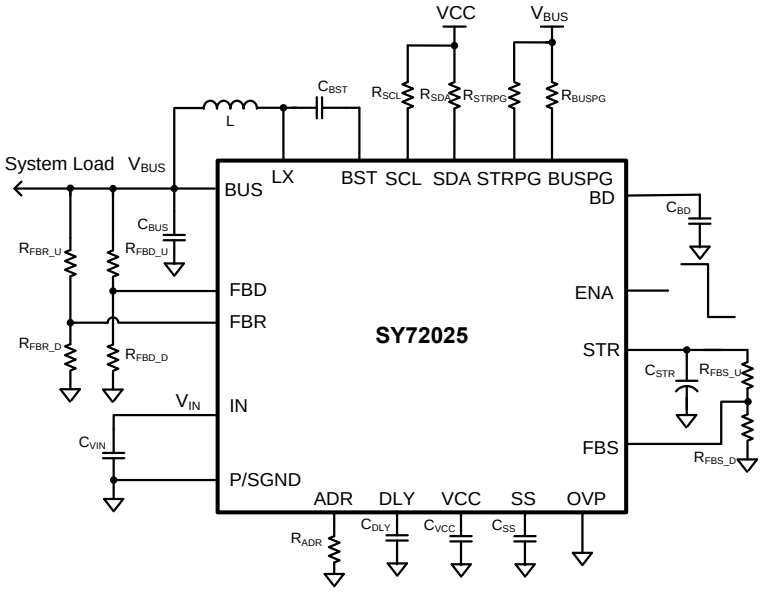
Features

- Low $R_{DS(ON)}$ for internal switches
  - Input Reverse Blocking Switch: 24 mΩ (Typical)
  - High-side and Low-side Switches of Bi-directional Dc-Dc Regulator: 70 mΩ /70 mΩ (Typical)
  - Disconnect Switch: 40 mΩ (Typical)
- 2.6V-16V Input Voltage Range with Maximum 36V Storage Voltage
- IN/BUS/STR Voltage and Input Current ADC
- Programmable Input Current Limit from 1.2A to 6.2A
- Selectable Over Voltage Protection: 3.8V, 5.7V, and 14.05V
- Input Power Source Detection to guarantee boost working under stable input condition
- Reverse Blocking at Input Side to Prevent from Leakage Current
- BUS Auto-discharge Function
- Programmable Reverse Blocking Switch Turn On Delay Time and Soft-start Time
- Integrated High-efficiency Bi-directional Dc-Dc Regulator:
  - Programmable Boost Charging Peak Current
  - Programmable Quasi-Fixed Frequency Constant Off Time Control for Steady-State Operation
  - Selectable Boost CV Mode and Burst Mode
  - STR Pin Open Detection in Burst Mode
  - Programmable Boost Soft Start Time
  - Programmable Storage Voltage with flexible OVP Threshold
  - Selectable Pulse Pre-charge Current for super capacitor Application
- MTP (Multi-Times Programming) Available for Control Parameters Programming by I^2C
- Short-circuit Protection at Energy Storage Side
- Storage Capacitance Measurement
- Independent Load Switch Enable Control Pin
- RoHS Compliant and Halogen Free
- Compact package: QFN4×4-25

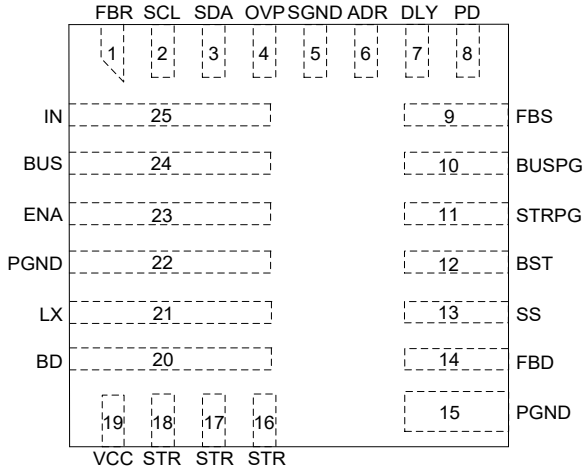
Applications

- Solid-State Drivers
- Backup Power Supply

Typical Applications



Pin out

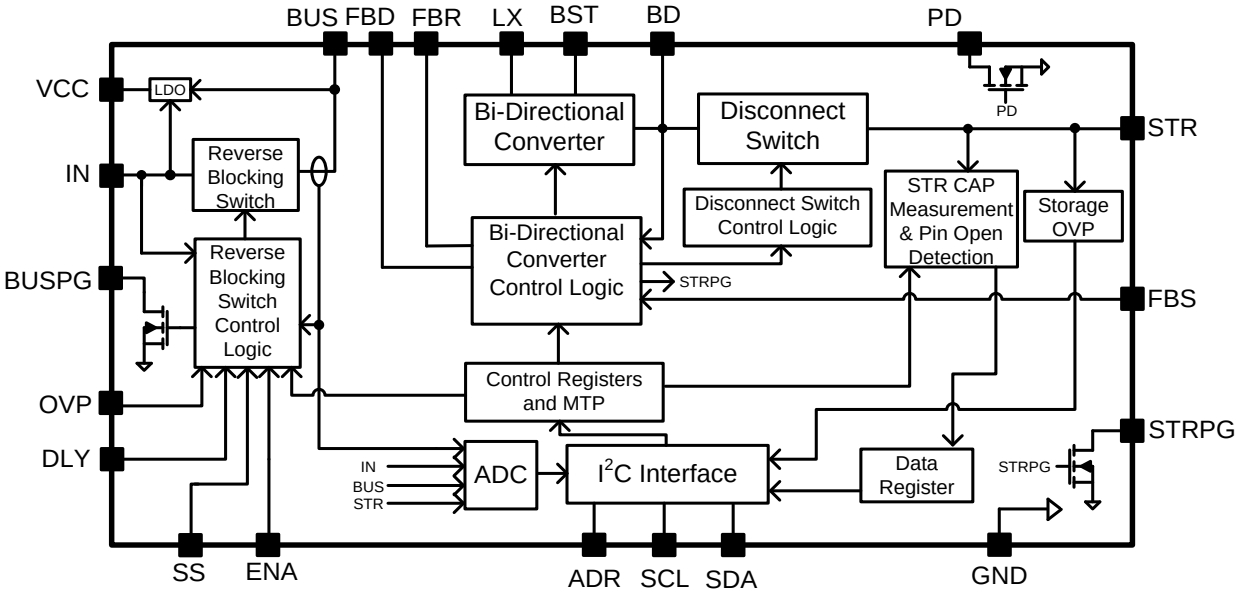


Top Mark: DRE*xyz* (device code: DRE, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin Number	Pin Description
FBR	1	Buck mode regulation voltage feedback pin. Using external resistor divider to program the buck regulation point. The internal voltage reference is 0.6V.
SCL	2	I^2C interface clock pin.
SDA	3	I^2C interface data pin.

<table>
<tr><td>OVP</td><td>4</td><td>Input over voltage threshold selection for the applications with different input voltage. Pull OVP pin to IN directly to have HIGH logic, or pull OVP pin to GND directly to have LOW logic, or float OVP Pin to select different input over voltage thresholds.
<table>
<tr><td rowspan="2">OVP</td><td rowspan="2">IN</td><td colspan="3">OVP Threshold</td></tr>
<tr><td>Min</td><td>Typ</td><td>Max</td></tr>
<tr><td>Low</td><td>3.3V</td><td>3.5V</td><td>3.8V</td><td>4.1V</td></tr>
<tr><td>High</td><td>5V</td><td>5.3V</td><td>5.7V</td><td>6.1V</td></tr>
<tr><td>Float</td><td>12V</td><td>13.45V</td><td>14.05V</td><td>14.65V</td></tr>
</table></td></tr>
<tr><td>SGND</td><td>5</td><td>Signal Ground pin.</td></tr>
<tr><td>ADR</td><td>6</td><td>I^2C address selection pin. Pull ADR pin to HIGH by connecting a resistor to IN, or pull ADR pin to LOW by connecting a resistor to ground, or float ADR Pin to select different I^2C address. If ADR pin is pulled high, the I^2C address is 59H. If ADR pin is pulled low, the I^2C address is 5AH. If ADR pin is floated, the I^2C address is 5BH;</td></tr>
<tr><td>DLY</td><td>7</td><td>Reverse blocking switch turn on delay time program pin. Connect a capacitor to GND to program reverse blocking switch turn-on delay time.</td></tr>
<tr><td>PD</td><td>8</td><td>Boost mode pre-charge done indicator pin. This pin is an open drain output. PD is pulled high if pre-charge not done, and is pulled low when pre-charge is done</td></tr>
<tr><td>FBS</td><td>9</td><td>Energy storage capacitor voltage feedback pin. Connect resistor divider to this pin to program the storage voltage. The internal reference is 1.1V for CV mode and 1.2V for burst Mode. If the resistor connected between FBS and GND is R1, the resistor connected between STR and FBS is R2, then the programmed STR CV voltage is V_{STR}=1.1*(1+R2/R1).</td></tr>
<tr><td>BUSPG</td><td>10</td><td>BUS voltage power good indicator pin. This pin is an open drain output. BUSPG is pulled low if voltage on FBD pin falls below 0.6V, and is pulled high when voltage on FBR pin exceeds 0.63V.</td></tr>
<tr><td>STRPG</td><td>11</td><td>STR voltage power good indicator pin. This pin is an open drain output. STRPG is pulled low if voltage on FBS pin falls below 1V, and is pulled high when voltage on FBS pin exceeds 1.05V.</td></tr>
<tr><td>BST</td><td>12</td><td>Boost-Strap pin for bi-directional DC-DC converter to supply high side FET’s gate driver. Connect a MLCC cap at least 0.1uF from this pin to LX.</td></tr>
<tr><td>SS</td><td>13</td><td>Reverse blocking switch soft start program pin. Using external capacitor to program the soft start time.</td></tr>
<tr><td>FBD</td><td>14</td><td>Buck mode detection feedback pin. The bi-directional converter will enter buck mode when voltage on FBD falls to below 0.6V. Using external resistor divider to program the buck mode detection point.</td></tr>
<tr><td>PGND</td><td>15,22</td><td>Power Ground pin.</td></tr>
<tr><td>STR</td><td>16,17,18</td><td>Energy storage capacitor pin. Connect to the energy storage capacitor. Decouple this pin to GND with at least 2.2uF MLCC cap with enough voltage rating.</td></tr>
<tr><td>VCC</td><td>19</td><td>Output of internal 3.3V LDO. Decouple this pin to GND with at least 1uF MLCC cap.</td></tr>
<tr><td>BD</td><td>20</td><td>Connect to the Drain of internal Disconnect FET. Also the input pin of step down DC-DC converter. Decouple this pin to GND with at least 2.2uF MLCC cap with enough voltage rating.</td></tr>
<tr><td>LX</td><td>21</td><td>Switching node pin. Connect to external inductor.</td></tr>
<tr><td>ENA</td><td>23</td><td>Enable control for input load switch. High logic to enable the load switch.</td></tr>
<tr><td>BUS</td><td>24</td><td>BUS voltage output pin. Decouple this pin to GND pin with at least 66uF MLCC cap.</td></tr>
<tr><td>IN</td><td>25</td><td>Input power supply. Decouple this pin to GND with at least 0.1uF MLCC cap.</td></tr>
</table>

Block Diagram



Absolute Maximum Ratings (Note 1)

STR, BD, LX, BST, FBS---------- -0.3V to 38V
IN, BUS, BUSPG, PD, OVP, STRPG, FBD, FBR, ENA, BD-STR---------- -0.3V to 18V
SS, SCL, DLY, ADR, SDA---------- -0.3V to 6V
VCC, BST-LX---------- -0.3V to 4V
Power Dissipation, P_D @ T_A = 25°C QFN4×4-25 ---------- 1.5W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 82°C/W
θ_{JC} ---------- 10.7°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

STR, BD, LX, BST, FBS---------- -0.3V to 36V
IN, BUS, BUSPG, PD, OVP, STRPG, FBD, FBR, ENA, BD-STR---------- -0.3V to 16V
SS, SCL, DLY, ADR, SDA----------0.3V to 5V
VCC, BST-LX---------- -0.3V to 3.3V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, V_{BUS} = 5V, L = 4.7uH, V_{BD}=V_{STR}=12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OVP Switch Part						
Input Voltage Range	V_{IN}		2.6		16	V
Input UVLO Rising Threshold	V_{UVLOR}	OVP=LOW	2.4		2.6	V
		OVP=HIGH	3.4		3.7	
		OVP=FLOATING	8.25		8.85	
Input UVLO Falling Threshold	V_{UVLOF}	OVP=LOW	2.0		2.4	V
		OVP=HIGH	3.2		3.5	
		OVP= FLOATING	7.55		8.25	
On Resistance of Reverse Blocking FET	$R_{DS(ON)R}$			24	34	mΩ
Reverse blocking Current	I_{RB}	V_{IN}=0V, V_{BUS}=16V, V_{ENA}=0V		2	5	μA
Bias Current	I_{BIAS}	V_{IN}=5V, V_{ENCON}=0V		750		μA
Reverse blocking Range	V_{RB}				16	V
Input Over Voltage Threshold	V_{OVPTH}	OVP=LOW	3.5	3.8	4.1	V
		OVP=HIGH	5.3	5.7	6.1	V
		OVP= FLOATING	13.45	14.05	14.65	V
Input OVP Clamp Voltage	V_{OVP_Clamp}	OVP=LOW	3.5	3.8	4.1	V
		OVP=HIGH	5.3	5.7	6.1	V
		OVP= FLOATING	13.45	14.05	14.65	V
Input Over Voltage Threshold Hysteresis	V_{OVP_HYS}	OVP=LOW		140		mV
		OVP=HIGH		190		mV
		OVP= FLOATING		400		mV
Switch Turn On Delay Time	T_{DLY}	C_{DLY}=105nF(Note 5)		29.4		ms
Soft-start Time	T_{SS}	C_{SS}=105nF(Note 6)		14.7		ms
Current Limit Program Range	I_{LIM}		1.2		6.2	A
Current Limit Accuracy			-10%I_{LIM}			
BUSPG Threshold	V_{BUSPGH}	V_{FBR} Rising		0.63		V
	V_{BUSPGL}	V_{FBD} Falling		0.6		V
Internal LDO Output Voltage	V_{VCC}	V_{IN}>3.3V		3.3		V
		V_{IN}<=3.3V		V_{IN}		
ENA Logic	V_{ENAH}		1.5			V
	V_{ENAL}				0.4	V
Bi-Directional DC-DC Regulator Part						
Operation Voltage Range	V_{BUSOP}		2.6		16	V
BUS Operation Falling UVLO Threshold	$V_{BUSUVLO}$		2.2	2.4	2.6	V
Buck Operation Voltage Range	V_{STROP}		2.6		36	V
$R_{DS(ON)}$ of High Side FET	$R_{DS(ON)H1}$			70		mΩ
$R_{DS(ON)}$ of Low Side FET	$R_{DS(ON)L1}$			70		mΩ
$R_{DS(ON)}$ of Disconnect FET	$R_{DS(ON)D}$			37		mΩ
Boost Minimum Peak Current	I_{PMIN}			300		mA
Boost/Buck Mode Switching Frequency	F_{SWBST}	SF[1:0]=01		500		kHz

LSFET Min ON Time	$t_{OFF,MINL}$	Boost Mode		80		ns
HSFET Min ON Time	$t_{ON,MINL}$	I_{PMIN}>1A		100	120	ns
Burst Mode Boost OVP Threshold	V_{OVPBST}	V_{FBS} Rising		1.2		V
Burst Mode Boost OVP Release Threshold	V_{OVPBST}	V_{FBS} Falling		1.17		V
Burst Mode Boost OVP Threshold Accuracy		Burst Mode		±2.7 %		
CV Mode Boost OVP Rising Threshold	V_{OVPBST}	FBS Rising		1.2		V
CV Mode Boost OVP Falling Threshold	V_{OVPBST}	FBS Falling		1.17		V
CV Mode Boost Regulation Voltage Reference	V_{FBS}			1.1		V
CV Mode Boost Regulation Voltage Reference Accuracy				±1.5 %		
STRPG Threshold	V_{STRPGH}	V_{FBS} Rising		1.05		V
	V_{STRPGL}	V_{FBS} Falling		1		V
STR Short Circuit Threshold	V_{STRSC}			1.2		V
Pre-charge Current	I_{PRECHG}			160		mA
Boost Detection Voltage Reference	V_{MCHGH}	V_{FBR} Rising	0.62	0.635	0.65	V
Buck Detection Voltage Reference	V_{BUCK_DET}	V_{FBD} Falling	0.588	0.6	0.612	V
Buck Regulation Voltage Reference	V_{BUCK_REG}		0.593	0.6	0.607	V
Maximum Buck Peak Current				8		A
LSFET Min ON Time	$t_{OFF,MINL}$	Buck Mode		80		ns
HSFET Min ON Time	$t_{ON,MINL}$	Buck Mode		80		ns
Capacitance Measurement Part						
Capacitance Measurement Discharge Current	$I_{DISCHARGE}$	DCP[7:6]=11		20		mA
Internal Counter Clock	f_{CLK}			8000		Hz
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Recovery Hysteresis	T_{HYS}			15		°C
I²C Control						
Input Voltage	$V_{IH,I2C}$	SCL, SDA Logic-High	1.6	--	--	V
	$V_{IL,I2C}$	SCL, SDA Logic-Low	--	--	0.4	
Low Period of SCL	t_{LOW}		1.3	--	--	µs
High Period of SCL	t_{HIGH}		0.6	--	--	µs
SCL Clock Frequency	f_{SCL}		--	--	400	kHz
I2C Clock	t_{SCHi}	High-Level	0.6	--	--	µs
	t_{SCLo}	Low-Level	1.2	--	--	
I2C Data Set-up Time	$t_{SU,DAT}$		100	--	--	ns
I2C Data Hold Time	$t_{HD,DAT}$		0	--	900	ns
SDA and SCL Rising Time	t_R		--	--	1000	ns
SDA and SCL Falling Time	t_F		--	--	300	ns
SDA and SCL Input Capacitance			5	pF		
Start Condition of Setup Time	$t_{SU,STA}$		0.6	--	--	ns

Start Condition of Hold Time	$t_{HD,STA}$	10% of SDA to 90% of SCL	0.6	--	--	ns
Stop Condition of Setup Time	$t_{SU,STO}$		0.6	--	--	ns
I2C Input Filter Spike Suppression	t_{SP}		0	--	50	ns
Minimum Bus Free Time Between Stop to Start	t_{BUF}		4.7	--	--	μs

Note 1: Stresses beyond "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Exposed pad of QFN4×4-25 packages is the case position for θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: V_{STR-P} is programmed STR voltage.

Note5. Recommended Delay Time Program Table

DLY cap (nF)	None	10	55	105
Delay time (ms)	1.4	2.8	15.4	29.4

Note6. Recommended Soft-start Time Program Table

SS cap (nF)	None	10	55	105
Rise time (ms)	1	1.4	7.7	14.7

Recommended Formula for C_{SS} & Soft-start Time Calculation

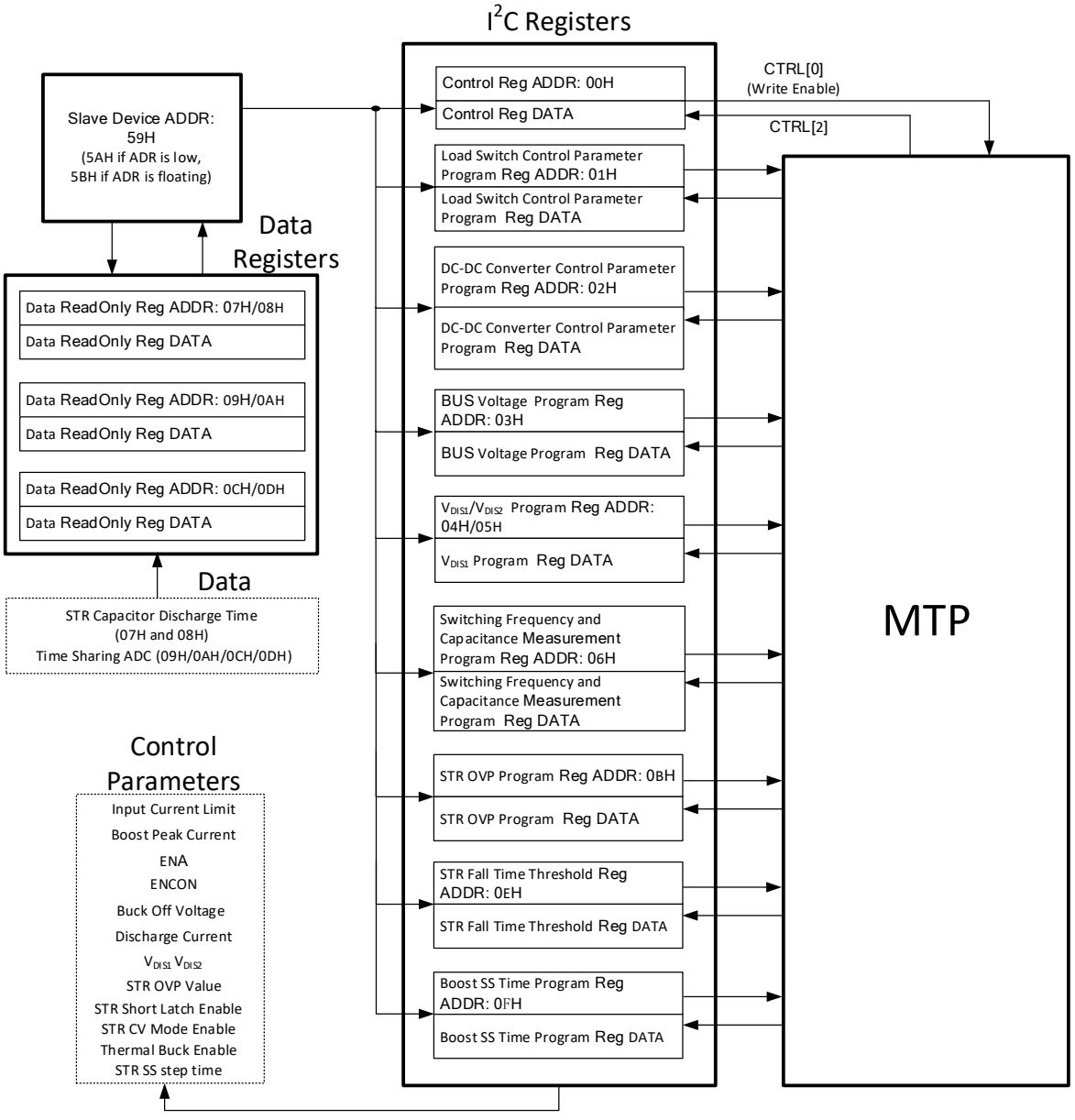
$$T_{SS} = \begin{cases} T_{SS\_DLT}, & \text{No external } C_{SS} \\ \dfrac{C_{SS}}{I_{INT\_SS}}, & T_{SS} > T_{SS\_DLT} \end{cases},$$

Where, TSS_DLT is the internally fixed default soft-start time, about 1ms, which means there's no any external C_{SS}; I_{INT_SS} is the internal current source, about 7.2uA.

Note 7: The typical value of thermal shut down recovery hysteresis is design guaranteed. Recommend to leave enough margin for the application design consideration.

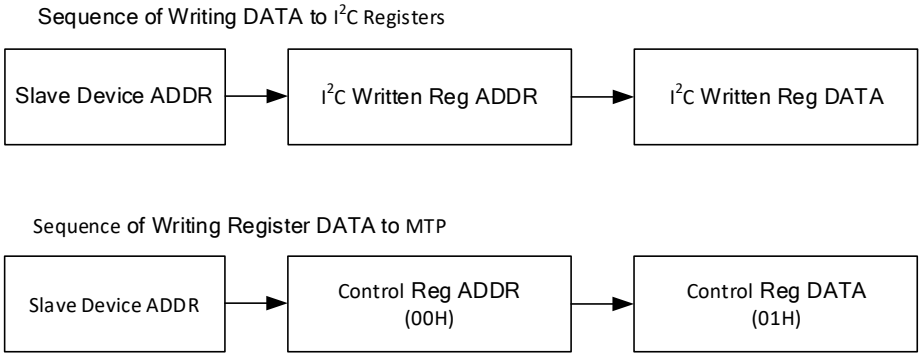
Control Parameters Programming Block Diagram, Register and Data

Block Diagram



NOTE: Internal current source discharge STR capacitor during capacitance measurement. The counter starts counting when STR voltage falls to V_{DIS1} and stops counting when STR voltage falls to V_{DIS2}.

Control Parameters Programming Sequence



NOTE: All the data in I²C registers is written to MTP when CTRL[0] is set to 1. All the data reserved in MTP is loaded to I²C registers when IC power up. Please make sure CTRL[2] is 0 before writing data to MTP.

- **Register Map Summary**

Register Address	Register name	Default Value (HEX)	Register Description	MTP Storage
0x00	MTP_CTRL	0x00	Controls MTP writing and reading	N
0x01	LSW_REG	0xB9	Input Load Switch setting register	Y
0x02	DC_DC_REG	0xC7	DC_DC Converter setting register	Y
0x03	BCK_OFF_REG	0x37	Buck off voltage program register	Y
0x04	VDIS1_REG	0x46	Capacitance detection start voltage	Y
0x05	VDIS2_REG	0x2F	Capacitance detection end voltage	Y
0x06	SF_REG	0x11	PLP Switching Frequency program register	Y
0x07	TDISH_REG	0x00	High 8-bit discharge time ADC register	N
0x08	TDISL_REG	0x00	Low 8-bit discharge time ADC register	N
0x09	LSC_REG	0x00	Load switch current ADC register	N
0x0A	BUS_REG	0x00	BUS voltage ADC register	N
0x0B	OVP_REG	0x17	STR OVP program register	Y
0x0C	IN_REG	0x00	IN voltage ADC register	N
0x0D	STR_REG	0x00	STR voltage ADC register	N
0x0E	TIMF_REG	0x00	STR fall time fault threshold register	Y
0x0F	Tstep_REG	0x01	PLP Boost soft start step time program register	Y

Register and Data

- **Slave Device Address: 59H(5AH or 5BH)+W/R**
- **MTP Control Register Address: 00H**

This register controls the MTP writing and reading.

Register Name	MTP_CTRL_REG		MTP Control Register	
Address			0x00	
	R/W	Default	Description	
CTRL[0]	R/W	0	MTP Write Control	
			0=MTP Write Disable	1=MTP Write Enable Write Register code to MTP, this control bit would self-clear to 0, when MTP write finished.
CTRL[1]	R/W	0	MTP Read Control	
			0=MTP Read Disable	1=MTP Read Enable Load MTP code to relevant register, this control bit would self-clear to 0, when MTP code load finished.
CTRL[7:2]	R/W	000000	Reserved	

- **Load Switch Control Parameter Program Register Address: 01H**

This register controls the Load Switch Parameter.

Register Name	LSW_CTRL_REG		LSW Control Register			
Address			0x01			
	R/W	Default	Description			
LSP[0]	R/W	1	Input Load Switch & PLP Enable Control			
			0= disable		1= enable	
LSP[1]	R/W	0	IN OVP Clamp Enable Control			
			0= Load Switch Shutdown & PLP on When IN OVP		1=Load Switch Clamp When IN OVP	
LSP[2]	R/W	0	Thermal condition Buck on/off control			
			0 = Buck is off when thermal		1 = Buck is on when thermal	
LSP[5:3]	R/W	111	Load Switch Current Limit			
			000=1.2A	001=2A	010=2.5A	011=3A
			100=3.5A	101=4A	110=4.5A	111=6.2A
LSP[6]	R/W	0	Load Switch Soft Shutdown control			
			0=LSW Soft shutdown disable		1=LSW Soft shutdown enable	
LSP[7]	R/W	1	ADC enable control			
			0=ADC is disabled		1=ADC is enabled	

- **DC-DC Converter Control Parameter Program Register Address: 02H**

This register controls the DC-DC Converter Parameter.

Register Name	PLP_CTRL_REG		PLP Control Register			
Address			0x02			
	R/W	Default	Description			
DCP[0]	R/W	1	PLP Enable Control			
			0= PLP is disabled		1=PLP is enabled	
DCP[3:1]	R/W	011	Boost Peak current control			
			000=300mA	001=500mA	010=600mA	011=800mA
			100=1A	101=1.5A	110=2A	111=2.5A
DCP[4]	R/W	0	PLP boost soft start control bit when set to '1' PLP charges STRG capacitor with maximum allowed inductor peak current REG0x0F function is disabled			
			0= PLP boost soft start is enabled		1= PLP boost soft start is disabled	
DCP[5]	R/W	0	Reserved			
DCP[7:6]	R/W	11	Capacitance measurement discharge current control			
			00=2.24mA	01=5.27mA	10=10mA	11=20mA

◆ Buck Off Voltage Program Register Address: 03H

This register controls Buck off voltage.

Register Name	BUCK_OFF_REG		Buck Off Voltage Register							
Address			0x03							
	R/W	Default	Description							
OFF[7:0]	R/W	00110111	Customer programmable threshold. When STR< this threshold during PLP release, PLP will stop switching							
			Hex Code	Voltage (V)	Hex Code	Voltage (V)	Hex Code	Voltage (V)	Hex Code	Voltage (V)
			0x00	0.000	0x40	3.072	0x80	6.144	0xC0	9.216
			0x01	0.048	0x41	3.120	0x81	6.192	0xC1	9.264
			0x02	0.096	0x42	3.168	0x82	6.240	0xC2	9.312
			0x03	0.144	0x43	3.216	0x83	6.288	0xC3	9.360
			0x04	0.192	0x44	3.264	0x84	6.336	0xC4	9.408
			0x05	0.240	0x45	3.312	0x85	6.384	0xC5	9.456
			0x06	0.288	0x46	3.360	0x86	6.432	0xC6	9.504
			0x07	0.336	0x47	3.408	0x87	6.480	0xC7	9.552
			0x08	0.384	0x48	3.456	0x88	6.528	0xC8	9.600
			0x09	0.432	0x49	3.504	0x89	6.576	0xC9	9.648
			0x0A	0.480	0x4A	3.552	0x8A	6.624	0xCA	9.696
			0x0B	0.528	0x4B	3.600	0x8B	6.672	0xCB	9.744
			0x0C	0.576	0x4C	3.648	0x8C	6.720	0xCC	9.792
			0x0D	0.624	0x4D	3.696	0x8D	6.768	0xCD	9.840
			0x0E	0.672	0x4E	3.744	0x8E	6.816	0xCE	9.888
			0x0F	0.720	0x4F	3.792	0x8F	6.864	0xCF	9.936
			0x10	0.768	0x50	3.840	0x90	6.912	0xD0	9.984
			0x11	0.816	0x51	3.888	0x91	6.960	0xD1	10.032
			0x12	0.864	0x52	3.936	0x92	7.008	0xD2	10.080
			0x13	0.912	0x53	3.984	0x93	7.056	0xD3	10.128
			0x14	0.960	0x54	4.032	0x94	7.104	0xD4	10.176
			0x15	1.008	0x55	4.080	0x95	7.152	0xD5	10.224
			0x16	1.056	0x56	4.128	0x96	7.200	0xD6	10.272
			0x17	1.104	0x57	4.176	0x97	7.248	0xD7	10.320
			0x18	1.152	0x58	4.224	0x98	7.296	0xD8	10.368
			0x19	1.200	0x59	4.272	0x99	7.344	0xD9	10.416
			0x1A	1.248	0x5A	4.320	0x9A	7.392	0xDA	10.464
			0x1B	1.296	0x5B	4.368	0x9B	7.440	0xDB	10.512
			0x1C	1.344	0x5C	4.416	0x9C	7.488	0xDC	10.560
			0x1D	1.392	0x5D	4.464	0x9D	7.536	0xDD	10.608
			0x1E	1.440	0x5E	4.512	0x9E	7.584	0xDE	10.656
			0x1F	1.488	0x5F	4.560	0x9F	7.632	0xDF	10.704
			0x20	1.536	0x60	4.608	0xA0	7.680	0xE0	10.752
			0x21	1.584	0x61	4.656	0xA1	7.728	0xE1	10.800
			0x22	1.632	0x62	4.704	0xA2	7.776	0xE2	10.848
			0x23	1.680	0x63	4.752	0xA3	7.824	0xE3	10.896
			0x24	1.728	0x64	4.800	0xA4	7.872	0xE4	10.944
			0x25	1.776	0x65	4.848	0xA5	7.920	0xE5	10.992
			0x26	1.824	0x66	4.896	0xA6	7.968	0xE6	11.040
			0x27	1.872	0x67	4.944	0xA7	8.016	0xE7	11.088
			0x28	1.920	0x68	4.992	0xA8	8.064	0xE8	11.136
			0x29	1.968	0x69	5.040	0xA9	8.112	0xE9	11.184
			0x2A	2.016	0x6A	5.088	0xAA	8.160	0xEA	11.232
			0x2B	2.064	0x6B	5.136	0xAB	8.208	0xEB	11.280
			0x2C	2.112	0x6C	5.184	0xAC	8.256	0xEC	11.328
			0x2D	2.160	0x6D	5.232	0xAD	8.304	0xED	11.376
			0x2E	2.208	0x6E	5.280	0xAE	8.352	0xEE	11.424
			0x2F	2.256	0x6F	5.328	0xAF	8.400	0xEF	11.472
			0x30	2.304	0x70	5.376	0xB0	8.448	0xF0	11.520
			0x31	2.352	0x71	5.424	0xB1	8.496	0xF1	11.568
			0x32	2.400	0x72	5.472	0xB2	8.544	0xF2	11.616
			0x33	2.448	0x73	5.520	0xB3	8.592	0xF3	11.664
			0x34	2.496	0x74	5.568	0xB4	8.640	0xF4	11.712
			0x35	2.544	0x75	5.616	0xB5	8.688	0xF5	11.760

			0x36	2.592	0x76	5.664	0xB6	8.736	0xF6	11.808
			0x37	2.640	0x77	5.712	0xB7	8.784	0xF7	11.856
			0x38	2.688	0x78	5.760	0xB8	8.832	0xF8	11.904
			0x39	2.736	0x79	5.808	0xB9	8.880	0xF9	11.952
			0x3A	2.784	0x7A	5.856	0xBA	8.928	0xFA	12.000
			0x3B	2.832	0x7B	5.904	0xBB	8.976	0xFB	12.048
			0x3C	2.880	0x7C	5.952	0xBC	9.024	0xFC	12.096
			0x3D	2.928	0x7D	6.000	0xBD	9.072	0xFD	12.144
			0x3E	2.976	0x7E	6.048	0xBE	9.120	0xFE	12.192
			0x3F	3.024	0x7F	6.096	0xBF	9.168	0xFF	12.240

◆ V_{DIS1} Program Register Address: 04H

This register controls capacitance detection start voltage.

Register Name	VDIS1_REG		Capacitance Detection Start Voltage Register							
Address			0x04							
	R/W	Default	Description							
VDIS1[7:0]	R/W	01000110	Capacitance detection threshold 1. When STR< this threshold during Capacitance detection, Timing start							
			Hex Code	Voltage (V)	Hex Code	Voltage (V)	Hex Code	Voltage (V)	Hex Code	Voltage (V)
			0x00	0.000	0x40	9.600	0x80	19.200	0xC0	28.800
			0x01	0.150	0x41	9.750	0x81	19.350	0xC1	28.950
			0x02	0.300	0x42	9.900	0x82	19.500	0xC2	29.100
			0x03	0.450	0x43	10.050	0x83	19.650	0xC3	29.250
			0x04	0.600	0x44	10.200	0x84	19.800	0xC4	29.400
			0x05	0.750	0x45	10.350	0x85	19.950	0xC5	29.550
			0x06	0.900	0x46	10.500	0x86	20.100	0xC6	29.700
			0x07	1.050	0x47	10.650	0x87	20.250	0xC7	29.850
			0x08	1.200	0x48	10.800	0x88	20.400	0xC8	30.000
			0x09	1.350	0x49	10.950	0x89	20.550	0xC9	30.150
			0x0A	1.500	0x4A	11.100	0x8A	20.700	0xCA	30.300
			0x0B	1.650	0x4B	11.250	0x8B	20.850	0xCB	30.450
			0x0C	1.800	0x4C	11.400	0x8C	21.000	0xCC	30.600
			0x0D	1.950	0x4D	11.550	0x8D	21.150	0xCD	30.750
			0x0E	2.100	0x4E	11.700	0x8E	21.300	0xCE	30.900
			0x0F	2.250	0x4F	11.850	0x8F	21.450	0xCF	31.050
			0x10	2.400	0x50	12.000	0x90	21.600	0xD0	31.200
			0x11	2.550	0x51	12.150	0x91	21.750	0xD1	31.350
			0x12	2.700	0x52	12.300	0x92	21.900	0xD2	31.500
			0x13	2.850	0x53	12.450	0x93	22.050	0xD3	31.650
			0x14	3.000	0x54	12.600	0x94	22.200	0xD4	31.800
			0x15	3.150	0x55	12.750	0x95	22.350	0xD5	31.950
			0x16	3.300	0x56	12.900	0x96	22.500	0xD6	32.100
			0x17	3.450	0x57	13.050	0x97	22.650	0xD7	32.250
			0x18	3.600	0x58	13.200	0x98	22.800	0xD8	32.400
			0x19	3.750	0x59	13.350	0x99	22.950	0xD9	32.550
			0x1A	3.900	0x5A	13.500	0x9A	23.100	0xDA	32.700
			0x1B	4.050	0x5B	13.650	0x9B	23.250	0xDB	32.850
			0x1C	4.200	0x5C	13.800	0x9C	23.400	0xDC	33.000
			0x1D	4.350	0x5D	13.950	0x9D	23.550	0xDD	33.150
			0x1E	4.500	0x5E	14.100	0x9E	23.700	0xDE	33.300
			0x1F	4.650	0x5F	14.250	0x9F	23.850	0xDF	33.450
			0x20	4.800	0x60	14.400	0xA0	24.000	0xE0	33.600
			0x21	4.950	0x61	14.550	0xA1	24.150	0xE1	33.750
			0x22	5.100	0x62	14.700	0xA2	24.300	0xE2	33.900
			0x23	5.250	0x63	14.850	0xA3	24.450	0xE3	34.050
			0x24	5.400	0x64	15.000	0xA4	24.600	0xE4	34.200
			0x25	5.550	0x65	15.150	0xA5	24.750	0xE5	34.350
			0x26	5.700	0x66	15.300	0xA6	24.900	0xE6	34.500
			0x27	5.850	0x67	15.450	0xA7	25.050	0xE7	34.650
			0x28	6.000	0x68	15.600	0xA8	25.200	0xE8	34.800
			0x29	6.150	0x69	15.750	0xA9	25.350	0xE9	34.950
			0x2A	6.300	0x6A	15.900	0xAA	25.500	0xEA	35.100

			0x2B	6.450	0x6B	16.050	0xAB	25.650	0xEB	35.250
			0x2C	6.600	0x6C	16.200	0xAC	25.800	0xEC	35.400
			0x2D	6.750	0x6D	16.350	0xAD	25.950	0xED	35.550
			0x2E	6.900	0x6E	16.500	0xAE	26.100	0xEE	35.700
			0x2F	7.050	0x6F	16.650	0xAF	26.250	0xEF	35.850
			0x30	7.200	0x70	16.800	0xB0	26.400	0xF0	36.000
			0x31	7.350	0x71	16.950	0xB1	26.550	0xF1	36.150
			0x32	7.500	0x72	17.100	0xB2	26.700	0xF2	36.300
			0x33	7.650	0x73	17.250	0xB3	26.850	0xF3	36.450
			0x34	7.800	0x74	17.400	0xB4	27.000	0xF4	36.600
			0x35	7.950	0x75	17.550	0xB5	27.150	0xF5	36.750
			0x36	8.100	0x76	17.700	0xB6	27.300	0xF6	36.900
			0x37	8.250	0x77	17.850	0xB7	27.450	0xF7	37.050
			0x38	8.400	0x78	18.000	0xB8	27.600	0xF8	37.200
			0x39	8.550	0x79	18.150	0xB9	27.750	0xF9	37.350
			0x3A	8.700	0x7A	18.300	0xBA	27.900	0xFA	37.500
			0x3B	8.850	0x7B	18.450	0xBB	28.050	0xFB	37.650
			0x3C	9.000	0x7C	18.600	0xBC	28.200	0xFC	37.800
			0x3D	9.150	0x7D	18.750	0xBD	28.350	0xFD	37.950
			0x3E	9.300	0x7E	18.900	0xBE	28.500	0xFE	38.100
			0x3F	9.450	0x7F	19.050	0xBF	28.650	0xFF	38.250

◆ **V_{DIS2} Program Register Address: 05H**

This register controls capacitance detection end voltage.

Register Name	VDIS2_REG		Capacitance Detection END Voltage Register							
Address			0x05							
	R/W	Default	Description							
VDIS2[7:0]	R/W	00101111	Capacitance detection threshold 2. When STR< this threshold during Capacitance detection, Timing ends.							
			Hex Code	Voltage (V)	Hex Code	Voltage (V)	Hex Code	Voltage (V)	Hex Code	Voltage (V)
			0x00	0.000	0x40	9.600	0x80	19.200	0xC0	28.800
			0x01	0.150	0x41	9.750	0x81	19.350	0xC1	28.950
			0x02	0.300	0x42	9.900	0x82	19.500	0xC2	29.100
			0x03	0.450	0x43	10.050	0x83	19.650	0xC3	29.250
			0x04	0.600	0x44	10.200	0x84	19.800	0xC4	29.400
			0x05	0.750	0x45	10.350	0x85	19.950	0xC5	29.550
			0x06	0.900	0x46	10.500	0x86	20.100	0xC6	29.700
			0x07	1.050	0x47	10.650	0x87	20.250	0xC7	29.850
			0x08	1.200	0x48	10.800	0x88	20.400	0xC8	30.000
			0x09	1.350	0x49	10.950	0x89	20.550	0xC9	30.150
			0x0A	1.500	0x4A	11.100	0x8A	20.700	0xCA	30.300
			0x0B	1.650	0x4B	11.250	0x8B	20.850	0xCB	30.450
			0x0C	1.800	0x4C	11.400	0x8C	21.000	0xCC	30.600
			0x0D	1.950	0x4D	11.550	0x8D	21.150	0xCD	30.750
			0x0E	2.100	0x4E	11.700	0x8E	21.300	0xCE	30.900
			0x0F	2.250	0x4F	11.850	0x8F	21.450	0xCF	31.050
			0x10	2.400	0x50	12.000	0x90	21.600	0xD0	31.200
			0x11	2.550	0x51	12.150	0x91	21.750	0xD1	31.350
			0x12	2.700	0x52	12.300	0x92	21.900	0xD2	31.500
			0x13	2.850	0x53	12.450	0x93	22.050	0xD3	31.650
			0x14	3.000	0x54	12.600	0x94	22.200	0xD4	31.800
			0x15	3.150	0x55	12.750	0x95	22.350	0xD5	31.950
			0x16	3.300	0x56	12.900	0x96	22.500	0xD6	32.100
			0x17	3.450	0x57	13.050	0x97	22.650	0xD7	32.250
			0x18	3.600	0x58	13.200	0x98	22.800	0xD8	32.400
			0x19	3.750	0x59	13.350	0x99	22.950	0xD9	32.550
			0x1A	3.900	0x5A	13.500	0x9A	23.100	0xDA	32.700
			0x1B	4.050	0x5B	13.650	0x9B	23.250	0xDB	32.850
			0x1C	4.200	0x5C	13.800	0x9C	23.400	0xDC	33.000
			0x1D	4.350	0x5D	13.950	0x9D	23.550	0xDD	33.150
			0x1E	4.500	0x5E	14.100	0x9E	23.700	0xDE	33.300
			0x1F	4.650	0x5F	14.250	0x9F	23.850	0xDF	33.450

			0x20	4.800	0x60	14.400	0xA0	24.000	0xE0	33.600
			0x21	4.950	0x61	14.550	0xA1	24.150	0xE1	33.750
			0x22	5.100	0x62	14.700	0xA2	24.300	0xE2	33.900
			0x23	5.250	0x63	14.850	0xA3	24.450	0xE3	34.050
			0x24	5.400	0x64	15.000	0xA4	24.600	0xE4	34.200
			0x25	5.550	0x65	15.150	0xA5	24.750	0xE5	34.350
			0x26	5.700	0x66	15.300	0xA6	24.900	0xE6	34.500
			0x27	5.850	0x67	15.450	0xA7	25.050	0xE7	34.650
			0x28	6.000	0x68	15.600	0xA8	25.200	0xE8	34.800
			0x29	6.150	0x69	15.750	0xA9	25.350	0xE9	34.950
			0x2A	6.300	0x6A	15.900	0xAA	25.500	0xEA	35.100
			0x2B	6.450	0x6B	16.050	0xAB	25.650	0xEB	35.250
			0x2C	6.600	0x6C	16.200	0xAC	25.800	0xEC	35.400
			0x2D	6.750	0x6D	16.350	0xAD	25.950	0xED	35.550
			0x2E	6.900	0x6E	16.500	0xAE	26.100	0xEE	35.700
			0x2F	7.050	0x6F	16.650	0xAF	26.250	0xEF	35.850
			0x30	7.200	0x70	16.800	0xB0	26.400	0xF0	36.000
			0x31	7.350	0x71	16.950	0xB1	26.550	0xF1	36.150
			0x32	7.500	0x72	17.100	0xB2	26.700	0xF2	36.300
			0x33	7.650	0x73	17.250	0xB3	26.850	0xF3	36.450
			0x34	7.800	0x74	17.400	0xB4	27.000	0xF4	36.600
			0x35	7.950	0x75	17.550	0xB5	27.150	0xF5	36.750
			0x36	8.100	0x76	17.700	0xB6	27.300	0xF6	36.900
			0x37	8.250	0x77	17.850	0xB7	27.450	0xF7	37.050
			0x38	8.400	0x78	18.000	0xB8	27.600	0xF8	37.200
			0x39	8.550	0x79	18.150	0xB9	27.750	0xF9	37.350
			0x3A	8.700	0x7A	18.300	0xBA	27.900	0xFA	37.500
			0x3B	8.850	0x7B	18.450	0xBB	28.050	0xFB	37.650
			0x3C	9.000	0x7C	18.600	0xBC	28.200	0xFC	37.800
			0x3D	9.150	0x7D	18.750	0xBD	28.350	0xFD	37.950
			0x3E	9.300	0x7E	18.900	0xBE	28.500	0xFE	38.100
			0x3F	9.450	0x7F	19.050	0xBF	28.650	0xFF	38.250

◆ Switching Frequency Program Register Address: 06H

This register controls the PLP Switching Frequency Parameter.

Register Name	SF_CTRL_REG		Switching Frequency Control Register	
Address			0x06	
	R/W	Default	Description	
SF[1:0]	R/W	01	PLP switching frequency	
			00=250kHz	01=500kHz
			10=1MHz	11=1.5MHz
SF[2]	R/W	0	Reserved	
SF[3]	R/W	0	Reserved	
SF[4]	R/W	1	Boost CV/Burst mode select	
			0 = Burst Mode	1 = CV Mode
SF[5]	R/W	0	Capacitance Measurement Enable control	
			Capacitance measurement starts when SF[5] changes from 0 to 1	
SF[6]	R/W	0	Reverse blocking enable control	
			0=Reverse blocking(VBUS-VIN>20mv) function is enabled	1=Reverse blocking(VBUS-VIN>20mv) function is disabled
SF[7]	R/W	0	Super Capacitor Pre-charge Enable Bit	
			0 = Super Capacitor Pre-charge is enabled. When LSW soft start down, Bi-directional DC-DC starts boost charging with hiccup pre-charge mode; but the IC still latches and STR short flag bit goes to '1' when STR short detect(VSTR < VBUS-0.2V) after pre-charge done.	1=Super Capacitor Pre-charge is disabled. When LSW soft start down and Bi-directional DC-DC has pre-charged for about 125ms, If STR voltage is lower than 1.2V, the IC latches and STR short flag bit sets to '1'.

◆ **STR Voltage Discharge Time ADC Register Address(High): 07H**

This register records the STR voltage discharge time ADC value(high 8 bits).

Register Name	TimH_REG		STR discharge time ADC(High) Register							
Address			0x07							
	R/W	Default	Description							
TimH[7:0]	R	00000000	High 8 bits for discharge time ADC value(T_{DIS_HI}), total discharge time can calculated with $T_{DIS\_total} = T_{DIS\_HI} + T_{DIS\_LOW}$							
			Hex Code	Time (ms)	Hex Code	Time (ms)	Hex Code	Time (ms)	Hex Code	Time (ms)
			0x00	0	0x40	2048	0x80	4096	0xC0	6144
			0x01	32	0x41	2080	0x81	4128	0xC1	6176
			0x02	64	0x42	2112	0x82	4160	0xC2	6208
			0x03	96	0x43	2144	0x83	4192	0xC3	6240
			0x04	128	0x44	2176	0x84	4224	0xC4	6272
			0x05	160	0x45	2208	0x85	4256	0xC5	6304
			0x06	192	0x46	2240	0x86	4288	0xC6	6336
			0x07	224	0x47	2272	0x87	4320	0xC7	6368
			0x08	256	0x48	2304	0x88	4352	0xC8	6400
			0x09	288	0x49	2336	0x89	4384	0xC9	6432
			0x0A	320	0x4A	2368	0x8A	4416	0xCA	6464
			0x0B	352	0x4B	2400	0x8B	4448	0xCB	6496
			0x0C	384	0x4C	2432	0x8C	4480	0xCC	6528
			0x0D	416	0x4D	2464	0x8D	4512	0xCD	6560
			0x0E	448	0x4E	2496	0x8E	4544	0xCE	6592
			0x0F	480	0x4F	2528	0x8F	4576	0xCF	6624
			0x10	512	0x50	2560	0x90	4608	0xD0	6656
			0x11	544	0x51	2592	0x91	4640	0xD1	6688
			0x12	576	0x52	2624	0x92	4672	0xD2	6720
			0x13	608	0x53	2656	0x93	4704	0xD3	6752
			0x14	640	0x54	2688	0x94	4736	0xD4	6784
			0x15	672	0x55	2720	0x95	4768	0xD5	6816
			0x16	704	0x56	2752	0x96	4800	0xD6	6848
			0x17	736	0x57	2784	0x97	4832	0xD7	6880
			0x18	768	0x58	2816	0x98	4864	0xD8	6912
			0x19	800	0x59	2848	0x99	4896	0xD9	6944
			0x1A	832	0x5A	2880	0x9A	4928	0xDA	6976
			0x1B	864	0x5B	2912	0x9B	4960	0xDB	7008
			0x1C	896	0x5C	2944	0x9C	4992	0xDC	7040
			0x1D	928	0x5D	2976	0x9D	5024	0xDD	7072
			0x1E	960	0x5E	3008	0x9E	5056	0xDE	7104
			0x1F	992	0x5F	3040	0x9F	5088	0xDF	7136
			0x20	1024	0x60	3072	0xA0	5120	0xE0	7168
			0x21	1056	0x61	3104	0xA1	5152	0xE1	7200
			0x22	1088	0x62	3136	0xA2	5184	0xE2	7232
			0x23	1120	0x63	3168	0xA3	5216	0xE3	7264
			0x24	1152	0x64	3200	0xA4	5248	0xE4	7296
			0x25	1184	0x65	3232	0xA5	5280	0xE5	7328
			0x26	1216	0x66	3264	0xA6	5312	0xE6	7360
			0x27	1248	0x67	3296	0xA7	5344	0xE7	7392
			0x28	1280	0x68	3328	0xA8	5376	0xE8	7424
			0x29	1312	0x69	3360	0xA9	5408	0xE9	7456
			0x2A	1344	0x6A	3392	0xAA	5440	0xEA	7488
			0x2B	1376	0x6B	3424	0xAB	5472	0xEB	7520
			0x2C	1408	0x6C	3456	0xAC	5504	0xEC	7552
			0x2D	1440	0x6D	3488	0xAD	5536	0xED	7584
			0x2E	1472	0x6E	3520	0xAE	5568	0xEE	7616
			0x2F	1504	0x6F	3552	0xAF	5600	0xEF	7648
			0x30	1536	0x70	3584	0xB0	5632	0xF0	7680
			0x31	1568	0x71	3616	0xB1	5664	0xF1	7712
			0x32	1600	0x72	3648	0xB2	5696	0xF2	7744
			0x33	1632	0x73	3680	0xB3	5728	0xF3	7776
			0x34	1664	0x74	3712	0xB4	5760	0xF4	7808
			0x35	1696	0x75	3744	0xB5	5792	0xF5	7840

			0x36	1728	0x76	3776	0xB6	5824	0xF6	7872
			0x37	1760	0x77	3808	0xB7	5856	0xF7	7904
			0x38	1792	0x78	3840	0xB8	5888	0xF8	7936
			0x39	1824	0x79	3872	0xB9	5920	0xF9	7968
			0x3A	1856	0x7A	3904	0xBA	5952	0xFA	8000
			0x3B	1888	0x7B	3936	0xBB	5984	0xFB	8032
			0x3C	1920	0x7C	3968	0xBC	6016	0xFC	8064
			0x3D	1952	0x7D	4000	0xBD	6048	0xFD	8096
			0x3E	1984	0x7E	4032	0xBE	6080	0xFE	8128
			0x3F	2016	0x7F	4064	0xBF	6112	0xFF	8160

◆ STR Voltage Discharge Time ADCRegister Address(Low): 08H

This register records the STR voltage discharge time ADC value(Low 8 bits).

Register Name	TimL_REG		STR discharge time ADC(Low) Register							
Address			0x08							
	R/W	Default	Description							
TimL[7:0]	R	00000000	Low 8 bits for discharge time ADC value(T_{DIS_LOW}), total discharge time can calculated with $T_{DIS\_total} = T_{DIS\_HI} + T_{DIS\_LOW}$							
			Hex Code	Time (ms)	Hex Code	Time (ms)	Hex Code	Time (ms)	Hex Code	Time (ms)
			0x00	0	0x40	8	0x80	16	0xC0	24
			0x01	0.125	0x41	8.125	0x81	16.125	0xC1	24.125
			0x02	0.25	0x42	8.25	0x82	16.25	0xC2	24.25
			0x03	0.375	0x43	8.375	0x83	16.375	0xC3	24.375
			0x04	0.5	0x44	8.5	0x84	16.5	0xC4	24.5
			0x05	0.625	0x45	8.625	0x85	16.625	0xC5	24.625
			0x06	0.75	0x46	8.75	0x86	16.75	0xC6	24.75
			0x07	0.875	0x47	8.875	0x87	16.875	0xC7	24.875
			0x08	1	0x48	9	0x88	17	0xC8	25
			0x09	1.125	0x49	9.125	0x89	17.125	0xC9	25.125
			0x0A	1.25	0x4A	9.25	0x8A	17.25	0xCA	25.25
			0x0B	1.375	0x4B	9.375	0x8B	17.375	0xCB	25.375
			0x0C	1.5	0x4C	9.5	0x8C	17.5	0xCC	25.5
			0x0D	1.625	0x4D	9.625	0x8D	17.625	0xCD	25.625
			0x0E	1.75	0x4E	9.75	0x8E	17.75	0xCE	25.75
			0x0F	1.875	0x4F	9.875	0x8F	17.875	0xCF	25.875
			0x10	2	0x50	10	0x90	18	0xD0	26
			0x11	2.125	0x51	10.125	0x91	18.125	0xD1	26.125
			0x12	2.25	0x52	10.25	0x92	18.25	0xD2	26.25
			0x13	2.375	0x53	10.375	0x93	18.375	0xD3	26.375
			0x14	2.5	0x54	10.5	0x94	18.5	0xD4	26.5
			0x15	2.625	0x55	10.625	0x95	18.625	0xD5	26.625
			0x16	2.75	0x56	10.75	0x96	18.75	0xD6	26.75
			0x17	2.875	0x57	10.875	0x97	18.875	0xD7	26.875
			0x18	3	0x58	11	0x98	19	0xD8	27
			0x19	3.125	0x59	11.125	0x99	19.125	0xD9	27.125
			0x1A	3.25	0x5A	11.25	0x9A	19.25	0xDA	27.25
			0x1B	3.375	0x5B	11.375	0x9B	19.375	0xDB	27.375
			0x1C	3.5	0x5C	11.5	0x9C	19.5	0xDC	27.5
			0x1D	3.625	0x5D	11.625	0x9D	19.625	0xDD	27.625
			0x1E	3.75	0x5E	11.75	0x9E	19.75	0xDE	27.75
			0x1F	3.875	0x5F	11.875	0x9F	19.875	0xDF	27.875
			0x20	4	0x60	12	0xA0	20	0xE0	28
			0x21	4.125	0x61	12.125	0xA1	20.125	0xE1	28.125
			0x22	4.25	0x62	12.25	0xA2	20.25	0xE2	28.25
			0x23	4.375	0x63	12.375	0xA3	20.375	0xE3	28.375
			0x24	4.5	0x64	12.5	0xA4	20.5	0xE4	28.5
			0x25	4.625	0x65	12.625	0xA5	20.625	0xE5	28.625
			0x26	4.75	0x66	12.75	0xA6	20.75	0xE6	28.75
			0x27	4.875	0x67	12.875	0xA7	20.875	0xE7	28.875
			0x28	5	0x68	13	0xA8	21	0xE8	29
			0x29	5.125	0x69	13.125	0xA9	21.125	0xE9	29.125
			0x2A	5.25	0x6A	13.25	0xAA	21.25	0xEA	29.25

			0x2B	5.375	0x6B	13.375	0xAB	21.375	0xEB	29.375
			0x2C	5.5	0x6C	13.5	0xAC	21.5	0xEC	29.5
			0x2D	5.625	0x6D	13.625	0xAD	21.625	0xED	29.625
			0x2E	5.75	0x6E	13.75	0xAE	21.75	0xEE	29.75
			0x2F	5.875	0x6F	13.875	0xAF	21.875	0xEF	29.875
			0x30	6	0x70	14	0xB0	22	0xF0	30
			0x31	6.125	0x71	14.125	0xB1	22.125	0xF1	30.125
			0x32	6.25	0x72	14.25	0xB2	22.25	0xF2	30.25
			0x33	6.375	0x73	14.375	0xB3	22.375	0xF3	30.375
			0x34	6.5	0x74	14.5	0xB4	22.5	0xF4	30.5
			0x35	6.625	0x75	14.625	0xB5	22.625	0xF5	30.625
			0x36	6.75	0x76	14.75	0xB6	22.75	0xF6	30.75
			0x37	6.875	0x77	14.875	0xB7	22.875	0xF7	30.875
			0x38	7	0x78	15	0xB8	23	0xF8	31
			0x39	7.125	0x79	15.125	0xB9	23.125	0xF9	31.125
			0x3A	7.25	0x7A	15.25	0xBA	23.25	0xFA	31.25
			0x3B	7.375	0x7B	15.375	0xBB	23.375	0xFB	31.375
			0x3C	7.5	0x7C	15.5	0xBC	23.5	0xFC	31.5
			0x3D	7.625	0x7D	15.625	0xBD	23.625	0xFD	31.625
			0x3E	7.75	0x7E	15.75	0xBE	23.75	0xFE	31.75
			0x3F	7.875	0x7F	15.875	0xBF	23.875	0xFF	31.875

◆ Load Switch Current ADC Register Address: 09H

This register records the load switch current ADC value.

Register Name	LSC_REG		Load Switch Current ADC Register							
Address			0x09							
	R/W	Default	Description							
LSC[0]	R	0	Reserved							
LSC[1]	R	0	0= boost not latch				1= boost latch			
LSC[7:2]	R	000000	Load Switch current							
			Binary Code	Current (A)	Binary Code	Current (A)	Binary Code	Current (A)	Binary Code	Current (A)
			000000	0.00	010000	2.40	100000	4.80	110000	7.20
			000001	0.15	010001	2.55	100001	4.95	110001	7.35
			000010	0.30	010010	2.70	100010	5.10	110010	7.50
			000011	0.45	010011	2.85	100011	5.25	110011	7.65
			000100	0.60	010100	3.00	100100	5.40	110100	7.80
			000101	0.75	010101	3.15	100101	5.55	110101	7.95
			000110	0.90	010110	3.30	100110	5.70	110110	8.10
			000111	1.05	010111	3.45	100111	5.85	110111	8.25
			001000	1.20	011000	3.60	101000	6.00	111000	8.40
			001001	1.35	011001	3.75	101001	6.15	111001	8.55
			001010	1.50	011010	3.90	101010	6.30	111010	8.70
			001011	1.65	011011	4.05	101011	6.45	111011	8.85
			001100	1.80	011100	4.20	101100	6.60	111100	9.00
			001101	1.95	011101	4.35	101101	6.75	111101	9.15
			001110	2.10	011110	4.50	101110	6.90	111110	9.30
			001111	2.25	011111	4.65	101111	7.05	111111	9.45

◆ BUS ADC Register Address: 0AH

This register records the BUS voltage ADC value.

Register Name	BUS_REG		BUS Voltage ADC Register							
Address			0x0A							
	R/W	Default	Description							
BUS[7:0]	R	00000000	BUS voltage							
			Hex Code	Voltage (V)	Hex Code	Voltage (V)	Hex Code	Voltage (V)	Hex Code	Voltage (V)
			0x00	0.000	0x40	4.096	0x80	8.192	0xC0	12.288
			0x01	0.064	0x41	4.160	0x81	8.256	0xC1	12.352
			0x02	0.128	0x42	4.224	0x82	8.320	0xC2	12.416
			0x03	0.192	0x43	4.288	0x83	8.384	0xC3	12.480

			0x04	0.256	0x44	4.352	0x84	8.448	0xC4	12.544
			0x05	0.320	0x45	4.416	0x85	8.512	0xC5	12.608
			0x06	0.384	0x46	4.480	0x86	8.576	0xC6	12.672
			0x07	0.448	0x47	4.544	0x87	8.640	0xC7	12.736
			0x08	0.512	0x48	4.608	0x88	8.704	0xC8	12.800
			0x09	0.576	0x49	4.672	0x89	8.768	0xC9	12.864
			0x0A	0.640	0x4A	4.736	0x8A	8.832	0xCA	12.928
			0x0B	0.704	0x4B	4.800	0x8B	8.896	0xCB	12.992
			0x0C	0.768	0x4C	4.864	0x8C	8.960	0xCC	13.056
			0x0D	0.832	0x4D	4.928	0x8D	9.024	0xCD	13.120
			0x0E	0.896	0x4E	4.992	0x8E	9.088	0xCE	13.184
			0x0F	0.960	0x4F	5.056	0x8F	9.152	0xCF	13.248
			0x10	1.024	0x50	5.120	0x90	9.216	0xD0	13.312
			0x11	1.088	0x51	5.184	0x91	9.280	0xD1	13.376
			0x12	1.152	0x52	5.248	0x92	9.344	0xD2	13.440
			0x13	1.216	0x53	5.312	0x93	9.408	0xD3	13.504
			0x14	1.280	0x54	5.376	0x94	9.472	0xD4	13.568
			0x15	1.344	0x55	5.440	0x95	9.536	0xD5	13.632
			0x16	1.408	0x56	5.504	0x96	9.600	0xD6	13.696
			0x17	1.472	0x57	5.568	0x97	9.664	0xD7	13.760
			0x18	1.536	0x58	5.632	0x98	9.728	0xD8	13.824
			0x19	1.600	0x59	5.696	0x99	9.792	0xD9	13.888
			0x1A	1.664	0x5A	5.760	0x9A	9.856	0xDA	13.952
			0x1B	1.728	0x5B	5.824	0x9B	9.920	0xDB	14.016
			0x1C	1.792	0x5C	5.888	0x9C	9.984	0xDC	14.080
			0x1D	1.856	0x5D	5.952	0x9D	10.048	0xDD	14.144
			0x1E	1.920	0x5E	6.016	0x9E	10.112	0xDE	14.208
			0x1F	1.984	0x5F	6.080	0x9F	10.176	0xDF	14.272
			0x20	2.048	0x60	6.144	0xA0	10.240	0xE0	14.336
			0x21	2.112	0x61	6.208	0xA1	10.304	0xE1	14.400
			0x22	2.176	0x62	6.272	0xA2	10.368	0xE2	14.464
			0x23	2.240	0x63	6.336	0xA3	10.432	0xE3	14.528
			0x24	2.304	0x64	6.400	0xA4	10.496	0xE4	14.592
			0x25	2.368	0x65	6.464	0xA5	10.560	0xE5	14.656
			0x26	2.432	0x66	6.528	0xA6	10.624	0xE6	14.720
			0x27	2.496	0x67	6.592	0xA7	10.688	0xE7	14.784
			0x28	2.560	0x68	6.656	0xA8	10.752	0xE8	14.848
			0x29	2.624	0x69	6.720	0xA9	10.816	0xE9	14.912
			0x2A	2.688	0x6A	6.784	0xAA	10.880	0xEA	14.976
			0x2B	2.752	0x6B	6.848	0xAB	10.944	0xEB	15.040
			0x2C	2.816	0x6C	6.912	0xAC	11.008	0xEC	15.104
			0x2D	2.880	0x6D	6.976	0xAD	11.072	0xED	15.168
			0x2E	2.944	0x6E	7.040	0xAE	11.136	0xEE	15.232
			0x2F	3.008	0x6F	7.104	0xAF	11.200	0xEF	15.296
			0x30	3.072	0x70	7.168	0xB0	11.264	0xF0	15.360
			0x31	3.136	0x71	7.232	0xB1	11.328	0xF1	15.424
			0x32	3.200	0x72	7.296	0xB2	11.392	0xF2	15.488
			0x33	3.264	0x73	7.360	0xB3	11.456	0xF3	15.552
			0x34	3.328	0x74	7.424	0xB4	11.520	0xF4	15.616
			0x35	3.392	0x75	7.488	0xB5	11.584	0xF5	15.680
			0x36	3.456	0x76	7.552	0xB6	11.648	0xF6	15.744
			0x37	3.520	0x77	7.616	0xB7	11.712	0xF7	15.808
			0x38	3.584	0x78	7.680	0xB8	11.776	0xF8	15.872
			0x39	3.648	0x79	7.744	0xB9	11.840	0xF9	15.936
			0x3A	3.712	0x7A	7.808	0xBA	11.904	0xFA	16.000
			0x3B	3.776	0x7B	7.872	0xBB	11.968	0xFB	16.000
			0x3C	3.840	0x7C	7.936	0xBC	12.032	0xFC	16.000
			0x3D	3.904	0x7D	8.000	0xBD	12.096	0xFD	16.000
			0x3E	3.968	0x7E	8.064	0xBE	12.160	0xFE	16.000
			0x3F	4.032	0x7F	8.128	0xBF	12.224	0xFF	16.000

◆ STR OVP Program Register Address: 0BH

This register control the STR OVP value.

Register Name	OVP_REG		STR Voltage Control Register							
Address			0x0B							
	R/W	Default	Description							
OVP[4:0]	R/W	10111	STR voltage							
			Binary Code	Voltage (V)	Binary Code	Voltage (V)	Binary Code	Voltage (V)	Binary Code	Voltage (V)
			00000	7	01000	15	10000	23	11000	31
			00001	8	01001	16	10001	24	11001	32
			00010	9	01010	17	10010	25	11010	33
			00011	10	01011	18	10011	26	11011	34
			00100	11	01100	19	10100	27	11100	35
			00101	12	01101	20	10101	28	11101	36
			00110	13	01110	21	10110	29	11110	37
			00111	14	01111	22	10111	30	11111	38
OVP[7:5]	R		Reserved							

◆ IN Voltage ADC Register Address: 0CH

This register records the IN voltage ADC value.

Register Name	IN_REG		IN Voltage ADC Register							
Address			0x0C							
	R/W	Default	Description							
IN[7:0]	R	00000000	IN voltage							
			Hex Code	Voltage (V)	Hex Code	Voltage (V)	Hex Code	Voltage (V)	Hex Code	Voltage (V)
			0x00	0.000	0x40	4.096	0x80	8.192	0xC0	12.288
			0x01	0.064	0x41	4.160	0x81	8.256	0xC1	12.352
			0x02	0.128	0x42	4.224	0x82	8.320	0xC2	12.416
			0x03	0.192	0x43	4.288	0x83	8.384	0xC3	12.480
			0x04	0.256	0x44	4.352	0x84	8.448	0xC4	12.544
			0x05	0.320	0x45	4.416	0x85	8.512	0xC5	12.608
			0x06	0.384	0x46	4.480	0x86	8.576	0xC6	12.672
			0x07	0.448	0x47	4.544	0x87	8.640	0xC7	12.736
			0x08	0.512	0x48	4.608	0x88	8.704	0xC8	12.800
			0x09	0.576	0x49	4.672	0x89	8.768	0xC9	12.864
			0x0A	0.640	0x4A	4.736	0x8A	8.832	0xCA	12.928
			0x0B	0.704	0x4B	4.800	0x8B	8.896	0xCB	12.992
			0x0C	0.768	0x4C	4.864	0x8C	8.960	0xCC	13.056
			0x0D	0.832	0x4D	4.928	0x8D	9.024	0xCD	13.120
			0x0E	0.896	0x4E	4.992	0x8E	9.088	0xCE	13.184
			0x0F	0.960	0x4F	5.056	0x8F	9.152	0xCF	13.248
			0x10	1.024	0x50	5.120	0x90	9.216	0xD0	13.312
			0x11	1.088	0x51	5.184	0x91	9.280	0xD1	13.376
			0x12	1.152	0x52	5.248	0x92	9.344	0xD2	13.440
			0x13	1.216	0x53	5.312	0x93	9.408	0xD3	13.504
			0x14	1.280	0x54	5.376	0x94	9.472	0xD4	13.568
			0x15	1.344	0x55	5.440	0x95	9.536	0xD5	13.632
			0x16	1.408	0x56	5.504	0x96	9.600	0xD6	13.696
			0x17	1.472	0x57	5.568	0x97	9.664	0xD7	13.760
			0x18	1.536	0x58	5.632	0x98	9.728	0xD8	13.824
			0x19	1.600	0x59	5.696	0x99	9.792	0xD9	13.888
			0x1A	1.664	0x5A	5.760	0x9A	9.856	0xDA	13.952
			0x1B	1.728	0x5B	5.824	0x9B	9.920	0xDB	14.016
			0x1C	1.792	0x5C	5.888	0x9C	9.984	0xDC	14.080
			0x1D	1.856	0x5D	5.952	0x9D	10.048	0xDD	14.144
			0x1E	1.920	0x5E	6.016	0x9E	10.112	0xDE	14.208
			0x1F	1.984	0x5F	6.080	0x9F	10.176	0xDF	14.272
			0x20	2.048	0x60	6.144	0xA0	10.240	0xE0	14.336
			0x21	2.112	0x61	6.208	0xA1	10.304	0xE1	14.400
			0x22	2.176	0x62	6.272	0xA2	10.368	0xE2	14.464
			0x23	2.240	0x63	6.336	0xA3	10.432	0xE3	14.528

			0x24	2.304	0x64	6.400	0xA4	10.496	0xE4	14.592
			0x25	2.368	0x65	6.464	0xA5	10.560	0xE5	14.656
			0x26	2.432	0x66	6.528	0xA6	10.624	0xE6	14.720
			0x27	2.496	0x67	6.592	0xA7	10.688	0xE7	14.784
			0x28	2.560	0x68	6.656	0xA8	10.752	0xE8	14.848
			0x29	2.624	0x69	6.720	0xA9	10.816	0xE9	14.912
			0x2A	2.688	0x6A	6.784	0xAA	10.880	0xEA	14.976
			0x2B	2.752	0x6B	6.848	0xAB	10.944	0xEB	15.040
			0x2C	2.816	0x6C	6.912	0xAC	11.008	0xEC	15.104
			0x2D	2.880	0x6D	6.976	0xAD	11.072	0xED	15.168
			0x2E	2.944	0x6E	7.040	0xAE	11.136	0xEE	15.232
			0x2F	3.008	0x6F	7.104	0xAF	11.200	0xEF	15.296
			0x30	3.072	0x70	7.168	0xB0	11.264	0xF0	15.360
			0x31	3.136	0x71	7.232	0xB1	11.328	0xF1	15.424
			0x32	3.200	0x72	7.296	0xB2	11.392	0xF2	15.488
			0x33	3.264	0x73	7.360	0xB3	11.456	0xF3	15.552
			0x34	3.328	0x74	7.424	0xB4	11.520	0xF4	15.616
			0x35	3.392	0x75	7.488	0xB5	11.584	0xF5	15.680
			0x36	3.456	0x76	7.552	0xB6	11.648	0xF6	15.744
			0x37	3.520	0x77	7.616	0xB7	11.712	0xF7	15.808
			0x38	3.584	0x78	7.680	0xB8	11.776	0xF8	15.872
			0x39	3.648	0x79	7.744	0xB9	11.840	0xF9	15.936
			0x3A	3.712	0x7A	7.808	0xBA	11.904	0xFA	16.000
			0x3B	3.776	0x7B	7.872	0xBB	11.968	0xFB	16.000
			0x3C	3.840	0x7C	7.936	0xBC	12.032	0xFC	16.000
			0x3D	3.904	0x7D	8.000	0xBD	12.096	0xFD	16.000
			0x3E	3.968	0x7E	8.064	0xBE	12.160	0xFE	16.000
			0x3F	4.032	0x7F	8.128	0xBF	12.224	0xFF	16.000

◆ STR Voltage ADC Register Address: 0DH

This register records the STR voltage ADC value.

Register Name	STR_REG		STR Voltage ADC Register							
Address			0x0D							
	R/W	Default	Description							
STR[7:0]	R	00000000	STR voltage							
			Hex Code	Voltage (V)	Hex Code	Voltage (V)	Hex Code	Voltage (V)	Hex Code	Voltage (V)
			0x00	0.00	0x40	9.60	0x80	19.20	0xC0	28.80
			0x01	0.15	0x41	9.75	0x81	19.35	0xC1	28.95
			0x02	0.30	0x42	9.90	0x82	19.50	0xC2	29.10
			0x03	0.45	0x43	10.05	0x83	19.65	0xC3	29.25
			0x04	0.60	0x44	10.20	0x84	19.80	0xC4	29.40
			0x05	0.75	0x45	10.35	0x85	19.95	0xC5	29.55
			0x06	0.90	0x46	10.50	0x86	20.10	0xC6	29.70
			0x07	1.05	0x47	10.65	0x87	20.25	0xC7	29.85
			0x08	1.20	0x48	10.80	0x88	20.40	0xC8	30.00
			0x09	1.35	0x49	10.95	0x89	20.55	0xC9	30.15
			0x0A	1.50	0x4A	11.10	0x8A	20.70	0xCA	30.30
			0x0B	1.65	0x4B	11.25	0x8B	20.85	0xCB	30.45
			0x0C	1.80	0x4C	11.40	0x8C	21.00	0xCC	30.60
			0x0D	1.95	0x4D	11.55	0x8D	21.15	0xCD	30.75
			0x0E	2.10	0x4E	11.70	0x8E	21.30	0xCE	30.90
			0x0F	2.25	0x4F	11.85	0x8F	21.45	0xCF	31.05
			0x10	2.40	0x50	12.00	0x90	21.60	0xD0	31.20
			0x11	2.55	0x51	12.15	0x91	21.75	0xD1	31.35
			0x12	2.70	0x52	12.30	0x92	21.90	0xD2	31.50
			0x13	2.85	0x53	12.45	0x93	22.05	0xD3	31.65
			0x14	3.00	0x54	12.60	0x94	22.20	0xD4	31.80
			0x15	3.15	0x55	12.75	0x95	22.35	0xD5	31.95
			0x16	3.30	0x56	12.90	0x96	22.50	0xD6	32.10
			0x17	3.45	0x57	13.05	0x97	22.65	0xD7	32.25
			0x18	3.60	0x58	13.20	0x98	22.80	0xD8	32.40

			0x19	3.75	0x59	13.35	0x99	22.95	0xD9	32.55
			0x1A	3.90	0x5A	13.50	0x9A	23.10	0xDA	32.70
			0x1B	4.05	0x5B	13.65	0x9B	23.25	0xDB	32.85
			0x1C	4.20	0x5C	13.80	0x9C	23.40	0xDC	33.00
			0x1D	4.35	0x5D	13.95	0x9D	23.55	0xDD	33.15
			0x1E	4.50	0x5E	14.10	0x9E	23.70	0xDE	33.30
			0x1F	4.65	0x5F	14.25	0x9F	23.85	0xDF	33.45
			0x20	4.80	0x60	14.40	0xA0	24.00	0xE0	33.60
			0x21	4.95	0x61	14.55	0xA1	24.15	0xE1	33.75
			0x22	5.10	0x62	14.70	0xA2	24.30	0xE2	33.90
			0x23	5.25	0x63	14.85	0xA3	24.45	0xE3	34.05
			0x24	5.40	0x64	15.00	0xA4	24.60	0xE4	34.20
			0x25	5.55	0x65	15.15	0xA5	24.75	0xE5	34.35
			0x26	5.70	0x66	15.30	0xA6	24.90	0xE6	34.50
			0x27	5.85	0x67	15.45	0xA7	25.05	0xE7	34.65
			0x28	6.00	0x68	15.60	0xA8	25.20	0xE8	34.80
			0x29	6.15	0x69	15.75	0xA9	25.35	0xE9	34.95
			0x2A	6.30	0x6A	15.90	0xAA	25.50	0xEA	35.10
			0x2B	6.45	0x6B	16.05	0xAB	25.65	0xEB	35.25
			0x2C	6.60	0x6C	16.20	0xAC	25.80	0xEC	35.40
			0x2D	6.75	0x6D	16.35	0xAD	25.95	0xED	35.55
			0x2E	6.90	0x6E	16.50	0xAE	26.10	0xEE	35.70
			0x2F	7.05	0x6F	16.65	0xAF	26.25	0xEF	35.85
			0x30	7.20	0x70	16.80	0xB0	26.40	0xF0	36.00
			0x31	7.35	0x71	16.95	0xB1	26.55	0xF1	36.00
			0x32	7.50	0x72	17.10	0xB2	26.70	0xF2	36.00
			0x33	7.65	0x73	17.25	0xB3	26.85	0xF3	36.00
			0x34	7.80	0x74	17.40	0xB4	27.00	0xF4	36.00
			0x35	7.95	0x75	17.55	0xB5	27.15	0xF5	36.00
			0x36	8.10	0x76	17.70	0xB6	27.30	0xF6	36.00
			0x37	8.25	0x77	17.85	0xB7	27.45	0xF7	36.00
			0x38	8.40	0x78	18.00	0xB8	27.60	0xF8	36.00
			0x39	8.55	0x79	18.15	0xB9	27.75	0xF9	36.00
			0x3A	8.70	0x7A	18.30	0xBA	27.90	0xFA	36.00
			0x3B	8.85	0x7B	18.45	0xBB	28.05	0xFB	36.00
			0x3C	9.00	0x7C	18.60	0xBC	28.20	0xFC	36.00
			0x3D	9.15	0x7D	18.75	0xBD	28.35	0xFD	36.00
			0x3E	9.30	0x7E	18.90	0xBE	28.50	0xFE	36.00
			0x3F	9.45	0x7F	19.05	0xBF	28.65	0xFF	36.00

◆ STR Voltage Fall Time Fault Register Address: 0EH

This register Controls the burst mode STR fall time Fault threshold.

Register Name	TimF_REG		Burst mode fall time fault register							
Address			0x0E							
	R/W	Default	Description							
TimF[6:0]	R/W	0000000	Burst mode fall time fault threshold, when test Fall time is smaller than setting value, TimF[7] will be set to '1'.							
			Binary Code	Time (ms)	Binary Code	Time (ms)	Binary Code	Time (ms)	Binary Code	Time (ms)
			0000000		0100000	640	1000000	1280	1100000	1920
			0000001	20	0100001	660	1000001	1300	1100001	1940
			0000010	40	0100010	680	1000010	1320	1100010	1960
			0000011	60	0100011	700	1000011	1340	1100011	1980
			0000100	80	0100100	720	1000100	1360	1100100	2000
			0000101	100	0100101	740	1000101	1380	1100101	2020
			0000110	120	0100110	760	1000110	1400	1100110	2040
			0000111	140	0100111	780	1000111	1420	1100111	2060
			0001000	160	0101000	800	1001000	1440	1101000	2080
			0001001	180	0101001	820	1001001	1460	1101001	2100
			0001010	200	0101010	840	1001010	1480	1101010	2120
			0001011	220	0101011	860	1001011	1500	1101011	2140
			0001100	240	0101100	880	1001100	1520	1101100	2160
			0001101	260	0101101	900	1001101	1540	1101101	2180

			0001110	280	0101110	920	1001110	1560	1101110	2200
			0001111	300	0101111	940	1001111	1580	1101111	2220
			0010000	320	0110000	960	1010000	1600	1110000	2240
			0010001	340	0110001	980	1010001	1620	1110001	2260
			0010010	360	0110010	1000	1010010	1640	1110010	2280
			0010011	380	0110011	1020	1010011	1660	1110011	2300
			0010100	400	0110100	1040	1010100	1680	1110100	2320
			0010101	420	0110101	1060	1010101	1700	1110101	2340
			0010110	440	0110110	1080	1010110	1720	1110110	2360
			0010111	460	0110111	1100	1010111	1740	1110111	2380
			0011000	480	0111000	1120	1011000	1760	1111000	2400
			0011001	500	0111001	1140	1011001	1780	1111001	2420
			0011010	520	0111010	1160	1011010	1800	1111010	2440
			0011011	540	0111011	1180	1011011	1820	1111011	2460
			0011100	560	0111100	1200	1011100	1840	1111100	2480
			0011101	580	0111101	1220	1011101	1860	1111101	2500
			0011110	600	0111110	1240	1011110	1880	1111110	2520
			0011111	620	0111111	1260	0011111	1900	1111111	2540
TimF[7]	R	0	0= STR fall time pass (Test value > setting threshold)				1= STR fall time fault (Test value < setting threshold)			

◆ STR Soft Start Time Setting Register Address: 0FH

This register controls PLP boost mode SS step time.

Register Name	Tstep_REG		STR soft start time register							
Address			0x0F							
	R/W	Default	Description							
Tstep[7:0]	R/W	00000001	PLP soft start time step setting register, SS time = 256 × T_{step}							
			Hex Code	Time (us)	Hex Code	Time (us)	Hex Code	Time (us)	Hex Code	Time (us)
			0x00	250	0x40	16000	0x80	32000	0xC0	48000
			0x01	250	0x41	16250	0x81	32250	0xC1	48250
			0x02	500	0x42	16500	0x82	32500	0xC2	48500
			0x03	750	0x43	16750	0x83	32750	0xC3	48750
			0x04	1000	0x44	17000	0x84	33000	0xC4	49000
			0x05	1250	0x45	17250	0x85	33250	0xC5	49250
			0x06	1500	0x46	17500	0x86	33500	0xC6	49500
			0x07	1750	0x47	17750	0x87	33750	0xC7	49750
			0x08	2000	0x48	18000	0x88	34000	0xC8	50000
			0x09	2250	0x49	18250	0x89	34250	0xC9	50250
			0x0A	2500	0x4A	18500	0x8A	34500	0xCA	50500
			0x0B	2750	0x4B	18750	0x8B	34750	0xCB	50750
			0x0C	3000	0x4C	19000	0x8C	35000	0xCC	51000
			0x0D	3250	0x4D	19250	0x8D	35250	0xCD	51250
			0x0E	3500	0x4E	19500	0x8E	35500	0xCE	51500
			0x0F	3750	0x4F	19750	0x8F	35750	0xCF	51750
			0x10	4000	0x50	20000	0x90	36000	0xD0	52000
			0x11	4250	0x51	20250	0x91	36250	0xD1	52250
			0x12	4500	0x52	20500	0x92	36500	0xD2	52500
			0x13	4750	0x53	20750	0x93	36750	0xD3	52750
			0x14	5000	0x54	21000	0x94	37000	0xD4	53000
			0x15	5250	0x55	21250	0x95	37250	0xD5	53250
			0x16	5500	0x56	21500	0x96	37500	0xD6	53500
			0x17	5750	0x57	21750	0x97	37750	0xD7	53750
			0x18	6000	0x58	22000	0x98	38000	0xD8	54000
			0x19	6250	0x59	22250	0x99	38250	0xD9	54250
			0x1A	6500	0x5A	22500	0x9A	38500	0xDA	54500
			0x1B	6750	0x5B	22750	0x9B	38750	0xDB	54750
			0x1C	7000	0x5C	23000	0x9C	39000	0xDC	55000
			0x1D	7250	0x5D	23250	0x9D	39250	0xDD	55250
			0x1E	7500	0x5E	23500	0x9E	39500	0xDE	55500
			0x1F	7750	0x5F	23750	0x9F	39750	0xDF	55750
			0x20	8000	0x60	24000	0xA0	40000	0xE0	56000
			0x21	8250	0x61	24250	0xA1	40250	0xE1	56250

			0x22	8500	0x62	24500	0xA2	40500	0xE2	56500
			0x23	8750	0x63	24750	0xA3	40750	0xE3	56750
			0x24	9000	0x64	25000	0xA4	41000	0xE4	57000
			0x25	9250	0x65	25250	0xA5	41250	0xE5	57250
			0x26	9500	0x66	25500	0xA6	41500	0xE6	57500
			0x27	9750	0x67	25750	0xA7	41750	0xE7	57750
			0x28	10000	0x68	26000	0xA8	42000	0xE8	58000
			0x29	10250	0x69	26250	0xA9	42250	0xE9	58250
			0x2A	10500	0x6A	26500	0xAA	42500	0xEA	58500
			0x2B	10750	0x6B	26750	0xAB	42750	0xEB	58750
			0x2C	11000	0x6C	27000	0xAC	43000	0xEC	59000
			0x2D	11250	0x6D	27250	0xAD	43250	0xED	59250
			0x2E	11500	0x6E	27500	0xAE	43500	0xEE	59500
			0x2F	11750	0x6F	27750	0xAF	43750	0xEF	59750
			0x30	12000	0x70	28000	0xB0	44000	0xF0	60000
			0x31	12250	0x71	28250	0xB1	44250	0xF1	60250
			0x32	12500	0x72	28500	0xB2	44500	0xF2	60500
			0x33	12750	0x73	28750	0xB3	44750	0xF3	60750
			0x34	13000	0x74	29000	0xB4	45000	0xF4	61000
			0x35	13250	0x75	29250	0xB5	45250	0xF5	61250
			0x36	13500	0x76	29500	0xB6	45500	0xF6	61500
			0x37	13750	0x77	29750	0xB7	45750	0xF7	61750
			0x38	14000	0x78	30000	0xB8	46000	0xF8	62000
			0x39	14250	0x79	30250	0xB9	46250	0xF9	62250
			0x3A	14500	0x7A	30500	0xBA	46500	0xFA	62500
			0x3B	14750	0x7B	30750	0xBB	46750	0xFB	62750
			0x3C	15000	0x7C	31000	0xBC	47000	0xFC	63000
			0x3D	15250	0x7D	31250	0xBD	47250	0xFD	63250
			0x3E	15500	0x7E	31500	0xBE	47500	0xFE	63500
			0x3F	15750	0x7F	31750	0xBF	47750	0xFF	63750

General Operation Description

SY72025 is a power management IC for the applications of power backup in Solid-State Driver or other backup power supplies which can achieve backup power storage and release functions. The energy is transferred bi-directionally between the BUS side and the energy storage side with high efficiency by bi-directional Dc-Dc regulator. Fast transient response and excellent stability are achieved by the quasi-fixed frequency constant off time control strategy.

A reverse blocking switch is integrated at the input side to prevent from energy leaking when the input power source is removed. The reverse blocking switch also has the programmable current limit function with the program range from 1.2A to 6.2A. Three different BUS over voltage protection (OVP) thresholds are selectable by OVP pin for the applications with different kind of input power source.

I^2C interface is internally integrated in SY72025 to reduce the amount of external components. Control parameters such as input current limit, switching frequency, and boost peak current limit can be programmed by I^2C.

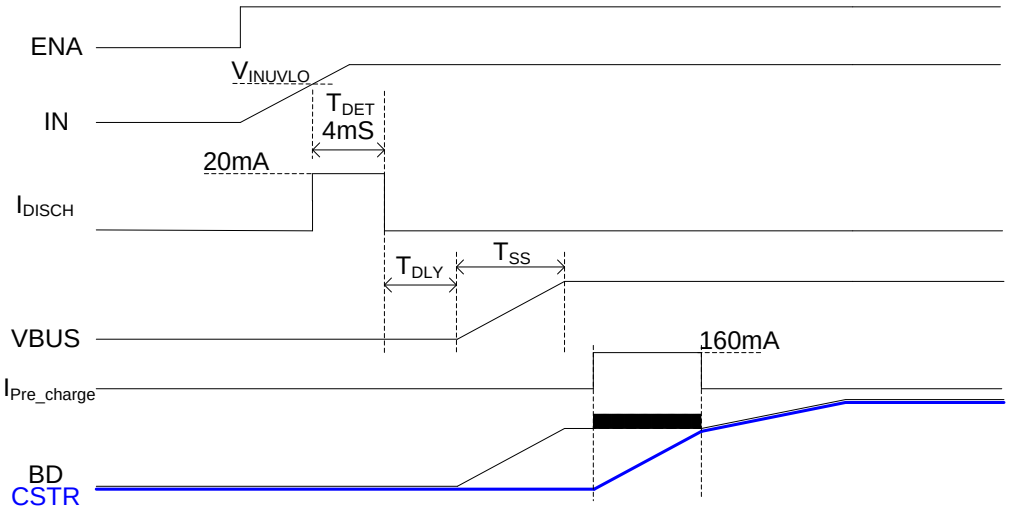
Storage capacitance measurement is integrated inside of SY72025. The measurement results are stored in internal read only data registers for MCU reading by I^2C interface.

SY72025 along with QFN4×4-25 package provides compact PCB layout to save circuit area for the increase of SSD memory capacity.

Function Description

Startup Sequence

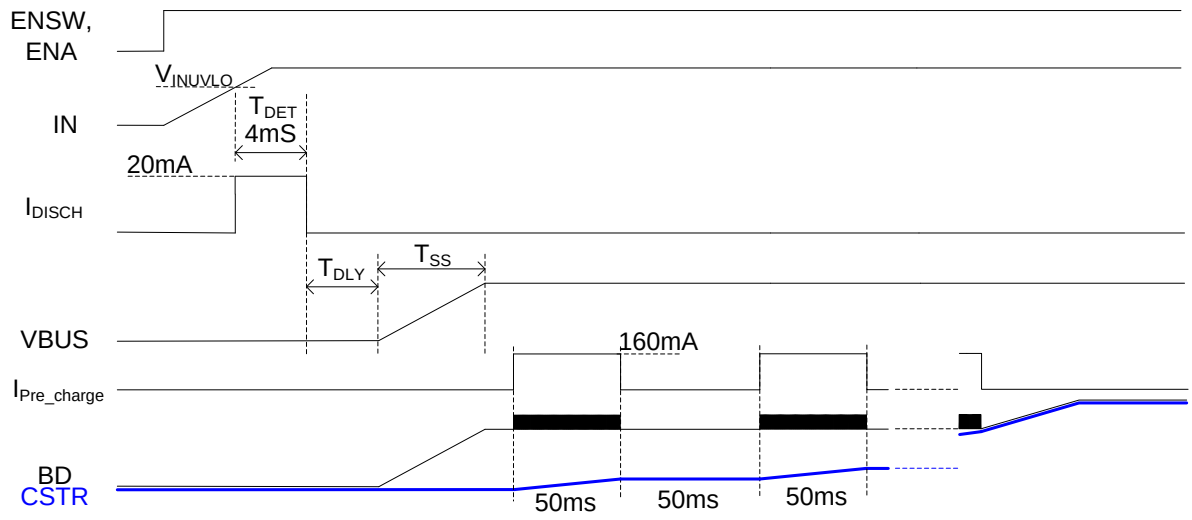
When voltage on IN pin is higher than UVLO level and load switch is enabled which means EN bit (LSP[0]) is 1 and external ENA pin is pulled high, an internal 20mA current source discharges the IN for about 4ms, if IN voltage remains above UVLO level during the deglitch time, soft start period begins after the programmed switch turn on delay time. The soft start time is programmed by the capacitor on SS pin. Capacitor on BD pin will also be charged during the soft start period. When the voltage on BUS pin rises above boost threshold and ENCON (DCP [0]) is 1, pre-charge period starts. The BD voltage is regulated at around 120% - 135% of the BUS voltage and the capacitor on STR pin is charged with around 160mA pre-charge current. The pre-charge period ends when the voltage across the disconnection switch located from BD pin to STR pin is lower than an internal threshold and then the disconnection switch will be fully turned on. Boost converter starts to detect FBS voltage when pre-charge ends.



Power up sequence

The chip is also suitable for super capacity STR capacitance application. When change SF[7] code of REG06 to '0', if the pre-charge current lasts for 50ms and the voltage across the disconnection switch located from BD pin to STR

pin is still larger than an internal threshold, DC-DC converter will stop pre-charge for 50ms, then restart and repeat pre-charge.



Input Load Switch

Input current limit, input current ADC, over voltage protection and reverse blocking functions are all integrated in reverse blocking switch control module. Load switch will be turned off and buck mode will be active when IN voltage exceed OVP threshold when LSP[1] code is 0 or OCP is triggered and last for around 6.6mS. Input current limit is set by I^2C interface. Load switch will be into clamp mode and BUS will be regulated at the Input OVP value when LSP[1] code is 1 and Input voltage exceed input OVP threshold.
Reverse blocking FET will be turned off if any of the following conditions happens:

1. IN voltage falls below UVLO;
2. EN (LSP[0]) is 0 or ENA pin is pulled to GND;
3. V_{BUS} is higher than V_{IN} (V_{BUS}-V_{IN}>20mV) for 1us if SF[6] is 0;

Burst Mode STR Fall Time ADC(STR Pin Open Detection)

When the DC/DC converter operates in Burst Mode, Internal 25Hz counter calculates the time that FBS voltage falls from 1.2V to 1.17V and compare with the time data of REG0E[6:0], if the Fall time is smaller than REG0E Time data, Burst Mode Fall Time Fault flag bit TIMF[7] will change to '1'.

For example, if REG0E is 0x78H, the STR fall time can be calculated by:

$T_{STRFALL}$=0X78H=(7*16^1+8*16^0)*20ms=2400ms

Time-Sharing ADC

If the LSP[7] code is '1', Time-Sharing ADC is enabled and IN/BUS/CSTR and Input current ADC output will be updated every 0.8ms; Once the LSP[7] code has been refreshed to '1', the ADC register will be cleared and updated every 0.8ms.

Buck Mode Restart

When IN is higher than UVLO and DC/DC works in Buck Mode, Input Load Switch starts up and PLP buck stop working and goes to boost charge mode once LSW soft start done.

Bi-directional DC-DC Regulator

1) Boost Burst Mode

DC-DC regulator can operate in burst mode by setting SF[4] to '0', and which can minimize the power loss. DC-DC converter starts working to charge STR capacitor when the pre-charge period is done. Quasi-fixed frequency constant off time control is used and the peak current is programmed by I^2C interface. The maximum storage voltage is programmed by FBS pin. Boost converter stops working when voltage on FBS pin reaches 1.2V and starts to charge the storage capacitor again when FBS voltage falls below around 1.17V.

2) Boost CV Mode

DC-DC regulator operates in CV mode if SF[4] code is '1', and CV mode can minimize STR output ripple. The peak current can be programmed by I^2C interface to limit the inrush current in CV mode, the internal voltage reference is 1.1V in CV mode. Boost converter triggers OVP when voltage on FBS pin reaches 1.2V or STR voltage exceed Register 0x0B setting value, and returns to close loop control when FBS voltage falls below around 1.17V.

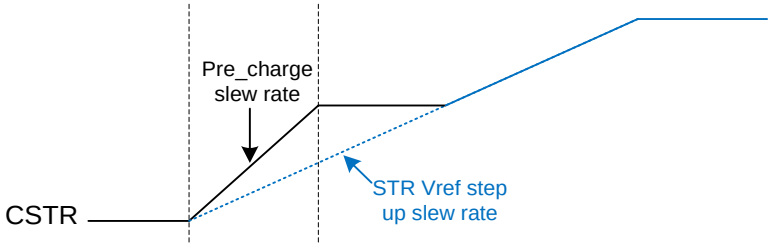
3) Buck Mode

Buck mode is triggered immediately when the voltage on FBD pin falls below 0.6V or ENA pin pull low. Quasi-fixed frequency constant off time control is also used in buck mode to achieve fast dynamic response. Regulated voltage on BUS pin is programmed by FBR pin. The maximum peak current of buck converter is internally clamped at around 8A. Buck mode will change to boost mode when load switch is turned on and FBR voltage rise above 0.63V. If STR voltage falls below buck off threshold which is programmed by I^2C interface, buck converter will stop working.

Adjustable STR Soft Start Time

STR Soft Start time can be changed by I2C interface and the data can be stored into MTP, there are two situations as below need to be concerned in CV Mode;

1) Pre_charge Slew Rate is faster the STR V_{ref} step up slew rate

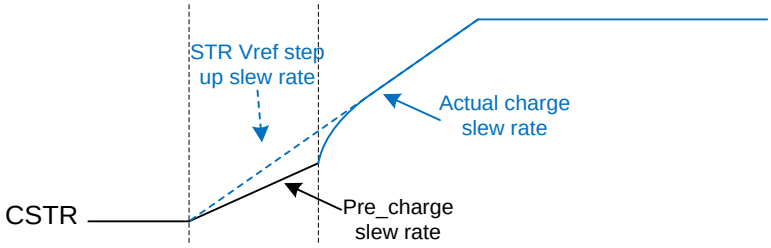


If the pre-charge slew rate is faster than STR V_{ref} step up slew rate, when pre-charge is done STR feedback voltage is higher than STR V_{ref}, Boost will be into standby mode and stop switching. The soft start time can be calculated by

$$T_{ss} = 256 \times T_{step}$$

T_{step} is controlled by Register REG0F [7:0].

2) Soft Start Time V_{ref} slew rate is faster than the pre-charge slew rate



If the pre-charge slew rate is slower than STR V_{ref} during pre-charge, The soft start time also can be calculated by

$$T_{ss} = 256 \times T_{step}$$

If Burst Mode is preset, When V_{ref} rise to 1.1V and soft start is done, internal control loop will directly switch from CV mode control to Bust mode control. So the FBS will rise to 1.2V and boost stop switching unless FBS fall below 1.17V.

BUS Short Protection

If short circuit happens on BUS pin and BUS voltage is still higher than VBUS UVLO threshold, DC-DC converter switches from boost charge mode to buck release mode, and backs up the VBUS load with maximum peak current till STR voltage falls below buck off point; OTP could be triggered and all the block stop working if PLP Power MOSFET temperature is higher than the internal thermal threshold. But if LSP[2] code is '1', even if the PLP Power MOSFET temperature is extremely high, PLP Buck still works until STR voltage falls below Buck off Point.

If BUS voltage falls to below VBUS UVLO threshold when BUS short to GND, PLP stop switching immediately, then Reverse blocking switch limits the input current at the programmed level for about 6.6ms.

STR Short Protection

When PLP start pre-charging and SF[7] is '0', hiccup pre-charge mode is enabled. After 50ms pre-charge, the disconnection switch and the DC-DC shut down for about 50ms, then the Bi-directional DC-DC block repeats 50ms pre-charge process until STR voltage reaches to VBD voltage.

When PLP start pre-charging and SF[7] is '1'. After 125ms pre-charge, if STR is still lower than 1.2V, IC latches and STR short flag bit LSC[1] goes to '1'.

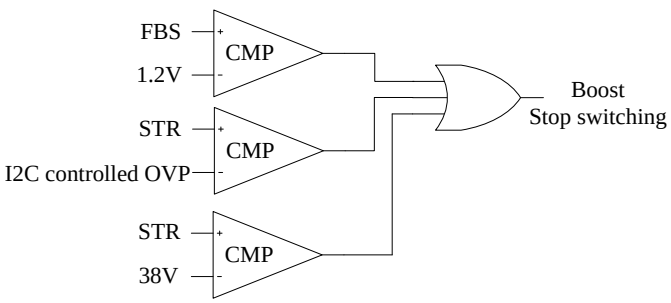
When Pre-charge done, no matter SF[7] is '0' or '1' STR short is detected once VSTR < VBUS-0.2V, then STR short latch flag bit LSC[1] goes to '1'. It is recommended that STR buck off point should not set below VIN when QPOR is required.

STR short detection is also enabled during the STR capacitance measurement period, so it is better not to set VDIS2 below VIN voltage.

The latch state can be cleared by restarting from IN or ENA pin or resetting EN bit.

STR OVP

STR OVP value can be set from 7V to 38V by programming Register REG0B [4:0], also STR OVP can be set by FBS pin. When FBS pin voltage is up to 1.2V or STR pin voltage exceed register setting value or STR voltage exceed 38V, the DC-DC converter stop switching.



Storage Capacitance Measurement

MCU can start measuring by setting SF[5] to 1.

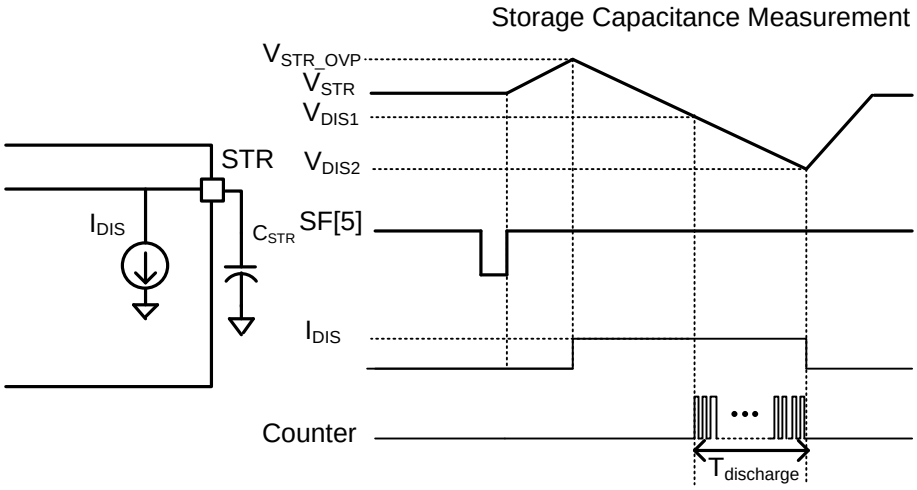
Firstly, V_{STR} will be charged up to OVP value, programmed discharge current I_{DIS} starts to discharge STR capacitors. Internal 8kHz counter calculates the discharge time starting from when STR voltage falls below $V_{DIS1}$to when STR voltage falls below V_{DIS2} (V_{DIS2} should not be set below VIN voltage). With high accuracy internal current source and time counter, the measured capacitance accuracy can be within ±5%.

The discharge time data $T_{DISCHARGE}$ is stored to data register REG07 and REG08. For example, if data read from REG07 is 0x12H, data read from REG08 is 0x34H, the $T_{DISCHARGE}$ should be calculated below:

$T_{DISCHARGE}$=0X1234H=$(1*16^3+2*16^2+3*16^1+4*16^0)*0.125ms$=582.5ms

And then, the capacitance can be calculated below:

$C_{STR}=I_{DIS}*T_{DISCHARGE}/(V_{DIS1}-V_{DIS2})$



Boost Peak Current Selection

If boost peak current is programmed lower than 1000mA (300mA, 500mA or 600mA,800mA), HSFET will not be turned on in burst/CV mode to reduce the negative inductor current. If boost peak current is programmed higher than 1000mA there will be negative inductor current because of the min on time of the high side MOSFET. The STR voltage could not be charged up to the programmed voltage level due to the negative inductor current. In order to charge the STR capacitors to desired value, it is recommended to set the boost peak current at a proper level and choose proper inductor. The maxim T_{MINON} value of HSFET is 120ns. The formula presented below is for proper boost peak current setting reference.

$V_{STR}-V_{IN}=L\ dI / dT \rightarrow dI=(V_{STR}-V_{IN})*dT / L=(V_{STR}-V_{IN})*T_{MINON} / L;$

$I_{PEAK} \geqq dI / 2 \rightarrow I_{PEAK} \geqq (V_{STR}-V_{IN})*T_{MINON} / 2*L;$

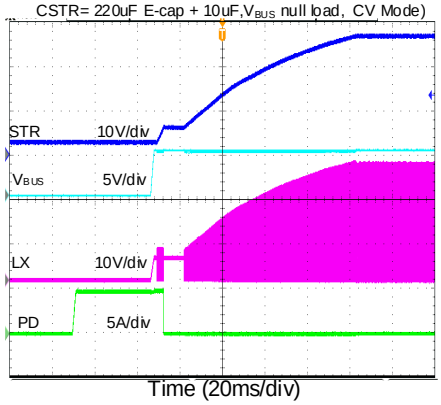
BUS Auto Discharge

When DC-DC converter and input load switch are all off, BUS voltage will be discharged by internal current source. Once IN voltage is above UVLO high point, auto-discharge is disabled.

Typical Performance Characteristics

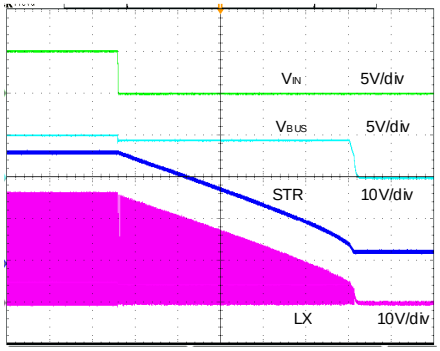
CV Mode VIN ON/OFF Test

(V_{IN}=5V, STR=28V,FBR threshold set to 4.4V, Buck regulated Voltage set to 4.2V CSTR= 220uF E-cap + 10uF,V_{BUS} null load, CV Mode)



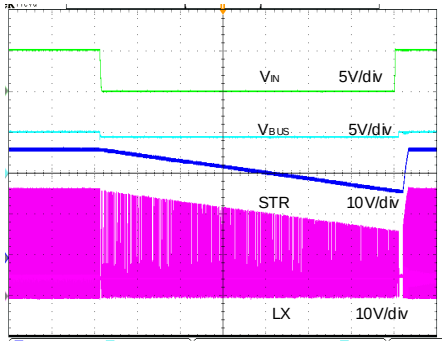
CV Mode VIN ON/OFF Test

(V_{IN}=5V, STR=28V,FBR threshold set to 4.4V, Buck regulated Voltage set to 4.2V CSTR= 220uF E-cap + 10uF,V_{BUS} null load, CV Mode)



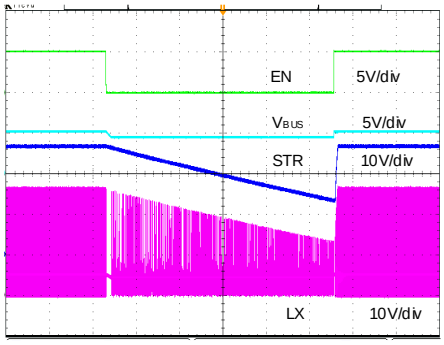
VIN Restart Test

(V_{IN}=5V~0~5V,STR=28V,FBR threshold set to 4.4V, Buck regulated Voltage set to 4.2V,CSTR= 220uF E-cap + 10uF, CV Mode, V_{BUS} null load)



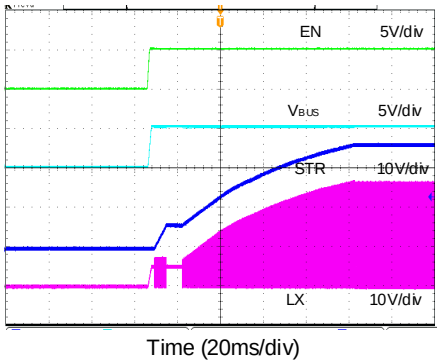
EN Deglitch Test

(V_{IN}=5V,STR=28V,FBR threshold set to 4.4V, Buck regulated Voltage set to 4.2V CSTR= 220uF E-cap + 10uF, CV Mode, V_{BUS} null load)



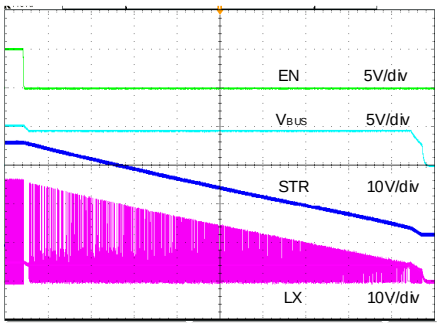
EN ON/OFF Test

(V_{IN}=5V,STR=28V,FBR threshold set to 4.4V, Buck regulated Voltage set to 4.2V CSTR= 220uF E-cap + 10uF, V_{BUS} null load, CV Mode)



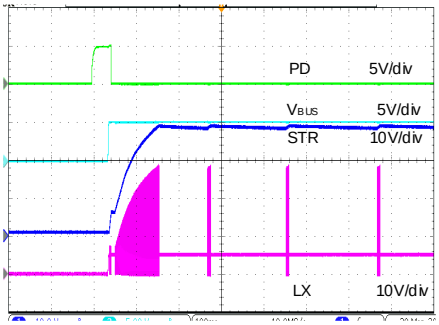
EN ON/OFF Test

(V_{IN}=5V,STR=28V,FBR threshold set to 4.4V, Buck regulated Voltage set to 4.2V CSTR= 220uF E-cap + 10uF, V_{BUS} null load, CV Mode)



Burst Mode VIN ON/OFF

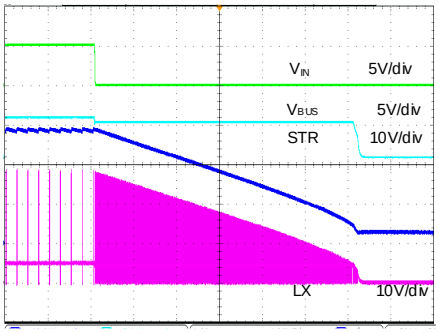
(V_{IN}=5V, STR=28V, FBR threshold set to 4.4V, Buck regulated Voltage set to 4.2V CSTR= 220uF E-cap + 10uF, V_{BUS} null load, CV Mode)



Time (100ms/div)

Burst Mode VIN ON/OFF

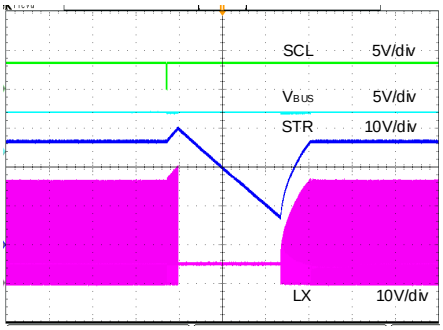
(V_{IN}=5V, STR=28V, FBR threshold set to 4.4V, Buck regulated Voltage set to 4.2V CSTR= 220uF E-cap + 10uF, V_{BUS} null load, CV Mode)



Time (1s/div)

CAP Detection Test

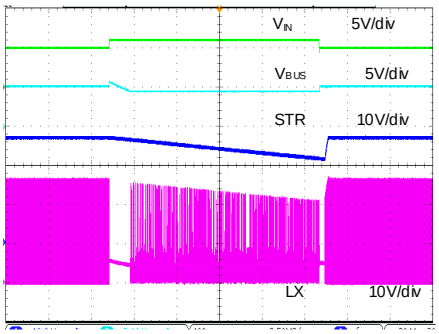
(V_{IN}=5V, STR=28V, FBR threshold set to 4.4V, Buck regulated Voltage set to 4.2V CSTR= 220uF E-cap + 10uF, V_{BUS} null load, CV Mode)



Time (100ms/div)

V_{IN} OVP Test

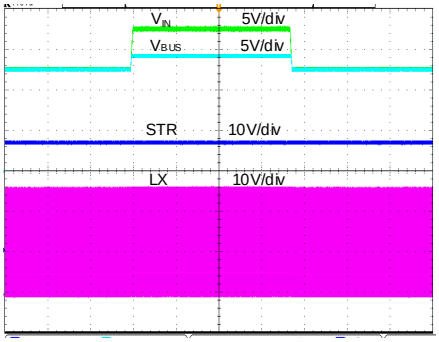
(V_{IN}=5V~6V~5V, STR=28V, FBR threshold set to 4.4V, Buck regulated Voltage set to 4.2V CSTR= 220uF E-cap + 10uF, V_{BUS} null load, CV Mode)



Time (400ms/div)

Load Switch OVP Clamp Test

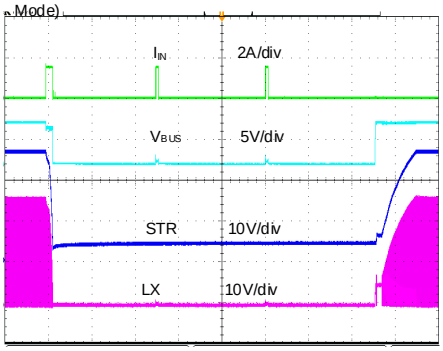
(V_{IN}=5V~6V~5V, VBUS null load, OVP clamp function is enabled)



Time (400ms/div)

Load Switch OCP Test

(V_{IN}=5V, STR=28V, FBR threshold set to 4.4V, Buck regulated Voltage set to 4.2V, LSW Current limit set to 1.2A, I_{BUS} =0~1.5A, ICSTR= 220uF E-cap + 10uF, CV Mode)

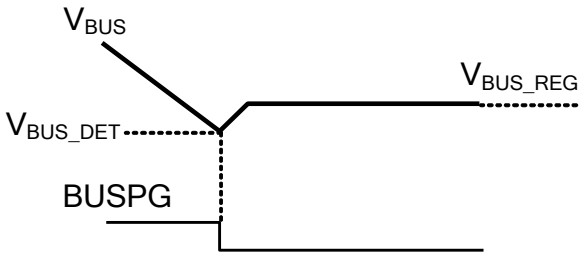


Time (100ms/div)

Application Information

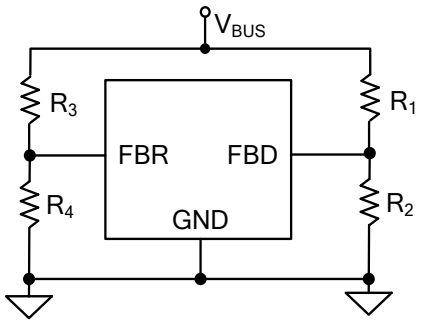
Feedback resistor dividers

Choose R_1 and R_2 to program proper BUS detection voltage V_{BUS_DET}. Choose R_3 and R_4 to program proper BUS regulation voltage V_{BUS_REG}. When BUS voltage falls to below V_{BUS_DET}, SY72025 enters buck mode and regulates the BUS voltage at V_{BUS_REG} as shown below. BUSPG is pulled low when SY72025 enters buck mode:



It is recommended to set the V_{BUS_DET} be lower than 1.05*V_{BUS_REG}.

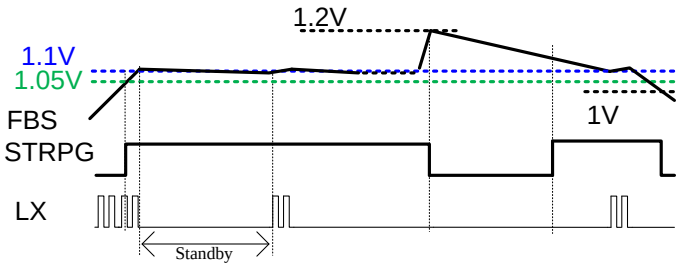
To minimize the power consumption under light load condition, it is recommended to choose relatively large resistance values for R_1, R_2, R_3 and R_4. A value of between 10kΩ and 1MΩ is more suitable for all resistors. If V_{BUS_DET} is programmed at 3.8V, R_1=250k is given, then using following equation, R_2 can be calculated to be 47k; If V_{BUS_REG} is programmed at 4.2V, R_3=250k is given, then using following equation, R_4 can be calculated to be 42k :



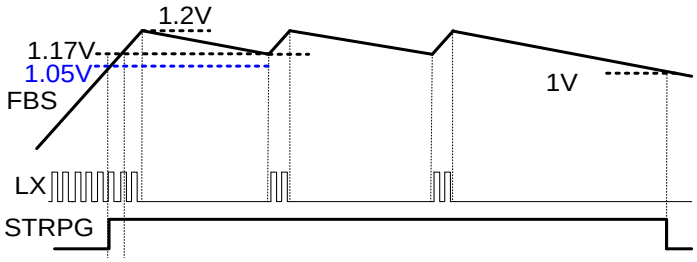
$$R_2 = \frac{0.6V}{V_{SYS\_DET} - 0.6V} R_1$$

$$R_4 = \frac{0.6V}{V_{SYS\_REG} - 0.6V} R_3$$

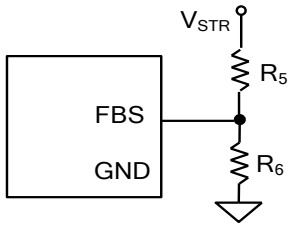
Choose R_5 and R_6 to program STR voltage and STR OVP value. In CV mode, FBS is regulated at 1.1V to minimize the STR output ripple. STRPG is pulled high when FBS voltage rises up to be higher than 1.05V and is pulled low when FBS voltage falls below 1V as shown below:



In burst mode, Boost converter stops working when FBS voltage rises up to be higher than 1.2V and starts working again when FBS voltage falls below 1.17V. STRPG is pulled high when FBS voltage rises up to be higher than 1.05V and is pulled low when FBS voltage falls below 1V as shown below:



To minimize the power consumption, it is recommended to choose relatively large resistance values for R_5 and R_6 both. A value of between 10kΩ and 1MΩ is more suitable for both resistors. If V_{STR} OVP is programmed at 12V, R_5=400k is given, then using following equation, R_6 can be calculated to be 44k:



$$R_6 = \frac{1.2V}{V_{CSTR\_OVP} - 1.2V} R_5 \cdot$$

Input capacitor C_{IN}

To minimize the potential noise problem, place MLCC cap with X5R or better grade really close to the IN and GND pins to decouple the high frequency noise. Be careful to minimize the loop size formed by C_{IN}, and IN/GND pins. A 0.1uF low ESR ceramic capacitor is recommended to minimum the input inrush current.

BUS capacitor C_{BUS}

The BUS capacitor is the input capacitor of boost converter and also the output capacitor of buck converter. Both steady state ripple and transient requirements must be taken into account to select proper capacitor. For most applications, MLCC cap which has total capacitance greater than 66uF with X5R or better grade can work well. The real capacitance derating with DC voltage must be considered.

STR capacitor C_{STR}

The STR capacitor is used to store energy and transfers it to BUS side when the power supply at input side is plugged out. BUS voltage can be hold for long time if larger STR capacitance is used. The total capacitance is calculated below:

$$C_{STR} = \frac{2 \times V_{BUS\_REG} \times I_{BUS} \times t_{HOLD}}{\eta \times (V_{STR}^2 - V_{BUS}^2)}$$

where C_{STR} is total capacitance of STR capacitors, V_{BUS_REG} is the programmed BUS regulation voltage, I_{BUS} is BUS load current, t_{HOLD} is desired BUS voltage hold time after IN is plug out, and V_{STR} is programmed STR voltage, η is the efficiency of the buck converter, can use 85% as a typical efficiency value

Selection of Inductor L

Choose proper inductance to achieve the desired ripple current. If ripple current equals to 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where Fsw is the switching frequency; $I_{OUT,MAX}$ is the maximum BUS load current; V_{out} is programmed BUS output voltage and $V_{IN,MAX}$ is programmed STR OVP voltage.

Normally, it is recommended to use 4.7uH inductor for 500kHz buck application and 2.2uH inductor for 1MHz application.

External Bootstrap Cap

This capacitor provides the gate driver voltage for internal high side MOSFET. A 100nF low ESR MLCC capacitor is connected between BST pin and LX pin.

Boost Inductor Peak Current Limit

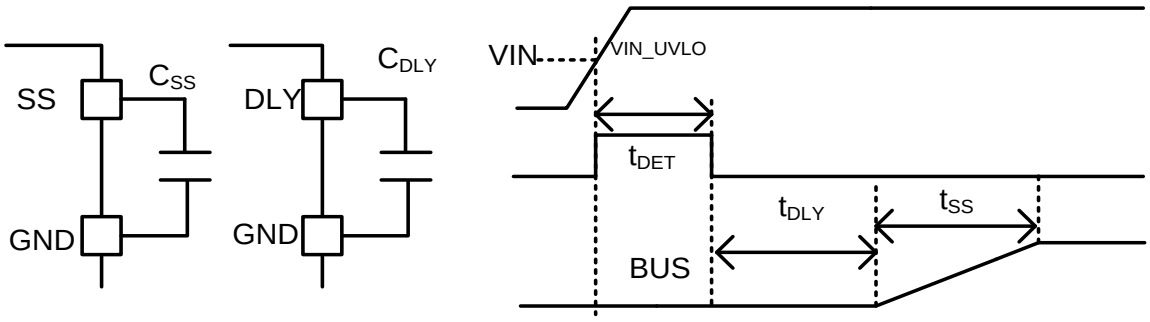
There's negative inductor current because of the min on time of the high side MOSFET when boost peak current is programmed higher than 800mA. The STR voltage could not be charged up to the programmed voltage level due to the negative inductor current. In order to charge the STR capacitors to desired value, it is recommended to set the boost peak current at a proper level. The maxim T_{MINON} value of HSFET is 120ns when boost peak current is programmed at 1A, 1.5A, 2A and 2.5A. The formula is presented below for proper boost peak current setting reference.

V_{STR}-V_{IN}=L dI / dT → dI=(V_{STR}-V_{IN})*dT / L=(V_{STR}-V_{IN})*T_{MINON} / L;

I_{PEAK} ≧ dI / 2 → I_{PEAK} ≧ (V_{STR}-V_{IN})*T_{MINON} / 2*L;

Delay Time and Soft Start Time Program

Connect a capacitor between DLY pin and GND to program the load switch turn on delay time. Connect a capacitor between SS pin and GND to program the load switch soft start time.



The turn on delay time calculation formula is shown below:

$$T_{DLY} = \begin{cases} T_{DLY\_DLT}, & \text{No external } C_{DLY} \\ \dfrac{C_{DLY}}{I_{INT\_DLY}}, & T_{DLY} > T_{DLY\_DLT} \end{cases},$$

Where, T_{DLY_DLT} is the internally fixed default soft-start time, about 1.4ms, which means there's no any external C_{DLY}; I_{INT_DLY} is the internal current source, about 3.6uA.

The soft start time calculation formula is shown as below:

$$T_{SS} = \begin{cases} T_{SS\_DLT}, & \text{No external } C_{SS} \\ \dfrac{C_{SS}}{I_{INT\_SS}}, & T_{SS} > T_{SS\_DLT} \end{cases},$$

Where, T_{SS_DLT} is the internally fixed default soft-start time, about 1ms, which means there's no any external C_{SS}; I_{INT_SS} is the internal current source, about 7.2uA.

STR Capacitance Measurement

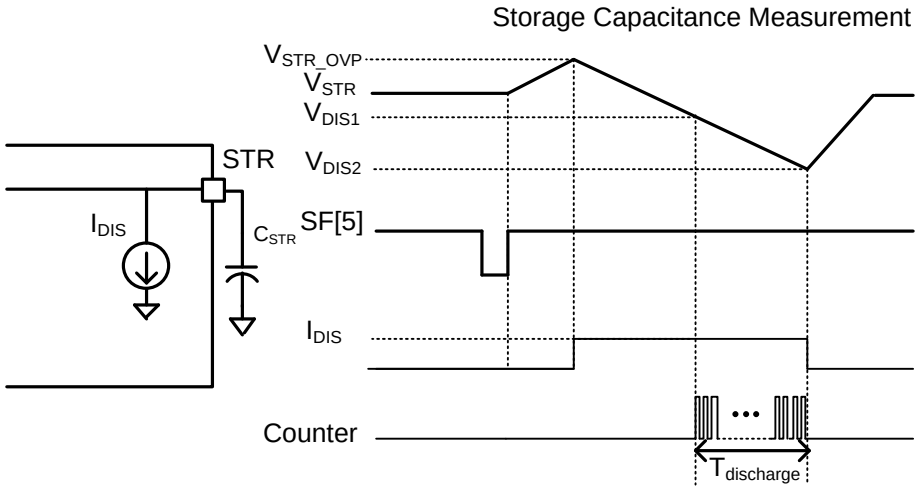
Storage capacitance measurement starts when a rising edge on SF[5] is detected. MCU can start measuring by setting SF[5] to 1.

Programmed discharge current I_{DIS} starts to discharge STR capacitors. Internal 8kHz counter calculates the discharge time starting from when STR voltage falls below $V_{DIS1}$to when STR voltage falls below V_{DIS2}. The discharge time data $T_{DISCHARGE}$ is stored to data register REG07 and REG08. For example, if data read from REG07 is 0x12H, data read from REG08 is 0x34H, the $T_{DISCHARGE}$ should be calculated below:

$T_{DISCHARGE}$=0X1234H=$(1*16^3+2*16^2+3*16^1+4*16^0)$*0.125ms=582.5ms

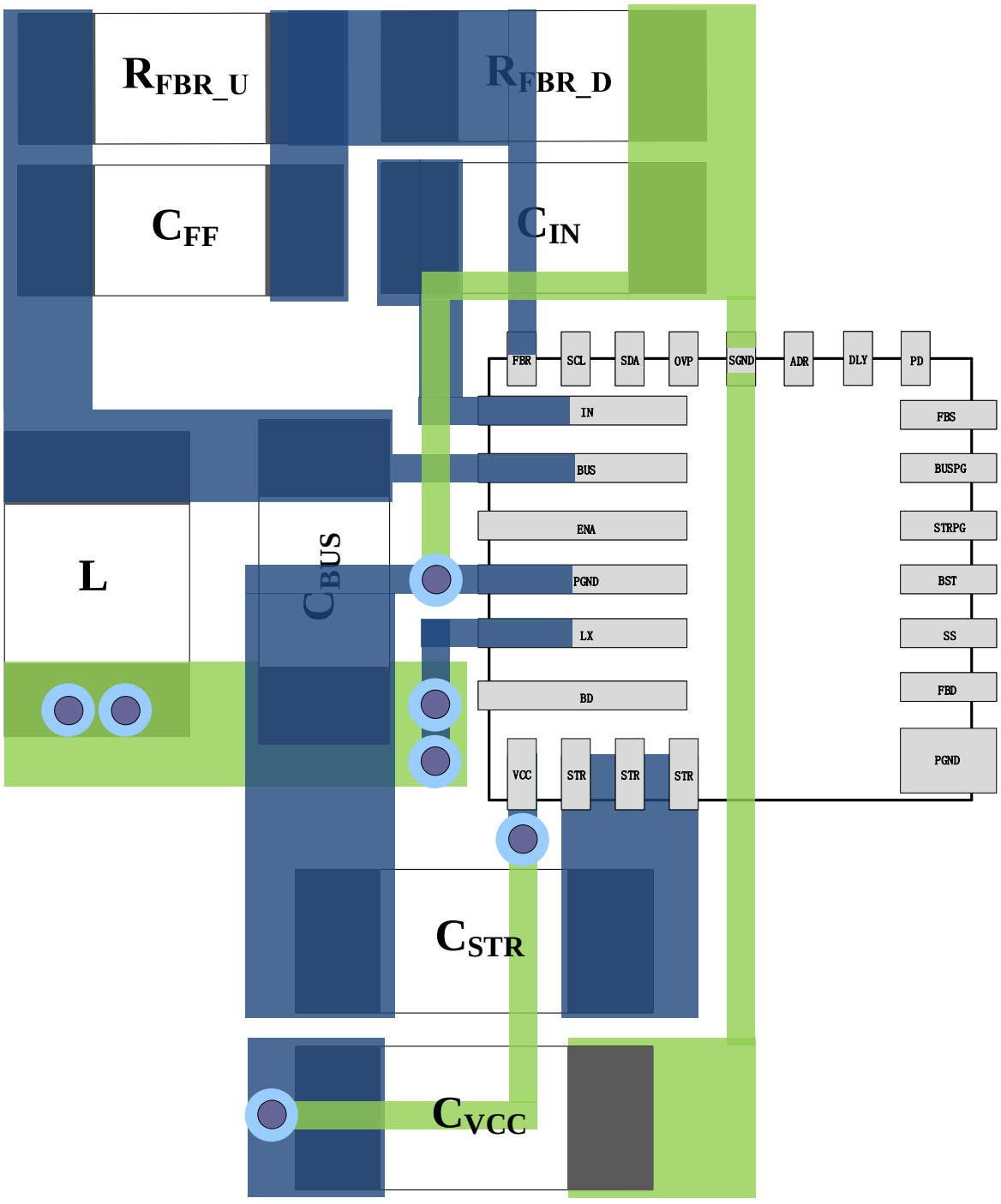
And then, the capacitance can be calculated below:

$C_{STR}=I_{DIS}*T_{DISCHARGE}/(V_{DIS1}-V_{DIS2})$

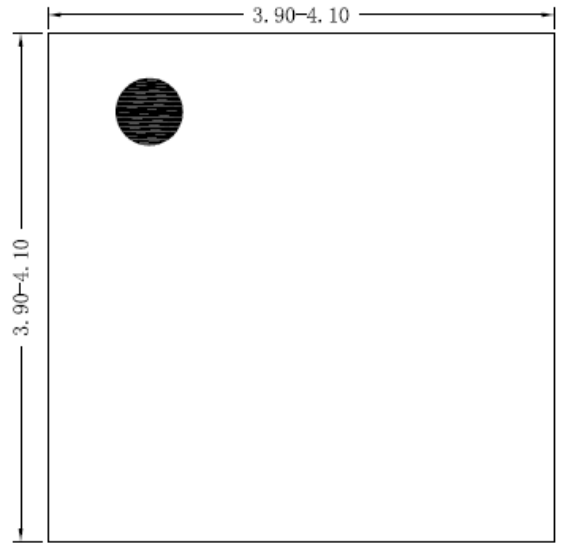


PCB Layout Recommendation

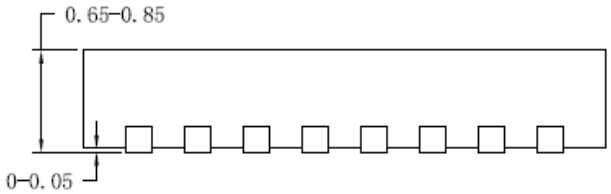
Put C_{IN}, C_{BUS}, C_{STR}, R_{FBR_D} as close as possible to the IC. Decouple C_{STR} to PGND. Decouple C_{VCC} to SGND. Connect the SGND PIN and the PGND PIN together at a single point.



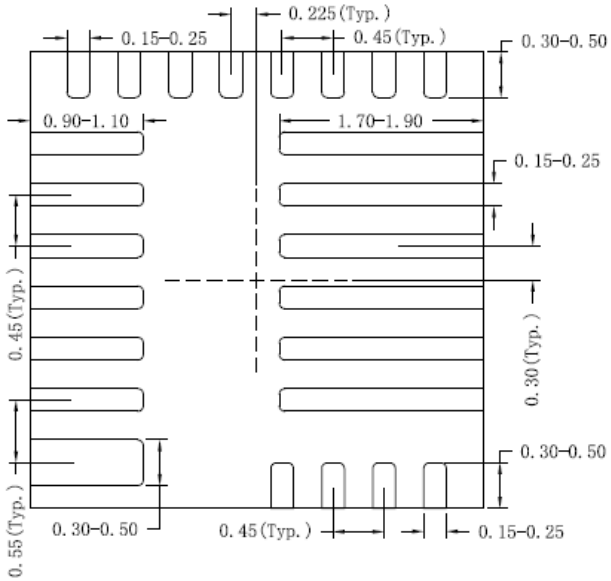
QFN4×4-25 Package Outline Drawing



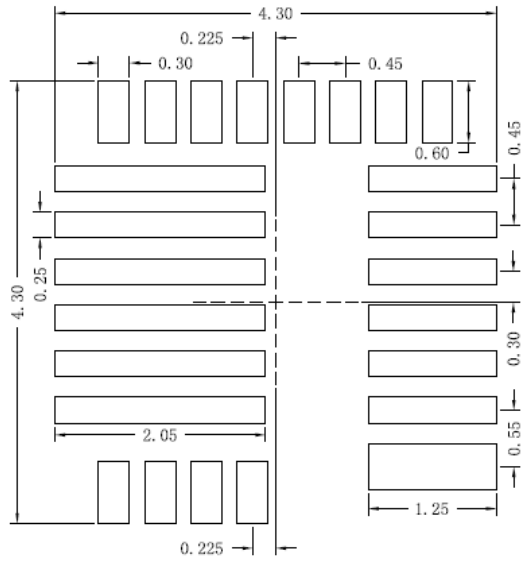
Top View



Side View



Bottom View

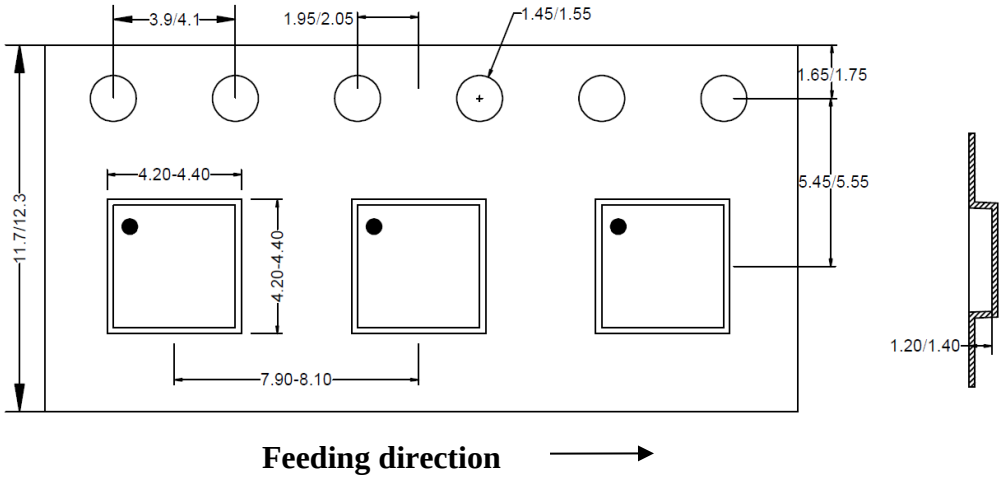


Recommended PCB layout
(Reference only)

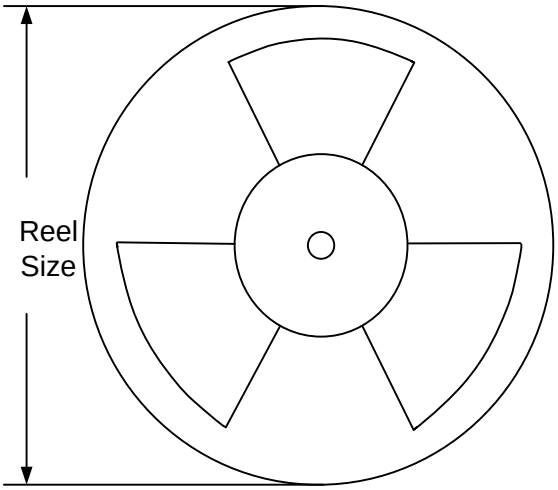
Notes: **All dimension in MM and exclude mold flash & metal burr.**

Taping & Reel Specification

1. QFN4×4 Taping Orientation



2. Carrier Tape & Reel Specification for Packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN4×4	12	8	13"	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Apr. 14, 2023	Revision 0.9	Initial risk production release.
Jul. 07, 2023	Revision 0.9A	Remove cap test reset description.
Sep. 27, 2023	Revision 0.9B	1. Change second VDIS1_REG to VIDS2_REG of Register MAP summary. 2. Remove current limit soft start description. 3. Update STRG short latch detection deglitch time from 50ms to 125ms.
Apr.10, 2024	Revision 0.9C	Add detail dimension of taping.
Mar.24, 2025	Revision 1.0	Initial production release.

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