

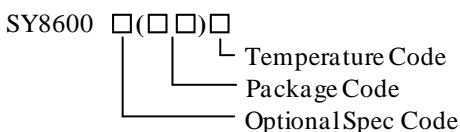
### General Description

The SY8600F is a high efficiency PMIC with 5-channel synchronous buck converters and 2-channel LDOs. It is a single chip total power solution for SSD system.

The output voltage of each channel is controlled by the processor using I<sup>2</sup>C interface. It therefore supports DVS (Dynamic Voltage Scaling) function for each channel. SY8600F can generate an open-drain reset output for the processor with certain delay time.

The SY8600F operates over a wide input voltage range from 2.8V to 5.5V. It is available in CSP3.23x3.23-52 package.

### Ordering Information



Ordering Number	Package type	Note
SY8600FPZS	CSP3.23×3.23-52	----

### Features

- 2.8V to 5.5V Input Voltage Range
- Channel 1 Synchronous Buck:
  - Low R<sub>DS(ON)</sub> for Internal Switches (PFET/NFET): 150/150 mΩ
  - 0.9A Maximum Output Current Capability
  - Default Output Voltage: V<sub>OUT1</sub>=1.2V
- Channel 2 LDO1:
  - 0.3A Output Current Capability
  - Default Output Voltage V<sub>OUT2</sub>=1.8V
- Channel 3 Synchronous Buck:
  - Low R<sub>DS(ON)</sub> for Internal Switches (PFET/NFET): 45/20 mΩ
  - 4.0A Maximum Output Current Capability
  - Default Output Voltage V<sub>OUT3</sub>=0.90V
  - 0.7V to 1.1V Programmable, 10mV Step
- Channel 4 Synchronous Buck:
  - Low R<sub>DS(ON)</sub> for Internal Switches (PFET/NFET): 35/45 mΩ
  - 4.0A Maximum Output Current Capability
  - 2.1V to 3.0V Programmable, 100mV Step
  - Default Output Voltage:

VSEL4	V <sub>OUT4</sub>
0	2.5V
1	Bypass

- Channel 5 Synchronous Buck:

- Low R<sub>DS(ON)</sub> for Internal Switches (PFET/NFET): 60/40 mΩ
- 2.0A Output Current Capability
- Default Output Voltage:

VSEL5	V <sub>OUT5</sub>
0	1.8V
1	1.2V

- Channel 6 LDO2:
  - 0.3A Output Current Capability
  - Default Output Voltage V<sub>OUT6</sub>=2.5V
- Channel 7 Synchronous Buck:
  - Low R<sub>DS(ON)</sub> for Internal Switches (PFET/NFET): 60/40 mΩ
  - 2.0A Output Current Capability
  - Default Output Voltage V<sub>OUT7</sub>=1.2V
- Reset Input/Output Function
- 2.0MHz Switching Frequency for Buck Converters
- Auto PWM/PFM Mode or Forced PWM Mode Controlled by I<sup>2</sup>C Interface
- I<sup>2</sup>C Interface up to 3.4MHz
- Output Voltage Level of CH3/CH4 Controlled by I<sup>2</sup>C Interface with DVS Function
- 2 Kinds of Power on Reset Detection Voltage Level Selected by PORSEL Pin
- Dedicated Sleep Mode Controlled by GPIO1/GPIO2, PMRST
- Reliable Protections:
  - Over Voltage Protection (OVP)
  - Over Current Protection (OCP)
  - Short Circuit Protection (SCP)
  - Over Temperature Protection (OTP)
- Compact Package: CSP3.23x3.23-52(0.4mm pitch)

### Applications

- SSD Power System

## Typical Applications

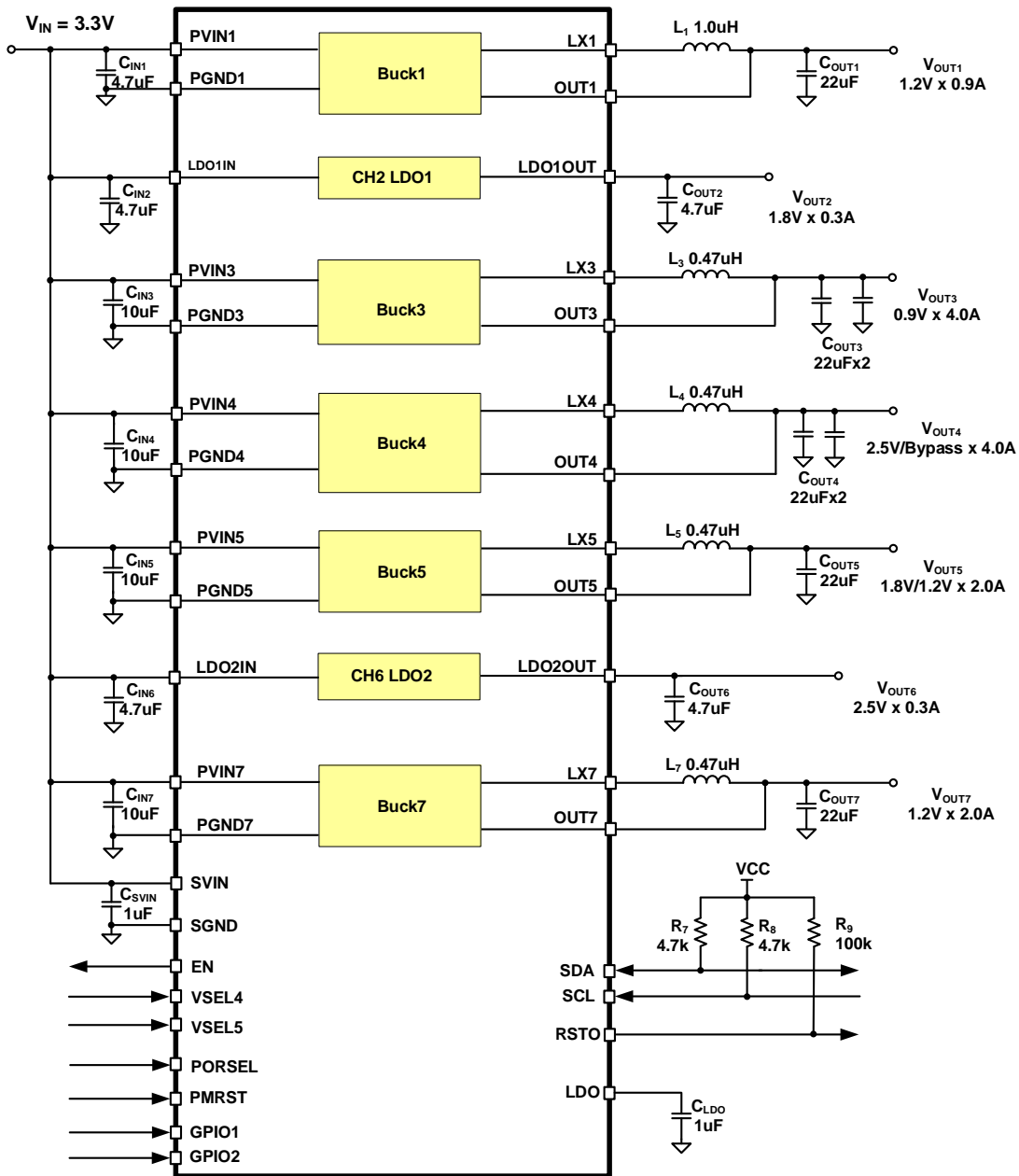
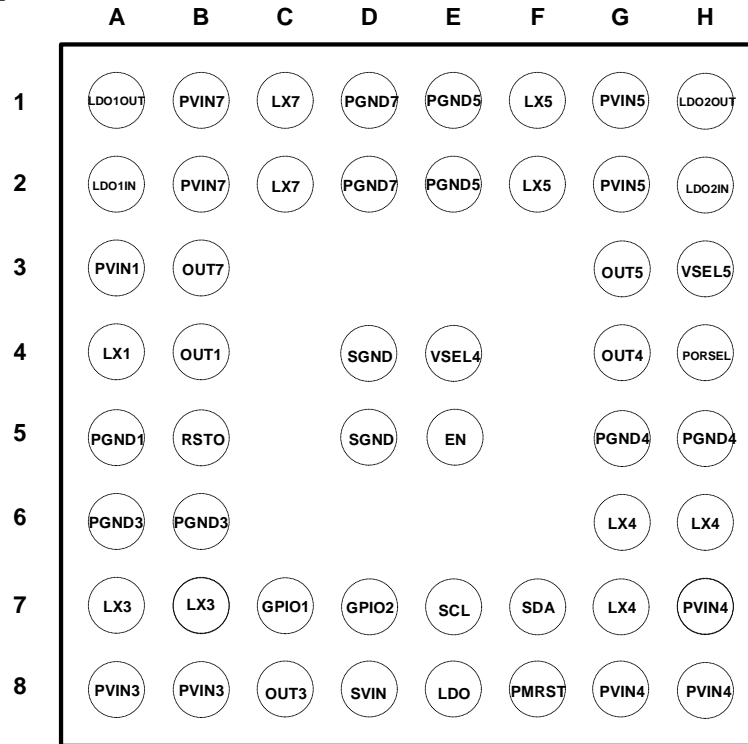


Figure 1. Schematic Diagram

## PINOUT (Top View)



Top Mark:ENQxyz (Device code: ENQ, *x*=year code, *y*=week code, *z*=lot number code)

Pin Name	Pin Number	Pin Description
LDO1OUT	A1	CH2 LDO1 power output pin. Decouple this pin to GND with at least 2.2uF MLCC cap.
LDO1IN	A2	CH2 LDO1 power input pin. Decouple this pin to GND with at least 2.2uF MLCC cap.
PVIN1	A3	Power input pin of Buck1. Decouple this pin to PGND1 with 10uF MLCC cap.
LX1	A4	Switching node pin for Buck1. Connect this pin to the switching node of inductor.
PGND1	A5	Power ground pin of Buck1.
OUT7	B3	Output feedback pin of Buck7. Connect this pin to VOUT7 to regulate the output voltage.
PVIN7	B1,B2	Power ground pin of Buck7.
LX7	C1,C2	Switching node pin for Buck7. Connect this pin to the switching node of inductor.
PGND7	D1,D2	Power input pin of Buck7. Decouple this pin to PGND7 with 10uF MLCC cap.
PGND5	E1,E2	Power input pin of Buck5. Decouple this pin to PGND5 with 10uF MLCC cap.
LX5	F1,F2	Switching node pin for Buck5. Connect this pin to the switching node of inductor.
PVIN5	G1,G2	Power ground pin of Buck5.
OUT5	G3	Feedback pin of Buck5. Connect this pin to VOUT5 to regulate the output voltage.
LDO2OUT	H1	LDO2 power output pin. Decouple this pin to GND with at least 2.2uF MLCC cap.
LDO2IN	H2	LDO2 power input pin. Decouple this pin to GND with at least 2.2uF MLCC cap.
VSEL5	H3	Channel5 default output voltage selection pin.
PORSEL	H4	POR threshold selection pin.
VSEL4	E4	Channel4 default output voltage selection pin.
OUT4	G4	Feedback pin of Buck4. Connect this pin to VOUT4 to regulate the output voltage.
PGND4	G5,H5	Power ground pin of Buck4.

LX4	G6,G7,H6	Switching node pin for Buck4. Connect this pin to the switching node of inductor.
PVIN4	H7,G8,H8	Power input pin of Buck4. Decouple this pin to PGND4 with 10uF MLCC cap.
SDA	F7	Data line for the I <sup>2</sup> C interface. Open drain.
SCL	E7	Clock input for the I <sup>2</sup> C interface. Open drain input.
LDO	E8	Internal LDO output pin, decouple this pin to PGND with 1uF MLCC cap.
PMRST	F8	PMIC reset input pin. All of the channels will go back to previous value before when PMRST falling edge is detected. Internally, a 2M $\Omega$ resistor is integrated to pull low this pin when it is not used.
SGND	D4,D5	Signal power ground pin.
EN	E5	Enable output pin to enable/disable external DCDC.
GPIO1	C7	Dedicated Sleep mode control pin1.
GPIO2	D7	Dedicated Sleep mode control pin2.
SVIN	D8	Signal power supply input pin. Decouple this pin to GND with at least 1uF MLCC cap.
OUT3	C8	Output feedback pin of Buck3. Connect this pin to VOUT3 to regulate the output voltage.
PVIN3	A8,B8	Power input pin of Buck3. Decouple this pin to PGND3 with 10uF MLCC cap.
LX3	A7,B7	Switching node pin for Buck3. Connect this pin to the switching node of inductor.
PGND3	A6,B6	Power ground pin of Buck3.
RSTO	B5	Reset output pin.
OUT1	B4	Output feedback pin of Buck1. Connect this pin to VOUT1 to regulate the output voltage.

## Absolute Maximum Ratings (Note 1)

All PINs	-0.3V to 6.0V
Power Dissipation, PD @ TA = 25°C CSP3.23x3.23-52	5W
Package Thermal Resistance (Note 2) $\theta_{JA}$ , CSP3.23x3.23-52	24W/°C
$\theta_{JC}$ , CSP3.23x3.23-52	1W/°C
Junction Temperature Range	150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	-55°C to 150°C

## Recommended Operating Conditions (Note 3)

Supply Input Voltage	2.8V to 5.5V
Junction Temperature Range	-40°C to 125°C
Ambient Temperature Range	-40°C to 85°C

## Electrical Characteristics

( $V_{IN}=3.3V/5V$ ,  $T_A = 25^{\circ}C$ , unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	$V_{IN}$		2.8		5.5	V
Input Voltage UVLO Threshold	$V_{UVLO,FALLING}$	PORSEL=0 $V_{IN}$ falling	2.561	2.6	2.639	V
		PORSEL=1 $V_{IN}$ falling	3.546	3.6	3.654	V
Input Voltage UVLO Hysteresis	$V_{UVLO,HYS}$	Hysteresis		100		mV
POR Threshold	$V_{POR,FALLING}$	PORSEL=0 $V_{IN}$ falling	2.561	2.6	2.639	V
		PORSEL=1 $V_{IN}$ falling	3.546	3.6	3.654	V
POR Hysteresis	$V_{POR,HYS}$	Hysteresis		100		mV
System delay time from UVLO	$T_{SYS}$			1		ms
Quiescent Current	$I_Q$	No load input current. $V_{in}=3.3V$		140	170	$\mu A$
		No load input current. $V_{in}=5V$		180	210	$\mu A$
<b>VSEL4,VSEL5, PORSEL, PMRST, GPIO1, GPIO2</b>						
Logic level high	$V_{HIGH}$		1.2			V
Logic level low	$V_{LOW}$				0.4	V
<b>EN</b>						
Output high voltage	$V_{OH}$	$R_{EN}=100k$ to GND	0.8x		$V_{IN}$	V
Output low voltage	$V_{OL}$	$R_{EN}=100k$ to GND			$0.2xV_{IN}$	V
EN turn high delay time from $V_{IN}$	$T_{EN}$	After system delay time		1.5		ms
<b>Power-On Reset(POR)</b>						
POR Deglitch delay		$V_{in}$ Falling		2		$\mu s$
RSTO output low resistance				10		$\Omega$
RSTO Delay time from UVLO threshold	$T_{POR,DEL}$	$V_{IN}=3.3V$	10.8	12	13.2	ms
<b>I2C COMPATIBLE I/O (SDA,SCL)</b>						
Maximum operating frequency	$f_{SCL}$				3.4	MHz
I2C supply voltage				1.8	5.5	V
SDA and SCL pin input logic thresholds	Logic low				0.5	V
	Logic high		1.2			V
<b>Channel 1 Synchronous Buck Converter</b>						
Output Voltage Default Value	$V_{OUT1,DEF}$			1.2		
Output voltage Accuracy	$\Delta V_{OUT1}$	PWM mode operation	-1		+1	%
Switching frequency	$F_{OSC1}$			2.0		MHz
Main PFET $R_{ON}$	$R_{DS(ON),P1}$			150		m $\Omega$
Synchronous NFET $R_{ON}$	$R_{DS(ON),N1}$			150		m $\Omega$
High side FET Current Limit	$I_{LIM1\_HS}$		1.6			A
Max output DC load current	$I_{OUT1}$		0.9			A

Internal Softstart Time	T <sub>SS1</sub>	V <sub>OUT</sub> rising from 10% to 90%		200		us
Start-up default delay time	T <sub>DELAY1</sub>	After system delay		2		ms
Discharge Resistor	R <sub>DIS1</sub>			10		Ω
SCP Threshold	V <sub>SCP1</sub>	V <sub>SCP1</sub> <V <sub>OUT1</sub> ×30%		30		%
SCP Deglitch Time	t <sub>SCP1</sub>			10		μs
<b>Channel 2 LDO</b>						
Output Voltage Default Value	V <sub>LDO1OUT</sub>			1.8		V
Output Voltage Accuracy	V <sub>OUT2</sub>	I <sub>OUT2</sub> =10mA	-1%		+1%	
Current Limit	I <sub>LIM2</sub>		0.35			A
Max output DC load current	I <sub>OUT2</sub>		0.3			A
Dropout Voltage		I <sub>OUT2</sub> =0.3A			300	mV
Internal Softstart Time	T <sub>SS2</sub>	V <sub>OUT</sub> rising from 10% to 90%		200		us
Start-up default delay time	T <sub>DELAY2</sub>	After system delay		1.5		ms
Discharge Resistor	R <sub>DIS2</sub>			10		Ω
SCP Threshold	V <sub>SCP2</sub>	V <sub>SCP2</sub> <V <sub>OUT2</sub> ×60%		60		%
SCP Deglitch Time	t <sub>SCP2</sub>			100		μs
<b>Channel 3 Synchronous Buck Converter</b>						
Output Voltage Default Value	V <sub>OUT3,DEF</sub>			0.9		V
DVS Voltage Step	V <sub>OUT3,DVS,STEP</sub>	Controllable by I <sup>2</sup> C interface		10		mV
DVS Voltage Range	V <sub>OUT3,DVS</sub>	Controllable by I <sup>2</sup> C interface	0.7		1.1	mV
Output voltage Accuracy	ΔV <sub>OUT3</sub>	PWM mode operation	-1		+1	%
Switching frequency	F <sub>OSC3</sub>			2.0		MHz
Main PFET R <sub>ON</sub>	R <sub>DS(ON),P3</sub>			45		mΩ
Synchronous NFET R <sub>ON</sub>	R <sub>DS(ON),N3</sub>			20		mΩ
High side FET Current Limit	I <sub>LIM3_HS</sub>		5.0			A
Low side FET Current Limit	I <sub>LIM3_LS</sub>		4.0			A
Max output DC load current	I <sub>OUT3</sub>		4.0			A
Internal Softstart Time	T <sub>SS3</sub>	V <sub>OUT</sub> rising from 10% to 90%		200		us
Start-up default delay time	T <sub>DELAY3</sub>	After system delay		0.5		ms
Discharge Resistor	R <sub>DIS3</sub>			10		Ω
SCP Threshold	V <sub>SCP3</sub>	V <sub>SCP3</sub> <V <sub>OUT3</sub> ×30%		30		%
SCP Deglitch Time	t <sub>SCP3</sub>			10		μs
<b>Channel 4 Synchronous Buck Converter</b>						
Output Voltage Default Value	V <sub>OUT4,DEF</sub>	VSEL4=0		2.5		V
		VSEL4=1		Bypass		
DVS Voltage Step	V <sub>OUT4,DVS,STEP</sub>	Controllable by I <sup>2</sup> C interface		100		mV
DVS Voltage Range	V <sub>OUT4,DVS</sub>	Controllable by I <sup>2</sup> C interface	2.1		3.0	V
Output voltage Accuracy	ΔV <sub>OUT4</sub>	PWM mode operation	-1		+1	%

Switching frequency	F <sub>OSC4</sub>			2.0		MHz
Main PFET R <sub>ON</sub>	R <sub>DS(ON),P4</sub>			35		mΩ
Synchronous NFET R <sub>ON</sub>	R <sub>DS(ON),N4</sub>			45		mΩ
High side FET Current Limit	I <sub>LIM4_HS</sub>		5.0			A
Low side FET Current Limit	I <sub>LIM4_LS</sub>		4.0			A
Max output DC load current	I <sub>OUT4</sub>		4.0			A
Internal Softstart Time	T <sub>SS4</sub>	V <sub>OUT</sub> rising from 10% to 90%		200		us
Start-up default delay time	T <sub>DELAY4</sub>			3.0		ms
Discharge Resistor	R <sub>DIS4</sub>			10		Ω
SCP Threshold	V <sub>SCP4I</sub>	V <sub>SCP4</sub> <V <sub>OUT4</sub> x30%		30		%
SCP Deglitch Time	t <sub>SCP4</sub>			10		μs
<b>Channel 5 Synchronous Buck Converter</b>						
Output Voltage Default Value	V <sub>OUT5,DEF</sub>	VSEL5=0		1.8		V
		VSEL5=1		1.2		
Output voltage Accuracy	ΔV <sub>OUT5</sub>	PWM mode operation	-1		+1	%
Switching frequency	F <sub>OSC5</sub>			2.0		MHz
Main PFET R <sub>ON</sub>	R <sub>DS(ON),P5</sub>			60		mΩ
Synchronous NFET R <sub>ON</sub>	R <sub>DS(ON),N5</sub>			40		mΩ
High side FET Current Limit	I <sub>LIM5_HS</sub>		3.0			A
Low side FET Current Limit	I <sub>LIM5_LS</sub>		2.0			A
Max output DC load current	I <sub>OUT5</sub>		2.0			A
Internal Softstart Time	T <sub>SS5</sub>	V <sub>OUT</sub> rising from 10% to 90%		200		us
Start-up default delay time	T <sub>DELAY5</sub>	After system delay		5.5		ms
Discharge Resistor	R <sub>DIS5</sub>			10		Ω
SCP Threshold	V <sub>SCP5</sub>	V <sub>SCP5</sub> <V <sub>OUT5</sub> x30%		30		%
SCP Deglitch Time	t <sub>SCP5</sub>			10		μs
<b>Channel 6 LDO</b>						
LDO input voltage range	V <sub>IN,LDO</sub>		2.8	3.3	5.5	V
Output Voltage Default Value	V <sub>OUT6,DEF</sub>			2.5		V
Output Voltage Accuracy	V <sub>OUT6</sub>	I <sub>OUT6</sub> =10mA	-1%		+1%	
Current Limit	I <sub>LIM6</sub>		0.35			A
Max output DC load current	I <sub>OUT6</sub>		0.3			A
Dropout Voltage		I <sub>OUT6</sub> =0.3A			300	mV
Internal Softstart Time	T <sub>SS6</sub>	V <sub>OUT</sub> rising from 10% to 90%		200		us
Start-up default delay time	T <sub>DELAY6</sub>	After system delay		4.5		ms
Discharge Resistor	R <sub>DIS6</sub>			10		Ω
SCP Threshold	V <sub>SCP6</sub>	V <sub>SCP6</sub> <V <sub>OUT6</sub> x60%		60		%

SCP Deglitch Time	tSCP6			100		μs
<b>Channel 7 Synchronous Buck Converter</b>						
Output Voltage Default Value	V <sub>OUT7,DEF</sub>			1.2		V
Output voltage Accuracy	ΔV <sub>OUT7</sub>	PWM mode operation	-1		+1	%
Switching frequency	F <sub>OSC5</sub>			2.0		MHz
Main PFET R <sub>ON</sub>	R <sub>DS(ON),P7</sub>			60		mΩ
Synchronous NFET R <sub>ON</sub>	R <sub>DS(ON),N7</sub>			40		mΩ
High side FET Current Limit	I <sub>LIM7_HS</sub>		3.0			A
Low side FET Current Limit	I <sub>LIM7_LS</sub>		2.0			A
Max output DC load current	I <sub>OUT7</sub>		2.0			A
Internal Softstart Time	T <sub>SS7</sub>	V <sub>OUT</sub> rising from 10% to 90%		200		us
Start-up default delay time	T <sub>DELAY7</sub>	After system delay		5		ms
Discharge Resistor	R <sub>DIS7</sub>			10		Ω
SCP Threshold	V <sub>SCP7</sub>	V <sub>SCP7</sub> < V <sub>OUT7</sub> × 30%		30		%
SCP Deglitch Time	tSCP7			10		μs
<b>Protection</b>						
Thermal Shut Down Threshold	T <sub>SD</sub>			155		°C
Thermal Shutdown Hysteresis				20		°C
External V <sub>IN</sub> OVP Protection Threshold		V <sub>IN</sub> rising, PORSEL=0	3.7	3.85	4.0	V
		V <sub>IN</sub> rising, PORSEL=1	5.75	6.0	6.25	
Input OVP Hysteresis		V <sub>IN</sub> falling		0.15		V
External V <sub>IN</sub> OVP deglitch time				5		μs

**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:** JA is measured in the natural convection at T<sub>A</sub> = 25°C on a four-layer Silergy Evaluation Board.

**Note 3:** The device is not guaranteed to function outside its operating conditions.

## Description

### 1. Targeted Output Voltage:

		Default Output Voltage(V)		Out Voltage Range(V)	DVS Step (mV)	RDS(ON) (mΩ)		IOUT MAX (A)	Power On Delay Time (ms)	SS Time (us)
						High Side	Low Side			
CH1	Buck	1.2		-	-	150	150	0.9	2	200
CH2	LDO	1.8		-	-	-	-	0.3	1.5	200
CH3	Buck	0.9		0.7~1.1	10	45	20	4	0.5	200
CH4	Buck	VSEL4	VOUT4	2.1~3.0	100	35	45	4	3	200
		0	2.5							
		1	Bypass							
CH5	Buck	VSEL5	VOUT5	-	-	60	40	2	5.5	200
		0	1.8							
		1	1.2							
CH6	LDO	2.5		-	-	-	-	0.3	4.5	200
CH7	Buck	1.2		-	-	60	40	2	5	200
RSTO	-	-		-	-	-	-	-	12	-

### 2. POR Threshold and RSTO Delay:

POR threshold selection:

PORSEL pin is pulled low to select the default 2.6V threshold voltage for 3.3V input application;

PORSEL pin is pulled high to select the default 3.6V threshold voltage for 5.0V input application;

	Default Falling Detection Threshold
PORSEL=0	2.6V
PORSEL=1	3.6V

POR sequence:

When  $V_{IN}$  exceeds the threshold voltage, RSTO will provide a high-level output signal after an fixed 12ms delay time  $T_{POR,DEL}$ .

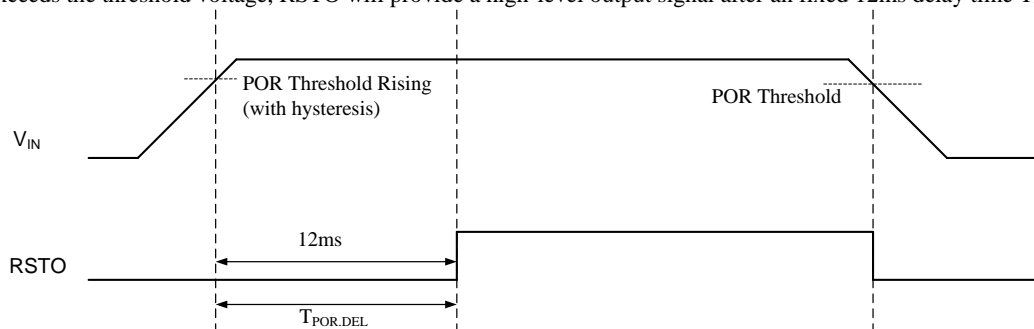


Figure 3. RSTO Delay

### 3. $V_{IN}$ Power-on / Power-off Sequence:

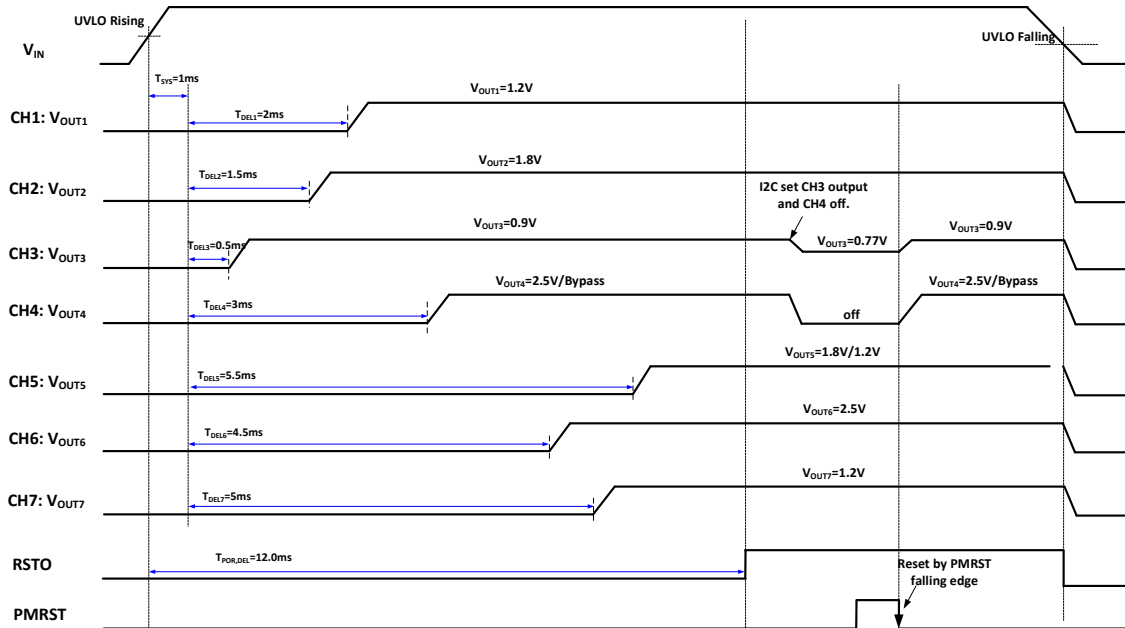


Figure 4.  $V_{IN}$  power on/off sequence

1. When input voltage  $V_{IN}$  exceeds input UVLO rising threshold, after system delay  $T_{SYS}=1\text{ms}$ , each channel will power on with fixed delay time  $T_{DELn}$ .
2. When  $V_{in}$  exceeds input UVLO threshold, RSTO will provide a high-level output signal after fixed delay time  $T_{POR,DEL}=12\text{ms}$ .
3. All channels would go back to previous value at same time when PMRST falling edge is detected.
4. Power off stage: All channels will be turned off immediately at same time if  $V_{in}$  is lower than UVLO falling threshold. The discharge resistor is turned on at power off stage if the corresponding discharge register bit is set to 1.

### 4. SLEEP mode controlled by GPIO1/GPIO2 pin.

GPIO1 and GPIO2 can be used to make PMIC enter dedicated sleep mode as below: GPIO1 and GPIO2 are effective after RSTO delay time finished.

	GPIO1	GPIO2	Channel on/off state
Normal MODE	1	X	ON/OFF controlled by I2C
Low Power Mode1(PS3.5)	0	1	CH4/CH5 OFF, other channels ON; CH3: keep 0.90V.
Low Power Mode2(PS4.0)	0	0	CH4/CH5/CH7 OFF, other channels ON; CH3: 0.9V $\rightarrow$ 0.77V.

#### Case I: Low Power Mode1(PS3.5)

When GPIO2 keeps high level and GPIO1 is pulled low, PMIC enters Low Power Mode1(PS3.5), CH4/CH5 are turned off, other channels ON and Ch3 output voltage keeps 0.9V.

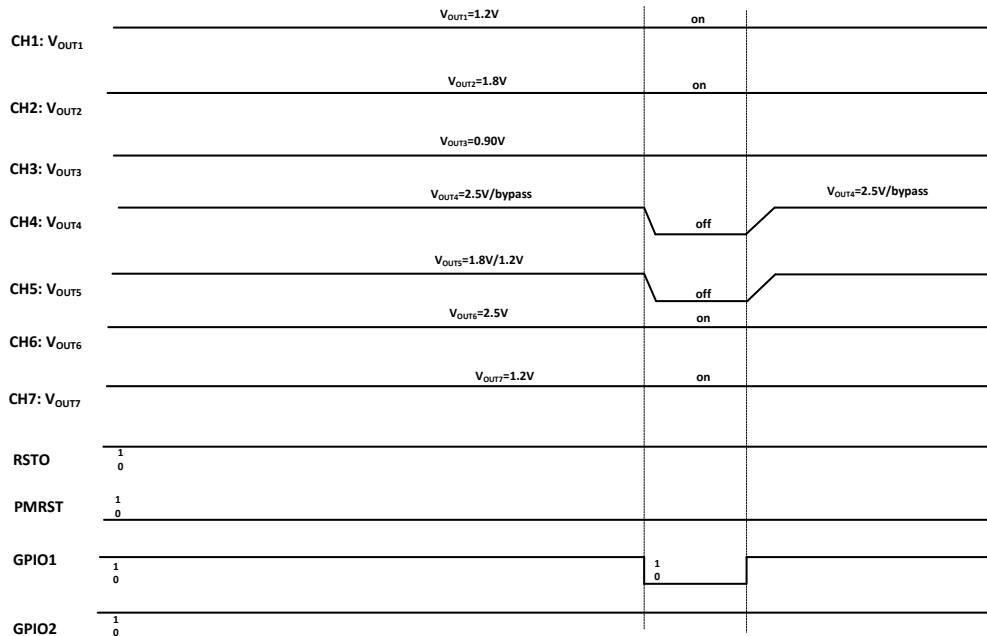


Figure 5.

### Case 2: Low Power Mode2(PS4.0)

When GPIO1 and GPIO2 are pulled low at same time, PMIC enters Low Power Mode2(PS4.0), CH4/CH5/CH7 are turned off and other channels keep on and Ch3 output voltage changes to 0.77V. When GPIO1 and GPIO2 are pulled high at same time, PMIC exist sleep mode and CH4/CH5/CH7 are turned on at same time.

In hardware sleep mode, CH3 output voltage can't be changed by I2C register. And off channels are fixed and can't be selected by SLP\_Enable\_REG(0x08) register. Only in I2C sleep mode, CH3/CH4 output voltage can be changed by SLP\_OUT3\_SET(0x06) and SLP\_OUT4\_SET(0x07) registers, off channels in sleep mode can be selected by SLP\_Enable\_REG(0x08) register.

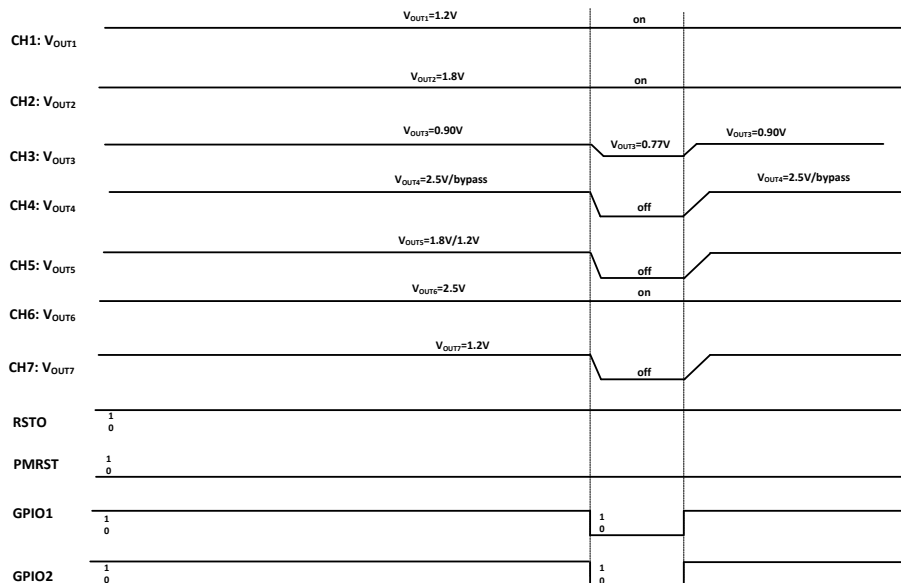


Figure 6.

## 5. Default Output Voltage selection

Ch4 output voltage selection:

CH4	Default Output Voltage(V)		Output Voltage Range(V)	DVS Step(mV)	Note
	VSEL4	V <sub>OUT4</sub>			
	0	2.5V	2.1V~3.0V	100mV	PORSEL=0/1
1	Bypass	-	-	PORSEL=0 for 3.3V application only	

In CH4 Bypass mode, the inductor should be removed to avoid the voltage drop.

Ch5 output voltage selection:

CH5	VSEL5	V <sub>OUT5</sub>
	0	1.8V
	1	1.2V

## 6. Protection Function

### 6.1. Buck and LDO Under Voltage Protection and Hard Short Protection:

All of the buck channel and LDO work in hic-cup and auto retry mode in hard short protection mode.

LDO1, LDO2 will internally counter 200us when hard short condition happens, if hard short condition lasts longer than 200us, the related channel will turn off for 3ms to avoid the thermal increase, and start again.

LDO1, LDO2 hard short condition will not affect other channels normal operation.

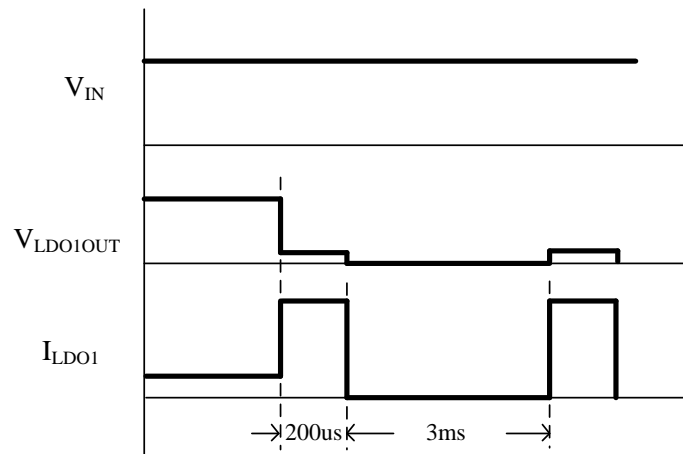


Figure 7

### 6.2. VIN Over Voltage Protection:

If input voltage exceeds the input OVP threshold, over voltage protection will be triggered and all channels will be turned off at same time. And if  $V_{in}$  falls below the threshold, it could exit protection status and all channels will start up again with pre-defined delay time.

The input OVP threshold varies with PORSEL status as above EC table.

### 6.3. Over Temperature Protection:

If the temperature of the junction exceeds 155°C, SY8600F will turn off all of the channels. And when junction temp falls below the threshold, it could exit protection status and all channels start up again with pre-defined delay time.

PMIC protection table:

	Threshold	Action
DC/DC SCP	30%	Auto-Retry
Input OVP	PORSEL=0, VIN OVP=3.85V	Whole chip turn off and recover when Vin falls below OVP threshold.
	PORSEL=1, VIN OVP=6V	
Thermal Shut Down	155 degree	Whole chip turn off and recover when Vin falls below OTP threshold.

## 7. I2C Compatible Interface

The SY8600F features an I<sup>2</sup>C interface that allows the HOST processor to control the output voltage level of all channels to achieve the DVS function. The I<sup>2</sup>C interface supports clock speeds of up to 3.4MHz and uses standard I<sup>2</sup>C commands. The SY8600F always operates as a slave device, and is addressed using a 7-bit slave address followed by an 8<sup>th</sup> bit, which indicates whether the transaction is a read-operation or a write-operation.

I2C address of the SY8600F consists of 8-bit data, and the LSB determines the read or write mode, and LSB=0 indicates Write mode and LSB=1 indicates Read mode.

SY8600F Slave address is as below table:

Binary	Hex	Read/Write
0110 0000	0x60	Write
0110 0001	0x61	Read

### START and STOP Conditions:

The SY8600F is controlled via an I2C compatible interface. The START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition. The I2C master always generates the START and STOP conditions.

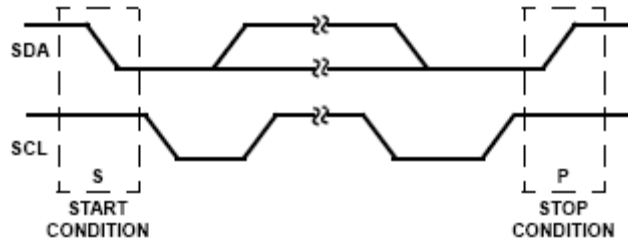


Figure 8

### Data Validity:

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

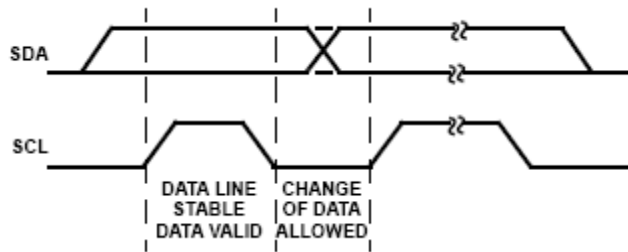


Figure 9

### Acknowledge:

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the master sends 7-slave address bits and an R/W bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.

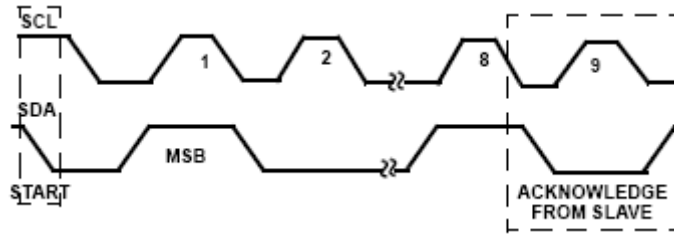


Figure 10

**Data Transactions:**

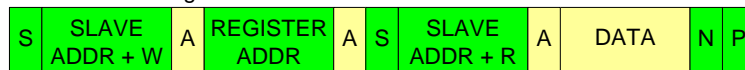
All transactions start with a control byte sent from the I2C master device. The control byte begins with a START condition, followed by 7-bits of slave address (0110000x) for the SY8600F, this address can be changed if necessary) followed by the 8<sup>th</sup>

bit, R/W bit. The R/W bit is 0 for a write or 1 for a read. If any slave devices on the I2C bus recognize their address, they will acknowledge by pulling the SDA line low for the last clock cycle in the control byte. If no slaves exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition. Once the control byte is sent, and the SY8600F acknowledges it, the 2nd byte sent by the master must be a register address byte. The register address byte tells the SY8600F which register the master will write or read. Once SY8600F receives a register address byte it responds with an acknowledge.

**Write To A Register**



**Read From A Register**



- S START      A ACKNOWLEDGE        DRIVEN BY THE MASTER
- P STOP      N NO ACKNOWLEDGE        DRIVEN BY THE SLAVE

**Register Map Summary:**

Register Address	Register name	Default Description	Default Value (HEX)	Register Description
0x01	OUT3_SET	0.90V	0x14	Voltage setting for Buck Channel3
0x02	OUT4_SET	2.5V/Bypass	0x04	Voltage setting for Buck Channel4
0x03	Enable_REG	All channels ON	0xFF	Channel Enable/Disabled
0x04	Discharge_REG	Discharge ON	0x3F	Channel Discharge Enable/Disabled
0x05	Mode_REG	Auto PWM/PFM	0x1F	Auto PWM/PFM mode or forced PWM mode control
0x06	SLP_OUT3_SET	0.77V	0x07	Sleep mode Voltage setting for Buck Channel3
0x07	SLP_OUT4_SET	2.5V	0x04	Sleep mode Voltage setting for Buck Channel4
0x08	SLP_Enable_REG	CH1/CH2/CH3 ON, other channels OFF.	0x07	Sleep mode Channel Enable/Disabled, and Sleep mode control.

## Register Settings:

### 1. Channel3 Output Voltage Setting Register (0x01)

This register set Channel3 output voltage.  $V_{OUT3\_DEFAULT}=0.90V$

Register Name	OUT3_REG			Output voltage setting register for channel 3			
Address				0x01			
Field	Bit	R/W	Default	Output voltage setting for OUT3. DVS from 0.7V to 1.1V in 10mV steps.			
VOUT3_SET	5:0	R/W	Default 0x14=0.90V	0x00=0.70V	0x01=0.71V	0x02=0.72V	0x03=0.73V
				0x04=0.74V	0x05=0.75V	0x06=0.76V	0x07=0.77V
				0x08=0.78V	0x09=0.79V	0x0A=0.80V	0x0B=0.81V
				0x0C=0.82V	0x0D=0.83V	0x0E=0.84V	0x0F=0.85V
				0x10=0.86V	0x11=0.87V	0x12=0.88V	0x13=0.89V
				0x14=0.90V	0x15=0.91V	0x16=0.92V	0x17=0.93V
				0x18=0.94V	0x19=0.95V	0x1A=0.96V	0x1B=0.97V
				0x1C=0.98V	0x1D=0.99V	0x1E=1.00V	0x1F=1.01V
				0x20=1.02V	0x21=1.03V	0x22=1.04V	0x23=1.05V
				0x24=1.06V	0x25=1.07V	0x26=1.08V	0x27=1.09V
				0x28=1.10V	0x29=1.10V	0x2A=1.10V	0x2B=1.10V
				0x2C=1.10V	0x2D=1.10V	0x2E=1.10V	0x2F=1.10V
Reserved	7:6	R/W	0	Reserved			

### 2. Channel4 Output Voltage Setting Register (0x02)

This register set Channel4 output voltage.  $V_{OUT4\_DEFAULT}=2.5V/bypass$ , CH4 default output voltage and register value table is as below:

VSEL4	$V_{OUT4}$	Register default value
0	2.5V	0x04
1	Bypass	-

Register Name	OUT4_REG			Output voltage setting register for channel 4			
Address				0x02			
Field	Bit	R/W	Default	Output voltage setting for OUT4. DVS from 2.1V to 3.0V in 100mV steps.			
VOUT4_SET	3:0	R/W	Default 0x04=2.5V	0x00=2.10V	0x01=2.20V	0x02=2.30V	0x03=2.40V
				0x04=2.50V	0x05=2.60V	0x06=2.70V	0x07=2.80V
				0x08=2.90V	0x09=3.00V	0x0A=3.00V	0x0B=3.00V
				0x0C=3.00V	0x0D=3.00V	0x0E=3.00V	0x0F=3.00V
Reserved	7:4	R/W	0	Reserved			

### 3. ON/OFF Control Register. (0x03)

Register Name	ON/OFF_Control			Channel ON/OFF Control register
Address				0x03
	Bit	R/W	Default	Description
EN1	0	R/W	1	CH1 ON/OFF control
				0: Disable
EN2/EN	1	R/W	1	CH2 and External DCDC ON/OFF control
				0: Disable
EN3	2	R/W	1	CH3 ON/OFF control
				0: Disable
EN4	3	R/W	1	CH4 ON/OFF control
				0: Disable
EN5	4	R/W	1	CH5 ON/OFF control
				0: Disable
EN6	5	R/W	1	CH6 ON/OFF control
				0: Disable
EN7	6	R/W	1	CH7 ON/OFF control
				0: Disable
Reserved	7	R/W	0	Reserved

### 4. Discharge Function Control Register. (0x04)

This register controls the output discharge function during PMIC shutdown mode. DCDC converter discharge function still works during power-off procedure at VIN off when the value is set to 1.

Register Name	Discharge Control			Channel Discharge Control
Address				0x04
	Bit	R/W	Default	Description
ENDIS_CH1	0	R/W	1	CH1 discharge control
				0: Disable
ENDIS_CH2	1	R/W	1	CH2 discharge control
				0: Disable
ENDIS_CH3	2	R/W	1	CH3 discharge control
				0: Disable
ENDIS_CH4	3	R/W	1	CH4 discharge control
				0: Disable
ENDIS_CH5	4	R/W	1	CH5 discharge control
				0: Disable
ENDIS_CH6	5	R/W	1	CH6 discharge control
				0: Disable

ENDIS_CH7	6	R/W	1	CH7 discharge control	
				0: Disable	1: Enable
Reserved	7	R/W	0	Reserved	

## 5. DCDC Mode Control Register. (0x05)

This register controls the DCDC operation mode.

This register controls Buck DC/DC Regulator PWM/PFM mode operation at light load condition. If MODE(n) bit is set to 1, CH(n) will always works in forced PWM mode. If MODE(n) bit is set to 0, CH(n) will always work in PFM mode at light load condition.

Register Name	PWM/PFM_REG			PWM/PFM mode selection Register
Address				0x05
	Bit	R/W	Default	Description
MODE1	0	R/W	1	Channel 1 mode Control bit
				0=Forced PWM
MODE3	1	R/W	1	Channel 3 mode Control bit
				0=Forced PWM
MODE4	2	R/W	1	Channel 4 mode Control bit
				0=Forced PWM
MODE5	3	R/W	1	Channel 5 mode Control bit
				0=Forced PWM
MODE7	4	R/W	1	Channel 7 mode Control bit
				0=Forced PWM
Reserved	7:5	R/W	0	Reserved

## 6. Sleep mode Channel3 Output Voltage Setting Register (0x06)

This register set Channel3 sleep mode output voltage.  $V_{OUT3\_DEFAULT}=0.77V$

Register Name	SLP_OUT3_REG			Output voltage setting register for channel 3			
Address				0x06			
Field	Bit	R/W	Default	Output voltage setting for OUT3. DVS from 0.7V to 1.1V in 10mV steps.			
SLP_VOUT3_SET	5:0	R/W	Default 0x07=0.77V	0x00=0.70V	0x01=0.71V	0x02=0.72V	0x03=0.73V
				0x04=0.74V	0x05=0.75V	0x06=0.76V	0x07=0.77V
				0x08=0.78V	0x09=0.79V	0x0A=0.80V	0x0B=0.81V
				0x0C=0.82V	0x0D=0.83V	0x0E=0.84V	0x0F=0.85V
				0x10=0.86V	0x11=0.87V	0x12=0.88V	0x13=0.89V
				0x14=0.90V	0x15=0.91V	0x16=0.92V	0x17=0.93V
				0x18=0.94V	0x19=0.95V	0x1A=0.96V	0x1B=0.97V
				0x1C=0.98V	0x1D=0.99V	0x1E=1.00V	0x1F=1.01V

				0x20=1.02V	0x21=1.03V	0x22=1.04V	0x23=1.05V
				0x24=1.06V	0x25=1.07V	0x26=1.08V	0x27=1.09V
				0x28=1.10V	0x29=1.10V	0x2A=1.10V	0x2B=1.10V
				0x2C=1.10V	0x2D=1.10V	0x2E=1.10V	0x2F=1.10V
Reserved	7:6	R/W	0	Reserved			

## 7. Sleep mode Channel4 Output Voltage Setting Register (0x07)

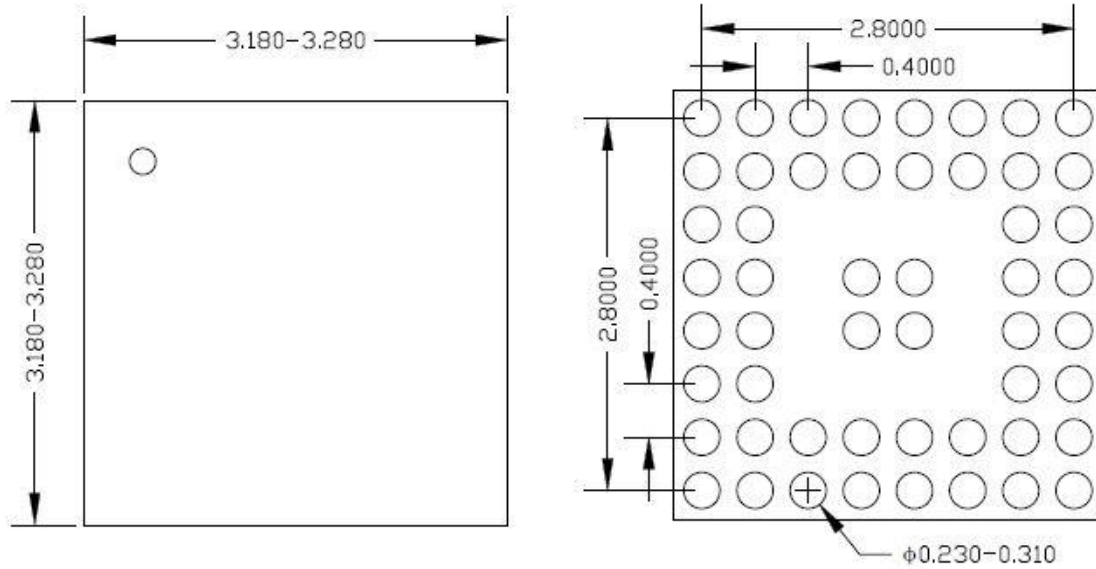
This register set Channel4 output voltage.  $V_{OUT4\_DEFAULT}=2.5V/bypass$ , CH4 default output voltage and register value table is as below:

Register Name	SLP_OUT4_REG			Output voltage setting register for channel 4			
Address				0x07			
Field	Bit	R/W	Default	Output voltage setting for OUT4. DVS from 2.1V to 3.0V in 100mV steps.			
SLP_VOUT4_SET	3:0	R/W	Default 0x04=2.5V	0x00=2.10V	0x01=2.20V	0x02=2.30V	0x03=2.40V
				0x04=2.50V	0x05=2.60V	0x06=2.70V	0x07=2.80V
				0x08=2.90V	0x09=3.00V	0x0A=3.00V	0x0B=3.00V
				0x0C=3.00V	0x0D=3.00V	0x0E=3.00V	0x0F=3.00V
Reserved	7:4	R/W	0	Reserved			

## 8. Sleep mode ON/OFF Control Register. (0x08)

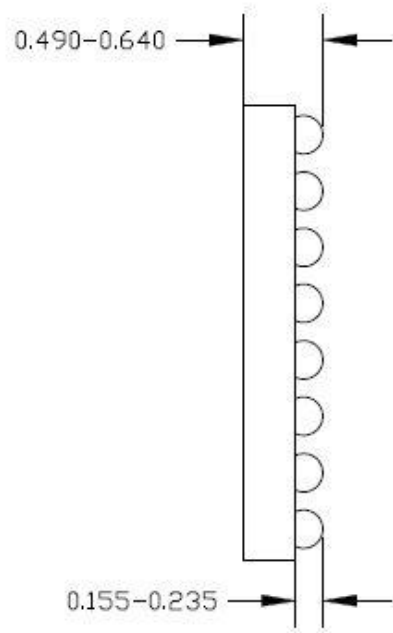
Register Name	SLP_ON/OFF_Control			Channel sleep mode ON/OFF Control register			
Address				0x08			
	Bit	R/W	Default	Description			
SLP_EN1	0	R/W	1	Sleep mode CH1 ON/OFF control			
				0: Disable		1: Enable	
SLP_EN2	1	R/W	1	Sleep mode CH2 ON/OFF control			
				0: Disable		1: Enable	
SLP_EN3	2	R/W	1	Sleep mode CH3 ON/OFF control			
				0: Disable		1: Enable	
SLP_EN4	3	R/W	0	Sleep mode CH4 ON/OFF control			
				0: Disable		1: Enable	
SLP_EN5	4	R/W	0	Sleep mode CH5 ON/OFF control			
				0: Disable		1: Enable	
SLP_EN6	5	R/W	0	Sleep mode CH6 ON/OFF control			
				0: Disable		1: Enable	
SLP_EN7	6	R/W	0	Sleep mode CH7 ON/OFF control			
				0: Disable		1: Enable	
SLEEP	7	R/W	0	Sleep mode control bit			
				0: PMIC exist sleep mode		1: PMIC enter sleep mode	

**CSP3.23×3.23-52 Package Outline Drawing**



**Top view**

**Bottom view**



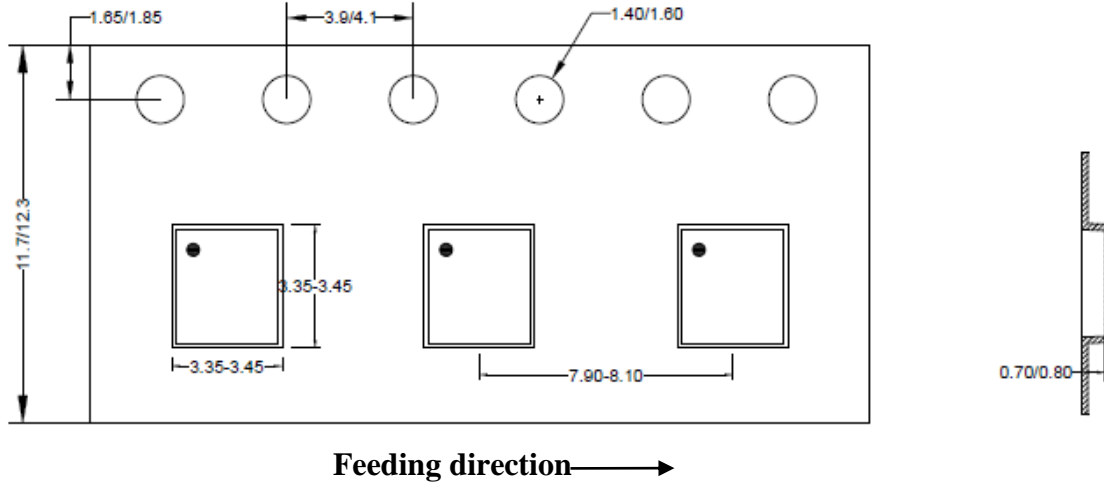
**Side View**

**Notes: All dimension in millimeter and exclude mold flash & metal burr.**

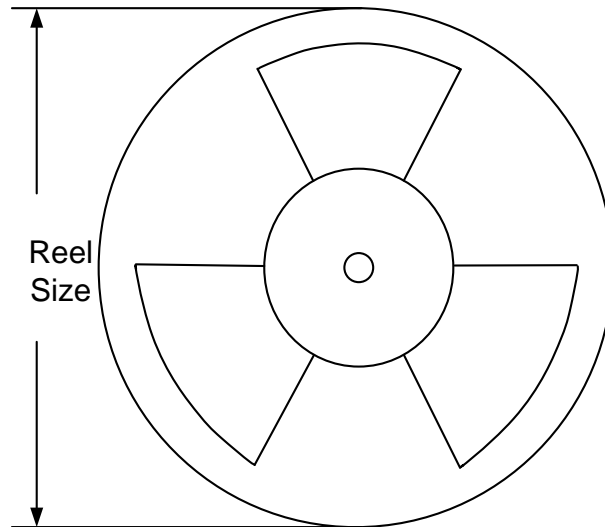
## Taping & Reel Specification

### 1. Taping orientation

CSP3.23×3.23



### 2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
CSP3.23×3.23	12	8	13"	400	400	5000

### 3. Others: NA



**Revision History**

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

<b>Date</b>	<b>Revision</b>	<b>Change</b>	<b>Pages Changed</b>
Aug.18, 2022	Revision 0.9	Initial risk production release.	-
Feb.13, 2023	Revision 0.9A	Modify the typo.	-
Mar.12, 2025	Revision 1.0	Initial production release.	-

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