SY70202K

High Efficiency and High Integration PMIC for SSD System

General Description

The SY70202K is an integrated power management unit. It is designed to power a wide range of microcontrollers and solid-state drive applications. The SY70202K includes 4 buck converters with integrated power FETs and 2 low-dropout regulators (LDOs). The Buck1, LDO1, and LDO2 can also be configured as load switch. The PMIC supports a variety of default configurations. It is programmed at the factory with a default configuration.

The SY70202K supports combination of multiple configurations, including output voltage, startup time, system level sequencing, sleep modes, deep sleep modes, and operating modes etc. Each of the regulators can be configured for a wide range of output voltages through the I^2C interface. Each buck converter requires only three small components to operate at switching frequency of 2MHz. All regulators can be configured for a wide range of output voltages through the I^2C interface.

The SY70202K is available in a BGA3.35×3.1-34 package.

Key Features

- Wide Input Voltage Range
  - V_{IN} = 2.8V to 3.7V
- Channel 1 Synchronous Buck:
  - 4A Maximum Output Current Capability
  - 1.6V to 3.0V Programmable, 25mV Step
  - Bypass Mode or Buck Mode Selection
  - 40mΩ/40mΩ R_{DS_ON}
- Channel 2 Synchronous Buck:
  - 3A Maximum Output Current Capability
  - 0.75V to 1.85V Programmable, 10mV Step
  - 80mΩ/50mΩ R_{DS_ON}
- Channel 3 Synchronous Buck:
  - 4A Maximum Output Current Capability
  - 0.5V to 1.2V Programmable, 10mV Step
  - 50mΩ/20mΩ R_{DS_ON}
- Channel 4 Synchronous Buck:
  - 2A Maximum Output Current Capability
  - 0.807V to 1.907V Programmable, 50mV Step
  - 80mΩ/50mΩ R_{DS_ON}
- Channel 5 LDO1:
  - 0.4A Maximum Output Current Capability
  - 1.0V to 2.7V Programmable, 50mV Step
  - Bypass Mode or LDO Mode Selection
- Channel 6 LDO2:
  - 0.4A Maximum Output Current Capability
  - 1.0V to 2.7V Programmable, 50mV Step
  - Bypass Mode or LDO Mode Selection
- I^2C Interface up to 3.4MHz
- Auto PWM/PFM or Forced PWM Controlled by I^2C Interface
- Output Voltage Level of Each Channel Controlled by I^2C Interface
- Reliable Protections:
  - Input/Output Over Voltage Protection (OVP)
  - Short Circuit Protection (SCP)
  - Over Temperature Protection (OTP)
- Compact Package: BGA3.35×3.1-34
- MSL Rating: MSL3

Applications

- Solid State Drives
- Microcontroller

Simplify Application Circuit

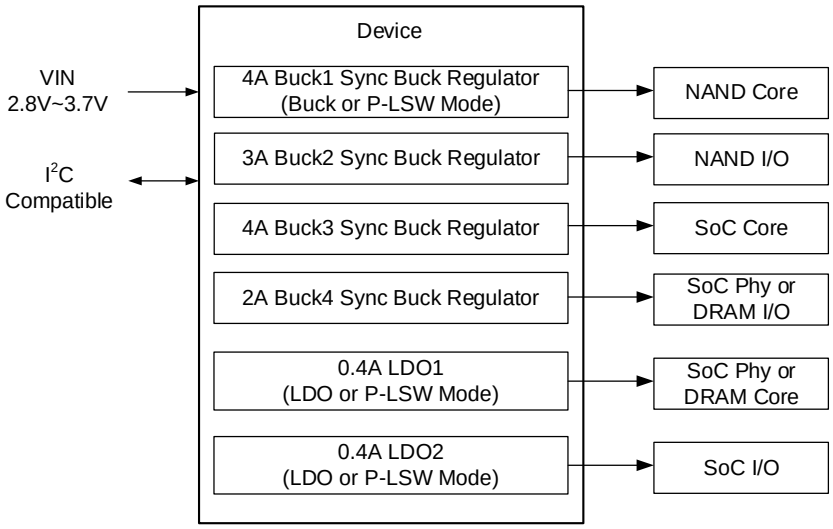


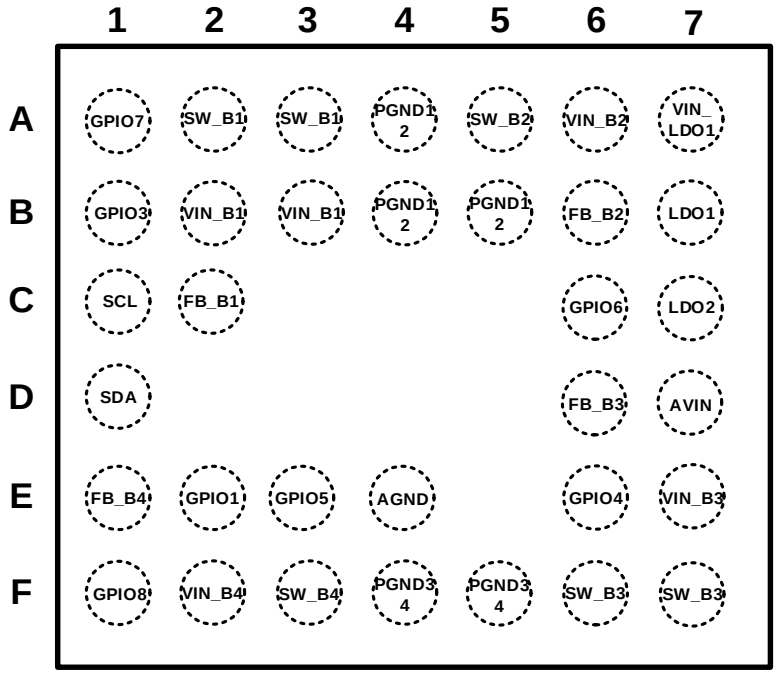
Figure 1. Simplified Application Circuit

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY70202KNSG	BGA3.35×3.1-34 RoHS-Compliant and Halogen-Free	**KPCxyz**

x = year code, y = week code, z = lot number code

Pin-out (top view)



(BGA3.35×3.1-34)

Pin Descriptions

Pin Number	Pin Name	Pin Description
A2, A3	SW_B1	Switch Pin for Buck 1 Regulator.
A4, B4, B5	PGND12	Dedicated Power Ground for Buck1 and Buck2 Regulator.
A5	SW_B2	Switch Pin for Buck 2 Regulator.
A6	VIN_B2	Dedicated VIN power input for Buck 2 Regulator.
A7	VIN_LDO1	Dedicated VIN power input for LDO Regulator.
B2, B3	VIN_B1	Dedicated VIN power input for Buck 1 Regulator.
B6	FB_B2	Feedback for Buck 2 Regulator. Connect to the Buck 2 output capacitor.
B7	LDO1	Output for LDO1 Regulator (Leave unconnected if LDO is not used and disabled).
B1	GPIO3	General purpose input pin.
A1	GPIO7	Configurable general purpose input/open drain output.
C2	FB_B1	Feedback for Buck 1 Regulator. Connect to the Buck 1 output capacitor.
E4	AGND	Analog Ground. Kelvin connects to the other ground pins on the IC.
C6	GPIO6	General purpose input pin.
C7	LDO2	Output for LDO2 Regulator (Leave unconnected if LDO is not used and disabled).
C1	SCL	I^2C Clock Input.
D1	SDA	I^2C Data Input and Output.
E3	GPIO5	Configurable general purpose input/open drain output.
D6	FB_B3	Feedback for Buck 3 Regulator. Connect to the Buck 3 output capacitor.
D7	AVIN	Analog Input supply. This is also the pin that is monitored for VIN OVP.
E1	FB_B4	Feedback for Buck 4 Regulator. Connect to the Buck 4 output capacitor.
F1	GPIO8	General purpose input pin.
E2	GPIO1	General purpose input pin.
F4, F5	PGND34	Dedicated Power Ground for Buck3 and Buck4 Regulators
E6	GPIO4	General purpose input pin.
E7	VIN_B3	Dedicated VIN power input for Buck 3 Regulator.
F2	VIN_B4	Dedicated VIN power input for Buck 4 Regulator.
F3	SW_B4	Switch Pin for Buck 4 Regulator.
F6, F7	SW_B3	Switch Pin for Buck 3 Regulator.

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
All Pins to GND	-0.3	6	V
Junction Temperature		150	°C
Lead Temperature (Soldering, 10 sec.)		260	
Storage Temperature Range	-55	150	
ESD Susceptibility			
HBM (Human Body Model)	±2000		V
CDM (Charge Device Model) All Pins	±500		
Latch-up	±200		mA

Thermal Information

Parameter (Note 2) (Note 3)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	35	°C/W
θ_{JC_TOP} Junction-to-Case (Top) Thermal Resistance	11	
θ_{JB} Junction-to-Board Thermal Resistance	18.5	
P_D Power Dissipation @ T_A = 25°C	3.6	W

Recommended Operating Conditions

Parameter (Note 4)	Min	Max	Unit
Supply Input Voltage, VIN	2.8	3.7	V
Ambient Temperature	-40	85	°C
Junction Temperature	-40	125	°C

Block Diagram

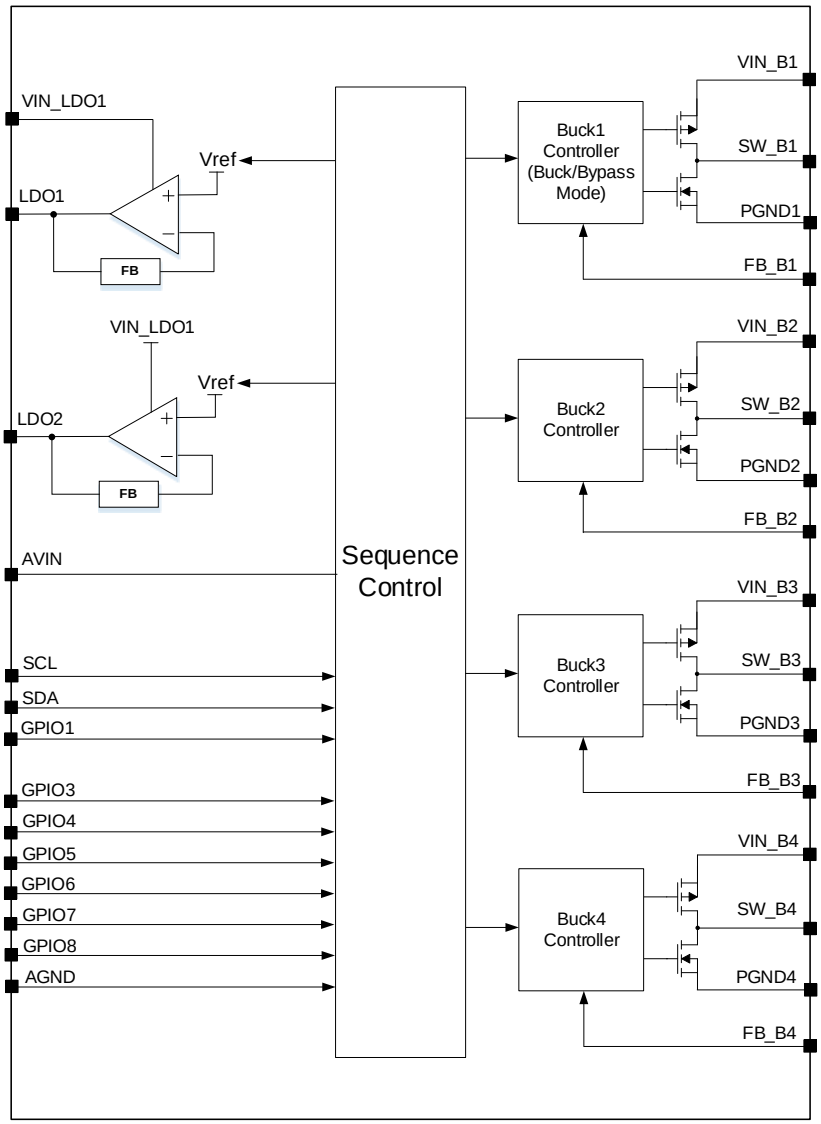


Figure 2. Function Block Diagram

Power On/Off Sequence

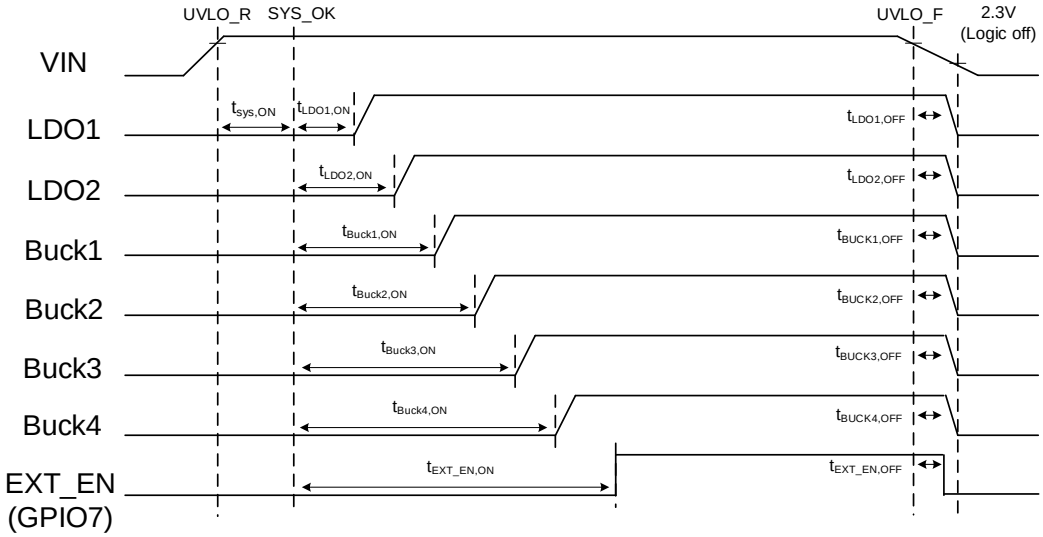


Figure 3. Power On/Off Sequence

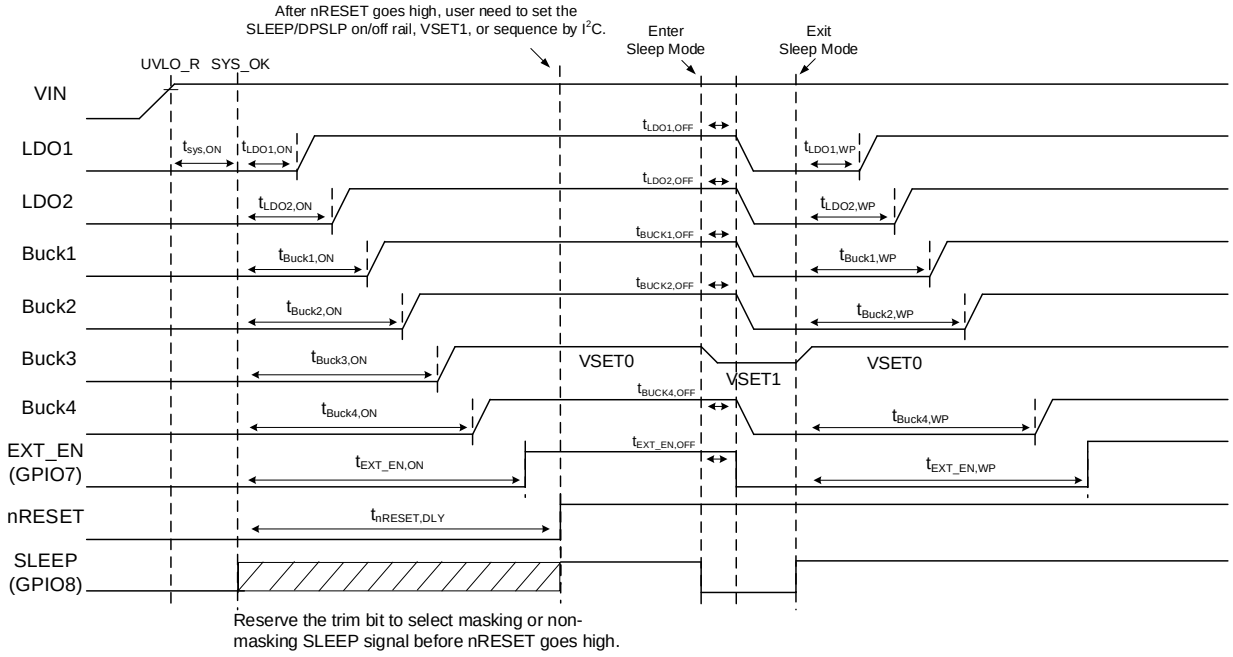
- Power-on delay time:

  $t_{LDO1,ON}$/ $t_{LDO2,ON}$/ $t_{Buck1,ON}$/ $t_{Buck2,ON}$/ $t_{Buck3,ON}$/$t_{Buck4,ON}$/$t_{EXT\_EN,ON}$ =0~7.5ms, 0.5ms/step.

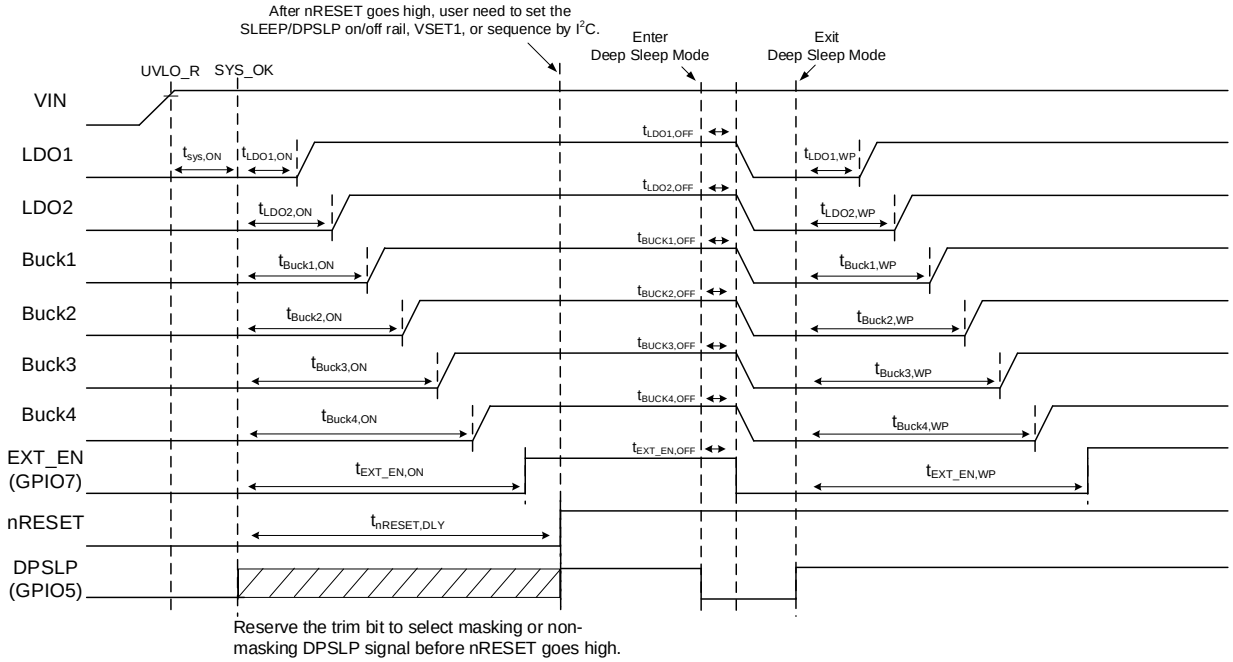
- Power-off delay time:

  $t_{LDO1,OFF}$/ $t_{LDO2,OFF}$/ $t_{Buck1,OFF}$/ $t_{Buck2,OFF}$/ $t_{Buck3,OFF}$/$t_{Buck4,OFF}$/$t_{EXT\_EN,OFF}$ =0ms, 0.25ms, 0.5ms, or 1ms.

SLEEP and DPSLE Sequence



(a)



(b)

Figure 4. Power On/Off Sequence
(a) Enter/Exist Sleep Mode and (b) Enter/Exist Deep Sleep Mode

- Wake up delay time:
  $t_{LDO1,WP}$/ $t_{LDO2,WP}$/ $t_{Buck1,WP}$/ $t_{Buck2,WP}$/ $t_{Buck3,WP}$/$t_{Buck4,WP}$/$t_{EXT\_EN,WP}$ =0~3ms, 1ms/step.

Electrical Characteristics

(V_{IN}=3.3V, T_A = 25°C, unless otherwise specified. (Note 5))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Digital I/O	GPIOs Output Low (Open drain)	V_{OL}	I_{OL}=1mA	-	-	0.35	V
	GPIOs Input Low (GPIO3/4)	V_{IO_Low}		-	-	0.35	V
	GPIOs Input Low (GPIO5/6/7/8)	V_{IO_Low}		-	-	0.55	V
	GPIOs Input High (GPIO3/4/5/6/7/8)	V_{IO_High}		1.2	-	-	V
System Control	Supply Input Voltage	V_{IN}		2.8	-	3.7	V
	UVLO Threshold Rising	$V_{UVLO,RISING}$		2.5	2.6	2.7	V
	UVLO Hysteresis	$V_{UVLO,HYS}$	(Note 6)	-	200	-	mV
	Operating Supply Current		All Regulators Disabled (Note 6)	-	20	-	μA
	Operating Supply Current		All Regulators Enabled but no load (Note 6)	-	120	-	μA
	VIN OV Shutdown Threshold Rising	$V_{IN\_OVP\_R}$	(Note 6)	-	3.9	-	V
	VIN OV Shutdown Threshold Falling	$V_{IN\_OVP\_F}$	(Note 6)	-	3.6	-	V
	VIN OVP Deglitch Time		(Note 6)		5		μs
	Thermal Shutdown	$T_{OTP,RISING}$	Temperature rising (Note 6)	-	155	-	°C
	Thermal Shutdown Hysteresis	$T_{OTP,HYS}$	(Note 6)	-	15	-	°C
	Startup Delay after initial AVIN	$t_{SYS,ON}$		-	1	1.5	ms
	OV/UV Retry Time		Channel off time (Note 6)	-	10	-	ms
nIRQ (SYSWARN)	System Warning (SYSWARN) - Falling Threshold	$V_{SYSWARN}$	(Note 6)	-	2.9	-	V
	System Warning (SYSWARN) Accuracy	$V_{SYSWARN,ACC}$		-3.5	-	3.5	%
	System Monitor (SYSWARN) Hysteresis	$V_{SYSWARN,HYS}$	(Note 6)	-	50	-	mV
BUCK1	Output Voltage Range	V_{OUT1}	Controllable by I^2C interface 25mV steps.	1.6	-	3.0	V
	Output Voltage Accuracy	ΔV_{OUT1_PWM}	PWM mode operation @ T_A=25°C, V_{OUT}=Default	-1	-	1	%
			PWM mode operation @ T_j=-40°C to 125°C , V_{OUT}=Default	-2	-	2	%
		ΔV_{OUT1_PFM}	PFM mode operation, I_{OUT}=1mA @ T_j=-40°C to 125°C , V_{OUT}=Default	-2.0	-	2.5	%
	Supply Current, Standby	I_{VIN_B1}	Regulator Only, No Load (Note 6)	-	22	-	μA
			Regulator Only, No Load @ Sleep(GPIO8)=Low (Note 6)	-	10	-	μA
			Regulator Disable	-	0.1	1	μA
	Switching Frequency	F_{OSC1}	(Note 6)	-	2	-	MHz
	Main PFET R_{DS_ON}	$R_{DS\_ON,P1}$	(Note 6)	-	40	-	mΩ

	Main NFET R_{DS_ON}	$R_{DS\_ON,N1}$	(Note 6)	-	40	-	mΩ
	High Side FET Current Limit	I_{LIM1_HS}		5.6	-	-	A
	Maximum Output DC Load Current	I_{OUT1}		4	-	-	A
	Internal Soft-Start Time	T_{SS1}	B1_SST=0. 10% to 90% of V_{NOM} (Note 6)	-	250	-	μs
			B1_SST=1. 10% to 90% of V_{NOM} (Note 6)	-	500	-	μs
	Discharge Resistor	R_{DIS1}		-	4.4	8.75	Ω
	OVP Threshold	V_{OVP1}		115	120	125	%
	OVP Hysteresis	$V_{OVP1,HYS}$	(Note 6)	-	5	-	%
	OVP Deglitch Time	t_{OVP1}	(Note 6)	-	10	-	μs
	Short Circuit Protection Threshold	V_{SCP1}	(Note 6)	-	30	-	%
	Short Circuit Protection Deglitch Time	t_{SCP1}	(Note 6)	-	50	-	μs
BUCK1 @ BYPASS MODE	Output Voltage Range	V_{OUT}		2.8	3.3	3.7	V
	Main PFET R_{ON}	$R_{DS\_ON,P1}$	(Note 6)	-	40	-	mΩ
	Load Switch Current Limit	I_{LIM1_HS}	Shut down after deglitch time and stays off for off-time	3.1	4.5	5.8	A
	Load Switch Current Shutdown Deglitch Time	t_{LIM1_HS}	(Note 6)	-	200	-	μs
	Load Switch Current Shutdown Off-Time		(Note 6)	-	10	-	ms
	Internal Soft-Start Time	T_{SS1}	B1_SST=0. 10% to 90% of V_{NOM} (Note 6)	-	250	-	μs
			B1_SST=1. 10% to 90% of V_{NOM} (Note 6)	-	500	-	μs
	Short Circuit Protection Threshold	V_{SCP1}	(Note 6)	-	80	-	$\%V_{IN}$
	Short Circuit Protection Deglitch Time	t_{SCP1}	(Note 6)	-	50	-	μs
BUCK2	Output Voltage Range	V_{OUT2}	Controllable by I^2C interface 10mV steps.	0.75	-	1.85	V
	Output Voltage Accuracy	ΔV_{OUT2_PWM}	PWM mode operation @ T_A=25°C , V_{OUT}=Default	-1	-	1	%
			PWM mode operation @ T_j=-40°C to 125°C , V_{OUT}=Default	-2	-	2	%
		ΔV_{OUT2_PFM}	PFM mode operation, I_{OUT}=1mA @ T_j=-40°C to 125°C , V_{OUT}=Default	-2.0	-	2.5	%
	Supply Current, Standby	I_{VIN_B2}	Regulator Only, No Load (Note 6)	-	22	-	μA
			Regulator Only, No Load @ Sleep(GPIO8)=Low (Note 6)	-	10	-	μA
			Regulator Disable	-	0.1	1	μA
	Switching Frequency	F_{OSC2}	(Note 6)	-	2	-	MHz
	Main PFET R_{DS_ON}	$R_{DS\_ON,P2}$	(Note 6)	-	80	-	mΩ
	Main NFET R_{DS_ON}	$R_{DS\_ON,N2}$	(Note 6)	-	50	-	mΩ

	High Side FET Current Limit	I_{LIM2_HS}		4.4	-	-	A
	Maximum Output DC Load Current	I_{OUT2}		3	-	-	A
	Internal Soft-Start Time	T_{SS2}	B2_SST=0. 10% to 90% of V_{NOM} (Note 6)	-	250	-	µs
			B2_SST=1. 10% to 90% of V_{NOM} (Note 6)	-	500	-	µs
	Discharge Resistor	R_{DIS2}		-	9.4	20	Ω
	OVP Threshold	V_{OVP2}		115	120	125	%
	OVP Hysteresis	$V_{OVP2,HYS}$	(Note 6)	-	5	-	%
	OVP Deglitch Time	t_{OVP2}	(Note 6)	-	10	-	µs
	Short Circuit Protection Threshold	V_{SCP2}	(Note 6)	-	30	-	%
	Short Circuit Protection Deglitch Time	t_{SCP2}	(Note 6)	-	50	-	µs
BUCK3	Output Voltage Range	V_{OUT3}	Controllable by I^2C interface 10mV steps.	0.5	-	1.2	V
	Output Voltage Accuracy	ΔV_{OUT3_PWM}	PWM mode operation @ T_A=25°C , V_{OUT}=Default	-1	-	1	%
			PWM mode operation @ T_j=-40°C to 125°C , V_{OUT}=Default	-2	-	2	%
		ΔV_{OUT3_PFM}	PFM mode operation, I_{OUT}=1mA @ T_j=-40°C to 125°C , V_{OUT}=Default	-2.0	-	2.5	%
	Supply Current, Standby	I_{VIN_B3}	Regulator Only, No Load (Note 6)	-	22	-	µA
			Regulator Only, No Load @ Sleep(GPIO8)=Low (Note 6)	-	10	-	µA
			Regulator Disable	-	0.1	1	µA
	Switching Frequency	F_{OSC3}	(Note 6)	-	2	-	MHz
	Main PFET R_{DS_ON}	$R_{DS\_ON,P3}$	(Note 6)	-	50	-	mΩ
	Main NFET R_{DS_ON}	$R_{DS\_ON,N3}$	(Note 6)	-	20	-	mΩ
	High Side FET Current Limit	I_{LIM3_HS}		5.6	-	-	A
	Maximum Output DC Load Current	I_{OUT3}		4	-	-	A
	Internal Soft-Start Time	T_{SS3}	B3_SST=0. 10% to 90% of V_{NOM} (Note 6)	-	250	-	µs
			B3_SST=1. 10% to 90% of V_{NOM} (Note 6)	-	500	-	µs
	Discharge Resistor	R_{DIS3}			9.4	20	Ω
	OVP Threshold	V_{OVP3}		115	120	125	%
	OVP Hysteresis	$V_{OVP3,HYS}$	(Note 6)	-	5	-	%
	OVP Deglitch Time	t_{OVP3}	(Note 6)	-	10	-	µs
	Short Circuit Protection Threshold	V_{SCP3}	(Note 6)	-	30	-	%

	Short Circuit Protection Deglitch Time	t_{SCP3}	(Note 6)	-	50	-	µs
BUCK4	Output Voltage Range	V_{OUT4}	Controllable by I²C interface 50mV steps.	0.807	-	1.907	V
	Output Voltage Accuracy	ΔV_{OUT4_PWM}	PWM mode operation @ T_A=25°C , V_{OUT}=Default	-1	-	1	%
			PWM mode operation @ T_j=-40°C to 125°C , V_{OUT}=Default	-2	-	2	%
		ΔV_{OUT4_PFM}	PFM mode operation, I_{OUT}=1mA @ T_j=-40°C to 125°C , V_{OUT}=Default	-2.0	-	2.5	%
	Supply Current, Standby	I_{VIN_B4}	Regulator Only, No Load (Note 6)	-	22	-	µA
			Regulator Only, No Load @ Sleep(GPIO8)=Low (Note 6)	-	10	-	µA
			Regulator Disable	-	0.1	1	µA
	Switching Frequency	F_{OSC4}	(Note 6)	-	2	-	MHz
	Main PFET R_{DS_ON}	$R_{DS\_ON,P4}$	(Note 6)	-	80	-	mΩ
	Main NFET R_{DS_ON}	$R_{DS\_ON,N4}$	(Note 6)	-	50	-	mΩ
	High Side FET Current Limit	I_{LIM4_HS}		3.6	-	-	A
	Maximum Output DC Load Current	I_{OUT4}		2	-	-	A
	Internal Soft-start Time	T_{SS4}	B4_SST=0.10% to 100% of V_{NOM} (Note 6)	-	150	-	µs
	Discharge Resistor	R_{DIS4}		-	9.4	20	Ω
	OVP Threshold	V_{OVP4}		115	120	125	%
	OVP Hysteresis	$V_{OVP4,HYS}$	(Note 6)	-	5	-	%
	OVP Deglitch Time	t_{OVP4}	(Note 6)	-	10	-	µs
	Short Circuit Protection Threshold	V_{SCP4}	(Note 6)	-	30	-	%
	Short Circuit Protection Deglitch Time	t_{SCP4}	(Note 6)	-	50	-	µs
LDO1	LDO1 Input Voltage Range	V_{IN_LDO1}	LDO Mode	2.8	-	3.7	V
	LDO1 Output Voltage Range	V_{OUT_LDO1}	Controllable by I²C interface, 50mV steps.	1.0	-	2.7	V
	Output Current	I_{OUT_LDO1}	V_{IN_LDO1}=2.8V to 3.7V,	0.4	-	-	A
	Output Voltage Accuracy	ΔV_{OUT_LDO1}	T_A=25°C, V_{OUT}=Default V_{IN_LDO}-V_{OUT_LDO1} > 0.4V	-1	-	1	%
			T_j=-40°C to 125°C, V_{OUT}=Default V_{IN_LDO}-V_{OUT_LDO1} > 0.4V	-2	-	2	%
	Supply Current	I_{VIN_LDO1}	Regulator Enable, No Load (Note 6)	-	10	-	µA
			Regulator Disable	-	0	1	µA
	Internal Soft-Start Time	T_{SS_LDO1}	LDO1_SST=0. 10% to 90% of V_{NOM} (Note 6)	-	200	-	µs
			LDO1_SST=1. 10% to 90% of V_{NOM} (Note 6)	-	360	-	µs
	OVP Threshold	V_{OVP_LDO1}	(Note 6)	-	115	-	%

	OVP Hysteresis	$V_{OVP\_LDO1,HYS}$	(Note 6)	-	5	-	%
	OVP Deglitch Time	t_{OVP_LDO1}	(Note 6)	-	10	-	
	Dropout Voltage	V_{DV_LDO1}	I_{LDO1} = 400mA, V_{IN_LDO1} > 2.8V,	-	-	400	mV
	Discharge Resistor	R_{DIS_LDO1}		-	20	35	Ω
	Current Limit	I_{LIM_LDO1}		400	500	600	mA
	Current Shutdown Deglitch Time	t_{LIM_LDO1}	(Note 6)	-	200	-	μs
	Short Circuit Protection Threshold	V_{SCP_LDO1}	(Note 6)	-	60	-	%
	Short Circuit Protection Deglitch Time	t_{SCP_LDO1}	(Note 6)	-	50	-	μs
LDO1 @ Load Switch	LDO1 Input Voltage Range	V_{IN_LDO1}	PLSW Mode	2.8	-	3.7	V
	Main FET R_{DS_ON}	$R_{DS\_ON,P,LDO1}$	PLSW Mode, V_{IN_LDO1}=3.3V, I_{LDO1}=100mA	-	300	500	mΩ
	Supply Current	I_{VIN_LDO1}	PLSW Mode, (Note 6)	-	12	-	μA
			Load Switch Disabled	-	0	1	μA
	Internal Soft-Start Time	T_{SS_LDO1}	10% to 90% of V_{NOM} (Note 6)	-	200	-	μs
	Load Switch Current Limit	I_{LIM_HS}	PLSW Mode	400	500	600	mA
	Load Switch Current Shutdown Deglitch Time	t_{LIM_HS}	(Note 6)	-	200	-	μs
	Load Switch Current Shutdown Off-Time		(Note 6)	-	10	-	ms
	Short Circuit Protection Threshold	$V_{SCP,LDO1}$	(Note 6)	-	60	-	%
	Short Circuit Protection Deglitch Time	$t_{SCP,LDO1}$	(Note 6)	-	50	-	μs
LDO2	LDO2 Input Voltage Range	V_{IN_LDO1}	LDO Mode	2.8	-	3.7	V
	LDO2 Output Voltage Range	V_{OUT_LDO2}	Controllable by I^2C interface, 50mV steps.	1.0	-	2.7	V
	Output Current	I_{OUT_LDO2}	V_{IN_LDO1}=2.8V to 3.7V,	0.4	-	-	A
	Output Voltage Accuracy	ΔV_{OUT_LDO2}	T_A=25°C, V_{OUT}=Default V_{IN_LDO1}-V_{OUT_LDO2} > 0.4V	-1	-	1	%
			T_j=-40°C to 125°C, V_{OUT}=Default V_{IN_LDO1}-V_{OUT_LDO2} > 0.4V	-2	-	2	%
	Supply Current	I_{VIN_LDO2}	Regulator Enable, No Load (Note 6)	-	10	-	μA
			Regulator Disable	-	0	1	μA
	Internal Soft-Start Time	T_{SS_LDO2}	LDO2_SST=0. 10% to 90% of V_{NOM} (Note 6)	-	200	-	μs
			LDO2_SST=1. 10% to 90% of V_{NOM} (Note 6)	-	360	-	μs
	OVP Threshold	V_{OVP_LDO2}	(Note 6)	-	115	-	%
	OVP Hysteresis	$V_{OVP\_LDO2,HYS}$	(Note 6)	-	5	-	%
	OVP Deglitch Time	t_{OVP_LDO2}	(Note 6)	-	10	-	μs

	Dropout Voltage	V_{DV_LDO2}	I_{LDO2} = 400mA, V_{IN_LDO1} > 2.8V	-	-	400	mV
	Discharge Resistor	R_{DIS_LDO2}		-	20	35	Ω
	Current Limit	I_{LIM_LDO2}		400	500	600	mA
	Current Shutdown Deglitch Time	t_{LIM_LDO2}	(Note 6)	-	200	-	μs
	Short Circuit Protection Threshold	V_{SCP_LDO2}	(Note 6)	-	60	-	%
	Short Circuit Protection Deglitch Time	t_{SCP_LDO2}	(Note 6)	-	50	-	μs
LDO2@ Load Switch	LDO2 Input Voltage Range	V_{IN_LDO1}	PLSW Mode	2.8	-	3.7	V
	Main FET R_{DS_ON}	$R_{DS\_ON,P,LDO2}$	PLSW Mode, V_{IN_LDO1}=3.3V, I_{LDO2}=100mA (Note 6)	-	300	-	mΩ
	Supply Current	I_{VIN_LDO2}	PLSW Mode, (Note 6)	-	12	-	μA
			Load Switch Disabled	-	0	1	μA
	Internal Soft-Start Time	T_{SS_LDO2}	10% to 90% of V_{NOM} (Note 6)	-	200	-	μs
	Load Switch Current Limit	I_{LIM_HS}		400	500	600	mA
	Load Switch Current Shutdown Deglitch Time	t_{LIM_HS}	(Note 6)	-	200	-	μs
	Load Switch Current Shutdown Off-Time		(Note 6)	-	10	-	ms
	Short Circuit Protection Threshold	$V_{SCP,LDO2}$	(Note 6)	-	60	-	%
	Short Circuit Protection Deglitch Time	$t_{SCP,LDO2}$	(Note 6)	-	50	-	μs

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective 4-layer thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

Note 3: θ_{JB} is measured in the natural convection at T_A = 25°C on a high effective 4-layer thermal conductivity board near the pin1 of the package (less than 1mm away from the edge of the package).

Note 4: The device is not guaranteed to function outside its operating conditions.

Note 5: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

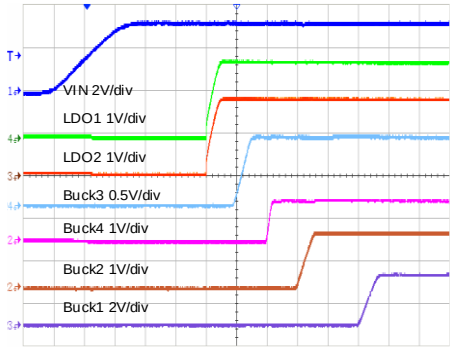
Note 6: Guaranteed by design or statistical correlation and not production tested.

Typical Performance Characteristics

(T_A=25°C)

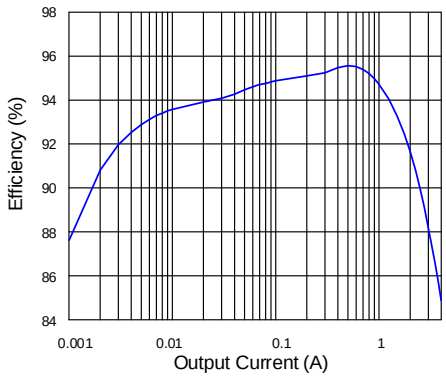
Power On Sequence

(V_{IN}=3.3V, V_{OUT1}=2.5V, V_{OUT2}=1.2V, V_{OUT3}=0.75V, V_{OUT4}=0.9V, V_{LDO1}=1.8V, V_{LDO2}=1.8V)



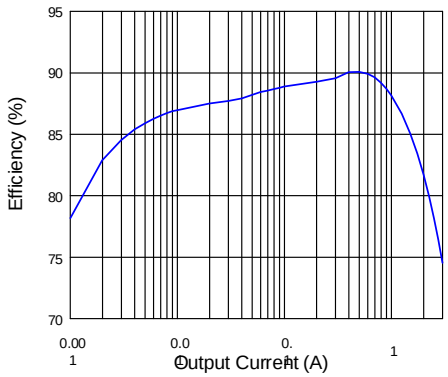
Efficiency vs Output Current

(V_{IN}=3.3V, V_{Buck1}=2.5V, L=0.47μH/DFE252012F-R47M=P2)



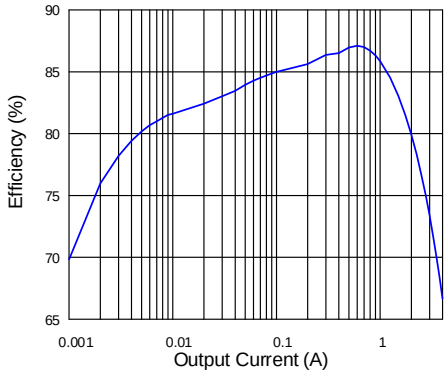
Efficiency vs Output Current

(V_{IN}=3.3V, V_{Buck2}=1.2V, L=0.47μH/DFE252012F-R47M=P2)



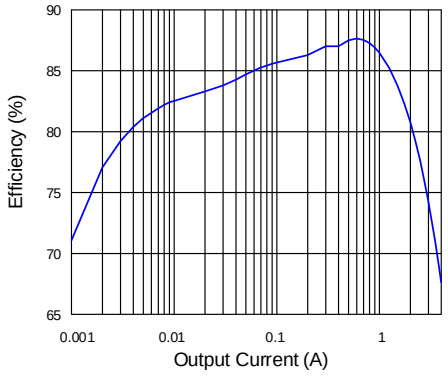
Efficiency vs Output Current

(V_{IN}=3.3V, V_{Buck3}=0.75V, L=0.47μH/DFE252012F-R47M=P2)



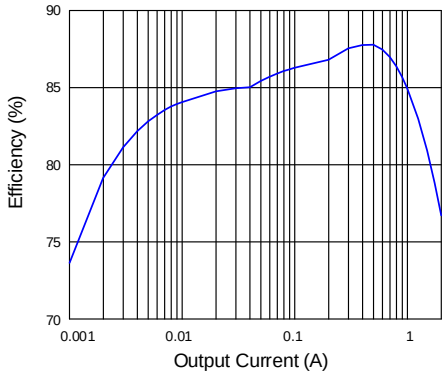
Efficiency vs Output Current

(V_{IN}=3.3V, V_{Buck3}=0.8V, L=0.47μH/DFE252012F-R47M=P2)



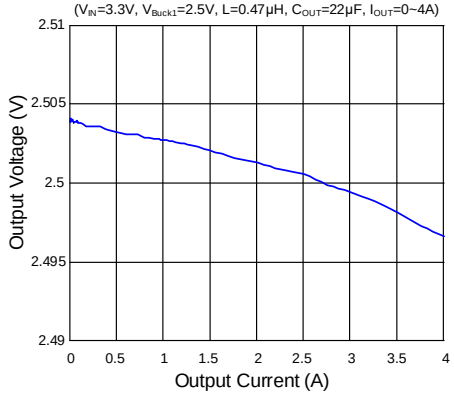
Efficiency vs Output Current

(V_{IN}=3.3V, V_{Buck4}=0.9V, L=0.47μH/DFE252012F-R47M=P2)



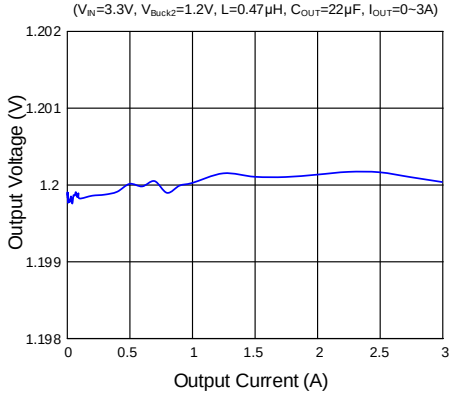
Output Voltage vs Load Current

(V_{IN}=3.3V, V_{Buck1}=2.5V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0~4A)



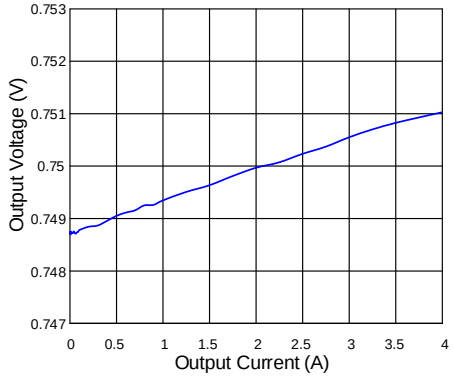
Output Voltage vs Load Current

(V_{IN}=3.3V, V_{Buck2}=1.2V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0~3A)



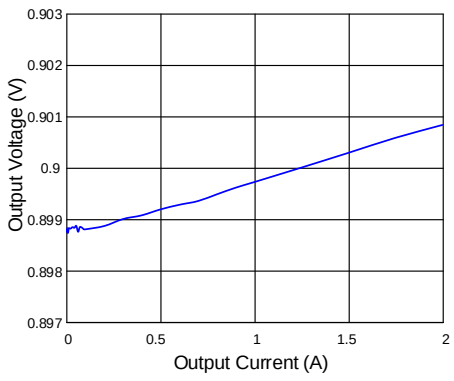
Output Voltage vs Load Current

(V_{IN}=3.3V, V_{Buck3}=0.75V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0~4A)



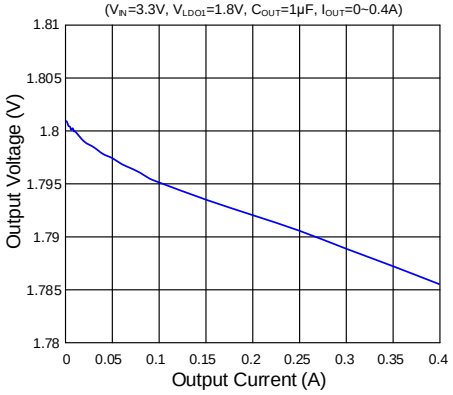
Output Voltage vs Load Current

(V_{IN}=3.3V, V_{Buck4}=0.9V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0~2A)



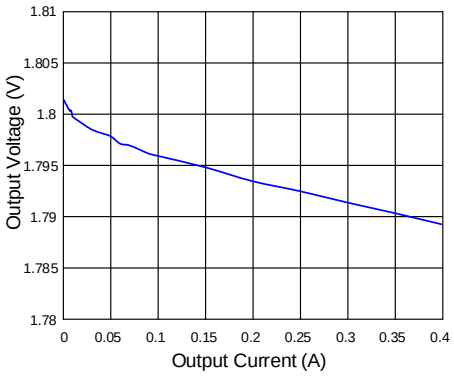
Output Voltage vs Load Current

(V_{IN}=3.3V, V_{LDO1}=1.8V, C_{OUT}=1μF, I_{OUT}=0~0.4A)



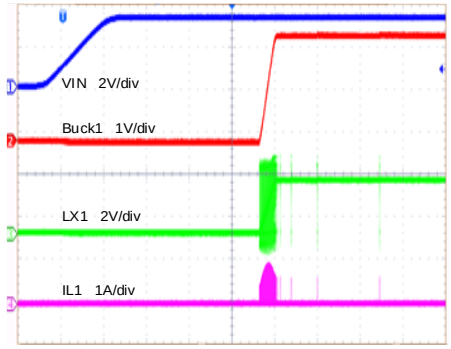
Output Voltage vs Load Current

(V_{IN}=3.3V, V_{LDO2}=1.8V, C_{OUT}=1μF, I_{OUT}=0~0.4A)



Buck1 Power On

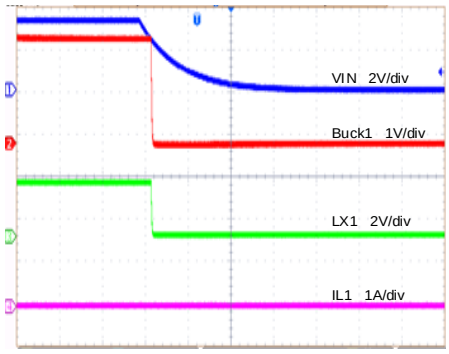
(V_{IN}=3.3V, V_{OUT1}=2.5V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A)



Time (0.8ms/div)

Buck1 Power Off

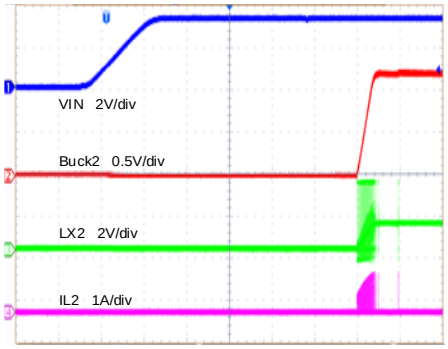
(V_{IN}=3.3V, V_{OUT1}=2.5V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A)



Time (4ms/div)

Buck2 Power On

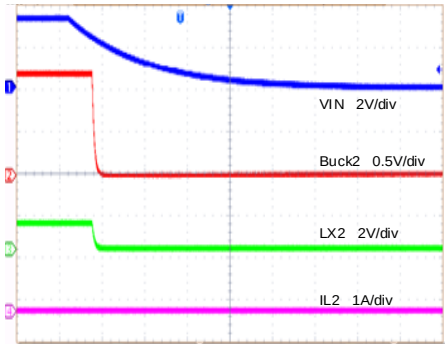
(V_{IN}=3.3V, V_{OUT2}=1.2V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A)



Time (0.8ms/div)

Buck2 Power Off

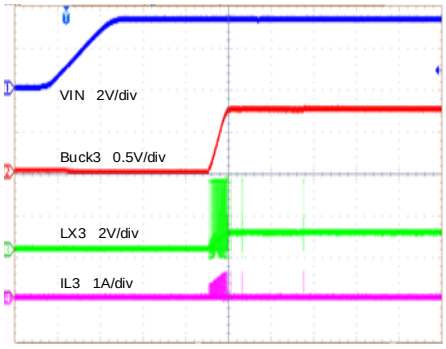
(V_{IN}=3.3V, V_{OUT2}=1.2V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A)



Time (2ms/div)

Buck3 Power On

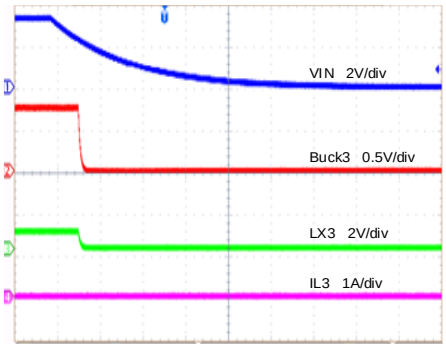
(V_{IN}=3.3V, V_{OUT3}=0.75V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A)



Time (0.8ms/div)

Buck3 Power Off

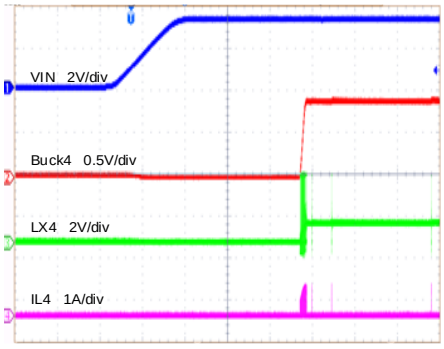
(V_{IN}=3.3V, V_{OUT3}=0.75V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A)



Time (2ms/div)

Buck4 Power On

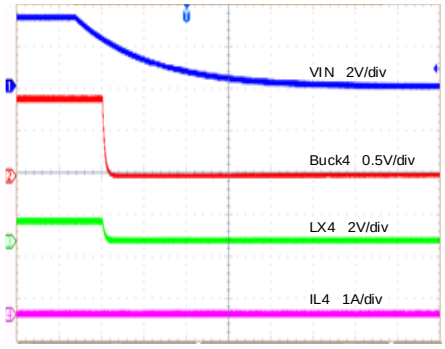
(V_{IN}=3.3V, V_{OUT4}=0.9V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A)



Time (0.8ms/div)

Buck4 Power Off

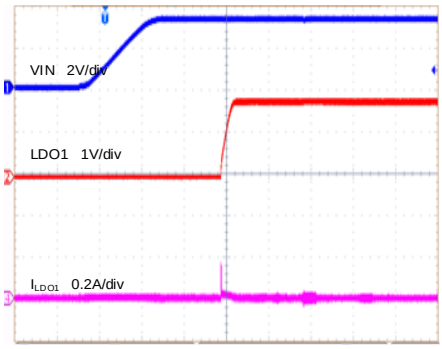
(V_{IN}=3.3V, V_{OUT4}=0.9V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A)



Time (2ms/div)

LDO1 Power On

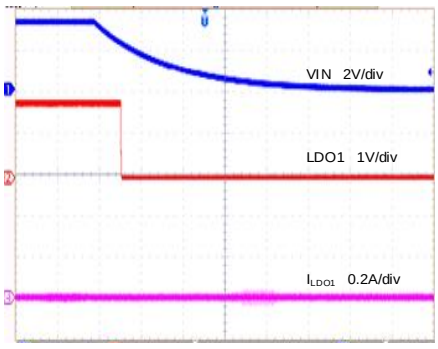
(V_{IN}=3.3V, V_{OUT}=1.8V, C_{OUT}=1μF, I_{OUT}=0A)



Time (0.8ms/div)

LDO1 Power Off

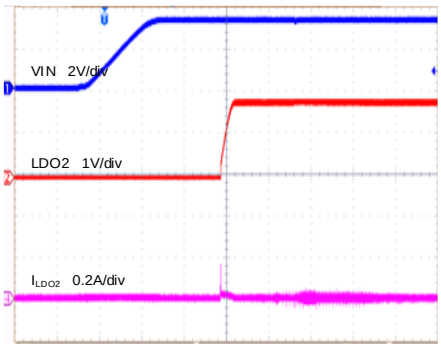
(V_{IN}=3.3V, V_{OUT}=1.8V, C_{OUT}=1μF, I_{OUT}=0A)



Time (2ms/div)

LDO2 Power On

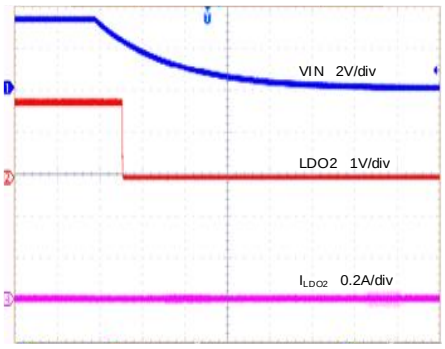
(V_{IN}=3.3V, V_{OUT}=1.8V, C_{OUT}=1μF, I_{OUT}=0A)



Time (0.8ms/div)

LDO2 Power Off

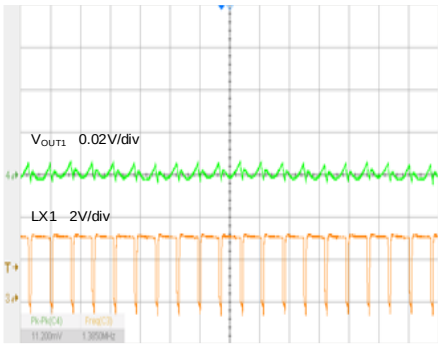
(V_{IN}=3.3V, V_{OUT}=1.8V, C_{OUT}=1μF, I_{OUT}=0A)



Time (2ms/div)

Buck1 Waveforms, FCCM Mode

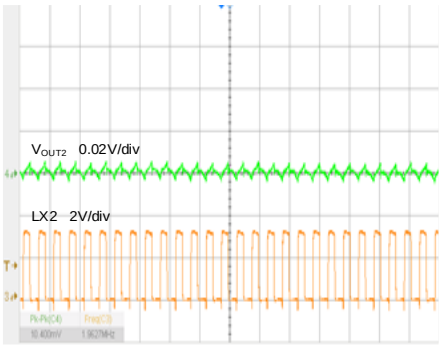
(V_{IN}=3.3V, V_{OUT1}=2.5V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=4A)



Time (1μs/div)

Buck2 Waveforms, FCCM Mode

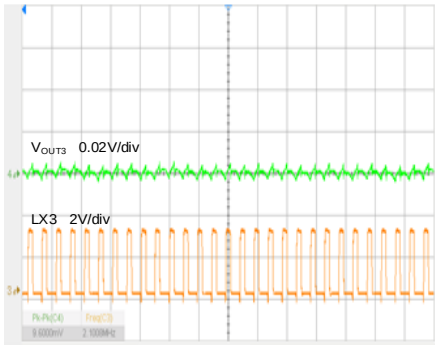
(V_{IN}=3.3V, V_{OUT2}=1.2V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=3A)



Time (1μs/div)

Buck3 Waveforms, FCCM Mode

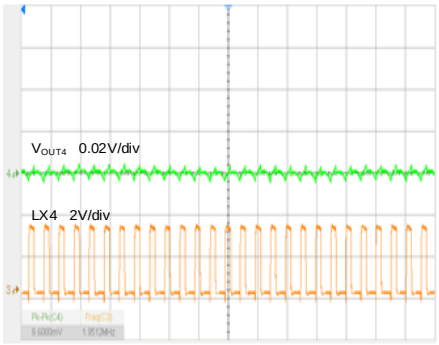
(V_{IN}=3.3V, V_{OUT3}=0.75V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=4A)



Time (1μs/div)

Buck4 Waveforms, FCCM Mode

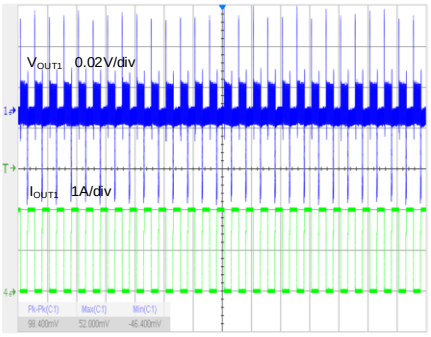
(V_{IN}=3.3V, V_{OUT4}=0.9V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=2A)



Time (1μs/div)

Buck1 Load Transient

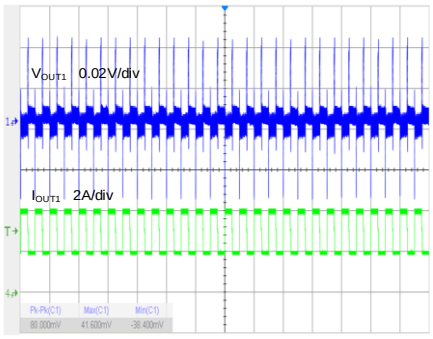
(V_{IN}=3.3V, V_{OUT1}=2.5V, L=0.47µH, C_{OUT}=22µF, I_{OUT}=0.05A~2A(0.2A/µs))



Time (2ms/div)

Buck1 Load Transient

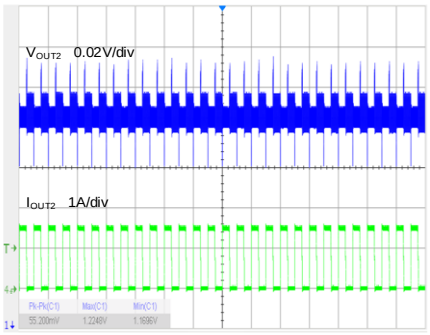
(V_{IN}=3.3V, V_{OUT1}=2.5V, L=0.47µH, C_{OUT}=22µF, I_{OUT}=2A~4A(0.2A/µs))



Time (2ms/div)

Buck2 Load Transient

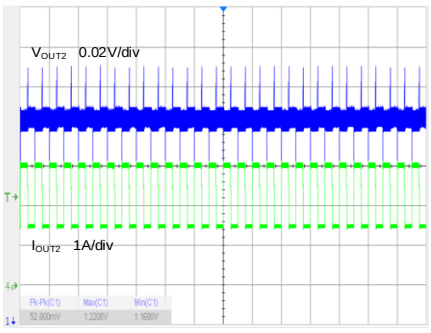
(V_{IN}=3.3V, V_{OUT2}=1.2V, L=0.47µH, C_{OUT}=22µF, I_{OUT}=0.05A~1.5A(0.2A/µs))



Time (2ms/div)

Buck2 Load Transient

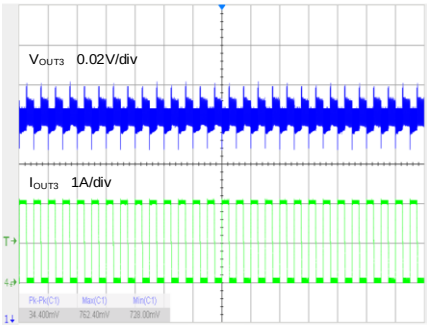
(V_{IN}=3.3V, V_{OUT2}=1.2V, L=0.47µH, C_{OUT}=22µF, I_{OUT}=1.5A~3A(0.2A/µs))



Time (2ms/div)

Buck3 Load Transient

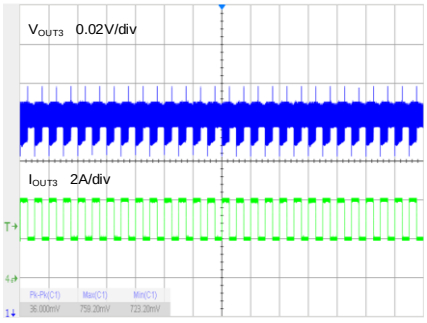
(V_{IN}=3.3V, V_{OUT3}=0.75V, L=0.47µH, C_{OUT}=22µF, I_{OUT}=0.05A~2A(0.2A/µs))



Time (2ms/div)

Buck3 Load Transient

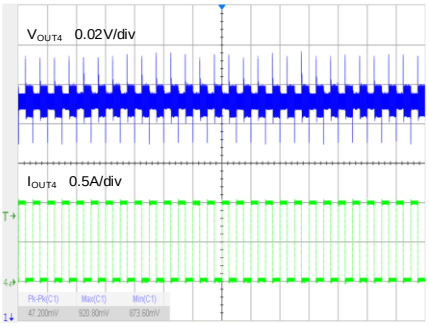
(V_{IN}=3.3V, V_{OUT3}=0.75V, L=0.47µH, C_{OUT}=22µF, I_{OUT}=2A~4A(0.2A/µs))



Time (2ms/div)

Buck4 Load Transient

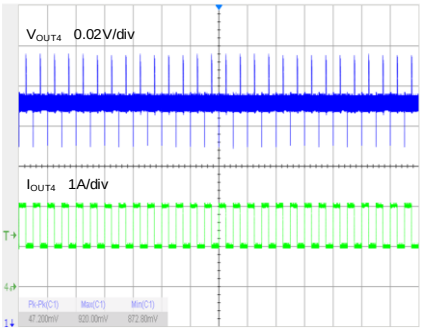
(V_{IN}=3.3V, V_{OUT4}=0.9V, L=0.47µH, C_{OUT}=22µF, I_{OUT}=0.05A~1A(0.2A/µs))



Time (2ms/div)

Buck4 Load Transient

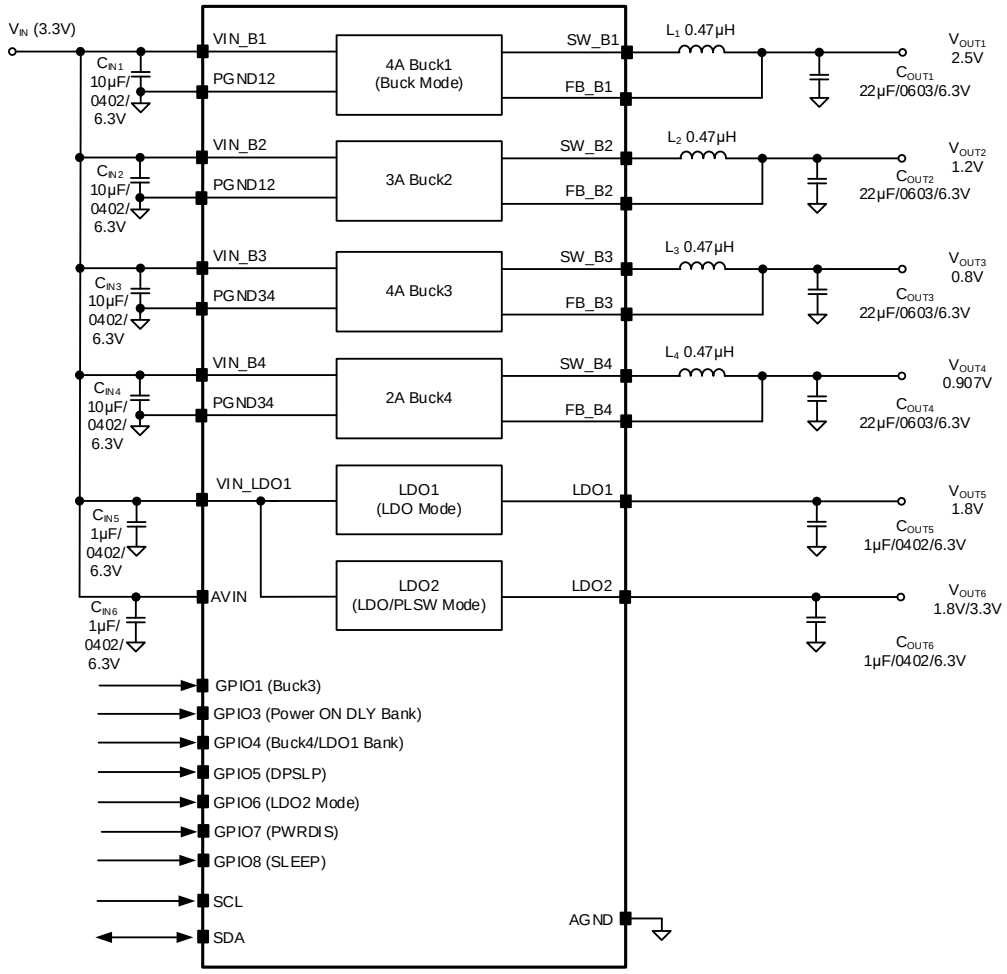
(V_{IN}=3.3V, V_{OUT4}=0.9V, L=0.47µH, C_{OUT}=22µF, I_{OUT}=1A~2A(0.2A/µs))



Time (2ms/div)

Typical Application

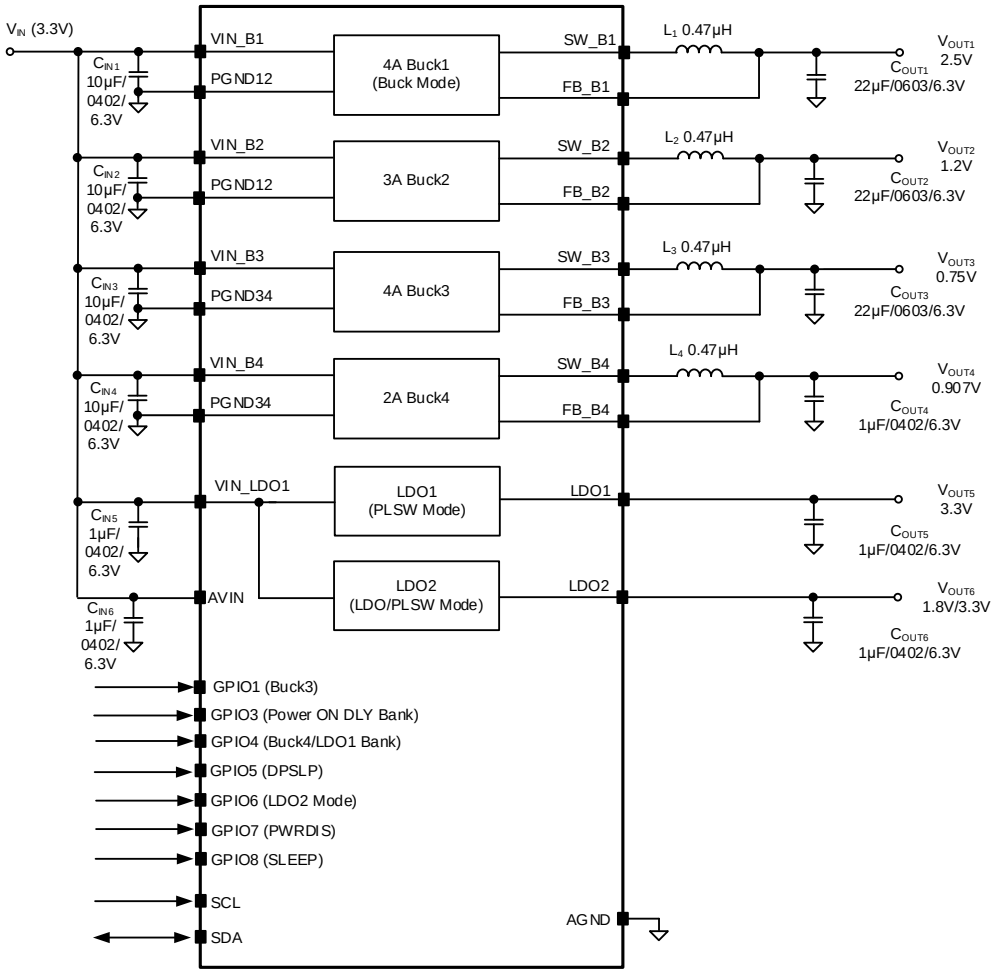
GPIO1=High, GPIO3=High, GPIO4=High.



Note: Buck1 I_{OUT} > 2.5A, C_{OUT}=22uF/0603/6.3V x2.

(a)

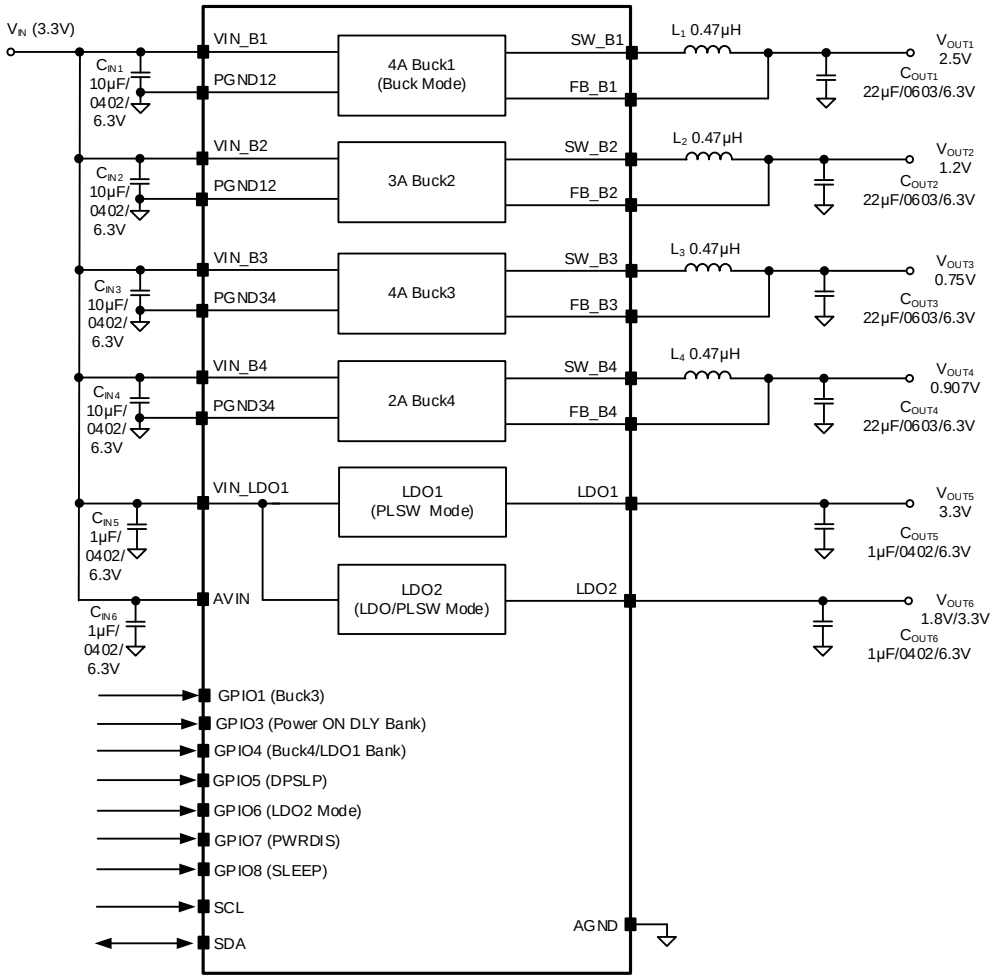
GPIO1=Floating, GPIO3=Floating, GPIO4=Floating.



Note: Buck1 I_{OUT} > 2.5A, C_{OUT}=22uF/0603/6.3V x2.

(b)

GPIO1=Low, GPIO3=Low, GPIO4=Low.



Note: Buck1 I_{OUT} > 2.5A, C_{OUT}=22uF/0603/6.3V x2.

(c)

Figure 5. Application Circuit for
(a) Application A, (b) Application B, (c) Application C

Description

Overview

	Output Program Range	Output Program Step	Mode	R_{DS_ON}		I_{OUT} MAX	HS Current Limit	Discharge Resistor	Soft Start Time
				HS	LS				
Buck1	1.6-3.0V	25mV	Buck or Bypass	40mΩ	40mΩ	4.0A	5.6A	4.4Ω	250/500μs
Buck2	0.75-1.85V	10mV	Buck	80mΩ	50mΩ	3.0A	4.4A	9.4Ω	250/500μs
buck3	0.5-1.2V	10mV	Buck	50mΩ	20mΩ	4.0A	5.6A	9.4Ω	250/500μs
buck4	0.807-1.907V	50mV	Buck	80mΩ	50mΩ	2.0A	3.6A	9.4Ω	150μs
LDO1	1.0-2.7V	50mV	LDO or PLSW	PLSW: 300mΩ		0.4A	LDO, PLSW: 0.5A	20Ω	200/360μs
LDO2	1.0-2.7V	50mV	LDO or PLSW	PLSW: 300mΩ		0.4A	LDO, PLSW: 0.5A	20Ω	200/360μs

Power Sequence

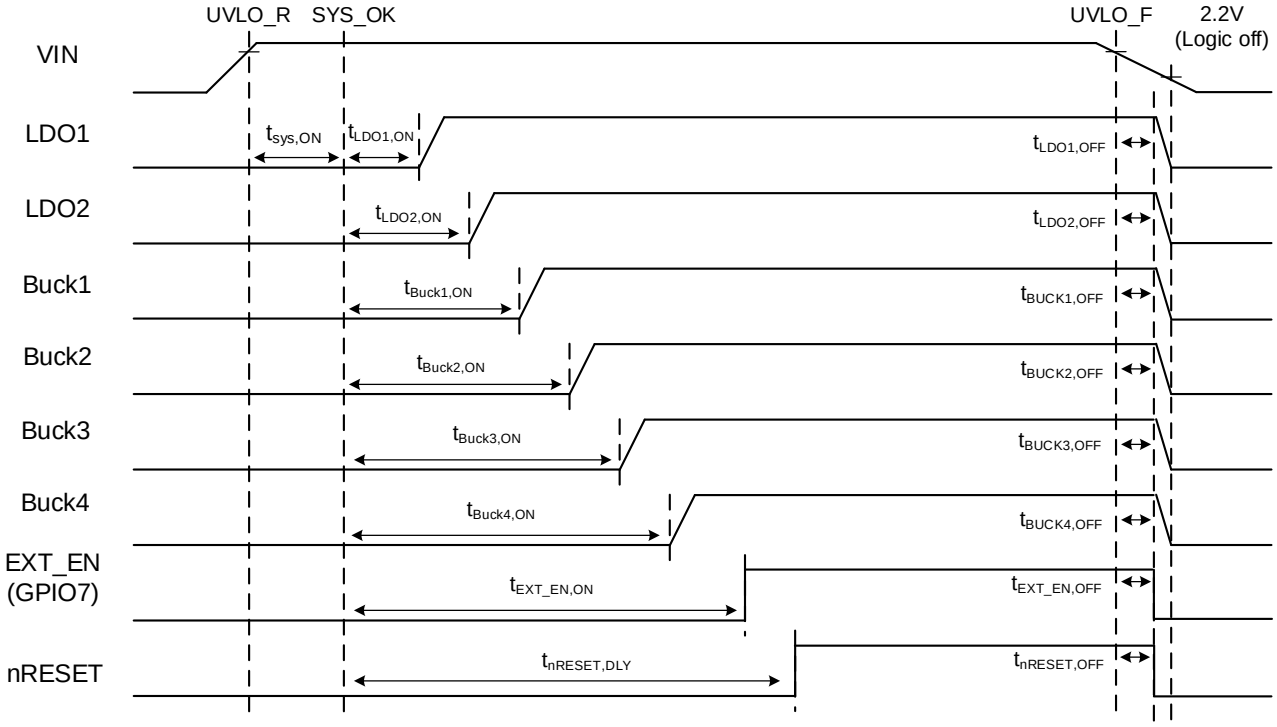


Figure 6. VIN Power On/Off Sequence

(1) When VIN exceeds the UVLO rising threshold, each channel will start after the system delay $t_{SYS,ON}$(1ms typ.). During the system delay, the device will detect the GPIO3/4 status to define each channel's default setting (operating mode, output voltage and power on delay, etc). The power-on delay time can be set from 0ms to 7.5ms (0.5ms/step) to provide a different power sequence as required by the application. If VIN is lower than the UVLO falling threshold, all channels will be turned off after the delay time. The power-off delay time can be set to 0ms, 0.25ms, 0.5ms, or 1ms.

(2) nRESET and EXT_EN(GPIO7) are open drain outputs; they are high impedance after a delay time that starts when VIN exceeds the UVLO rising threshold. The delay time of nRESET can be set 0.5ms to 16ms and the delay time of EXT_EN can be set from 0ms to 7.5ms (0.5ms/step). nRESET and EXT_EN will be pulled low immediately when any output is out of regulation. nRESET remains high in sleep and deep sleep mode.

(3) If the input pin is floating, the corresponding channel will be disabled internally after VIN power on.

(4) Before the rail enable, the discharge resistor is turned on.

Undervoltage Lockout (UVLO)

Undervoltage lockout is achieved by detecting VIN voltage. If the AVIN pin voltage exceeds $V_{IN,RISING}$ (2.6V typ.), all rails will start after a delay time. When AVIN pin voltage is lower than $V_{IN,FALLING}$ voltage(2.4V typ.), all rails are shut down after a delay time. The UVLO hysteresis (0.2V typ.) is designed to prevent shutdown caused by supply transients.

External Enable (EXT_EN)

The SY70202K provides an external power supply enable function, EXT_EN which is used to control an external regulator. If the AVIN pin voltage exceeds $V_{IN,RISING}$ (2.6V typ.), the EXT_EN will become high impedance after a fixed delay. When AVIN pin voltage is lower than $V_{IN,FALLING}$ (2.4V typ.) or fault occurs, EXT_EN will become low impedance after a delay time. EXT_EN can be set to enable or disable in sleep or deep sleep mode using bit[6] of registers 0x08h or 0x09h, respectively.

GPIOx Setting

The SY70202K has seven GPIO pins. Each GPIO can be programmed for a specific function to suit different application. GPIO1, GPIO3, and GPIO4 are 3.3-level GPIOs that can be configured to set the output voltage of the power rail, and the power on delay.

GPIO1:

GPIO1 is an input pin used to select Buck3 output voltage. There are three options for user to select the different default configuration. The GPIO1 status must be set before UVLO and cannot be changed while the converter is running. Once the converter is running, buck operating mode and output voltage settings can be changed by using I^2C.

Table 1. GPIO1 Function Selection

GPIO1	Buck3 Output Voltage
High	B3_VSET0=0.8V; B3_VSET1=0.7V
Floating	B3_VSET0=0.75V; B3_VSET1=0.65V
Low	B3_VSET0=0.75V; B3_VSET1=0.65V

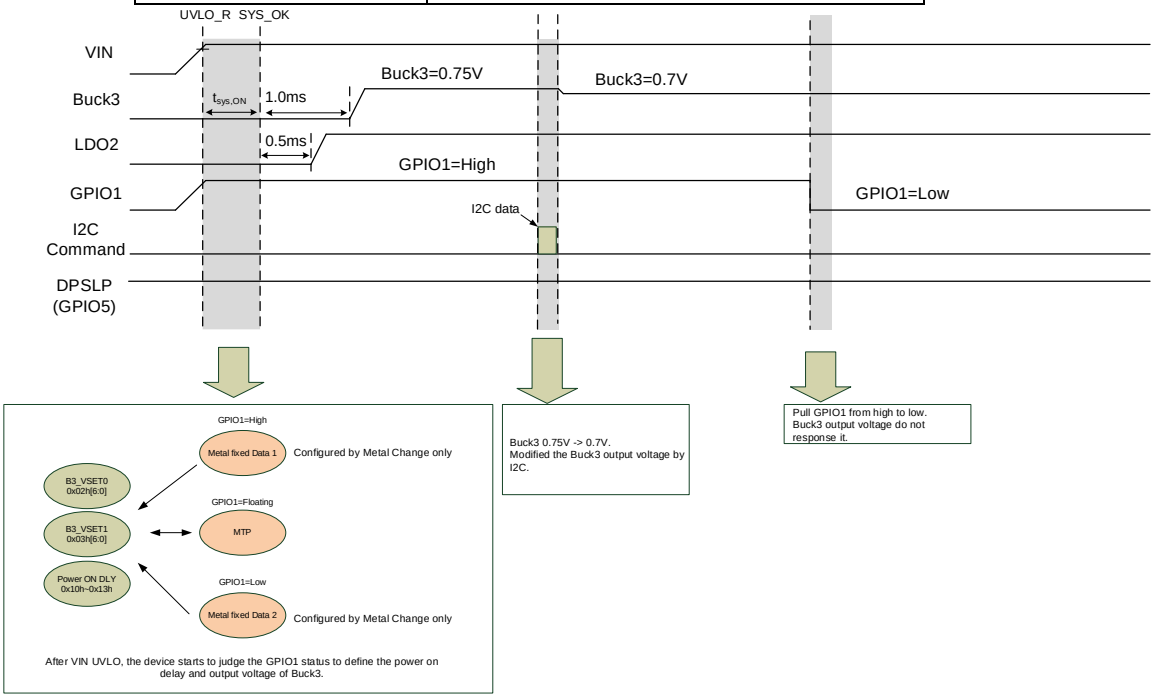


Figure 7. GPIO1 Sequence for Buck3 Configuration

Note: When the GPIO1 is high or low status, the default setting cannot modified by MTP.

Only when GPIO1 is floating status, the default value can be modified by MTP.

GPIO3:

GPIO3 is an input pin used to select power on delay option of each rail. There are three options for user to select the different default configuration. The GPIO3 status must be set before UVLO and cannot be changed while the converter is running. Once the converter is running, buck operating mode and output voltage settings can be changed by using I^2C.

Table 2. GPIO3 Function Selection

GPIO3	Power on Delay
High	Sequence A
Floating	Sequence B
Low	Sequence C

Table 3. Power-on Sequence

Rail	GPIO3=High Sequence A	GPIO3=Floating Sequence B	GPIO3=Low Sequence C
Buck1	3.00ms	2.00ms	2.00ms
Buck2	2.00ms	3.00ms	3.00ms
Buck3	1.00ms	1.00ms	1.00ms
Buck4	1.50ms	1.50ms	1.50ms
LDO1	0.50ms	0.50ms	0.50ms
LDO2	0.50ms	0.50ms	0.50ms
EXT_EN	1.50ms	1.50ms	1.50ms
nRESET	Input Trigger: SYS_OK Delay time=4.0ms		

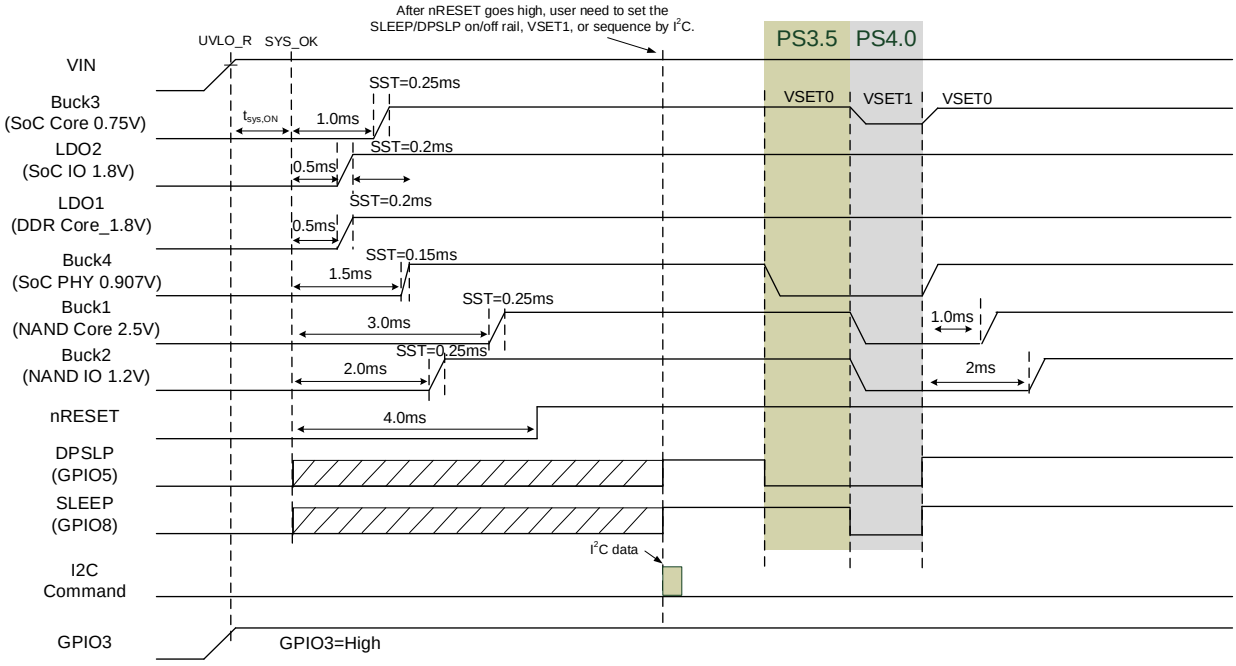


Figure 8. Power Sequence of Sequence A

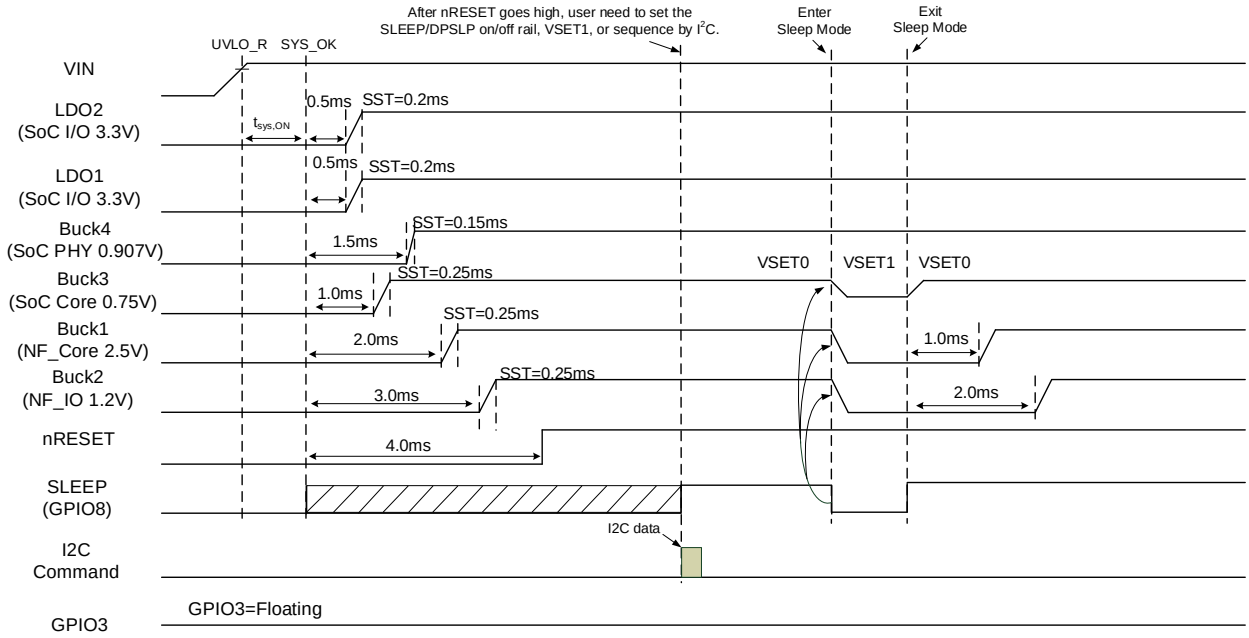


Figure 9. Power Sequence of Sequence B

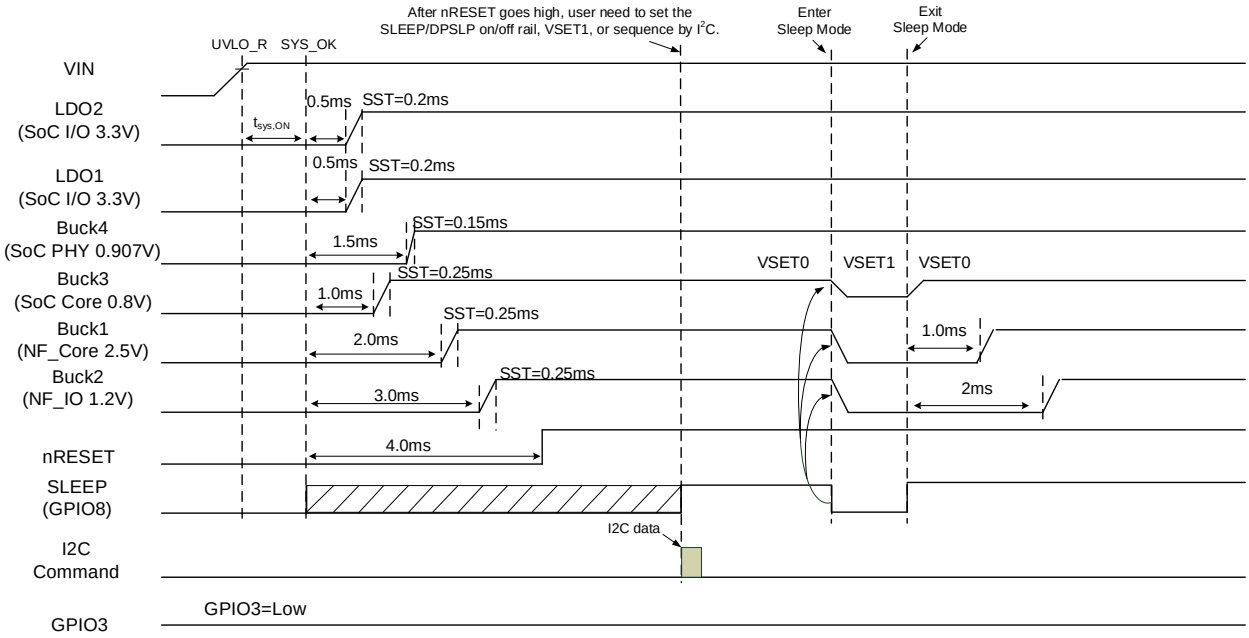


Figure 10. Power Sequence of Sequence C

GPIO4:

GPIO4 is an input pin used to select Buck4 or LDO1 mode. Buck4 is operating in buck mode, the output voltage can be set by register B4_VSET. LDO1 can be set to operate in LDO or PLSW mode using the register LDO1_Mode. If LDO1 is operating in LDO mode, the output voltage can be set by register LDO1_VSET. Buck4 and LDO1 have three configuration options as shown in Table 4. The GPIO4 status must be set before UVLO and cannot be changed while the converter is running. Once the converter is running, buck operating mode and output voltage settings can be changed using I²C.

Table 4. GPIO4 Function Selection

GPIO4	Buck4 Mode and Output Voltage	LDO1 Mode and Output Voltage
High	B4_VSET=0.907V	LDO1_Mode=LDO Mode LDO1_VSET=1.8V
Floating	B4_VSET=0.907V	LDO1_Mode=PLSW
Low	B4_VSET=0.907V	LDO1_Mode= PLSW

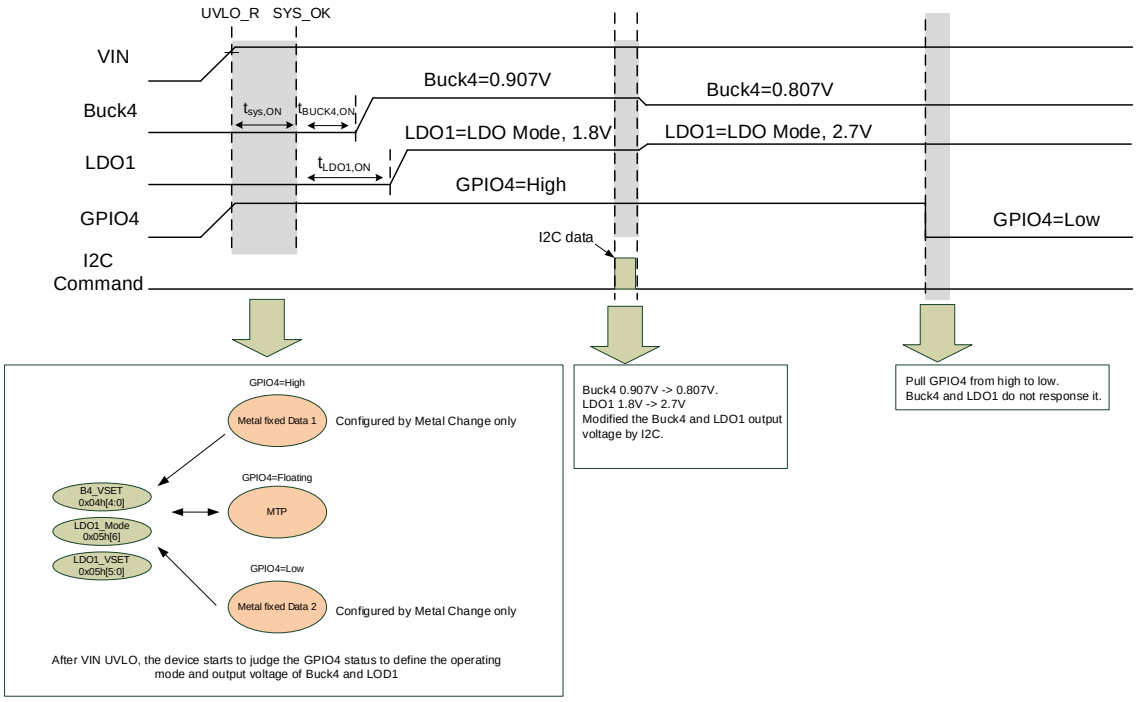


Figure 11. GPIO4 Sequence for Buck4 and LDO1 Configuration

Note: When the GPIO4 is high or low status, the default setting cannot modified by MTP.

Only when GPIO4 is floating status, the default value can be modified by MTP.

GPIO5:

GPIO5 can be configured as a DPSLP mode input pin, a nIRQ(SYSWARN) output pin, or an I²C controlled output pin by bit [7:6] at register 0x15h. User can modified the function of GPIO5 by I²C after nRESET goes high.

- **DPSLP mode**: Input pin. The GPIO5 pin is a level sensitive in DPSLP mode. If GPIO5 is pulled high (>1.2V), the device will operate in ACTIVE mode; if GPIO5 is pulled low (<0.55V), the device will operate in DPSLP mode.
- **I²C Controlled Output**: GPIO5 can be configured as the I²C controlled open drain output. The output can be selected as HIGH or LOW using bit [1] of register 0x15h.

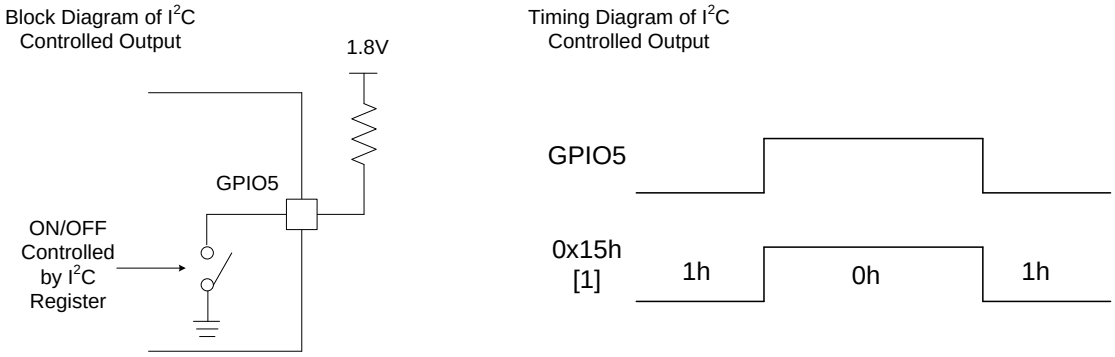


Figure 12. Block Diagram and Timing Diagram of I²C Controlled Output Function.

- **nIRQ(SYSWARN) Output**: GPIO5 can be configured as the nIRQ(SYSWARN) open-drain output. If AVIN < SYSWARN (2.9V typ.), the device will assert the nIRQ interrupt and GPIO5 will become low. The nIRQ pin only de-asserts when the fault condition is no longer present, and the corresponding fault bit is read via I²C.

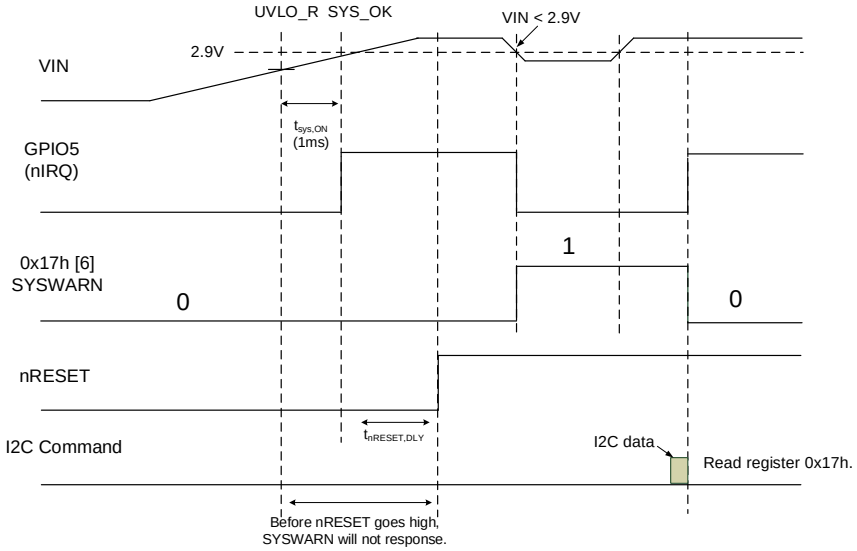


Figure 13. Timing Diagram of nIRQ (SYSWARN).

GPIO6:

GPIO6 is an input pin used to select LDO2 operating mode. If the GPIO6 is pulled high, it will operate in LDO mode; if GPIO6 is pulled low, it will operate in PLSW mode. LDO2 mode will be latched after a LDO2 power-on delay.

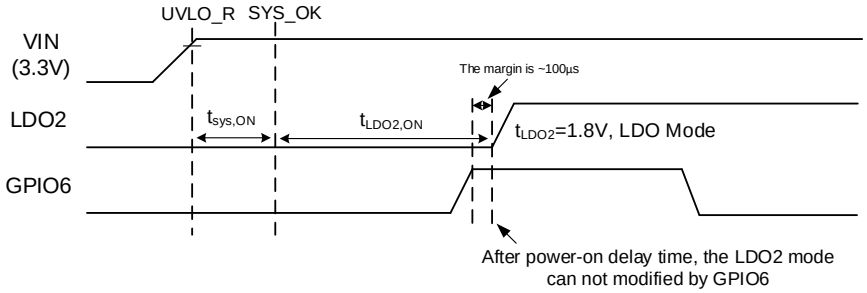


Figure 14. Timing Diagram of GPIO6 Function

GPIO7:

GPIO7 can be configured as an EXT_EN output pin, an I²C-controlled output pin, or a PWRDIS input pin using bit [5:4] of register 0x15h. GPIO7 function can be modified by I²C after nRESET goes high.

- **I²C-Controlled Output**: GPIO7 can be configured as an I²C-controlled open-drain output. The output can be selected HIGH or LOW using bit [0] of register 0x15h.

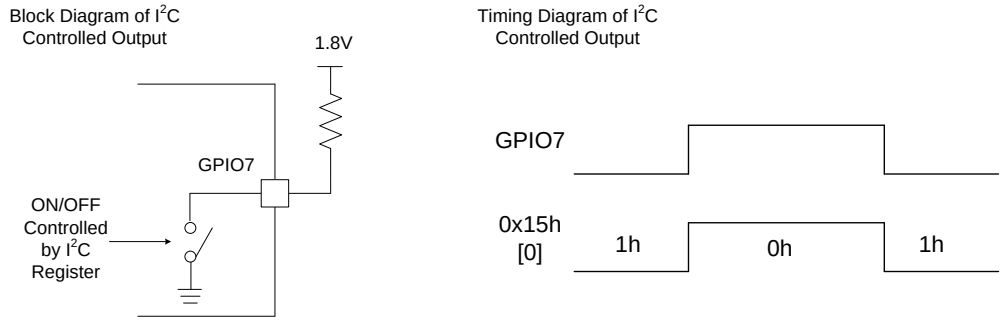


Figure 15. Block Diagram and Timing Diagram of I²C Controlled Output Function.

- **PWRDIS Input**: GPIO7 can be configured as the PWRDIS input. If GPIO7 is pulled high (>1.2V), all rails will be shut down; if GPIO7 is pulled low (<0.55V), all rails will power up with sequence. PWRDIS can be considered a global enable for the PMIC. If PWRDIS is high during power-on, this will prevent the device from turning on and powering on the rails.

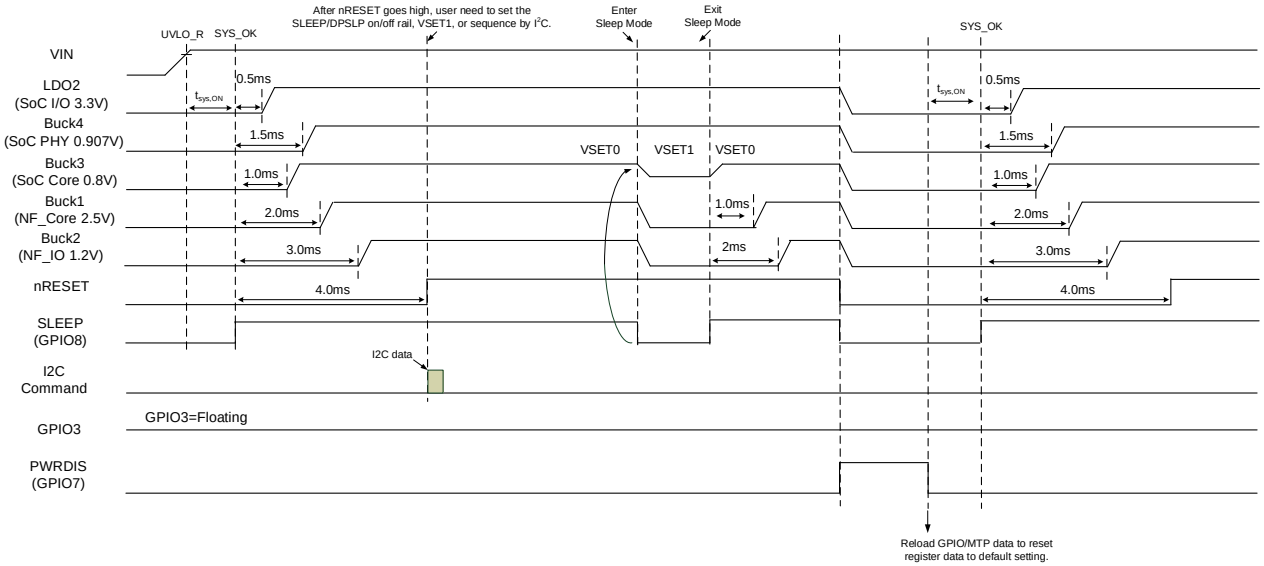


Figure 16. Conceptual of Timing Diagram for PWRDIS during Operating

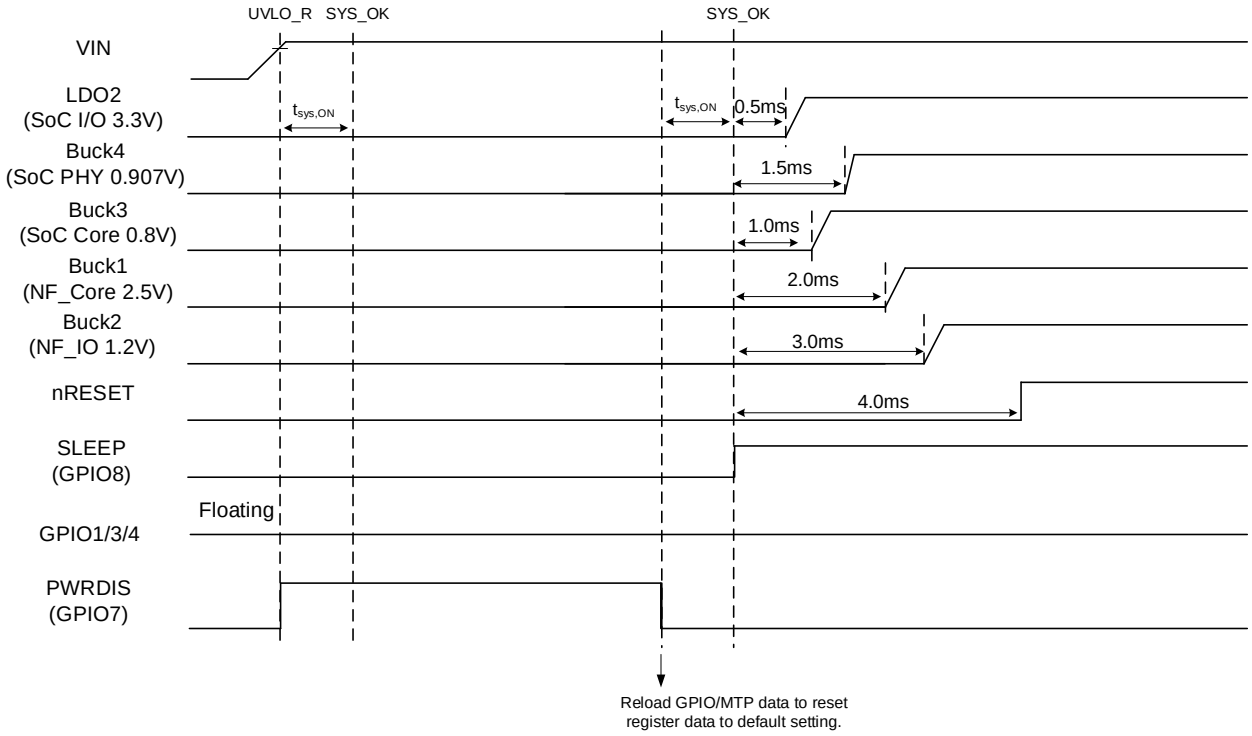


Figure 17. Conceptual of Timing Diagram for PWRDIS during VIN Power-on

GPIO8:

GPIO8 is an input pin used to select SLEEP state. This pin act as a level sensitive. If GPIO8 is pulled high (>1.2V), the device will operate in ACTIVE mode; if GPIO8 is pulled low (<0.55V), the device will operate in SLEEP mode.

GPIO Initial Status

GPIO	Function	Pin	Initial Status
GPIO1	Buck3 Bank	Input	NA
GPIO3	Power on delay Bank	Input	NA
GPIO4	Buck4 and LDO1 Bank	Input	
GPIO5	DPSLP, I²C Control Output, or nIRQ(SYSWARN)	Input or Open drain output	NA
GPIO6	LDO2 Mode	Input	Internal 1MΩ pull low
GPIO7	EXT_EN, I²C Control Output, or PWRDIS	Input or Open drain output	I²C Control Output *
GPIO8	SLEEP	Input	Internal 1MΩ pull low

* ***Note:*** *In PWRDIS, external 10kΩ pull low is need.*

State Machine

The SY70202K state machine contains six internal states, shown in Figure 18.

In the RESET state, the Device is waiting for the input voltage on VIN to be within a valid range between VIN_UVLO and VIN OVP threshold. In this state, all regulators are off. The ACTIVE state is the normal operating state when the input voltage is within the allowable range, all outputs are turned on, and no faults will be presented. When entering ACTIVE state from the RESET, THERMAL, or OV/SCP fault, all regulators are powered on following their power-up sequence. The regulators will not be sequenced when entering ACTIVE form SLEEP or DPSLP states.

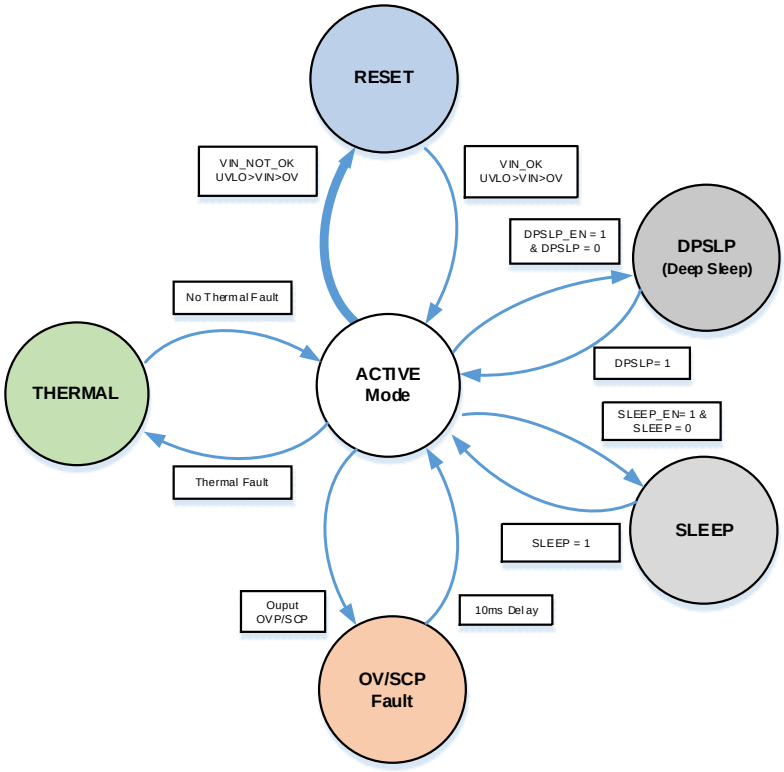


Figure 18. State Machine

Sleep Mode State

Each output can be programmed to be on or off in the sleep state. The regulators follow their programmed sequencing delay times when turning on or off as they exit or enter the SLEEP state. Bucks 1~4, LDO1/2, and EXT_EN can be programmed to turn off or turn on in the SLEEP state by I²C. The device can enter SLEEP state via the I²C register SLEEP bit or by a GPIO input. Each individual regulator output can be programmed to be either on or off in the SLEEP state. Buck3 can also be programmed to regulate to its VSET0 voltage, or VSET1 voltage (DVS), or be turned off in the SLEEP state. Table 5 shows the conditions to enter SLEEP state. The device I²C remains enabled in SLEEP state. The device exits the SLEEP state when the conditions to enter SLEEP state are no longer present.

Table 5. SLEEP Mode Truth Table

SLEEP	0x10h[1], SLEEP_EN	Result
0	1	Sleep mode
1	1	Active mode

Note: The SLEEP signal need masking before nRESET goes high, and reserve a trim bit to enable or disable the masking function.

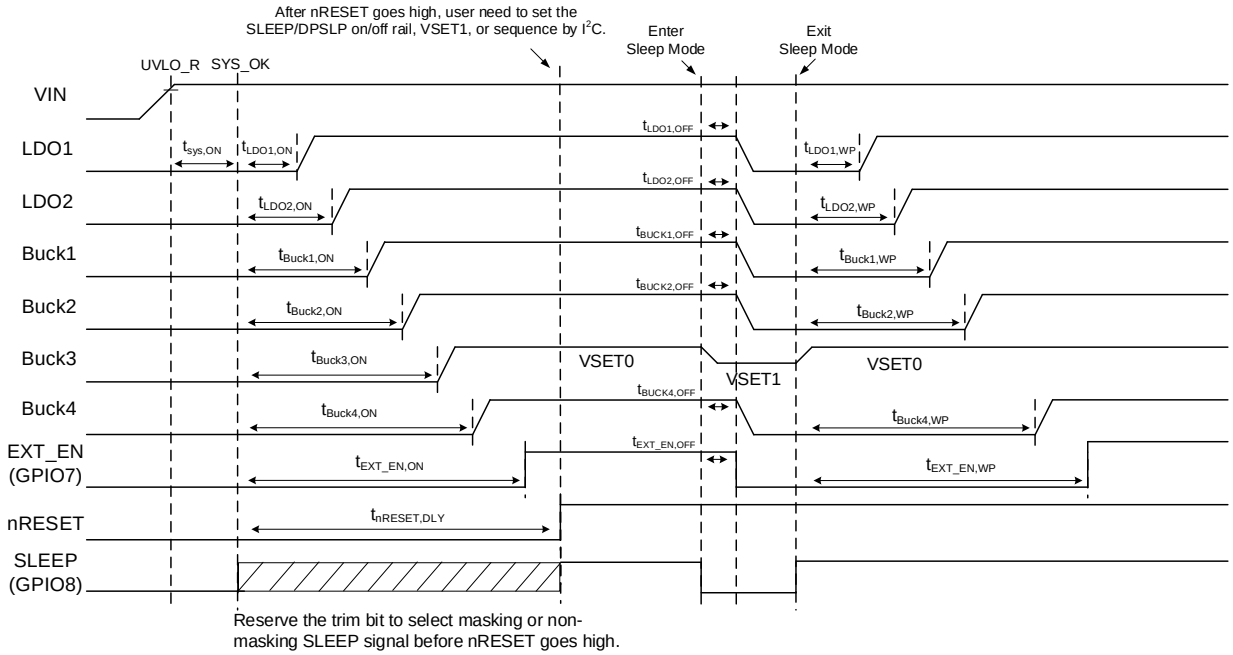


Figure 19. Conceptual of Sequence for Enter/exit SLEEP Mode

- Power-on delay time:
  $t_{LDO1,ON}$/ $t_{LDO2,ON}$/ $t_{Buck1,ON}$/ $t_{Buck2,ON}$/ $t_{Buck3,ON}$/$t_{Buck4,ON}$/$t_{EXT\_EN,ON}$ =0~7.5ms, 0.5ms/step.
- Power-off delay time:
  $t_{LDO1,OFF}$/ $t_{LDO2,OFF}$/ $t_{Buck1,OFF}$/ $t_{Buck2,OFF}$/ $t_{Buck3,OFF}$/$t_{Buck4,OFF}$/$t_{EXT\_EN,OFF}$ =0ms, 0.25ms, 0.5ms, or 1ms.
- nRESET delay time:
  $t_{nRESET,DLY}$ =0.5ms, 1ms, 2ms, 4ms, 8ms, or 16ms.
- Wake up delay time:
  $t_{LDO1,WP}$/ $t_{LDO2,WP}$/ $t_{Buck1,WP}$/ $t_{Buck2,WP}$/ $t_{Buck3,WP}$/$t_{Buck4,WP}$/$t_{EXT\_EN,WP}$ =0~3ms, 1ms/step.

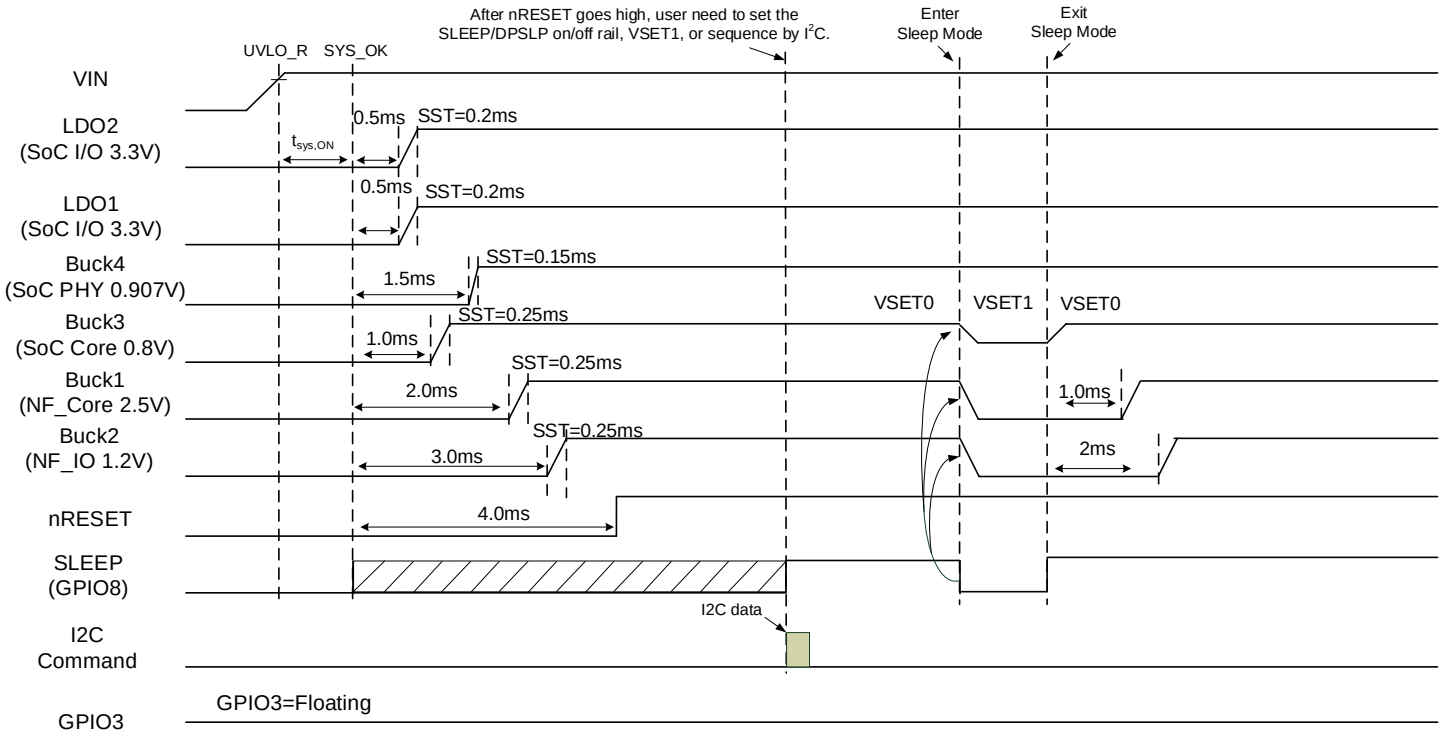


Figure 20. SLEEP Sequence for Application B

Deep Sleep (DPSLP) Mode State

The DPSLP state is another low-power operating mode similar to SLEEP state. Each output can be programmed to be on or off during DPSLP state. This programming can be different from the SLEEP state. The regulators follow their programmed sequencing delay times when turning on or off as they exit or enter the DPSLP state.

The device can enter DPSLP state via I²C registers DPSLE_EN and DPSLP pin**.** Table 6 shows the conditions to enter DPSLP state. Device I²C remains enabled in DPSLP state. The device exits the DPSLP state when the conditions to enter DPSLP state are no longer present.

The interval between entering two SLEEP/DPSLP states must be greater than 4ms. Within 4ms after entering the SLEEP/DPSLP state, the internal clock blocks the next instruction to enter the SLEEP/DPSLP state. However, power-off delay time is 0ms, which can be ignored.

Table 6. DPSLP Mode Truth Table

DPSLP	0x10h[0]	Result
	DPSLP_EN	
0	1	Deep Sleep Mode
1	1	Active Mode

Note: The DPSLP signal need masking before nRESET goes high, and reserve a trim bit to enable or disable the masking function.

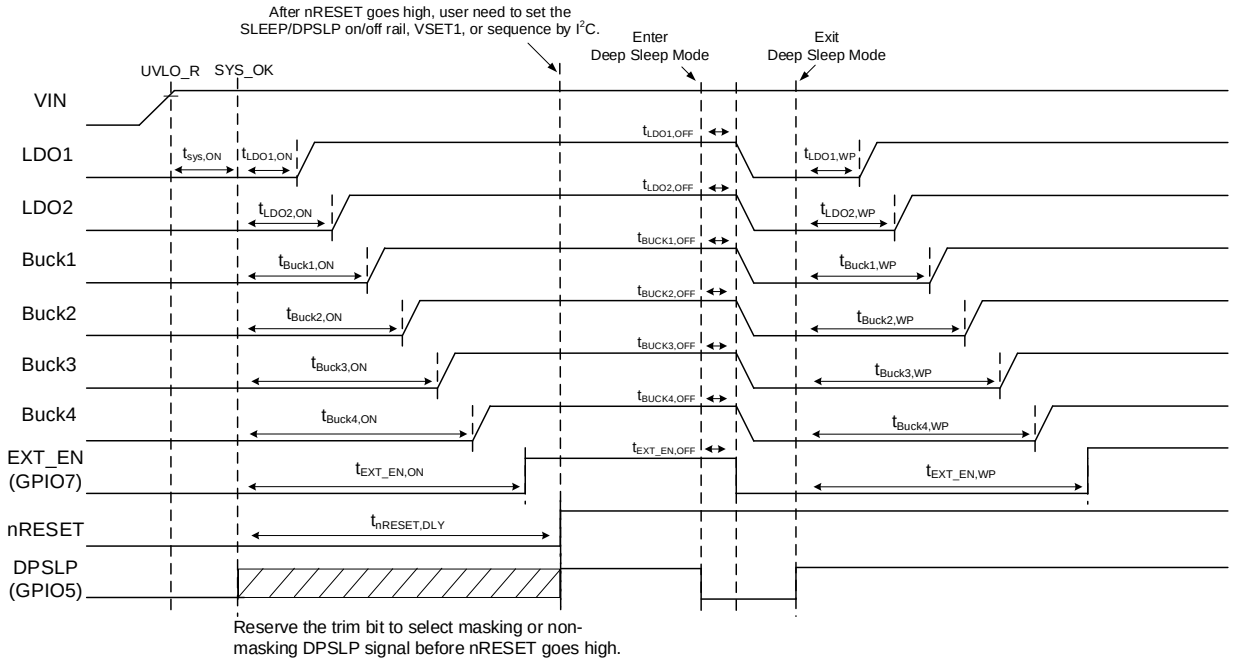


Figure 21. Conceptual of Sequence for Enter/exit DPSLP Mode

- Power-on delay time:
  $t_{LDO1,ON}$/ $t_{LDO2,ON}$/ $t_{Buck1,ON}$/ $t_{Buck2,ON}$/ $t_{Buck3,ON}$/$t_{Buck4,ON}$/$t_{EXT\_EN,ON}$ =0~7.5ms, 0.5ms/step.
- Power-off delay time:
  $t_{LDO1,OFF}$/ $t_{LDO2,OFF}$/ $t_{Buck1,OFF}$/ $t_{Buck2,OFF}$/ $t_{Buck3,OFF}$/$t_{Buck4,OFF}$/$t_{EXT\_EN,OFF}$ =0ms, 0.25ms, 0.5ms, or 1ms.
- nRESET delay time:
  $t_{nRESET,DLY}$ =0.5ms, 1ms, 2ms, 4ms, 8ms, or 16ms.
- Wake up delay time:
  $t_{LDO1,WP}$/ $t_{LDO2,WP}$/ $t_{Buck1,WP}$/ $t_{Buck2,WP}$/ $t_{Buck3,WP}$/$t_{Buck4,WP}$/$t_{EXT\_EN,WP}$ =0~3ms, 1ms/step.

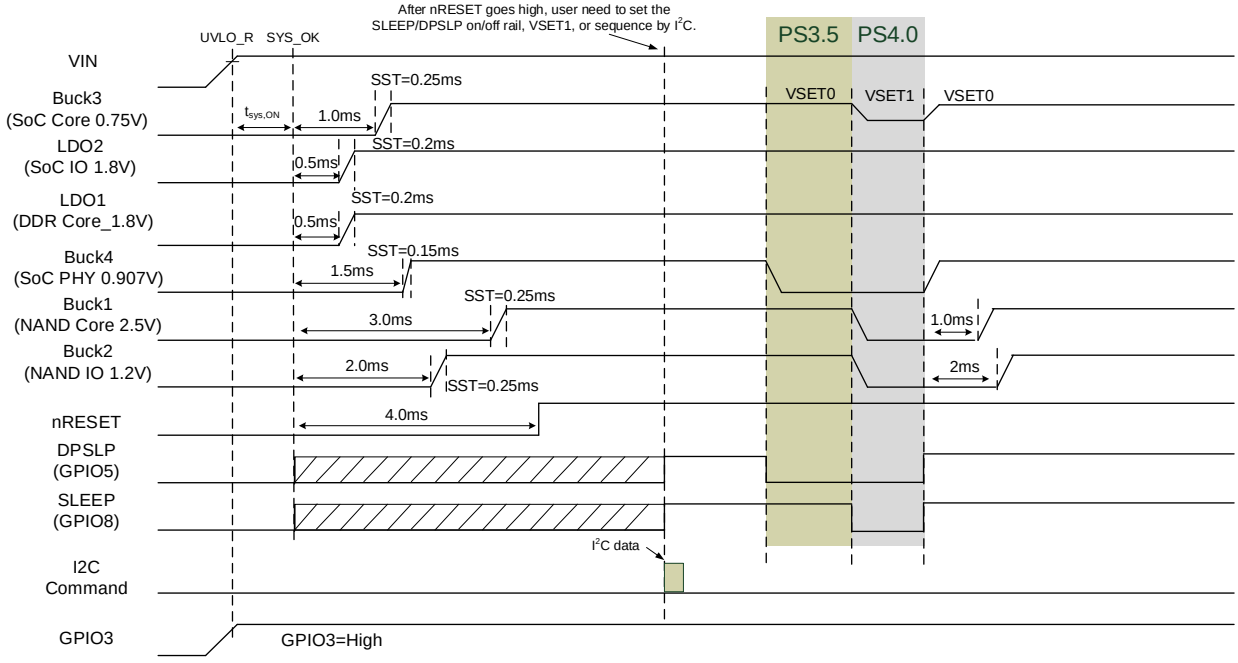


Figure 22. SLEEP and DPSLP Sequence for Application A

Protection Function

The following sections and Table 7 describe the SY70202K fault-protection functions.

Table 7. Protection Functions Summary

Protection		Mechanism
VIN Overvoltage Protection (VINOVP)		When VIN rises above 3.9V, the device shuts down and all the regulators are disabled. When VIN decreases to 3.6V, the device restarts with the power-up sequence.
Overtemperature Protection (OTP)		When temperature exceeds 155°C, the device shuts down. When temperature decreases below 140°C, it restarts following the power-up sequence.
Buck Output Over Voltage Protection (OVP)		When output voltage exceeds 125% of the target voltage for more than the 10μs deglitch time, the device shuts down all functions for 10ms, then restarts with the power-up sequence.
LDO Output Overvoltage Protection (LDO OVP)		>115% with 10μs deglitch time, open discharge loop at LDO output side with 2k resistance.
Output Short-Circuit Protection (SCP)		Buck output voltage: <30% for more than 50μs deglitch time, the device shuts down for 10ms then restarts with the power-up sequence. Buck1 @Bypass mode: output voltage <80% with 50μs deglitch time, the device shuts down all functions for 10ms, then restarts with the power up sequence. LDO: output voltage <60% with 50μs deglitch time, the device shuts down all functions for 10ms, then restarts with the power-up sequence.
Overcurrent Protection (OCP)	Buckx	Inductor current peak reaches current limit, and then maintain regulation.
	LDO	LDO current limit reached. If I_{OUT}=0.5A for more than 200μs, the device shuts down all functions for 10ms, then restarts with the power-up sequence.
	LDO1/2 PSLW Mode	Load switch current limit reached. If I_{OUT}=0.5A for more than 200μs, the device shuts down all functions for 10ms, then restarts with the power-up sequence.
	Buck1 Bypass Mode	Load switch current limit reached. If I_{OUT} = 4.5A or more than 200μs, the device shuts down all functions for 10ms, then restarts with the power-up sequence.

The device will reset to default settings after VINOVP, OTP, OVP, SCP, or OCP shutdown.

Output overvoltage and Short-Circuit Protection

If any output short-circuit or overvoltage condition occurs, this device will shut down for 10ms at once and then will restart with the power-up sequence. If the short-circuit or overvoltage condition still exists in the ACTIVE state, this device will shut down again for 10ms then restart, until the fault condition is removed.

LDO OVP function is enabled by 0x04 bit[6]. The 2k resistance discharge at LDO output side will be open when LDO output voltage exceeds 115% of reference voltage. And LDO OVP fault is triggered.

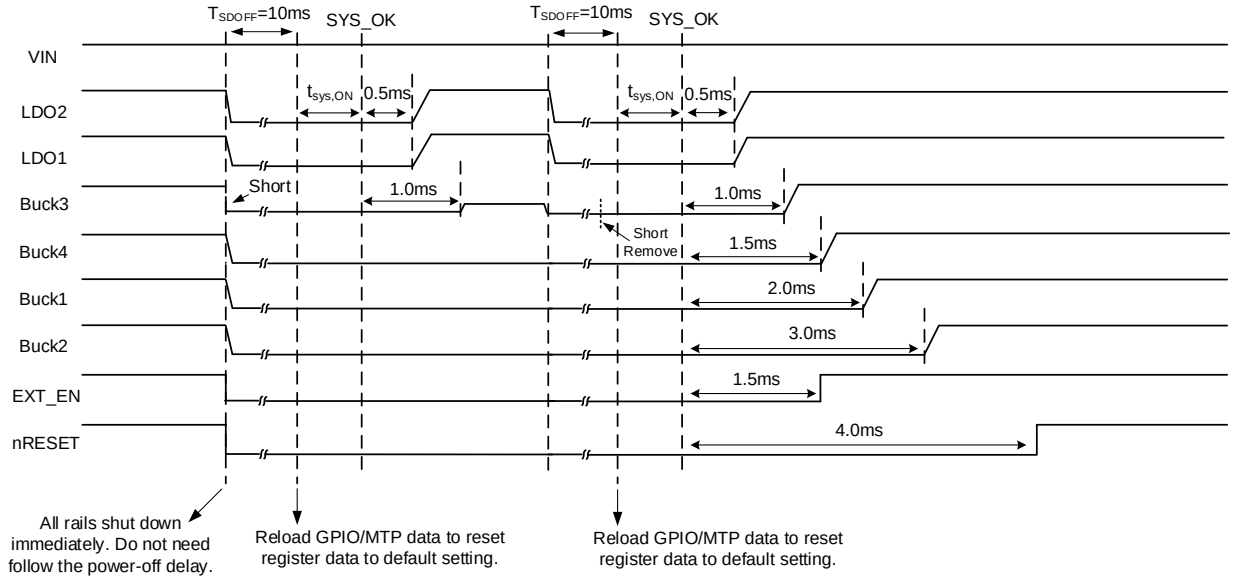


Figure 23. Conceptual of Buck3 Occurring Output Short-Circuit Event in Active Mode

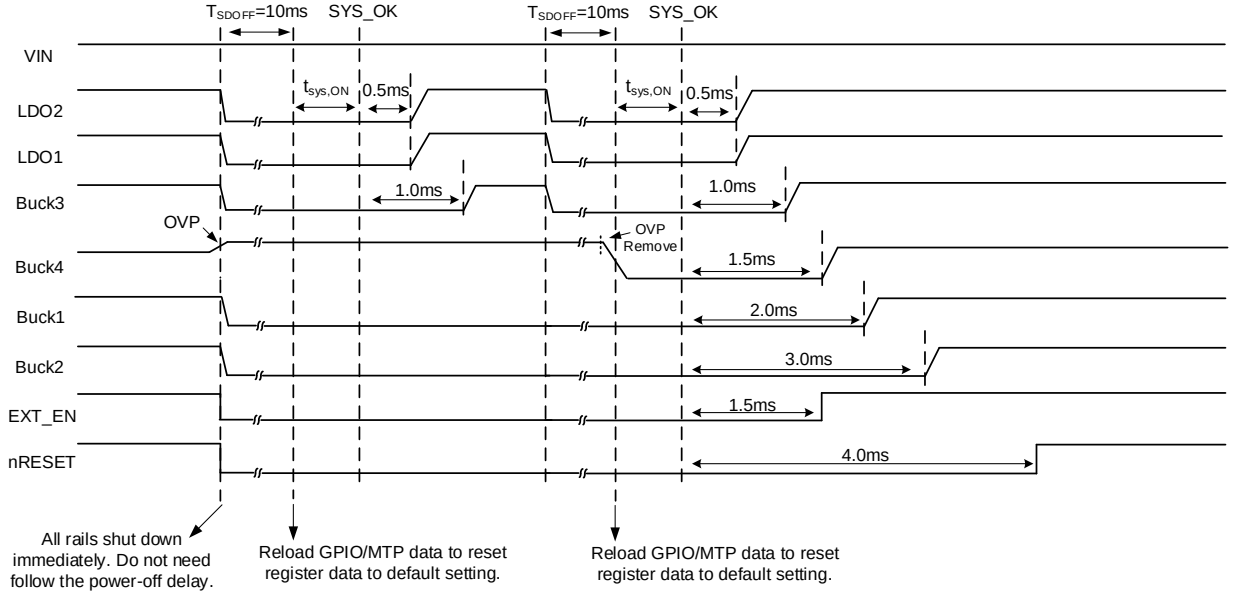


Figure 24. Conceptual of Buck4 Occurring Output Overvoltage Event in Active Mode

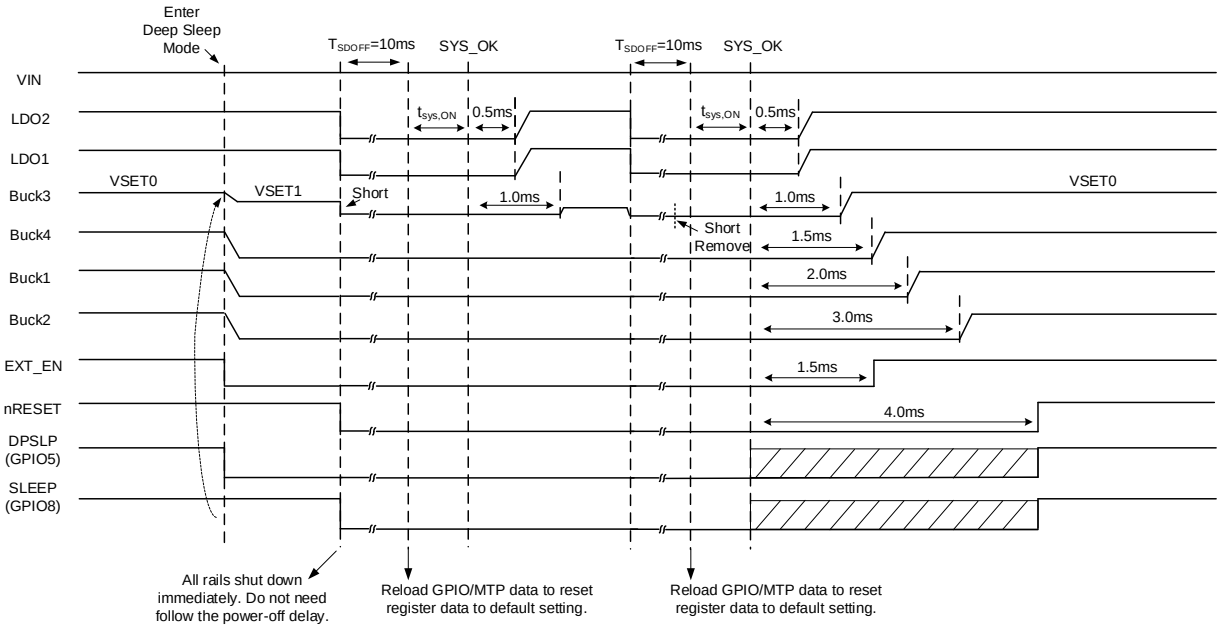


Figure 25. Conceptual of Buck3 Occurring Output Short-Circuit Event in Deep Sleep Mode

Input Overvoltage Protection

The VIN OVP threshold is 3.9V. When VIN exceeds 3.9V, all channels will be turned off. The OVP hysteresis is 0.3V. When VIN decreases to 3.6V, all channels will restart with the power-on sequence.

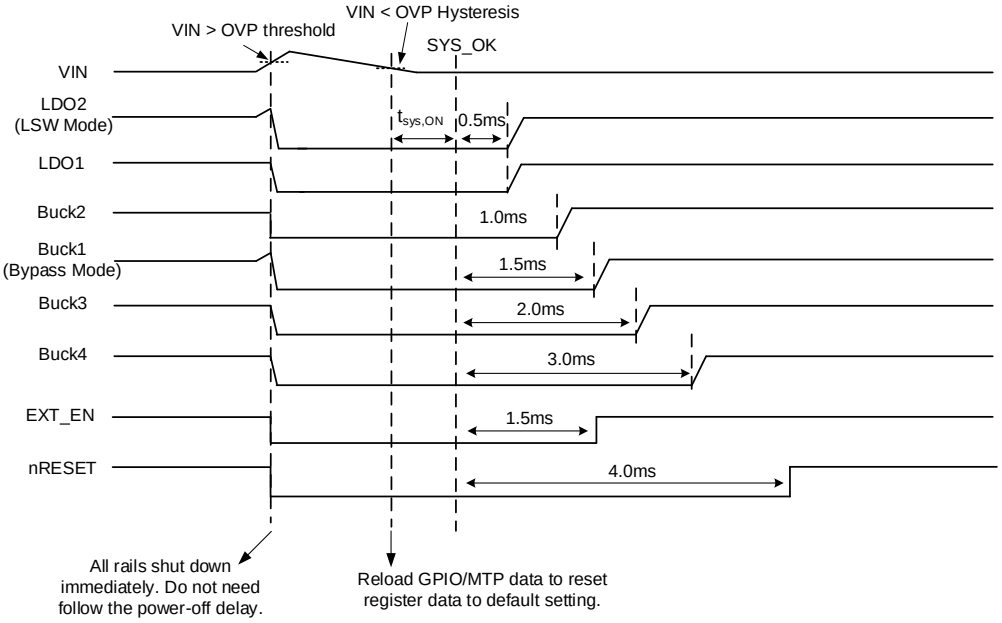


Figure 26. Conceptual of Input Overvoltage Protection Mechanism

Output Current Limit

The buck converter limits the HS switch current and LS switch current during each switching cycle. This reduces the effective duty cycle and causes the output voltage to drop, potentially creating a short circuit condition, and causing the device to turn off all supplies off for 10ms then restart with the power-up sequence.

For LDO, when the output current reaches the current limit threshold, the protection circuit will limit the output current. If the current limit is reached for 200μs or if short-circuit is detected, the device will shut down for 10ms then restart with the power-up sequence.

For load switch (bypass mode) of buck1, when the output current exceeds 4.5A, the protection circuit will limit the current. If the current limit is reached for 200μs, the device will shut down for 10ms then restart with the power-up sequence.

Thermal Shutdown

Thermal shutdown is implemented to prevent damage caused by excessive heat and power dissipation. When the junction temperature exceeds 155°C, the device will shut down at once. When the temperature falls below 140°C the device will automatically restart with the startup sequence using the default configuration.

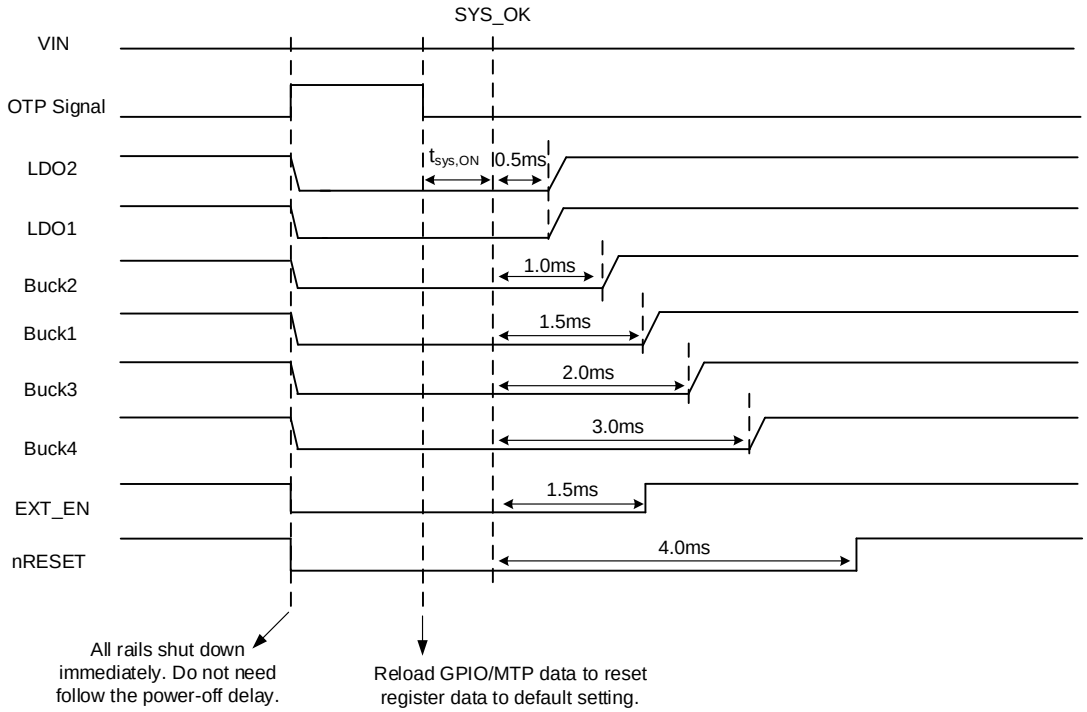


Figure 27. Conceptual of Overtemperature Protection Mechanism

Design Procedure

The following paragraphs provide information on selecting the external components for each of the buck converters, to match the application requirements.

Input Capacitor C_{INX}

For the best performance, select typical X5R or better grade ceramic capacitors with a 6.3V or higher rating, and at least 10µF capacitance. The capacitor should be placed as close as possible to the corresponding pin on the device, while also minimizing the loop area formed by C_{INx} and the IN/GND pins.

When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability, and high RMS current rating over a wide temperature and voltage range.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current. The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{IN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{sw} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at D = 0.5, the

$$V_{IN\_RIPPLE,CAP} = \frac{I_{OUT}}{4 \times f_{sw} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 10µF X5R capacitor is sufficient for each of the buck converters in most applications.

Output Inductor L_X

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{0.4 \times f_{sw} \times I_{OUT,MAX}}$$

Where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY70202K has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{sw} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Use an inductor with DCR less than 20mΩ to achieve good overall efficiency.

Output Capacitor C_{OUTX}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting C_{OUT}. For the best performance, use two X5R or better grade ceramic capacitors with a 10V rating, and capacitance of at least 22µF for each converter output.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed:

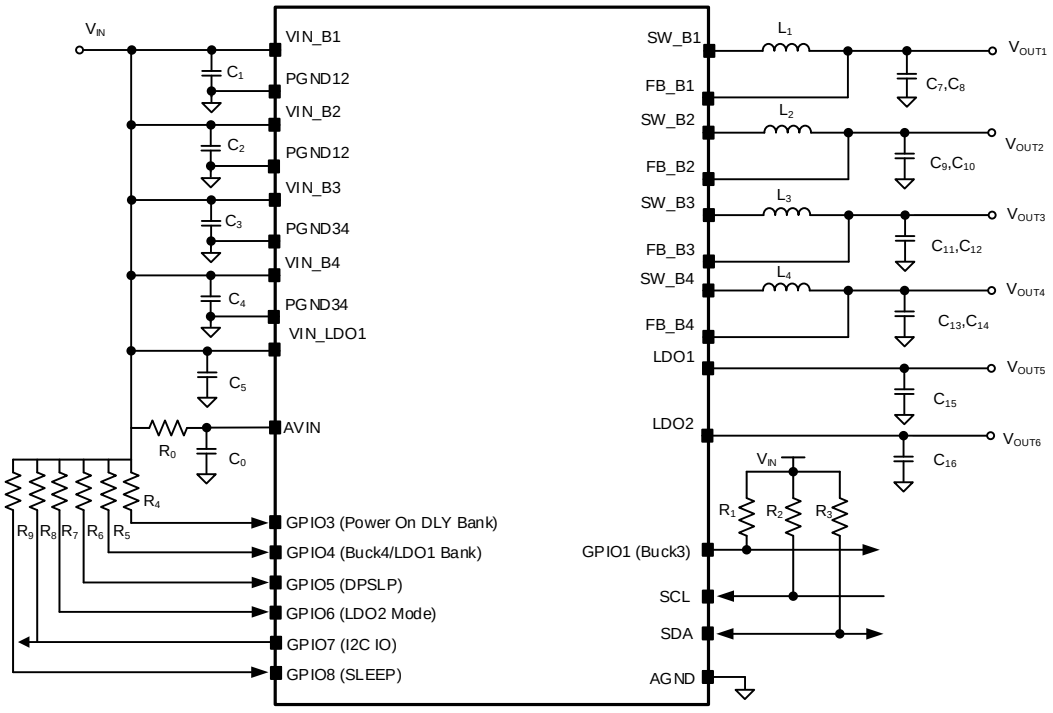
The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔIL) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, consider both.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times f_{sw} \times C_{OUT}} \times ESR$$

The measured capacitive ripple might be higher than the theoretical value because the effective capacitance for ceramic capacitors decreases with the voltage across its terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Application Schematic



BOM List

Reference Designator	Description	Part Number	Manufacturer
U_1	PMIC	SY70202KNSG	Silergy
C_1, C_2, C_3, C_4	10μF/6.3V,0402,X5R	GRM155R60J106ME47D	Murata
C_0, C_5, C_{15}, C_{16}	1μF/6.3V, 0603, X6S	GRM033C80G105MEA2D	Murata
C_7, C_8, C_9, C_{10}, C_{11}, C_{12}, C_{13}, C_{14}	22μF/6.3V, 0603, X5R	GRM186R60J226ME15D	Murata
L_1, L_2, L_3, L_4	0.47μH, 26mΩ, 4A 2016	DFE201612E-R47M	Murata
R_2, R_3	4.7k, 0603		
R_1, R_4, R_5, R_6, R_7, R_8, R_9	100k, 0603		

Layout Design

Follow these PCB layout guidelines for optimal performance:

- Place C_{INX} C_{OUTX} and L as close as possible to the device to improve efficiency and provide better noise immunity.
- Maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance.
- Place the decoupling capacitor of VIN_B1 close to the VIN_B1 and PGND12 pins. Minimize the loop area formed by the input capacitors, input pins, and PGND pins. Apply the same principle of decoupling capacitor placement for all buck converters and LDOs.
- Minimize the PCB copper area associated with the LX pin to improve noise immunity.

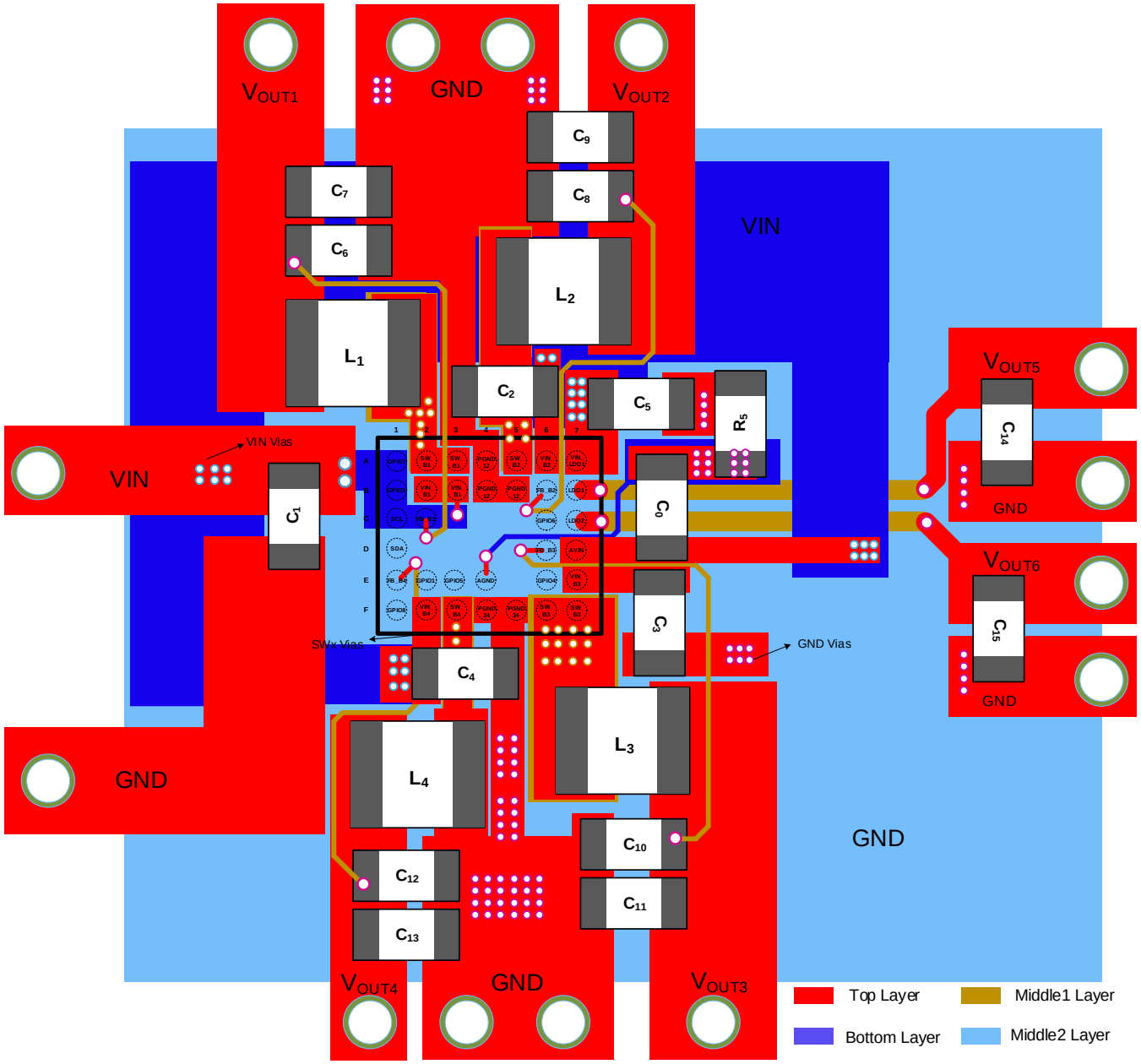


Figure 28. Suggested PCB Layout

I²C Compatible Interface

The SY70202K integrates an I²C compatible interface. To ensure compatibility with a wide range of system processors, the I²C interface supports clock speeds of up to 3.4MHz and uses standard I²C commands. The device always operates as a slave device, and is addressed using a 7-bit slave address followed by an 8th bit, which indicates whether the transaction is a read-operation or a write-operation.

The I²C interface is fully functional after VIN is above UVLO threshold.

I²C Interface Timing Diagram

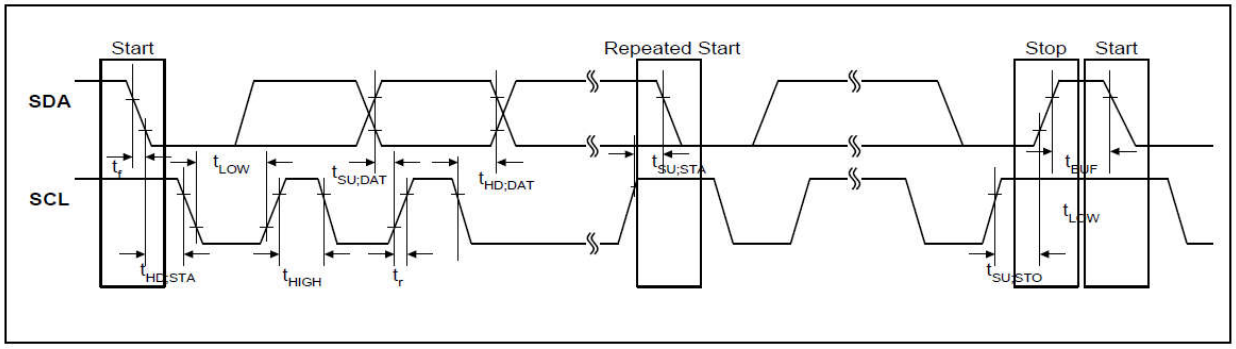


Figure 29. I²C Interface Timing Diagram

I²C EC Table

Characteristics	Symbol	Units	Standard Mode		Fast Mode		High-Speed Mode	
			Min	Max	Min	Max	Min	Max
Vin Voltage	V_{IN}	V	3.3V					
Pull-up Voltage	V_{PU}	V	1.7V to 3.6V					
SCL Clock Frequency	f_{SCL}	Hz	0 to 100k		0 to 400k		0 to 3.4M	
Hold Time (repeated) START Condition.	$t_{HD,STA}$	µs	4	-	0.6	-	0.16	-
LOW Period of the SCL Clock	t_{LOW}	µs	4.7	-	1.3	-	0.16	-
HIGH Period of the SCL Clock	t_{HIGH}	µs	4	-	0.6	-	0.06	-
Set-up Time for a Repeated START Condition	$t_{SU,STA}$	µs	4.7	-	0.6	-	0.16	-
DATA in Hold Time	$t_{HD;DI}$	ns	0	900	0	900	0	70
DATA out Hold Time	$t_{HD;DO}$	ns		900		900		70
Data Set-up Time	$t_{SU;DAT}$	ns	250	-	100	-	10	-
Rise Time of both SDA and SCL Signals	t_r	ns	-	1000	5	300	5	40
Fall Time Of Both SDA And SCL Signals	t_f	ns	-	300	5	300	5	40
Set-up Time for STOP Condition	$t_{SU;STO}$	µs	4	-	0.6	-	0.16	1
Bus Free Time between STOP and	t_{BUF}	µs	4.7	-	1.3	-	-	-

START Conditions								
Capacitive Load for Each Bus Line	C_b	pF	-	400	-	400	-	100
Low Level Input Voltage	V_{IL}	V	-	0.4	-	0.4	-	0.4
High Level Input Voltage	V_{IH}	V	1.4	-	1.4	-	1.4	-

I²C Device Address

When communicating with multiple devices using the I²C interface, each device must have its own unique address so the host can distinguish between the devices. The PMIC slave address is <0100101x> where 'x' is the read/write control bit.

START and STOP Conditions

The START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition. The I²C master always generates the START and STOP conditions.

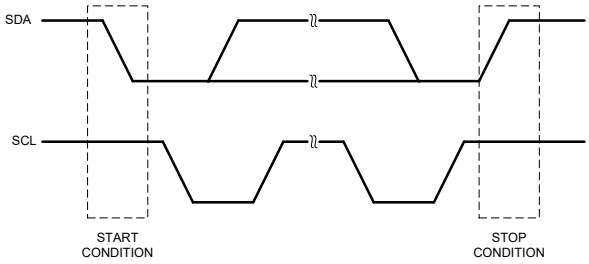


Figure 30. Start and Stop Conditions

Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

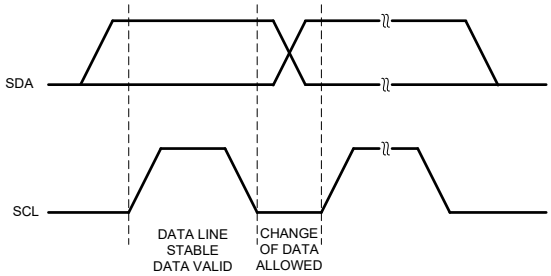


Figure 31. Data Validity

Acknowledge

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the master sends 7-slave address bits and an R/$\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.

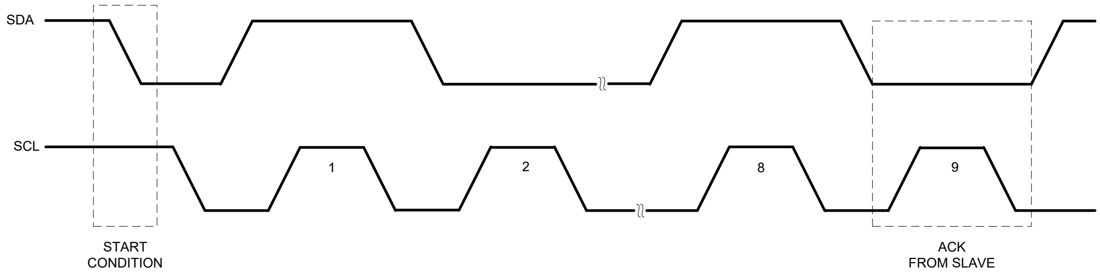


Figure 32. I²C Acknowledge

PMIC I²C Protocol

<table>
<tr><td rowspan="2">Write operation</td><td rowspan="2">Start</td><td colspan="7">Device address</td><td>R/W</td><td>ACK</td><td>Byte address</td><td>ACK</td><td rowspan="2" colspan="11">N-bytes DATA</td><td>ACK</td><td rowspan="2">STOP</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>N-bytes address</td><td>0</td><td>0</td></tr>
<tr><td rowspan="2">Read operation</td><td rowspan="2">Start</td><td colspan="7">Device address</td><td>R/W</td><td>ACK</td><td>Byte address</td><td>ACK</td><td rowspan="2">Repeated Start</td><td colspan="7">Device address</td><td>R/W</td><td>ACK</td><td rowspan="2">N-bytes DATA</td><td>ACK</td><td rowspan="2">STOP</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>N-bytes address</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td></tr>
</table>

- Data is written from the address that mentioned in the second byte as much as following N-bytes.

(ACK is occurred every 1-bytes)

- Data is read from the address that mentioned in the second byte to N-bytes address.

(ACK is occurred every 1-bytes)

Register Address Map

Address	D7	D6	D5	D4	D3	D2	D1	D0
0x00h	x	B1_Mode	B1_VSET					
0x01h	x	B2_VSET						
0x02h	x	B3_VSET0						
0x03h	x	B3_VSET1						
0x04h	x	LDO_OVP	B4_Add	B4_VSET				
0x05h	x	LDO1_ Mode	LDO1_VSET					
0x06h	x	x	LDO2_VSET					
0x07h	x	x	LDO2_CH _EN	LDO1_CH _EN	Buck4_CH _EN	Buck3_CH _EN	Buck2_CH _EN	Buck1_CH _EN
0x08h	B3_VID@SL EEP_EN	EXT_EN_ SLEEP_EN	LDO2_ SLEEP_ EN	LDO1_ SLEEP_ EN	Buck4_ SLEEP_ EN	Buck3_ SLEEP_ EN	Buck2_ SLEEP_ EN	Buck1_ SLEEP_ EN
0x09h	x	EXT_EN_ DPSLP_EN	LDO2_ DPSLP_ EN	LDO1_ DPSLP_ EN	Buck4_ DPSLP_ EN	Buck3_ DPSLP_ EN	Buck2_ DPSLP_ EN	Buck1_ DPSLP_ EN
0x0Ah	x	x	x	x	B4_PWM_ EN	B3_PWM_ EN	B2_PWM_ EN	B1_PWM_ EN
0x0Bh	x	x	LDO2_ SST	LDO1_ SST	B4_SST	B3_SST	B2_SST	B1_SST
0x0Ch	Buck1_Power OFF_ DLY		Buck2_Power OFF_ DLY		Buck3_Power OFF_ DLY		Buck4_Power OFF_ DLY	
0x0Dh	LDO1_Power OFF_ DLY		LDO2_Power OFF_ DLY		EXT_EN_Power OFF_ DLY		nRESET_Power OFF_ DLY	
0x0Eh	Buck1_Wake Up_ DLY		Buck2_Wake Up_ DLY		Buck3_Wake Up_ DLY		Buck4_Wake Up_ DLY	
0x0Fh	x	x	LDO1_Wake Up_ DLY		LDO2_Wake Up_ DLY		EXT_EN_Wake Up_ DLY	
0x10h	DIS_OVUV	DIS_OTP	DIS_ VINOVP	x	x	x	SLEEP_ EN	DPSLP_ EN
0x11h	B1_Power ON_DLY				B2_Power ON_DLY			
0x12h	B3_Power ON_DLY				B4_Power ON_DLY			
0x13h	LDO1_Power ON_DLY				LDO2_Power ON_DLY			
0x14h	nRESET_ Input Trigger	nRESET_Power ON_DLY			EXT_EN_ Power ON_ DLY			
0x15h	GPIO5 function		GPIO7 function		x	GPIO6 Lock	GPIO5 Open drain	GPIO7 Open drain
0x34h	x	x	x	Vendor ID	CMI Version			

Fault Register Map

Address	D7	D6	D5	D4	D3	D2	D1	D0
0x16h	TSP	VIN_ OVP	x	x	Buck4_ OVP	Buck3_ OVP	Buck2_ OVP	Buck1_ OVP
0x17h	x	SYSWARN	LDO2_ UVP(SCP)	LDO1_ UVP(SCP)	Buck4_ UVP(SCP)	Buck3_ UVP(SCP)	Buck2_ UVP(SCP)	Buck1_ UVP(SCP)

Note: The fault bit is latched status bit and keep asserted until read by I^2C.

Register Address Map

Address	Register	Default	EEPROM Bit	Range	Resolution
0x00h	B1_Mode [6]	Buck/00h	1bit	0 – Buck1 operating on Buck mode 1 – Buck1 operating on Bypass mode	-
	B1_VSET [5:0]	2.5V/24h	6bits	Buck1 output range is 1.6V-3.0V	25mV
0x01h	B2_VSET [6:0]	1.2V/2Dh	7bits	Buck2 output range is 0.75V-1.85V	10mV

Address	Register	Default GPIO1 =High	Default GPIO1 =Floating	Default GPIO1 =Low	EEPROM Bit	Range	Resolution
0x02h	B3_VSET0 [6:0]	0.8V/1Eh	0.75V/19h	0.75V/19h	7bits	Buck3 output range is 0.5V-1.2V	10mV
0x03h	B3_VSET1 [6:0]	0.7V/14h	0.65V/0Fh	0.65V/0Fh	7bits	Buck3 output range is 0.5V-1.2V	10mV

Address	Register	Default GPIO3 =High	Default GPIO3 =Floating	Default GPIO3 =Low	EEPROM Bit	Range	Resolution
0x11h	B1_Power ON_ DLY [7:4]	3.0ms/06h	2.0ms/04h	2.0ms/04h	4bits	0000: 0ms, 0001: 0.5ms, 1110: 7.0ms, 1111: 7.5ms	0.5ms
	B2_Power ON_ DLY [3:0]	2.0ms/04h	3.0ms/06h	3.0ms/06h	4bits	0000: 0ms, 0001: 0.5ms, 1110: 7.0ms, 1111: 7.5ms	0.5ms
0x12h	B3_Power ON_ DLY [7:4]	1.0ms/02h	1.0ms/02h	1.0ms/02h	4bits	0000: 0ms, 0001: 0.5ms, 1110: 7.0ms, 1111: 7.5ms	0.5ms
	B4_Power ON_ DLY [3:0]	1.5ms/03h	1.5ms/03h	1.5ms/03h	4bits	0000: 0ms, 0001: 0.5ms, 1110: 7.0ms, 1111: 7.5ms	0.5ms
0x13h	LDO1_Power ON_ DLY [7:4]	0.5ms/01h	0.5ms/01h	0.5ms/01h	4bits	0000: 0ms, 0001: 0.5ms, 1110: 7.0ms, 1111: 7.5ms	0.5ms
	LDO2_Power ON_ DLY [3:0]	0.5ms/01h	0.5ms/01h	0.5ms/01h	4bits	0000: 0ms, 0001: 0.5ms, 1110: 7.0ms, 1111: 7.5ms	0.5ms
0x14h	nRESET_ Input Trigger [7]	SYS_OK /01h	SYS_OK /01h	SYS_OK /01h	1bit	0: Buck2_PG 1: SYS_OK	-
	nRESET_ Power ON_ DLY [6:4]	4.0ms/03h	4.0ms/03h	4.0ms/03h	3bits	000: 0.5ms, 001: 1.0ms, 010: 2.0ms, 011: 4.0ms, 100: 8.0ms, 101: 16.0ms	-
	EXT_EN_ Power ON_ DLY [3:0]	1.5ms/03h	1.5ms/03h	1.5ms/03h	4bits	0000: 0ms, 0001: 0.5ms, 1110: 7.0ms, 1111: 7.5ms	0.5ms

Address	Register	Default GPIO4 =High	Default GPIO4 =Floating	Default GPIO4 =Low	EEPROM Bit	Range	Resolution
0x04h	LDO_OVP [6]	OVP_off/ 00h	OVP_off/ 00h	OVP_off/ 00h	1bit	0 –LDO1&LDO2 OVP discharge function off 1 –LDO1&LDO2 OVP discharge function on	-
	B4_Add[5]	0mV/00h	0mV /00h	0mV /00h	1bit	0 – Buck4 output default voltage 1 – Buck4 output voltage add 20mV	-

	B4_VSET [4:0]	0.907V/02h	0.907V/02h	0.907V/02h	5bits	Buck4 output range is 0.8V-1.9V	50mV
0x05h	LDO1_Mode [6]	LDO/00h	PLSW/01h	PLSW/01h	1bit	00h: LDO Mode, 01h: PLSW Mode,	-
	LDO1_VSET [5:0]	1.8V/10h	V_{IN}	V_{IN}	6bits	LDO1 output range is 1.0V-2.7V	50mV

Address	Register	Default	EEPROM Bit	Range	Resolution
0x06h	LDO2_VSET [5:0]	1.8V/10h	6bits	LDO2 output range is 1.0V-2.7V	50mV
0x07h	LDO2_CH_EN[5]	Enable/01h	1bit	0 – LDO2 Disable 1 – LDO2 Enable.	-
	LDO1_CH_EN[4]	Enable/01h	1bit	0 – LDO1 Disable, 1 – LDO1 Enable.	-
	Buck4_CH_EN[3]	Enable/01h	1bit	0 – Buck4 Disable, 1 –Buck4 Enable.	-
	Buck3_CH_EN[2]	Enable/01h	1bit	0 –Buck3 Disable, 1 –Buck3 Enable.	-
	Buck2_CH_EN[1]	Enable/01h	1bit	0 –Buck2 Disable, 1 –Buck2 Enable.	-
	Buck1_CH_EN[0]	Enable/01h	1bit	0 –Buck1 Disable, 1 –Buck1 Enable.	-
0x08h	B3_VID@SLEEP_ EN [7]	Enable/01h	1bit	0 – Buck3 disable VID function; Buck3 output keep VSET1 when the IC enters Sleep mode 1 – Buck3 enable VID function; Buck3 output change to VSET1 when the IC enters Sleep mode	-
	EXT_EN_SLEEP_ EN [6]	Stays on/00h	1bit	0 – EXT_EN stays on when the IC enters Sleep mode 1 – EXT_EN turns off when the IC enters Sleep mode	-
	LDO2_SLEEP_ EN [5]	Stays on/00h	1bit	0 – LDO2 stays on when the IC enters Sleep mode 1 – LDO2 turns off when the IC enters Sleep mode	-
	LDO1_SLEEP_ EN [4]	Stays on/00h	1bit	0 – LDO1 stays on when the IC enters Sleep mode 1 – LDO1 turns off when the IC enters Sleep mode	-
	Buck4_SLEEP_ EN [3]	Stays on/00h	1bit	0 – Buck4 stays on when the IC enters Sleep mode 1 – Buck4 turns off when the IC enters Sleep mode	-
	Buck3_SLEEP_ EN [2]	Stays on/00h	1bit	0 – Buck3 stays on when the IC enters Sleep mode 1 – Buck3 turns off when the IC enters Sleep mode	-
	Buck2_SLEEP_ EN [1]	Turns off/01h	1bit	0 – Buck2 stays on when the IC enters Sleep mode 1 – Buck2 turns off when the IC enters Sleep mode	-
	Buck1_SLEEP_ EN [0]	Turns off/01h	1bit	0 – Buck1 stays on when the IC enters Sleep mode 1 – Buck1 turns off when the IC enters Sleep mode	-

Address	Register	Default	EEPROM Bit	Range	Resolution
0x09h	EXT_EN_ DPSLP_EN [6]	Stays on/00h	1bit	0 – EXT_EN stays on when the IC enters Deep Sleep mode 1 – EXT_EN turns off when the IC enters Deep Sleep mode	-
	LDO2_ DPSLP_ EN [5]	Stays on/00h	1bit	0 – LDO2 stays on when the IC enters Deep Sleep mode 1 – LDO2 turns off when the IC enters Deep Sleep mode	-
	LDO1_ DPSLP_ EN [4]	Stays on/00h	1bit	0 – LDO1 stays on when the IC enters Deep Sleep mode 1 – LDO1 turns off when the IC enters Deep Sleep mode	-
	Buck4_ DPSLP_ EN [3]	Turns off/01h	1bit	0 – Buck4 stays on when the IC enters Deep Sleep mode	-

				1 – Buck4 turns off when the IC enters Deep Sleep mode	
	Buck3_ DPSLP_ EN [2]	Stays on/00h	1bit	0 – Buck3 stays on when the IC enters Deep Sleep mode 1 – Buck3 turns off when the IC enters Deep Sleep mode	-
	Buck2_ DPSLP_ EN [1]	Stays on/00h	1bit	0 – Buck2 stays on when the IC enters Deep Sleep mode 1 – Buck2 turns off when the IC enters Deep Sleep mode	-
	Buck1_ DPSLP_ EN [0]	Stays on/00h	1bit	0 – Buck1 stays on when the IC enters Deep Sleep mode 1 – Buck1 turns off when the IC enters Deep Sleep mode	-
0x0Ah	B4_PWM_EN [3]	LPM/00h	1bit	0 – Buck4 enters LPM at light load 1 – Buck4 forced into PWM at light load	-
	B3_PWM_EN [2]	LPM/00h	1bit	0 – Buck3 enters LPM at light load 1 – Buck3 forced into PWM at light load	-
	B2_PWM_EN [1]	LPM/00h	1bit	0 – Buck2 enters LPM at light load 1 – Buck2 forced into PWM at light load	-
	B1_PWM_EN [0]	LPM/00h	1bit	0 – Buck1 enters LPM at light load 1 – Buck1 forced into PWM at light load	-
0x0Bh	LDO2_SST [5]	200μs/00h	1bit	0 – LDO2 SST=200μs 1 – LDO2 SST=360μs	160μs
	LDO1_SST [4]	200μs/00h	1bit	0 – LDO1 SST=200μs 1 – LDO1 SST=360μs	160μs
	B4_SST [3]	150μs/00h	1bit	0 – Buck4 SST=150μs 1 – Buck4 SST larger and not recommended	150μs
	B3_SST [2]	250μs/00h	1bit	0 – Buck3 SST=250μs 1 – Buck3 SST=500μs	250μs
	B2_SST [1]	250μs/00h	1bit	0 – Buck2 SST=250μs 1 – Buck2 SST=500μs	250μs
	B1_SST [0]	250μs/00h	1bit	0 – Buck1 SST=250μs 1 – Buck1 SST=500μs	250μs

Address	Register	Default	EEPROM Bit	Range	Resolution
0x0Ch	Buck1_Power OFF_ DLY [7:6]	0ms/00h	2bits	00: 0ms, 01: 0.25ms, 10: 0.5ms, 11: 1.0ms	-
	Buck2_Power OFF_ DLY [5:4]	0ms/00h	2bits	00: 0ms, 01: 0.25ms, 10: 0.5ms, 11: 1.0ms	-
	Buck3_Power OFF_ DLY [3:2]	1.0ms/03h	2bits	00: 0ms, 01: 0.25ms, 10: 0.5ms, 11: 1.0ms	-
	Buck4_Power OFF_ DLY [1:0]	0ms/00h	2bits	00: 0ms, 01: 0.25ms, 10: 0.5ms, 11: 1.0ms	-
0x0Dh	LDO1_Power OFF_ DLY [7:6]	1.0ms/03h	2bits	00: 0ms, 01: 0.25ms, 10: 0.5ms, 11: 1.0ms	-
	LDO2_Power OFF_ DLY [5:4]	1.0ms/03h	2bits	00: 0ms, 01: 0.25ms, 10: 0.5ms, 11: 1.0ms	-
	EXT_EN _ Power OFF_ DLY [3:2]	0ms/00h	2bits	00: 0ms, 01: 0.25ms, 10: 0.5ms, 11: 1.0ms	-
	nRESET _ Power OFF_ DLY [1:0]	0ms/00h	2bits	00: 0ms, 01: 0.25ms, 10: 0.5ms, 11: 1.0ms	-
0x0Eh	Buck1Wake Up_ DLY [7:6]	1ms/01h	2bits	00:0ms, 01:1ms, 10:2ms, 11:3ms	1ms
	Buck2_Wake Up_ DLY [5:4]	2ms/02h	2bits	00:0ms, 01:1ms, 10:2ms, 11:3ms	1ms
	Buck3_Wake Up_	0ms/00h	2bits	00:0ms, 01:1ms, 10:2ms, 11:3ms	1ms

	DLY [3:2]				
	Buck4_Wake Up_ DLY [1:0]	0ms/00h	2bits	00:0ms, 01:1ms, 10:2ms, 11:3ms	1ms
0x0Fh	LDO1_Wake Up_ DLY [5:4]	0ms/00h	2bits	00:0ms, 01:1ms, 10:2ms, 11:3ms	1ms
	LDO2_Wake Up_ DLY [3:2]	0ms/00h	2bits	00:0ms, 01:1ms, 10:2ms, 11:3ms	1ms
	EXT_EN_ Wake Up_ DLY [1:0]	0ms/00h	2bits	00:0ms, 01:1ms, 10:2ms, 11:3ms	1ms
0x10h	DIS_OVUV [7]	Enable/00h	1bit	0 – Enable hiccup mode or OVUVFLT state in ACTIVE Mode 1 – Disable hiccup mode or OVUVFLT state in ACTIVE Mode (LDO1&2 OVP function is independent)	-
	DIS_OTP [6]	Enable/00h	1bit	0 – Enable OTP 1 – Disable OTP	-
	DIS_VINOVP [5]	Enable/00h	1bit	0 – Enable VINOVP 1 – Disable VINOVP	-
	SLEEP_EN [1]	Enable/01h	1bit	0 – SLEEP Mode is disabled 1 – SLEEP Mode is enabled	-
	DPSLP_EN [0]	Enable/01h	1bit	0 – DPSLP Mode is disabled 1 – DPSLP Mode is enabled	-

Address	Register	Default	EEPROM Bit	Range	Resolution
0x15h	GPIO5 Function [7:6]	DPSLP/00h	2bits	00: DPSLP Input. 01: I²C Controlled Output. 10: nIRQ(SYSWARN) Output	-
	GPIO7 Function [5:4]	I2C Control Output/01h	2bits	00: EXT_EN Output. 01: I²C Controlled Output. 10: PWRDIS Input	-
	GPIO6 Lock [2]	Lock/01h	1bit	0-GPIO6 status not lock and LDO2 mode can be changed when GPIO6 status change after power on (Not recommended due to trigger protection). 1-GPIO6 status lock and LDO mode will not change with GPIO6 status after power on.	
	GPIO5 Open drain [1]	Turn off/00h	1bit	0 – Open drain turn off 1 – Open drain turn on	-
	GPIO7 Open drain [0]	Turn off/00h	1bit	0 – Open drain turn off 1 – Open drain turn on	-
0x34h	Vendor ID [4]	Silergy/01h	1bit	01h	-
	CMI Version [3:0]	01h	4bits	01h	-

Fault Flag

Address	Register	Default	EEPROM Bit	Range	Resolution
0x16h	TSP [7]	Normal/00h	1bit	Thermal shutdown protection indicator. 0: Normal (default) 1: Fault	-
	VIN_OVP [6]	Normal/00h	1bit	Input over voltage protection indicator 0: Normal (default) 1: Fault	-
	Buck4_OVP [3]	Normal/00h	1bit	Buck4 over voltage protection indicator 0: Normal (default) 1: Fault	-
	Buck3_OVP [2]	Normal/00h	1bit	Buck3 over voltage protection indicator 0: Normal (default) 1: Fault	-

	Buck2_OVP [1]	Normal/00h	1bit	Buck2 over voltage protection indicator 0: Normal (default) 1: Fault	-
	Buck1_OVP [0]	Normal/00h	1bit	Buck1 over voltage protection indicator 0: Normal (default) 1: Fault	-
0x17h	SYSWARN [6]	Normal/00h	1bit	SYSWARN indicator 0: Normal (default) 1: Fault	-
	LDO2_UVP(SCP) [5]	Normal/00h	1bit	LDO2 over load protection indicator 0: Normal (default) 1: Fault	-
	LDO1_UVP(SCP) [4]	Normal/00h	1bit	LDO1 over load protection indicator 0: Normal (default) 1: Fault	-
	Buck4_UVP(SCP) [3]	Normal/00h	1bit	Buck4 over load protection indicator 0: Normal (default) 1: Fault	-
	Buck3_UVP(SCP) [2]	Normal/00h	1bit	Buck3 over load protection indicator 0: Normal (default) 1: Fault	-
	Buck2_UVP(SCP) [1]	Normal/00h	1bit	Buck2 over load protection indicator 0: Normal (default) 1: Fault	-
	Buck1_UVP(SCP) [0]	Normal/00h	1bit	Buck1 over load protection indicator 0: Normal (default) 1: Fault	-

Buck1 Output Voltage Adjustment

Address – 0x00h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	B1_Mode	B1_VSET					
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck1 Operating Mode B1_Mode[6]

Code	Buck1 Mode
00h	Buck1 operating on Buck mode
01h	Buck1 operating on Bypass mode

Set Buck1 Output Voltage VSET [5:0]

The output voltage is equal to B1_VSET*0.025+1.6V.

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
00h	1.6V	10h	2V	20h	2.4V	30h	2.8V
01h	1.625V	11h	2.025V	21h	2.425V	31h	2.825V
02h	1.65V	12h	2.05V	22h	2.45V	32h	2.85V
03h	1.675V	13h	2.075V	23h	2.475V	33h	2.875V
04h	1.7V	14h	2.1V	24h	2.5V	34h	2.9V
05h	1.725V	15h	2.125V	25h	2.525V	35h	2.925V
06h	1.75V	16h	2.15V	26h	2.55V	36h	2.95V
07h	1.775V	17h	2.175V	27h	2.575V	37h	2.975V
08h	1.8V	18h	2.2V	28h	2.6V	38h	3V
09h	1.825V	19h	2.225V	29h	2.625V		
0Ah	1.85V	1Ah	2.25V	2Ah	2.65V		
0Bh	1.875V	1Bh	2.275V	2Bh	2.675V		
0Ch	1.9V	1Ch	2.3V	2Ch	2.7V		
0Dh	1.925V	1Dh	2.325V	2Dh	2.725V		
0Eh	1.95V	1Eh	2.35V	2Eh	2.75V		
0Fh	1.975V	1Fh	2.375V	2Fh	2.775V		

Buck2 Output Voltage Adjustment

Address – 0x01h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	B2_VSET						
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

The output voltage is equal to B2_VSET*0.01+0.75V

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
00h	0.75V	20h	1.07V	40h	1.39V	60h	1.71V
01h	0.76V	21h	1.08V	41h	1.4V	61h	1.72V
02h	0.77V	22h	1.09V	42h	1.41V	62h	1.73V
03h	0.78V	23h	1.1V	43h	1.42V	63h	1.74V
04h	0.79V	24h	1.11V	44h	1.43V	64h	1.75V
05h	0.8V	25h	1.12V	45h	1.44V	65h	1.76V
06h	0.81V	26h	1.13V	46h	1.45V	66h	1.77V
07h	0.82V	27h	1.14V	47h	1.46V	67h	1.78V
08h	0.83V	28h	1.15V	48h	1.47V	68h	1.79V
09h	0.84V	29h	1.16V	49h	1.48V	69h	1.8V
0Ah	0.85V	2Ah	1.17V	4Ah	1.49V	6Ah	1.81V
0Bh	0.86V	2Bh	1.18V	4Bh	1.5V	6Bh	1.82V
0Ch	0.87V	2Ch	1.19V	4Ch	1.51V	6Ch	1.83V
0Dh	0.88V	2Dh	1.2V	4Dh	1.52V	6Dh	1.84V
0Eh	0.89V	2Eh	1.21V	4Eh	1.53V	6Eh	1.85V
0Fh	0.9V	2Fh	1.22V	4Fh	1.54V		
10h	0.91V	30h	1.23V	50h	1.55V		
11h	0.92V	31h	1.24V	51h	1.56V		
12h	0.93V	32h	1.25V	52h	1.57V		
13h	0.94V	33h	1.26V	53h	1.58V		
14h	0.95V	34h	1.27V	54h	1.59V		
15h	0.96V	35h	1.28V	55h	1.6V		
16h	0.97V	36h	1.29V	56h	1.61V		
17h	0.98V	37h	1.3V	57h	1.62V		
18h	0.99V	38h	1.31V	58h	1.63V		
19h	1V	39h	1.32V	59h	1.64V		
1Ah	1.01V	3Ah	1.33V	5Ah	1.65V		
1Bh	1.02V	3Bh	1.34V	5Bh	1.66V		
1Ch	1.03V	3Ch	1.35V	5Ch	1.67V		
1Dh	1.04V	3Dh	1.36V	5Dh	1.68V		
1Eh	1.05V	3Eh	1.37V	5Eh	1.69V		
1Fh	1.06V	3Fh	1.38V	5Fh	1.70V		

Buck3 Output Voltage Adjustment

Address – 0x02h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	B3_VSET0						
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

The output voltage is equal to B3_VSET*0.01+0.5V

Code	Voltage	Code	Voltage	Code	Voltage
00h	0.50V	20h	0.82V	40h	1.14V
01h	0.51V	21h	0.83V	41h	1.15V
02h	0.52V	22h	0.84V	42h	1.16V
03h	0.53V	23h	0.85V	43h	1.17V
04h	0.54V	24h	0.86V	44h	1.18V
05h	0.55V	25h	0.87V	45h	1.19V
06h	0.56V	26h	0.88V	46h	1.20V
07h	0.57V	27h	0.89V		
08h	0.58V	28h	0.90V		
09h	0.59V	29h	0.91V		
0Ah	0.60V	2Ah	0.92V		
0Bh	0.61V	2Bh	0.93V		
0Ch	0.62V	2Ch	0.94V		
0Dh	0.63V	2Dh	0.95V		
0Eh	0.64V	2Eh	0.96V		
0Fh	0.65V	2Fh	0.97V		
10h	0.66V	30h	0.98V		
11h	0.67V	31h	0.99V		
12h	0.68V	32h	1.00V		
13h	0.69V	33h	1.01V		
14h	0.70V	34h	1.02V		
15h	0.71V	35h	1.03V		
16h	0.72V	36h	1.04V		
17h	0.73V	37h	1.05V		
18h	0.74V	38h	1.06V		
19h	0.75V	39h	1.07V		
1Ah	0.76V	3Ah	1.08V		
1Bh	0.77V	3Bh	1.09V		
1Ch	0.78V	3Ch	1.10V		
1Dh	0.79V	3Dh	1.11V		
1Eh	0.80V	3Eh	1.12V		
1Fh	0.81V	3Fh	1.13V		

Buck3 Output Voltage Adjustment

Address – 0x03h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	B3_VSET1						
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

The output voltage is equal to B3_VSET*0.01+0.5V

Code	Voltage	Code	Voltage	Code	Voltage
00h	0.50V	20h	0.82V	40h	1.14V
01h	0.51V	21h	0.83V	41h	1.15V
02h	0.52V	22h	0.84V	42h	1.16V
03h	0.53V	23h	0.85V	43h	1.17V
04h	0.54V	24h	0.86V	44h	1.18V
05h	0.55V	25h	0.87V	45h	1.19V
06h	0.56V	26h	0.88V	46h	1.20V
07h	0.57V	27h	0.89V		
08h	0.58V	28h	0.90V		
09h	0.59V	29h	0.91V		
0Ah	0.60V	2Ah	0.92V		
0Bh	0.61V	2Bh	0.93V		
0Ch	0.62V	2Ch	0.94V		
0Dh	0.63V	2Dh	0.95V		
0Eh	0.64V	2Eh	0.96V		
0Fh	0.65V	2Fh	0.97V		
10h	0.66V	30h	0.98V		
11h	0.67V	31h	0.99V		
12h	0.68V	32h	1.00V		
13h	0.69V	33h	1.01V		
14h	0.70V	34h	1.02V		
15h	0.71V	35h	1.03V		
16h	0.72V	36h	1.04V		
17h	0.73V	37h	1.05V		
18h	0.74V	38h	1.06V		
19h	0.75V	39h	1.07V		
1Ah	0.76V	3Ah	1.08V		
1Bh	0.77V	3Bh	1.09V		
1Ch	0.78V	3Ch	1.10V		
1Dh	0.79V	3Dh	1.11V		
1Eh	0.80V	3Eh	1.12V		
1Fh	0.81V	3Fh	1.13V		

Buck4 Output Voltage Adjustment

Address – 0x04h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	LDO_OVP	B4_Add	B4_VSET				
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set DDR SEL[6]

Code	LDO_OVP
00h	LDO1 & LDO2 over voltage discharge function disable
01h	LDO1 & LDO2 over voltage discharge function enable

Set Buck4 Operating Mode B4_Mode[5]

Code	Buck4_Add
00h	Buck4 voltage keep B4_VSET
01h	Buck4 output voltage increase 20mV

Set Buck4 Output Voltage VSET [4:0]

The output voltage is equal to B4_VSET*0.05+0.907V

Code	Voltage	Code	Voltage	Code	Voltage
00h	0.807V	08h	1.207V	10h	1.607V
01h	0.857V	09h	1.257V	11h	1.657V
02h	0.907V	0Ah	1.307V	12h	1.707V
03h	0.957V	0Bh	1.357V	13h	1.757V
04h	1.007V	0Ch	1.407V	14h	1.807V
05h	1.057V	0Dh	1.457V	15h	1.857V
06h	1.107V	0Eh	1.507V	16h	1.907V
07h	1.157V	0Fh	1.557V		

LDO1 Output Voltage Adjustment

Address – 0x05h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	LDO1_Mode	LDO1_VSET					
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO1 Mode [6]

Code	LDO1 Mode
00h	LDO1 operating on LDO mode
01h	LDO1 operating on PLSW mode

Set LDO Output Voltage VSET [5:0]

The output voltage is equal to LDO1_VSET*0.05+1.0V

Code	Voltage	Code	Voltage	Code	Voltage
00h	1.00V	10h	1.80V	20h	2.60V
01h	1.05V	11h	1.85V	21h	2.65V
02h	1.10V	12h	1.90V	22h	2.70V
03h	1.15V	13h	1.95V		
04h	1.20V	14h	2.00V		
05h	1.25V	15h	2.05V		
06h	1.30V	16h	2.10V		
07h	1.35V	17h	2.15V		
08h	1.40V	18h	2.20V		
09h	1.45V	19h	2.25V		
0Ah	1.50V	1Ah	2.30V		
0Bh	1.55V	1Bh	2.35V		
0Ch	1.60V	1Ch	2.40V		
0Dh	1.65V	1Dh	2.45V		
0Eh	1.70V	1Eh	2.50V		
0Fh	1.75V	1Fh	2.55V		

LDO2 Output Voltage Adjustment

Address – 0x06h

DATA BIT	D7	D7	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	RFU	LDO2_VSET					
READ/WRITE	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO Output Voltage VSET [5:0]

The output voltage is equal to LDO2_VSET*0.05+1.0V

Code	Voltage	Code	Voltage	Code	Voltage
00h	1.00V	10h	1.80V	20h	2.60V
01h	1.05V	11h	1.85V	21h	2.65V
02h	1.10V	12h	1.90V	22h	2.70V
03h	1.15V	13h	1.95V		
04h	1.20V	14h	2.00V		
05h	1.25V	15h	2.05V		
06h	1.30V	16h	2.10V		
07h	1.35V	17h	2.15V		
08h	1.40V	18h	2.20V		
09h	1.45V	19h	2.25V		
0Ah	1.50V	1Ah	2.30V		
0Bh	1.55V	1Bh	2.35V		
0Ch	1.60V	1Ch	2.40V		
0Dh	1.65V	1Dh	2.45V		
0Eh	1.70V	1Eh	2.50V		
0Fh	1.75V	1Fh	2.55V		

Rail ON/OFF Adjustment

Address – 0x07h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	RFU	LDO2_CH_EN	LDO1_CH_EN	Buck4_CH_EN	Buck3_CH_EN	Buck2_CH_EN	Buck1_CH_EN
READ/WRITE	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO2 Enable/Disable [5]

Code	LDO2 ON/OFF
00h	LDO2 is disable
01h	LDO2 is enable

Set LDO1 Enable/Disable [4]

Code	LDO1 ON/OFF
00h	LDO1 is disable
01h	LDO1 is enable

Set Buck4 Enable/Disable [3]

Code	Buck4 ON/OFF
00h	Buck4 is disable
01h	Buck4 is enable

Set Buck3 Enable/Disable [2]

Code	Buck3 ON/OFF
00h	Buck3 is disable
01h	Buck3 is enable

Set Buck2 Enable/Disable [1]

Code	Buck2 ON/OFF
00h	Buck2 is disable
01h	Buck2 is enable

Set Buck1 Enable/Disable [0]

Code	Buck1 ON/OFF
00h	Buck1 is disable
01h	Buck1 is enable

Rail ON/OFF Adjustment on SLEEP mode

Address – 0x08h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	B3_VID @SLEEP_ EN	EXT_EN_ SLEEP_EN	LDO2_ SLEEP_EN	LDO1_ SLEEP_EN	Buck4_ SLEEP_EN	Buck3_ SLEEP_EN	Buck2_ SLEEP_EN	Buck1_ SLEEP_EN
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck3 VID ON/OFF in Sleep Mode [7]

Code	Buck3 VID ON/OFF in Sleep Mode
00h	Buck3 disable VID function; Buck3 output keep VSET1 when the IC enters Sleep mode
01h	Buck3 enable VID function; Buck3 output change to VSET1 when the IC enters sleep mode

Set EXT_EN ON/OFF in Sleep Mode [6]

Code	EXT_EN ON/OFF in Sleep Mode
00h	EXT_EN stays on when IC enters sleep mode
01h	EXT_EN turns off when IC enters sleep mode

Set LDO2 ON/OFF in Sleep Mode [5]

Code	LDO2 ON/OFF in Sleep Mode
00h	LDO2 stays on when IC enters sleep mode
01h	LDO2 turns off when IC enters sleep mode

Set LDO1 ON/OFF in Sleep Mode [4]

Code	LDO1 ON/OFF in Sleep Mode
00h	LDO1 stays on when IC enters sleep mode
01h	LDO1 turns off when IC enters sleep mode

Set Buck4 ON/OFF in Sleep Mode [3]

Code	Buck4 ON/OFF in Sleep Mode
00h	Buck4 stays on when IC enters sleep mode
01h	Buck4 turns off when IC enters sleep mode

Set Buck3 ON/OFF in Sleep Mode [2]

Code	Buck3 ON/OFF in Sleep Mode
00h	Buck3 stays on when IC enters sleep mode
01h	Buck3 turns off when IC enters sleep mode

Set Buck2 ON/OFF in Sleep Mode [1]

Code	Buck2 ON/OFF in Sleep Mode
00h	Buck2 stays on when IC enters sleep mode
01h	Buck2 turns off when IC enters sleep mode

Set Buck1 ON/OFF in Sleep Mode [0]

Code	Buck1 ON/OFF in Sleep Mode
00h	Buck1 stays on when IC enters sleep mode
01h	Buck1 turns off when IC enters sleep mode

Rail ON/OFF Adjustment on DPSLP mode

Address – 0x09h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	EXT_EN_ DPSLP_EN	LDO2_ DPSLP_EN	LDO1_ DPSLP_EN	Buck4_ DPSLP_EN	Buck3_ DPSLP_EN	Buck2_ DPSLP_EN	Buck1_ DPSLP_EN
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set EXT_EN ON/OFF in Deep Sleep Mode [6]

Code	EXT_EN ON/OFF in Deep Sleep Mode
00h	EXT_EN stays on when IC enters deep sleep mode
01h	EXT_EN turns off when IC enters deep sleep mode

Set LDO2 ON/OFF in Deep Sleep Mode [5]

Code	LDO2 ON/OFF in Deep Sleep Mode
00h	LDO2 stays on when IC enters deep sleep mode
01h	LDO2 turns off when IC enters deep sleep mode

Set LDO1 ON/OFF in Deep Sleep Mode [4]

Code	LDO1 ON/OFF in Deep Sleep Mode
00h	LDO1 stays on when IC enters deep sleep mode
01h	LDO1 turns off when IC enters deep sleep mode

Set Buck4 ON/OFF in Deep Sleep Mode [3]

Code	Buck4 ON/OFF in Deep Sleep Mode
00h	Buck4 stays on when IC enters deep sleep mode
01h	Buck4 turns off when IC enters deep sleep mode

Set Buck3 ON/OFF in Deep Sleep Mode [2]

Code	Buck3 ON/OFF in Deep Sleep Mode
00h	Buck3 stays on when IC enters deep sleep mode
01h	Buck3 turns off when IC enters deep sleep mode

Set Buck2 ON/OFF in Deep Sleep Mode [1]

Code	Buck2 ON/OFF in Deep Sleep Mode
00h	Buck2 stays on when IC enters deep sleep mode
01h	Buck2 turns off when IC enters deep sleep mode

Set Buck1 ON/OFF in Deep Sleep Mode [0]

Code	Buck1 ON/OFF in Sleep Mode
00h	Buck1 stays on when IC enters deep sleep mode
01h	Buck1 turns off when IC enters deep sleep mode

PWM ON/OFF and Buck3 VID Adjustment

Address – 0x0Ah

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	RFU	RFU	RFU	B4_PWM_EN	B3_PWM_EN	B2_PWM_EN	B1_PWM_EN
READ/WRITE	R	R	R	R	R/W	R/W	R/W	R/W

Description

Set Buck4 LPM/FCCM [3]

Code	Buck4 LPM/FCCM Selection
00h	Buck4 enters LPM at light load
01h	Buck4 forced into PWM at light load

Set Buck3 LPM/FCCM [2]

Code	Buck3 LPM/FCCM Selection
00h	Buck3 enters LPM at light load
01h	Buck3 forced into PWM at light load

Set Buck2 LPM/FCCM [1]

Code	Buck2 LPM/FCCM Selection
00h	Buck2 enters LPM at light load
01h	Buck2 forced into PWM at light load

Set Buck1 LPM/FCCM [0]

Code	Buck1 LPM/FCCM Selection
00h	Buck1 enters LPM at light load
01h	Buck1 forced into PWM at light load

Rail SST Adjustment

Address – 0x0Bh

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	RFU	LDO2_SST	LDO1_SST	B4_SST	B3_SST	B2_SST	B1_SST
READ/WRITE	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO2 Soft Start Time [5]

Code	LDO2 Soft Start Time
00h	200μs
01h	360μs

Set LDO1 Soft Start Time [4]

Code	LDO1 Soft Start Time
00h	200μs
01h	360μs

Set Buck4 Soft Start Time [3]

Code	Buck4 Soft Start Time
00h	150μs

Set Buck3 Soft Start Time [2]

Code	Buck3 Soft Start Time
00h	250μs
01h	500μs

Set Buck2 Soft Start Time [1]

Code	Buck2 Soft Start Time
00h	250μs
01h	500μs

Set Buck1 Soft Start Time [0]

Code	Buck1 Soft Start Time
00h	250μs
01h	500μs

Rail Power off Delay Time Adjustment

Address – 0x0Ch

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Buck1_Power Off_ DLY		Buck2_Power Off_ DLY		Buck3_Power Off_ DLY		Buck4_Power Off_ DLY	
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck1 Power off Delay Time [7:6]

Code	Buck1 Power off Delay Time
00h	0ms
01h	0.25ms
02h	0.5ms
03h	1.0ms

Set Buck2 Power off Delay Time [5:4]

Code	Buck2 Power off Delay Time
00h	0ms
01h	0.25ms
02h	0.5ms
03h	1.0ms

Set Buck3 Power off Delay Time [3:2]

Code	Buck3 Power off Delay Time
00h	0ms
01h	0.25ms
02h	0.5ms
03h	1.0ms

Set Buck4 Power off Delay Time [1:0]

Code	Buck4 Power off Delay Time
00h	0ms
01h	0.25ms
02h	0.5ms
03h	1.0ms

Rail Power off Delay Time Adjustment

Address – 0x0Dh

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	LDO1_ Power Off_ DLY		LDO2_ Power Off_ DLY		EXT_EN_ Power Off_ DLY		nRESET_ Power Off_ DLY	
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO1 Power off Delay Time [7:6]

Code	LDO1 Power off Delay Time
00h	0ms
01h	0.25ms
02h	0.5ms
03h	1.0ms

Set LDO2 Power off Delay Time [5:4]

Code	LDO2 Power off Delay Time
00h	0ms
01h	0.25ms
02h	0.5ms
03h	1.0ms

Set EXT_EN Power off Delay Time [3:2]

Code	EXT_EN Power off Delay Time
00h	0ms
01h	0.25ms
02h	0.5ms
03h	1.0ms

Set nRESET Power off Delay Time [1:0]

Code	nRESET Power off Delay Time
00h	0ms
01h	0.25ms
02h	0.5ms
03h	1.0ms

Rail Wake Up Delay Time Adjustment

Address – 0x0Eh

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Buck1_Wake Up_ DLY		Buck2_Wake Up_ DLY		Buck3_Wake Up_ DLY		Buck4_Wake Up_ DLY	
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck1 Wake Up Delay Time [7:6]

Code	Buck1 Wake Up Delay Time
00h	0ms
01h	1ms
02h	2ms
03h	3ms

Set Buck2 Wake Up Delay Time [5:4]

Code	Buck2 Wake Up Delay Time
00h	0ms
01h	1ms
02h	2ms
03h	3ms

Set Buck3 Wake Up Delay Time [3:2]

Code	Buck3 Wake Up Delay Time
00h	0ms
01h	1ms
02h	2ms
03h	3ms

Set Buck4 Wake Up Delay Time [1:0]

Code	Buck4 Wake Up Delay Time
00h	0ms
01h	1ms
02h	2ms
03h	3ms

Rail Power off Delay Time Adjustment

Address – 0x0Fh

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	RFU	LDO1_Wake Up_ DLY		LDO2_Wake Up_ DLY		EXT_EN_Wake Up_DLY	
READ/WRITE	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO1 Wake Up Delay Time [5:4]

Code	LDO1 Wake Up Delay Time
00h	0ms
01h	1ms
02h	2ms
03h	3ms

Set LDO2 Wake Up Delay Time [3:2]

Code	LDO2 Wake Up Delay Time
00h	0ms
01h	1ms
02h	2ms
03h	3ms

Set EXT_EN Wake Up Delay Time [1:0]

Code	EXT_EN Wake Up Delay Time
00h	0ms
01h	1ms
02h	2ms
03h	3ms

Protection ON/OFF, ROM Mode, and SLEEP/DPSLP Adjustment

Address – 0x10h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	DIS_OVUV	DIS_OTP	DIS_VINOVP	RFU	RFU	RFU	SLEEP_EN	DPSLP_EN
READ/WRITE	R/W	R/W	R/W	R	R	R	R/W	R/W

Description

Set OVUV Fault [7]

Code	OVUV Fault
00h	Enable hiccup mode or OVUVFLT state in ACTIVE Mode
01h	Disable hiccup mode or OVUVFLT state in ACTIVE Mode (LDO1 & LDO2 OVP discharge function is independent at 0x04 bit[6])

Set OTP [6]

Code	OTP
00h	Enable
01h	Disable

Set VINOVP [5]

Code	VIN_OVP
00h	Enable
01h	Disable

Set Sleep Mode EN [1]

Code	Sleep EN
00h	Sleep mode is disable
01h	Sleep mode is enable

Set Deep Sleep Mode EN [0]

Code	Deep Sleep EN
00h	Deep sleep mode is disable
01h	Deep sleep mode is enable

Power on Delay Time Adjustment

Address – 0x11h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	B1_Power ON_ DLY				B2_Power ON_ DLY			
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck1 Power on Delay Time [7:4]

Code	Buck1 Power on Delay Time	Code	Buck1 Power on Delay Time
00h	0ms	08h	4.0ms
01h	0.5ms	09h	4.5ms
02h	1.0ms	0Ah	5.0ms
03h	1.5ms	0Bh	5.5ms
04h	2.0ms	0Ch	6.0ms
05h	2.5ms	0Dh	6.5ms
06h	3.0ms	0Eh	7.0ms
07h	3.5ms	0Fh	7.5ms

Set Buck2 Power on Delay Time [3:0]

Code	Buck2 Power on Delay Time	Code	Buck2 Power on Delay Time
00h	0ms	08h	4.0ms
01h	0.5ms	09h	4.5ms
02h	1.0ms	0Ah	5.0ms
03h	1.5ms	0Bh	5.5ms
04h	2.0ms	0Ch	6.0ms
05h	2.5ms	0Dh	6.5ms
06h	3.0ms	0Eh	7.0ms
07h	3.5ms	0Fh	7.5ms

Power on Delay Time Adjustment

Address – 0x12h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	B3_Power ON_ DLY				B4_Power ON_ DLY			
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck3 Power on Delay Time [7:4]

Code	Buck3 Power on Delay Time	Code	Buck3 Power on Delay Time
00h	0ms	08h	4.0ms
01h	0.5ms	09h	4.5ms
02h	1.0ms	0Ah	5.0ms
03h	1.5ms	0Bh	5.5ms
04h	2.0ms	0Ch	6.0ms
05h	2.5ms	0Dh	6.5ms
06h	3.0ms	0Eh	7.0ms
07h	3.5ms	0Fh	7.5ms

Set Buck4 Power on Delay Time [3:0]

Code	Buck4 Power on Delay Time	Code	Buck4 Power on Delay Time
00h	0ms	08h	4.0ms
01h	0.5ms	09h	4.5ms
02h	1.0ms	0Ah	5.0ms
03h	1.5ms	0Bh	5.5ms
04h	2.0ms	0Ch	6.0ms
05h	2.5ms	0Dh	6.5ms
06h	3.0ms	0Eh	7.0ms
07h	3.5ms	0Fh	7.5ms

Power on Delay Time Adjustment

Address – 0x13h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	LDO1_Power ON_ DLY				LDO2_Power ON_ DLY			
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO1 Power on Delay Time [7:4]

Code	LDO1 Power on Delay Time	Code	LDO1 Power on Delay Time
00h	0ms	08h	4.0ms
01h	0.5ms	09h	4.5ms
02h	1.0ms	0Ah	5.0ms
03h	1.5ms	0Bh	5.5ms
04h	2.0ms	0Ch	6.0ms
05h	2.5ms	0Dh	6.5ms
06h	3.0ms	0Eh	7.0ms
07h	3.5ms	0Fh	7.5ms

Set LDO2 Power on Delay Time [3:0]

Code	LDO2 Power on Delay Time	Code	LDO2 Power on Delay Time
00h	0ms	08h	4.0ms
01h	0.5ms	09h	4.5ms
02h	1.0ms	0Ah	5.0ms
03h	1.5ms	0Bh	5.5ms
04h	2.0ms	0Ch	6.0ms
05h	2.5ms	0Dh	6.5ms
06h	3.0ms	0Eh	7.0ms
07h	3.5ms	0Fh	7.5ms

Power on Delay Time Adjustment

Address – 0x14h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	nRESET_ Input Trigger	nRESET_Power ON_ DLY			EXT_EN_Power ON_ DLY			
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set nRESET Input Trigger [7]

Code	nRESET Input Trigger
00h	Buck2_PG
01h	SYS_OK

Set nRESET Power on Delay Time [6:4]

Code	nRESET Power on Delay Time
00h	0.5ms
01h	1ms
02h	2ms
03h	4ms
04h	8ms
05h	16ms

Set EXT_EN Power on Delay Time [3:0]

Code	EXT_EN Power on Delay Time	Code	EXT_EN Power on Delay Time
00h	0ms	08h	4.0ms
01h	0.5ms	09h	4.5ms
02h	1.0ms	0Ah	5.0ms
03h	1.5ms	0Bh	5.5ms
04h	2.0ms	0Ch	6.0ms
05h	2.5ms	0Dh	6.5ms
06h	3.0ms	0Eh	7.0ms
07h	3.5ms	0Fh	7.5ms

GPIO5 and GPIO8 Adjustment

Address – 0x15h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	GPIO5 Function		GPIO7 Function		RFU	GPIO6 Lock	GPIO5 Open Drain	GPIO7 Open Drain
READ/WRITE	R/W	R/W	R/W	R/W	R	R	R/W	R/W

Description

Set GPIO5 Function [7:6]

Code	GPIO5 Function
00h	DPSLP Input
01h	I^2C Controlled Output
02h	nIRQ(SYSWARN) Output

Set GPIO7 Function [5:4]

Code	GPIO7 Function
00h	EXT_EN Output
01h	I^2C Controlled Output
02h	PWRDIS Input

Set GPIO6 Lock Function [2]

Code	GPIO6 Lock Function
00h	GPIO6 status not lock and LDO2 mode can be changed when GPIO6 status change after power on. (Not recommended due to trigger protection).
01h	GPIO6 status lock and LDO mode will not change with GPIO6 status after power on.

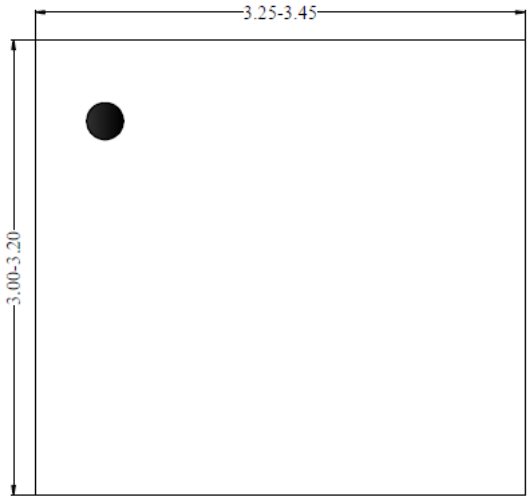
Set GPIO5 Open Drain ON/OFF [1]

Code	GPIO5 Open Drain ON/OFF
00h	Open drain turn off
01h	Open drain turn on

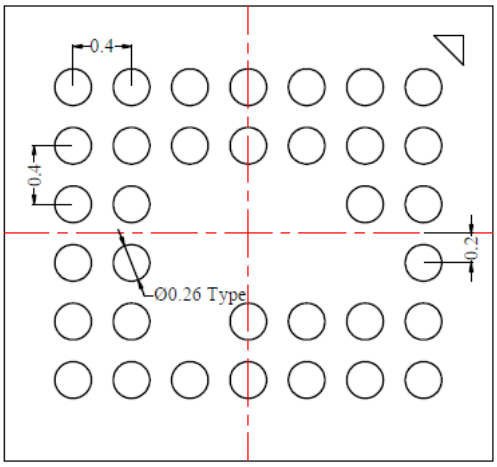
Set GPIO7 Open Drain ON/OFF [0]

Code	GPIO7 Open Drain ON/OFF
00h	Open drain turn off
01h	Open drain turn on

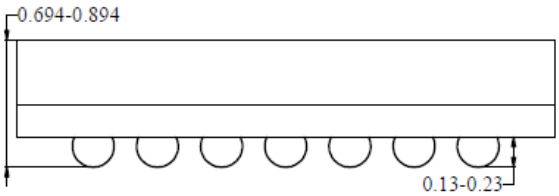
BGA3.35×3.1-34 Package Outline Drawing



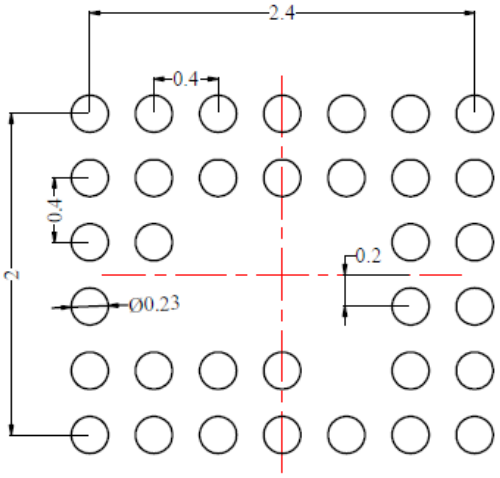
Top View



Bottom View



Front View



Recommended PCB Layout (Reference Only)

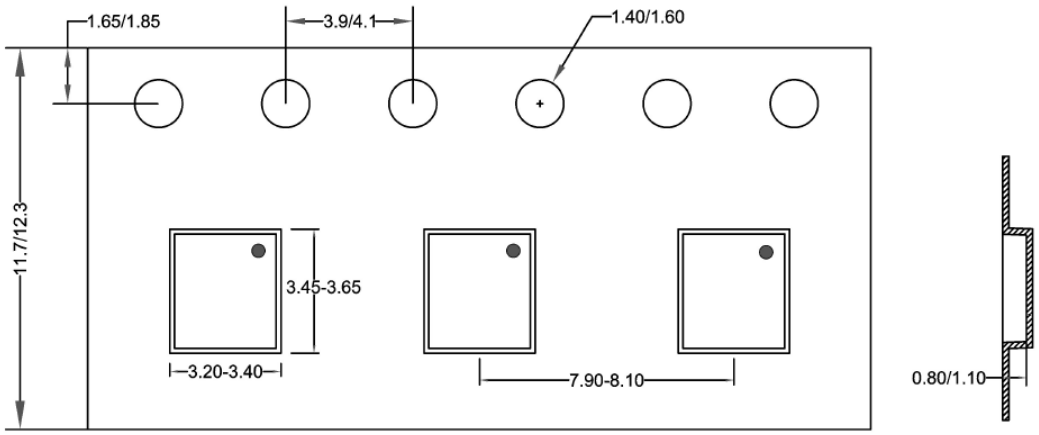
Notes:

1. *All dimensions are in millimeters and exclude mold flash and metal burr.*
2. *Center line refers to the chip body center.*

Tape and Reel Information

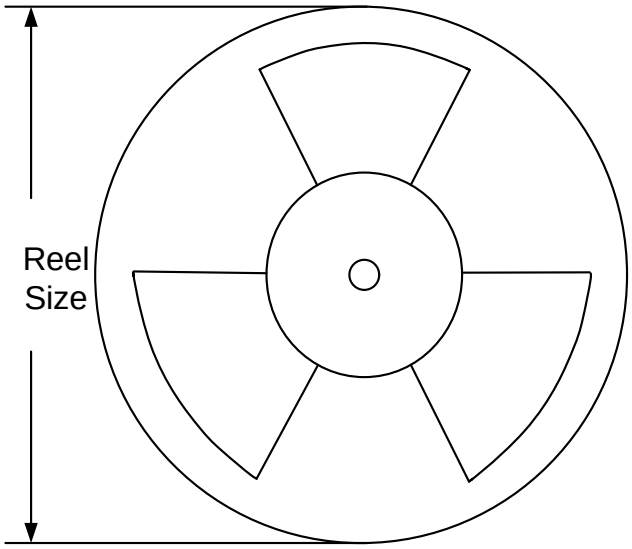
Tape Dimensions and Pin 1 Orientation

BGA3.35×3.1-34



Direction of feed ⟶

Reel Dimensions



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
BGA3.35×3.1-34	12	8	13"	400	400	5000

All Dimension are nominal

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
Aug.11, 2025	Revision 1.0	Initial Release	-

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