SY7304B

High Efficiency 33V, 1MHz 4A Current Limit Step-Up Regulator

General Description

The SY7304B high efficiency step-up regulator operates using current mode control over a wide input voltage range from 3V to 33V. It integrates an N-channel MOSFET with low 120mΩ $R_{DS(ON)}$ to minimize conduction loss.

The 1MHz switching frequency and internal compensation reduce external inductor and capacitor sizes, and the built-in internal soft-start circuitry minimizes inrush current at startup.

The device offers overcurrent and thermal shutdown protections.

The SY7304B is available in a compact CSP2.03×0.93-8 package.

Features

- 3V to 33V Input Voltage Range
- 33V Maximum Output Voltage
- 4A Main MOSFET Current Limit
- 15 µA Shutdown Current (Max.)
- 100 µA Quiescent Current (Typ.)
- Low $R_{DS(ON)}$ for Internal N-Channel MOSFET: 120mΩ
- 1MHz Switching Frequency
- Internal Soft-Start
- ±2% 0.6V Reference
- Cycle-by-Cycle Peak Current Limit
- Overtemperature Protection
- RoHS-Compliant and Halogen-Free
- Compact Package: CSP2.03×0.93-8
- Moisture Sensitivity Level (MSL): 1

Applications

- Portable Devices
- Battery Powered Systems
- Networking Cards Powered from PCI or PCI-Express Slots

Typical Application

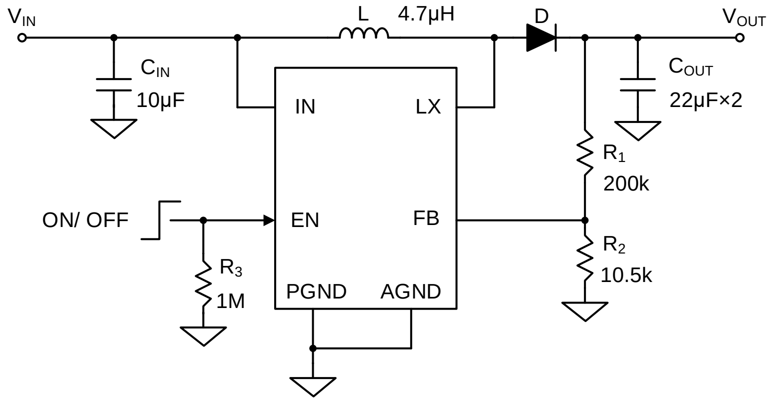


Figure 1. Typical Application Circuit

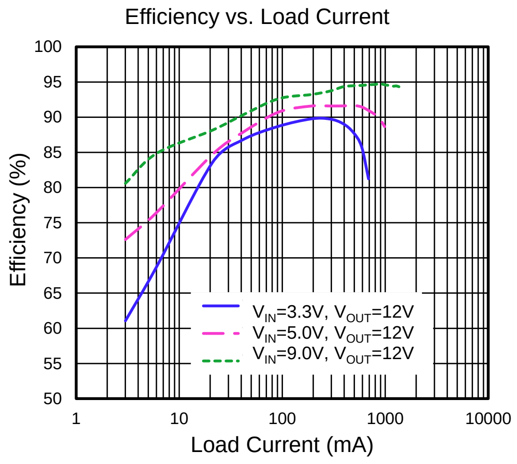


Figure 2. Efficiency vs. Output Current

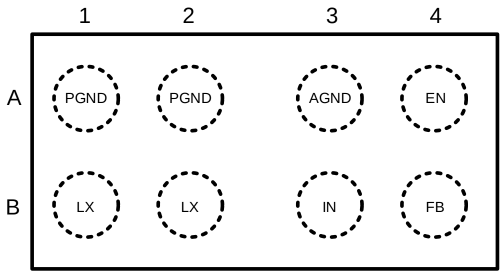
Ordering Information

Ordering Part Number	Package Type	Top Mark
SY7304BXES	CSP2.03×0.93-8 RoHS-Compliant and Halogen-Free	**LCF*xyz***

Device code: LCF

x = year code, y = week code, z = lot number code

Pinout (top view)



(CSP2.03×0.93-8)

Pin Description

Pin Name	Pin Number	Pin Description
PGND	A1, A2	Power ground.
AGND	A3	Analog signal ground. Connect to PGND external.
EN	A4	Enable pin. Drive low to disable the device, drive high to enable. Do not leave floating.
LX	B1, B2	Inductor node. Connect an inductor between the IN pin and the LX pin.
IN	B3	Input pin. Decouple this pin to the AGND pin with a 1μF ceramic capacitor.
FB	B4	Feedback pin. Connect a resistor R_1 between V_{OUT} and FB, and a resistor R_2 between FB and AGND to program the output voltage: $V_{OUT}=0.6V\times(R_1/R_2+1)$

Block Diagram

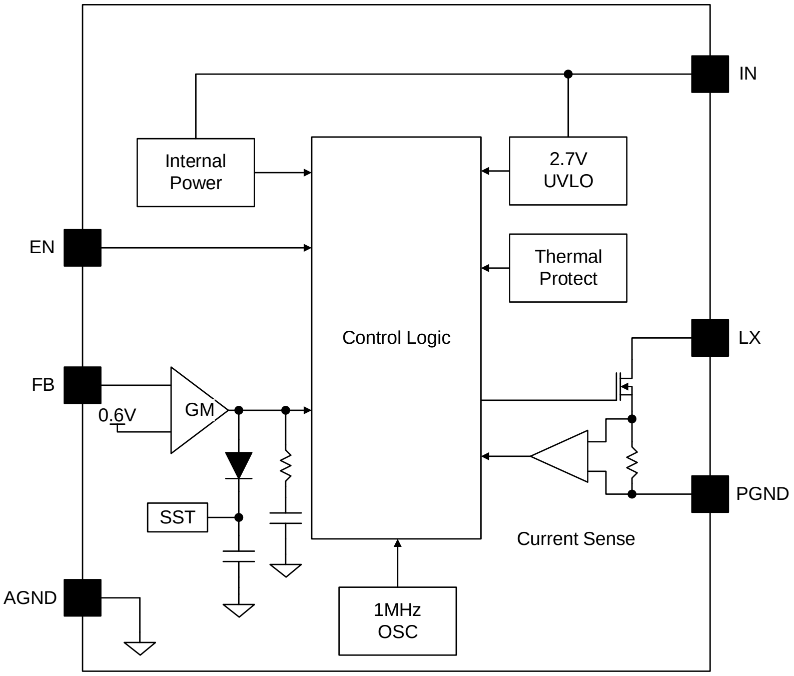


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
LX, IN, EN	-0.3	36	V
FB	-0.3	4	
LX, 50ns Duration	PGND-4	IN+3	
Lead Temperature (Soldering, 10 sec.)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	63	°C/W
θ_{JC} Junction-to-case Thermal Resistance	2	
P_D Power Dissipation T_A=25°C	1.6	W

Recommended Operating Conditions

Parameter (Note3)	Min	Max	Unit
IN	3	33	V
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{IN} = 5V, V_{OUT}=12V, I_{OUT}=100mA, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		3		33	V
Quiescent Current	I_Q	V_{FB} = 0.66V		100		μA
Shutdown Current	I_{SHDN}	EN = 0			15	μA
Low Side Main FET R_{ON}	$R_{DS(ON)}$			120		mΩ
Main FET Current Limit	I_{LIM}	Duty cycle = 80%	4		6	A
Switching Frequency	f_{SW}		0.8	1	1.2	MHz
Feedback Reference Voltage	V_{REF}		0.588	0.6	0.612	V
FB Pin Input Current	I_{FB}		-50		50	nA
IN UVLO Rising Threshold	$V_{IN,UVLO}$				2.7	V
UVLO Hysteresis	$U_{VLO,HYS}$			0.1		V
EN Rising Threshold	V_{ENH}		2			V
EN Falling Threshold	V_{ENL}				0.4	V
Maximum Duty Cycle	D_{MAX}			90		%
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Recovery Hysteresis	T_{HYS}			15		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

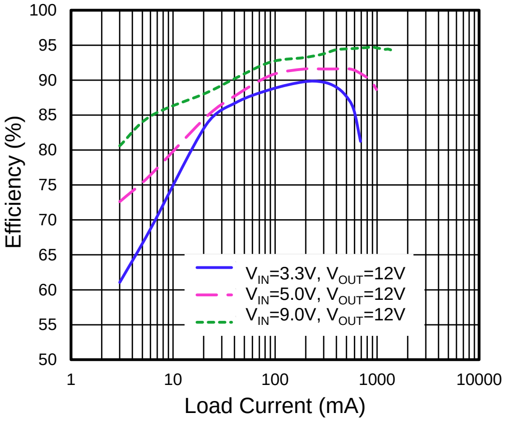
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

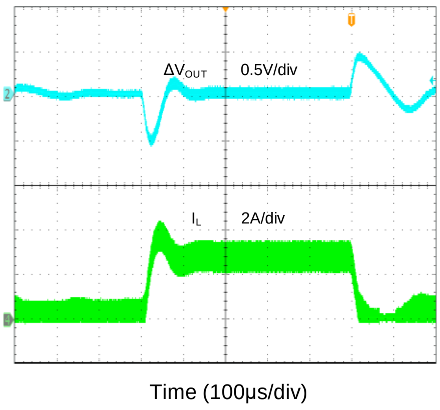
(T$_A$= 25℃, V$_{IN}$=5V, V$_{OUT}$ = 12V, L = 2.2µH, C$_{OUT}$= 44µF, unless otherwise specified.)

Efficiency vs. Load Current



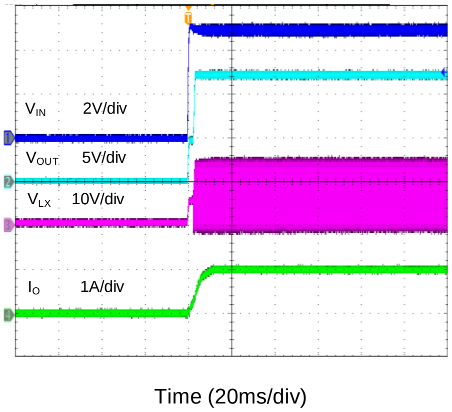
Load Transient

(V$_{IN}$=5.0V, V$_{OUT}$=12V, I$_O$=0.1 ~ 1.0A)



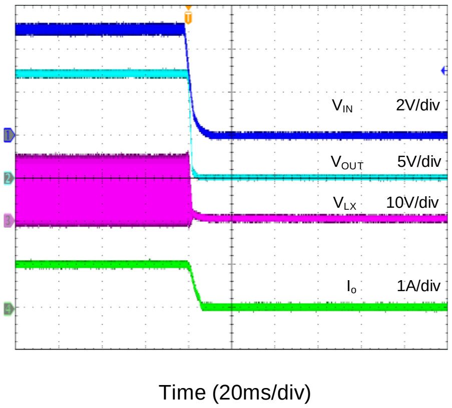
Startup from V$_{IN}$

(V$_{IN}$=5.0V, V$_{OUT}$=12V, I$_O$=1.0A)



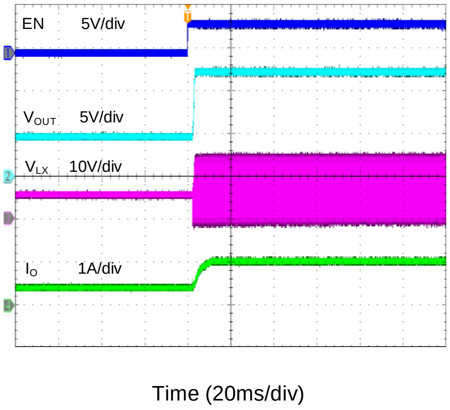
Shutdown from V$_{IN}$

(V$_{IN}$=5.0V, V$_{OUT}$=12V, I$_O$=1.0A)



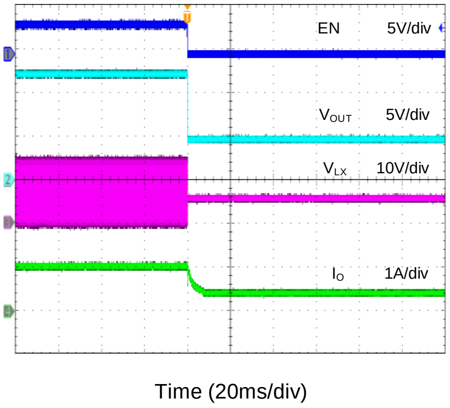
Startup from Enable

(V$_{IN}$=5.0V, V$_{OUT}$=12V, I$_O$=1.0A)



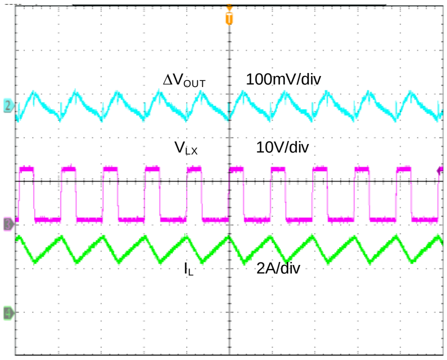
Shutdown from Enable

(V$_{IN}$=5.0V, V$_{OUT}$=12V, I$_O$=1.0A)



Output Ripple

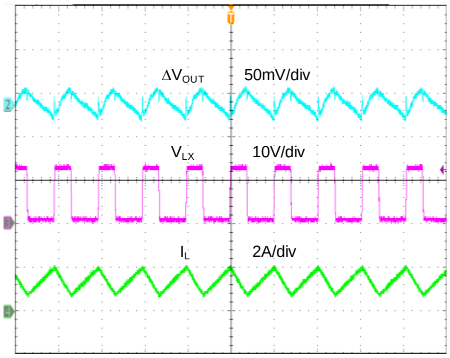
(V_{IN}=5.0V, V_{OUT}=12V, I_O=1.0A)



Time (1µs/div)

Output Ripple

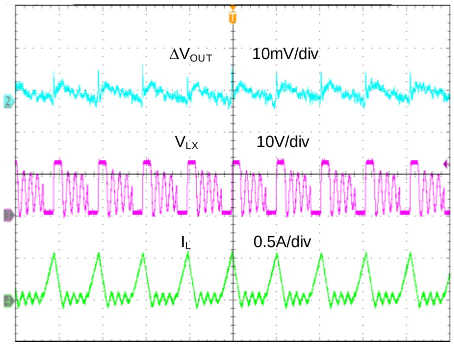
(V_{IN}=5.0V, V_{OUT}=12V, I_O=0.5A)



Time (1µs/div)

Output Ripple

(V_{IN}=5.0V, V_{OUT}=12V, I_O=0.05A)



Time (1µs/div)

Detailed Description

The SY7304B high efficiency step-up regulator operates using current mode control, over a wide input voltage range from 3V to 33V. It integrates an N-channel MOSFET with low 120mΩ $R_{DS(ON)}$ to minimize conduction loss.

The 1MHz switching frequency and internal compensation reduce external inductor and capacitor sizes, and the built-in internal soft-start circuitry minimizes inrush current at startup.

Enable Operation

Driving the EN pin high (>2V) enables normal operation. Driving the EN pin low (<0.4V) places the device in shutdown mode. During shutdown mode, the SY7304B current drops to less than 15μA.

Soft-Start (EN Control)

The SY7304B has a built-in soft-start to control the rising slew rate of the output voltage and limit the input current surge during IC startup. With a 2.1ms turn-on delay time before the initial soft-start, the typical soft-start time is 800μs.

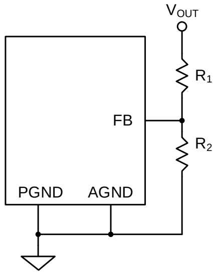
Application Information

The following paragraphs describe the selection process for the feedback resistors (R_1 and R_2), input capacitor C_{IN}, output capacitor C_{OUT}, boost inductor L, and diode D.

Feedback Resistor-Divider R_1 and R_2

Choose R_1 and R_2 to program the proper output voltage. Choose large resistance values between 10kΩ and 1MΩ for both R_1 and R_2 to minimize power consumption under light loads. If a value of 200kΩ is chosen for R_1, then R_2 can be calculated as:

$$R_2 = \frac{0.6\text{V}}{V_{\text{OUT}}\text{-}0.6\text{V}} R_1$$



Input Capacitor C_{IN}

Input filter capacitors reduce the ripple voltage on the input, filter the switched current drawn from the input supply, and reduce the EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating higher than the system requirements. X5R series ceramic capacitors are most often selected due to their small size, low cost, surge-current capability, and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum, or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{\sqrt[2]{3} \times L \times f_{SW} \times V_{OUT}}$$

For the best performance, select a typical X5R or better grade low ESR 10μF ceramic capacitor and place it as close as possible to the IN and AGND pins. Take care to minimize the loop area formed by C_{IN} and the IN/AGND pins.

Output Capacitor C_{OUT}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting the component. For the best performance, use an X5R or better grade ceramic capacitor with capacitance of at least 22μF.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed:

The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, both should be considered.

$$V_{RIPPLE,ESR1} = I_{LPEAK} \times ESR$$

$$V_{RIPPLE,ESR2} = I_{LPVALLEY} \times ESR$$

$$V_{RIPPLE,CAP} = \frac{I_{OUT} \times (1 - D)}{C_{OUT} \times f_{SW}}$$

The measured capacitive ripple might be higher than the calculated value because the effective capacitance for ceramic capacitors decreases with the voltage across the terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Boost Inductor L

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{V_{OUT} - V_{IN}}{f_{SW}\, I_{OUT,MAX} \times 0.4}$$

where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY7304B has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} = \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT,MAX} + \frac{V_{IN}(V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Choose an inductor with DCR less than 10mΩ to achieve good overall efficiency.

Rectifier Diode

For high efficiency, choose a Schottky diode with low forward voltage drop and fast reverse recovery. The maximum current rating of the diode must be higher than the maximum input current, and the average current rating of the diode must be higher than the output current. The reverse breakdown voltage must be higher than the maximum output voltage.

Maximum Output Current Estimation

The maximum current that the converter can provide to the load depends on the output voltage / input voltage ratio.

Use the following formulas to evaluate an approximate max current that the converter can deliver when driving the load.

$$D = 1 - V_{IN(MIN)} \times \frac{\eta}{V_{OUT}}$$

Estimate the maximum output current:

$$I_{MAXOUT} = \left(IL_{MIN} - \frac{\Delta IL}{2}\right) \times \frac{\eta \times V_{IN(MIN)}}{V_{OUT}}$$

$$I_{MAXOUT} = \left(I_{LIM(MIN)} - \frac{\Delta IL}{2}\right) \times (1 - D)$$

Where: $V_{IN(MIN)}$ is the minimum voltage at the boost input in the application, IL_{MIN} is the minimum device current datasheet limit (4A for SY7304B), ΔIL is the current ripple and η is the efficiency, which can be substituted with a value of 0.8 for simplicity.

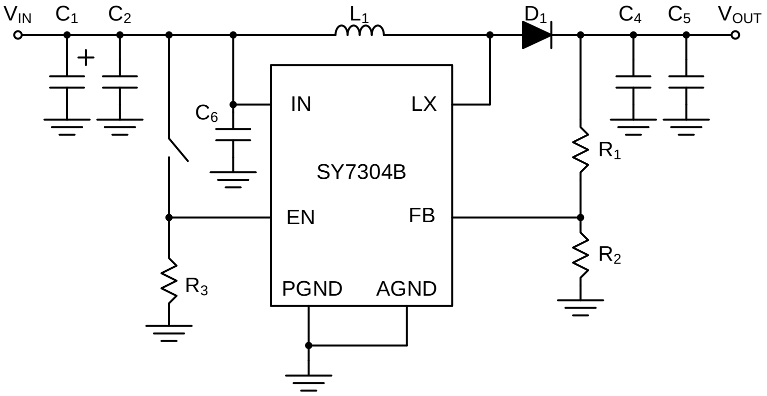
Thermal Protection

The SY7304B includes over temperature protection circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. When the junction temperature cools down by approximately 15°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the thermal protection threshold.

Over Current Protection

The SY7304B provides a cycle-by-cycle overcurrent protection and turns off the main power MOSFET once the inductor current reaches the overcurrent limit threshold. During the overcurrent protection, the output voltage drops as a function of the load. If the output voltage drops below the input voltage, the current will directly flow through L and rectifier diode. In this case the current is only limited by the DC resistance in the path during the event. As soon as the overload condition is removed, the converter resumes operation.

Application Schematic



Design Specifications

Input Voltage (V)	Output Voltage(V)	Output Current A)
3–12	12	1

BOM List

Reference Designator	Description	Part Number	Manufacturer
U_1	4A, 1MHz Async Boost(CSP2.03×0.98-8)	SY7304BXES	Silergy
L_1	2.2μH/6A inductor	VLP6045LT-2R2N	TDK
C_1	47μF/50V(electrolytic capacitor)		
C_2, C_4, C_5	22μF/25V,1206,X5R	C3216X5R1E226M	TDK
C_6	0.1μF/25V, 0603, X5R	GRM188R61E104K	muRata
D_1	5A Schottky diode	SS54	
R_1	200k,1%,0603		
R_2	10.5k,1%,0603		
R_3	1MΩ, 0603		

Recommend Components for Typical Applications

V_{OUT}(V)	R_1(kΩ)	R_2(kΩ)	L(μH)	C_{OUT}
12	200	10.5	2.2	2×22μF/25V/X7R,1206

Layout Design

To achieve optimal design, follow these PCB layout considerations:

- Place C_{IN}, L, R_1, and R_2 close to the IC.
- To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the PGND pin. A ground plane is highly recommended if cost allows.
- C_{IN} must be close to pins IN and AGND. Minimize the loop area formed by C_{OUT}, LX, and PGND.
- To reduce the switching noise, minimize the PCB copper area connected to the LX pin.
- In order to reduce crosstalk, R_1, R_2, and the trace connected to the FB pin must not be adjacent to the LX net on the PCB layout.
- If the system controller interfacing with the EN pin has a high impedance state during shutdown mode, and the IN pin is connected directly to a power source such as a Li-ion battery, add a 1MΩ pulldown resistor between the EN and AGND pins to prevent noise from falsely triggering the regulator during shutdown mode.

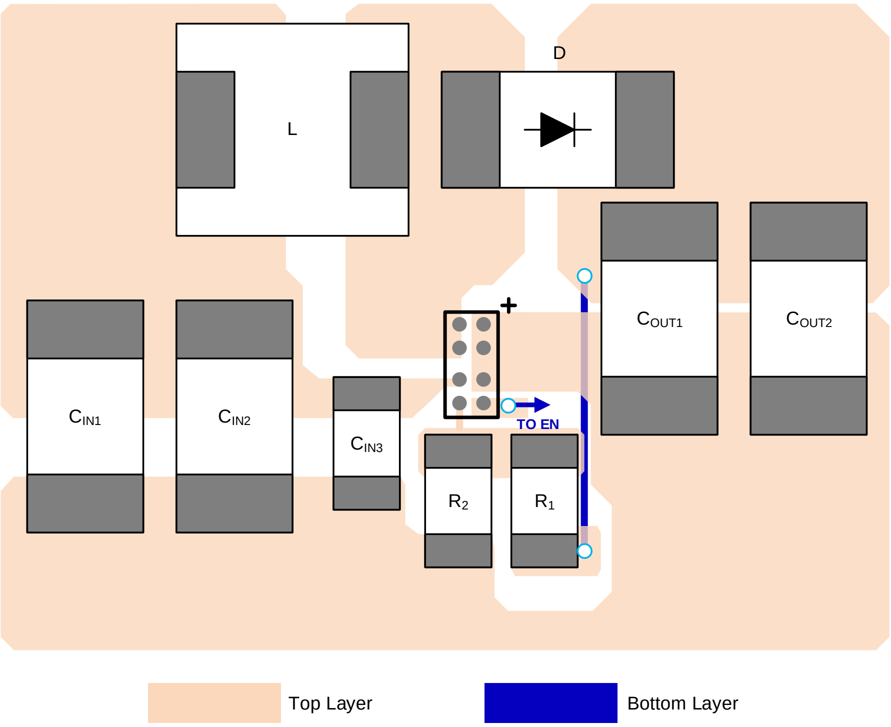
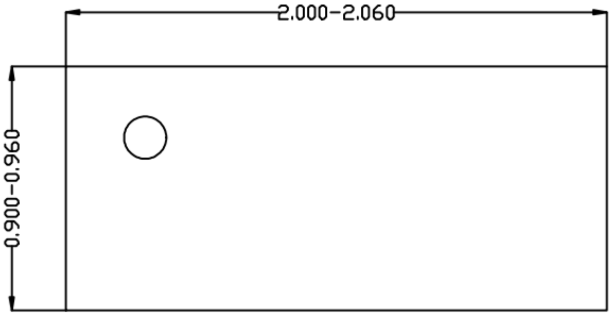
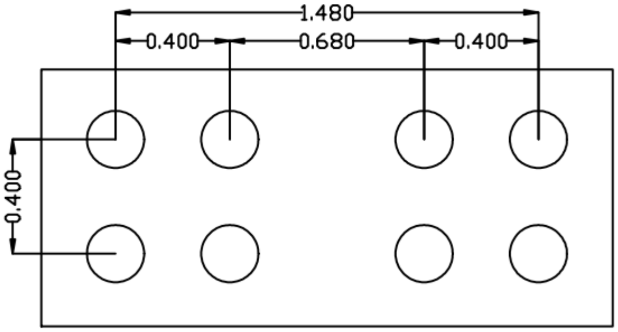


Figure 4. Suggested PCB Layout

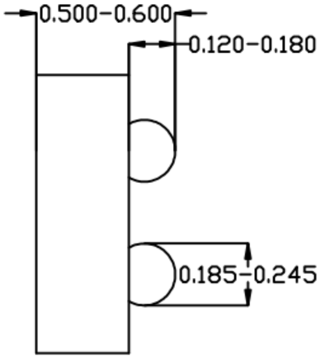
CSP2.03×0.93-8 Package Outline



Top view



Bottom view



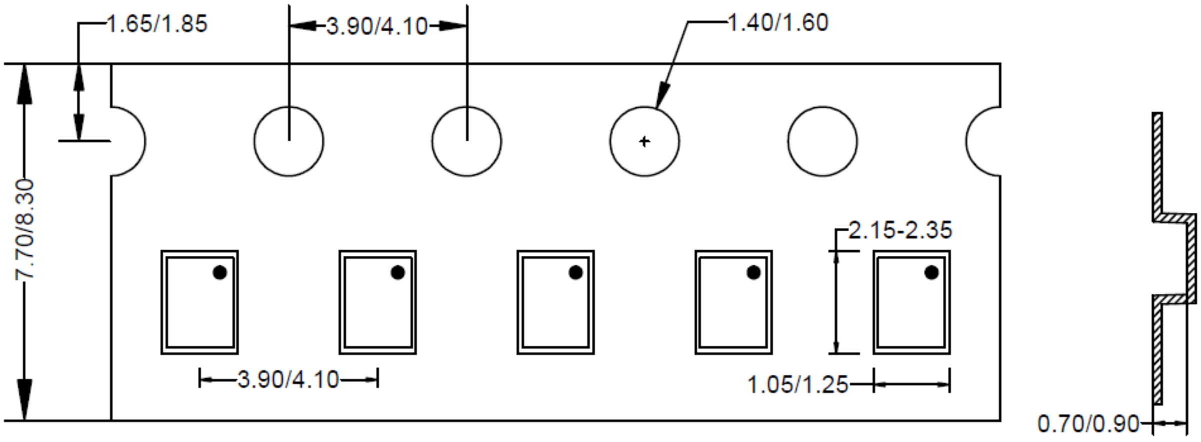
Side view

Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

Tape and Reel Information

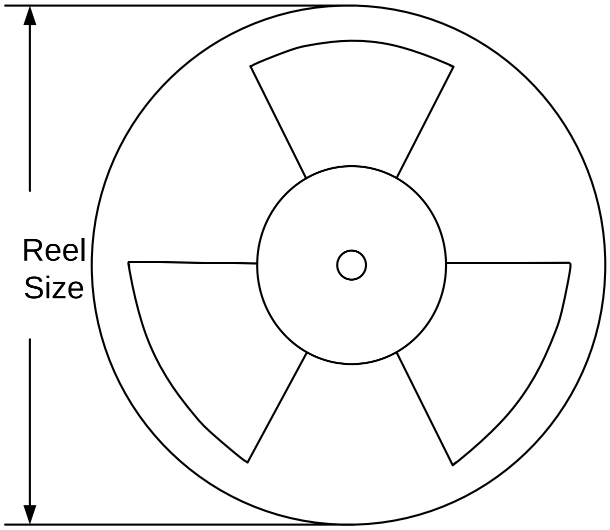
1. Tape Dimensions and Pin1 Orientation

CSP2.03×0.93



Feeding Direction →

2. Reel Dimensions



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
CSP2.03×0.93	8	4	7"	400	400	3000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Apr.14, 2026	Revision 1.0	Initial Release

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