SY6402

High Efficiency Bi-directional DC-DC Regulator With High Current Over Voltage Protection Switch

General Description

SY6402 is designed to achieve energy storage and release management for the applications of data backup in Solid-State Driver and other backup power supplies. The integrated bi-directional Dc-Dc regulator transfers the energy between the system side and the energy storage side with high efficiency. The quasi-fixed frequency constant off time control is employed to achieve stable operation and fast dynamic response. Besides, a reverse blocking switch is integrated at the input side to prevent from energy leaking when the input power source is removed or inserted with inverse polarity. The programmable input current limit cooperates with the bi-directional Dc-Dc regulator to achieve power path management for better dynamic load response at the system side. Three different input voltage OVP thresholds are selectable for the applications with different kind of input power source. SY6402 along with QFN3X4-19 package provides compact PCB layout.

Ordering Information

SY6402 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY6402QVC	QFN3x4-19	

Features

- Low $R_{DS(ON)}$ for internal switches
  - Input Reverse Blocking Switch: 50 mΩ
  - High-side and Low-side Switches of Bi-directional Dc-Dc Regulator: 60 mΩ /60 mΩ
  - Disconnect Switch: 30 mΩ
- 2.7V-16V Input Voltage Range
- 36V Storage Voltage Rating
- Programmable Input Current Limit from 1A to 5A
- Selectable Over Voltage Protection: 3.3V, 5.0V, and 12V
- Reverse Blocking at Input Side
- Programmable Soft-start Time
- Integrated High-efficiency Bi-directional Dc-Dc Regulator: Boost Charging Mode and Buck Discharging Mode Auto-alternating with Programmable System Voltage
- Quasi-Fixed Frequency Constant OFF Time Control for Stable Operation: 500kHz
- Programmable Boost Charging Current
- Programmable Storage Voltage
- Power Path Management
- Short-circuit Protection at Energy Storage Side
- Enable Control
- RoHS Compliant and Halogen Free
- Compact package: QFN3X4-19

Applications

- Solid-State Drivers
- Backup Power Supply

Typical Applications

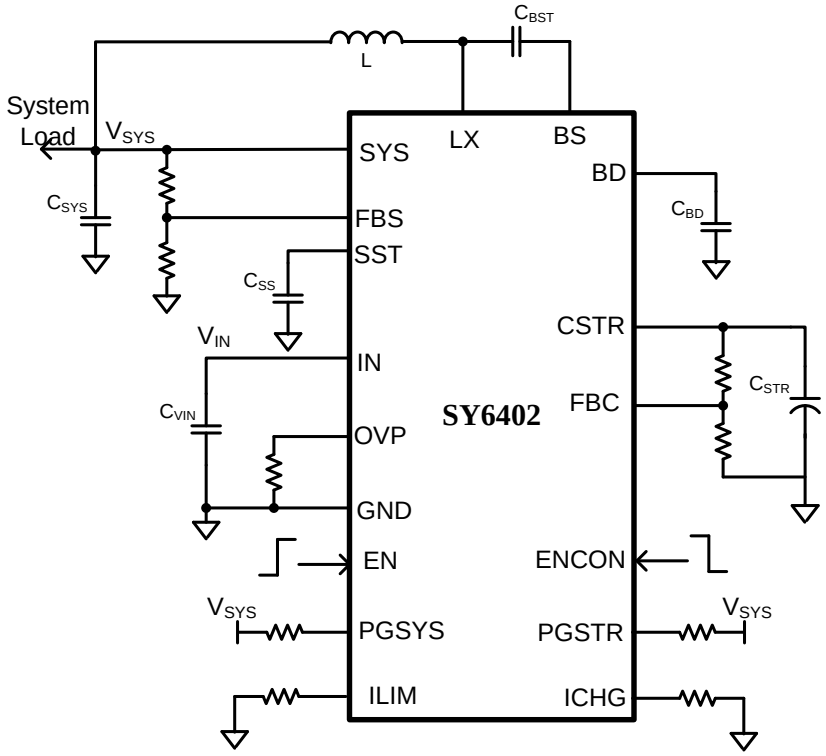
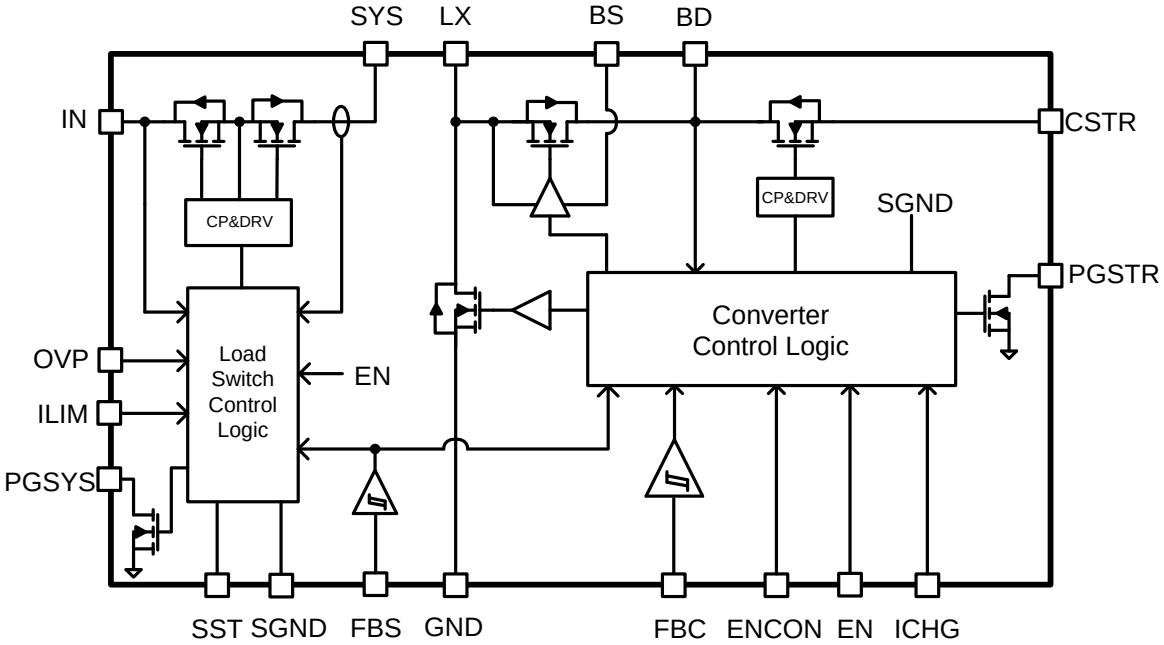
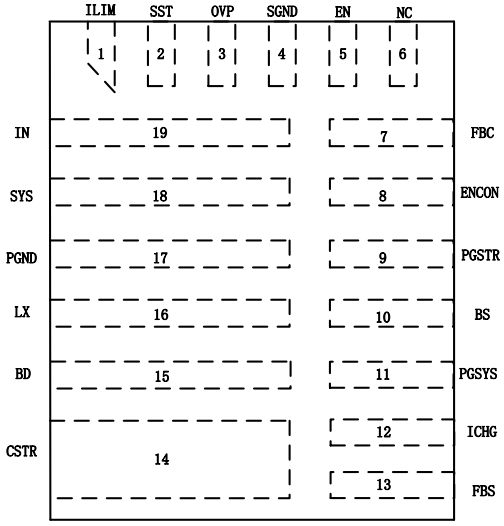


Figure 1. Schematic Diagram

Block Diagram



Pinout (top view)



(QFN3x4-19)

Top Mark: AVE*xyz* (device code: AVE, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin Number	Pin Description
ILIM	1	Input current limit program pin. Connect a resistor between this pin and GND to program input current limit.
SST	2	Soft-start time program pin. Connect a capacitor to ground to program the soft start time.
OVP	3	Output clamp voltage selection based on the input voltage. Pull OVP pin to High by connecting a resistor to IN, or pull OVP pin to Low by connecting a resistor to ground, or float OVP Pin to select different output clamping thresholds. Recommend to decoupling this pin with 0.1uF capacitor.
SGND	4	Signal Ground pin
EN	5	EN control pin. All the functions of SY6402 including OVP switch and DC-DC converter will be disabled when EN is pulled down.
FBC	7	Energy storage capacitor voltage feedback pin. Connect resistor divider to this pin to program the storage voltage. The internal reference is at 1.2V.
ENCON	8	Enable control pin for DC-DC converter. DC-DC converter will be disabled when ENCON is pulled down.
PGSTR	9	CSTR voltage power good indicator pin. This pin is an open drain output. PGSTR is pulled low if voltage on FBC pin falls below 1.14V, and is pulled high when voltage on FBC pin exceeds 1.17V.
BS	10	Boost-Strap pin. Supply high side FET's gate driver. Decouple this pin to LX with 0.1uF ceramic cap.
PGSYS	11	SYS voltage power good indicator pin. This pin is an open drain output. PGSYS is pulled low if voltage on FBS pin falls below 0.6V, and is pulled high when voltage on FBS pin exceeds 0.63V.
ICHG	12	Boost charge current program pin. (Note 6)

OVP	IN	Clamping Threshold		
		Min	Typ	Max
Low	3.3V	3.6V	3.8V	4.0V
High	5V	5.4V	5.7V	6.0V
Open	12V	12.6V	13.3V	14V

FBS	13	System voltage feedback pin. Internal reference of FBS is 0.6V.
CSTR	14	Energy storage capacitor pin. Connect to the energy storage capacitor.
BD	15	Connect to the Drain of internal Blocking FET. Bypass at least 4.7uF ceramic cap to GND.
LX	16	Switch node pin. Connect to external inductor.
PGND	17	Power Ground pin
SYS	18	System voltage output pin. Decouple this pin to GND pin with at least 22uF ceramic capacitor.
IN	19	Input power supply. Decouple this pin to GND with at least 10uF ceramic capacitor.

Absolute Maximum Ratings (Note 1)

CSTR, BD, LX, BS, FBC ---------- 36V
IN, OVP, SST, SYS, EN, FBS, ENCON, PGSYS, PGSTR, ILIM, BD-CSTR---------- 16V
ICHG ---------- 4V
BS-LX ---------- 4V
Power Dissipation, PD @ TA = 25°C QFN3X4-19 ---------- 3.2W
Package Thermal Resistance (Note 2)
θ JA ---------- 40°C/W
θ JC ---------- 3°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

CSTR, BD, LX, BS, FBC ----------less than 36V
IN, OVP, SST, SYS, FBS, EN, ENCON, PGSYS, PGSTR, ILIM, BD-CSTR---------- less than 16V
ICHG ---------- less than 4V
BS-LX ---------- less than 4V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, V_{SYS} = 5V, L = 10uH, V_{BD}=V_{CSTR}=12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OVP Switch Part						
Input Voltage Range	V_{IN}		2.7		16	V
Input UVLO Threshold	V_{UVLO}			2.5	2.7	V
Input UVLO Hysteresis	V_{HYS}			0.1		V
On Resistance of Reverse Blocking FET	$R_{DS(ON)R}$			45	50	mΩ
Reverse blocking Range	V_{RB}				16	V
Reverse blocking Current	I_{RB}	V_{IN}=0V, V_{SYS}=16V, V_{EN}=0V		2	5	μA
Bias Current	I_{BIAS}	V_{IN}=5V, V_{ENCON}=0V		100		μA
EN Enable threshold	V_{EN}	Rising	1.2			V
		Falling			0.5	V
Clamping Output Voltage	V_{CLP}	OVP=LOW	3.6	3.8	4.0	V
		OVP=HIGH	5.4	5.7	6.0	V
		OVP=OPEN	12.6	13.3	14.0	V
Soft-start Time	T_{SST}	C_{SST}=105nF(Note 4)		29.4		ms
Current Limit Accuracy				30%I_{LIM}		
Current Limit Program Range	I_{LIM}	(Note 5)	1		5	A
PGSYS Threshold	V_{PGSYSH}	V_{FBS} Rising		0.63		V
	V_{PGSYSL}	V_{FBS} Falling		0.6		V
DC-DC Regulator Part						
Switching Frequency	F_{SWBST}			500		kHz
HSFET Min ON Time	$t_{ON,MINL}$			80	160	ns
LSFET Min ON Time	$t_{OFF,MINL}$			80		ns
Peak Current of Boost	I_{PKBST}	R_{ICHG}=100kΩ (Note 6)		1500		mA
Boost OVP Threshold	V_{OVPBST}	V_{FBC} Rising		1.2	1.236	V
Boost OVP Release Threshold	V_{OVPBST}	V_{FBC} Falling	1.147	1.17		V
Mode Change Threshold	V_{MCHGH}	V_{FBS} Rising		0.63		V
	V_{MCHGL}	V_{FBS} Falling		0.6		V
Buck Regulate Voltage Reference	V_{BUCK_REF}			0.6		V
PGSTR Threshold	V_{PGSTRH}	V_{FBC} Rising		1.17		V
	V_{PGSTRL}	V_{FBC} Falling		1.14		V
CSTR Short Circuit Threshold	V_{CSTRSC}			0.7		V
Pre-charge Current	I_{PRECHG}			250		mA
$R_{DS(ON)}$ of High Side FET	$R_{DS(ON)H}$			60		mΩ
$R_{DS(ON)}$ of Low Side FET	$R_{DS(ON)L}$			60		mΩ
$R_{DS(ON)}$ of Disconnect FET	$R_{DS(ON)D}$			30		mΩ

Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Recovery Hysteresis	T_{HYS}			15		°C

Note 1: Stresses beyond "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θ JA is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Exposed pad of QFN3X3-16 packages is the case position for θ JC measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note4. Recommended Soft-start Time Program Table

SST cap (nF)	None	10	55	105
Rise time (ms)	1.4	2.8	15.4	29.4

Recommended Formula for C_{SST} & Soft-start Time Calculation

$$T_{SS} = \begin{cases} T_{SS\_DLT}, & \text{No external } C_{SST} \\ \dfrac{C_{SST}}{I_{INT}}, & T_{SS} > T_{SS\_DLT} \end{cases},$$

Where, TSS_DLT is the internally fixed default soft-start time, about 1.4ms, which means there's no any external C_{SST}; I_{INT} is the internal current source, about 3.0uA.

Note 5: Recommended Current Limit Program Table

Current Limit Resistor(kΩ)	9.6	4.8	3.84	3.2	2.74	2.4	1.92
Current Limit (A)	1	2	2.5	3	3.5	4	5

Note 6: Recommended Boost Peak Current Program Table

ICHG Resistor(kΩ)	Short	100	200	300	400	500
Peak Current (mA)	1500	1500	750	500	425	300

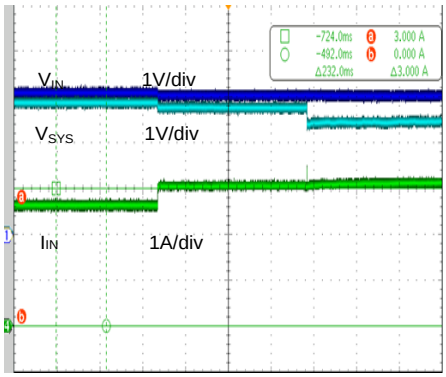
Recommended Formula for R_{ICHG} & Boost Peak Current Calculation

$$I_{Peak} = \begin{cases} 1500\,mA, & R_{ICHG} \le 100\,k\Omega \\ \dfrac{150000}{R_{ICHG}(k\Omega)}\,\text{mA}, & 100\text{k}\,\Omega < R_{ICHG} < 500\,k\Omega \\ 300\,mA, & R_{ICHG} \ge 500\,k\Omega \end{cases},$$

Typical Performance Characteristics

Current Limit

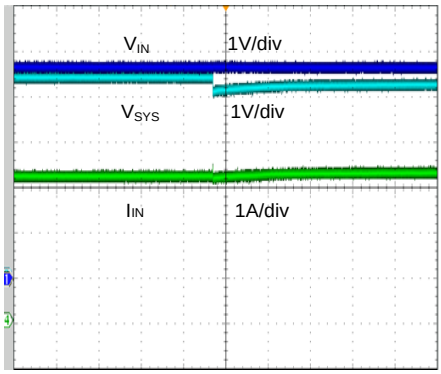
(R_{ILIM}=3.3K(I_{LIM}≈3A) 3.3V version)



Time (200ms/div)

Current Limit

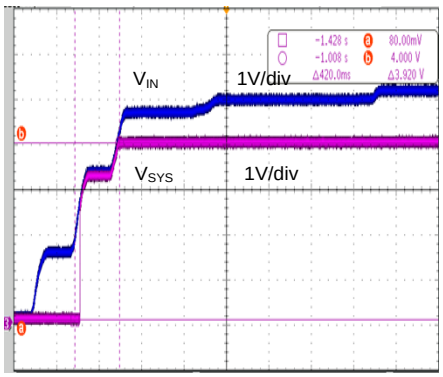
(R_{ILIM}=3.3K(I_{LIM}≈3A) 5V Version)



Time (200ms/div)

OVP

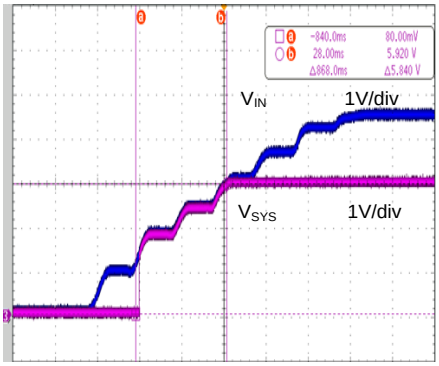
(R_{ILIM}=3.3K(I_{LIM}≈3A) 3.3V Version)



Time (400ms/div)

OVP

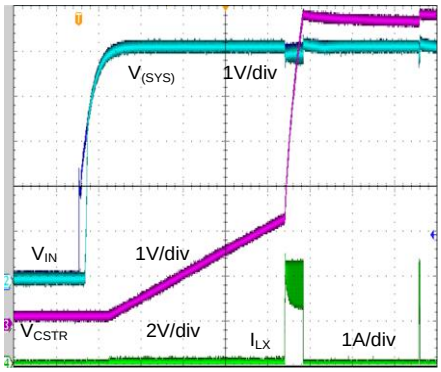
(R_{ILIM}=3.3K(I_{LIM}≈3A) 5V Version)



Time (400ms/div)

Startup

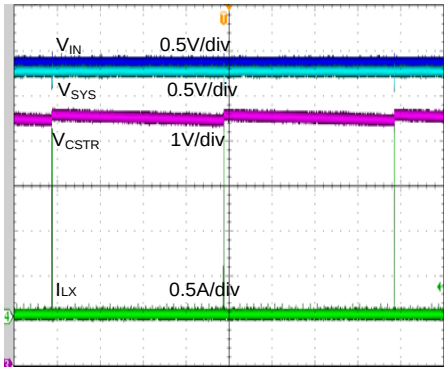
(R_{ILIM}=3.3K(I_{LIM}≈3A) 5V Version)



Time (10ms/div)

BOOST(3.3V version)

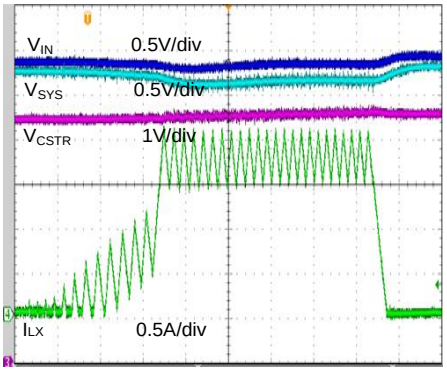
(V_{IN}=3.3V,I_{SYS}=2A,SYS_SET=3V,CSTR_SET=5V)



Time (20ms/div)

BOOST(3.3V version zoom in)

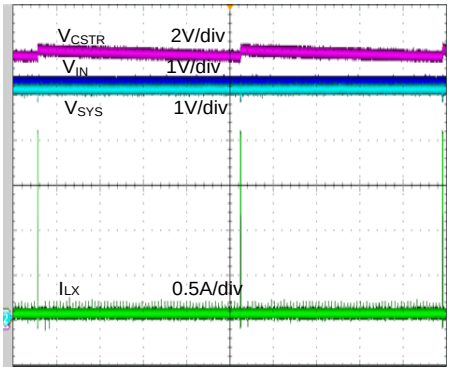
(V_{IN}=3.3V,I_{SYS}=2A,SYS_SET=3V,CSTR_SET=5V)



Time (10us/div)

BOOST(5V version)

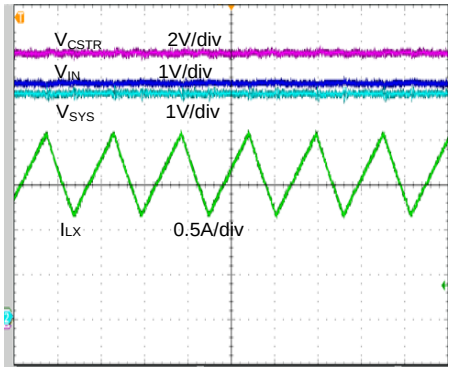
(V_{IN}=5V,I_{SYS}=2A,SYS_SET=4.6V,CSTR_SET=12V)



Time (40ms/div)

BOOST(5V version zoom in)

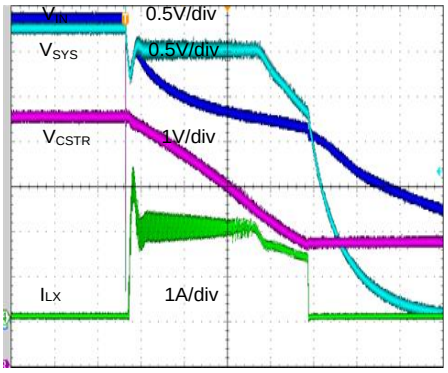
(V_{IN}=5V,I_{SYS}=2A,SYS_SET=4.6V,CSTR_SET=12V)



Time (1us/div)

BUCK(3.3V version)

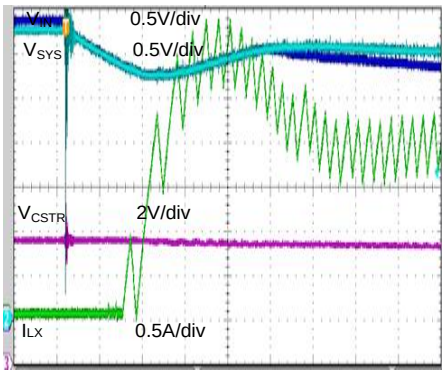
(V_{IN}=3.3V,I_{SYS}=2A,SYS_SET=3V,CSTR_SET=5V)



Time (200us/div)

BUCK(3.3V version zoom in)

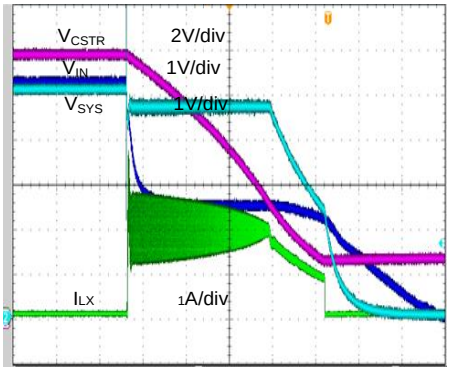
(V_{IN}=3.3V,I_{SYS}=2A,SYS_SET=3V,CSTR_SET=5V)



Time (10us/div)

BUCK(5V version)

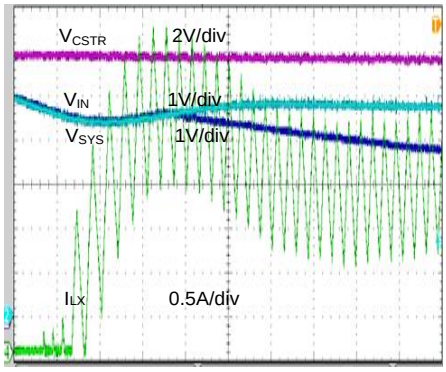
(V_{IN}=5V,I_{SYS}=2A,SYS_SET=4.6V,CSTR_SET=12V)



Time (800us/div)

BUCK(5V version zoom in)

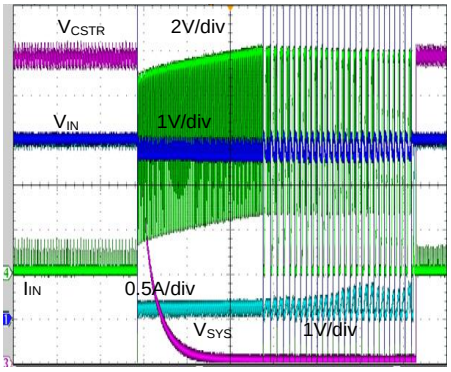
(V_{IN}=5V,I_{SYS}=2A,SYS_SET=4.6V,CSTR_SET=12V)



Time (10us/div)

Short Protection of Pin(SYS) 3.3V version

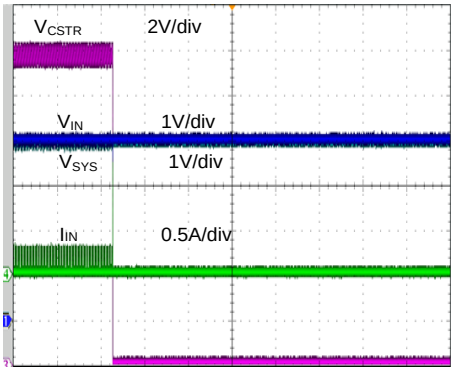
(V_{IN}=3.5V,SYS_SET=3V,CSTR_SET=13.2V)



Time (100ms/div)

Short Protection of Pin(CSTR) 3.3V version

(V_{IN}=3.5V,SYS_SET=3V,CSTR_SET=13.2V)



Time (200ms/div)

Function Description

Startup Sequence

Once voltage on IN pin exceeds UVLO level and EN is high, soft start begins and capacitor on SYS pin is charged with a current which slowly ramp up from 0 to programmed current limit. Soft start time is programmed by the capacitor connected on SST pin. Capacitor on BD pin will also be charged during soft start period. When voltage on SYS pin rise above pre-charge threshold, pre-charge process starts and capacitor on CSTR pin is charged with 100mA pre-charge current. Pre-charge process ends when voltage across disconnect switch is lower than an internal threshold and then disconnect switch will be fully turned on. DC-DC converter starts working when pre-charge end and ENCON is high. It is strongly recommended that ENCON should be enabled after soft start is ended and voltage on SYS pin is well settled down. Because SYS voltage may be pulled down by boost charge current and buck mode will be triggered if SYS voltage isn't high enough.

Bi-directional DC-DC Regulator

DC-DC converter starts working after pre-charge is done. If voltage on FBS pin is higher than 0.63V, converter works at boost mode and charge the storage capacitor. Quasi-fixed frequency constant off time control is used and the peak current is programmed by the resistor connected on ICHG pin. Burst mode is used to minimum power loss. The maxim storage voltage is programmed through FBC pin. Boost converter stop working when voltage on FBC pin reaches 1.2V and start to charge the storage capacitor again when FBC voltage falls below 1.17V.
Buck mode is triggered when voltage on FBS pin falls below 0.6V. Quasi-fixed frequency constant off time control is also used in buck mode. Regulated voltage on SYS pin is programmed through FBS pin. The internal reference of FBS is 0.6V. Peak current of buck converter is internally clamped at 5A. Buck mode will change to boost mode when FBS voltage rise above 0.63V.

Input Load Switch

Over voltage protection, input current limit and reverse blocking functions are all integrated in input load switch control module. SYS voltage will be clamped when IN voltage exceed OVP threshold. Clamped voltage and OVP threshold are both set by OVP pin. Input current limit is programmed by the resistor connected on ILIM pin. Reverse blocking FET will be turned off if any of the following conditions happens:

1. IN voltage falls below UVLO
2. EN is low.
3. V_{SYS} is higher than V_{IN} (V_{SYS}-V_{IN}>20mV)
4. Converter works in buck mode and V_{IN}-V_{SYS}<20mV

Short Circuit Protection at Energy Storage Side

CSTR voltage will be detected after pre-charge process last for 120ms. If CSTR voltage falls below 0.7V, disconnect switch will turn off. If CSTR voltage below 0.7V is detected when DC-DC converter is working, converter will stop working firstly and then disconnect switch will turn off. DC-DC converter will latch off if short circuit is detected on CSTR pin.

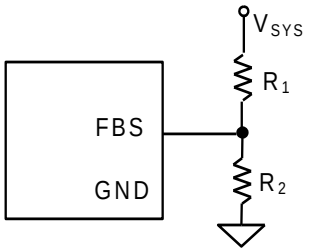
Boost Peak Current Program

There's negative inductor current because of the min on time of the high side MOSFET. The CSTR voltage could not be charged up to the programmed voltage level due to the negative inductor current. In order to charge the CSTR capacitors to desired value, it is recommended to set the boost peak current at a proper level. The maximum T_{MINON} value of HSFET is 160ns. The formula is presented below for proper boost peak current setting reference.
V_{CSTR}-V_{IN}=L dI / dT → dI=(V_{CSTR}-V_{IN})*dT / L=(V_{CSTR}-V_{IN})*160ns / L;
I_{PEAK} ≧ dI / 2 → I_{PEAK} ≧ (V_{CSTR}-V_{IN})*160ns / (2*L);
For example, the CSTR voltage is programmed at 36V and the VIN is 3.3V, the inductor is 4.7uH, then the Ipeak should be:
I_{PEAK} ≧ (V_{CSTR}-V_{IN})*160ns / 2*L=(36-3.3)*160ns/(2*4.7uH)=556mA.

Applications Information

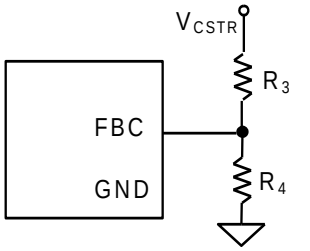
Feedback resistor dividers:

Choose R_1 and R_2 to program the proper SYS voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If V_{SYS} is programmed at 3V, R_1=200k is chosen, then using following equation, R_2 can be calculated to be 50k:



$$R_2 = \frac{0.6V}{V_{SYS} - 0.6V} R_1 .$$

Choose R_3 and R_4 to program desired CSTR OVP threshold. To minimize the power consumption, it is desirable to choose large resistance values for both R_3 and R_4. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If V_{CSTR} OVP is programmed at 6V, R_1=400k is chosen, then using following equation, R_2 can be calculated to be 100k:



$$R_4 = \frac{1.2V}{V_{CSTR\_OVP} - 1.2V} R_3 .$$

Input capacitor C_{IN}:

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. In this case, a 1uF low ESR ceramic capacitor is recommended to minimum inrush current.

SYS capacitor C_{SYS}:

The SYS capacitor is the input capacitor of boost converter and also the output capacitor of buck converter. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For most applications, an X5R or better grade ceramic capacitor greater than 66uF capacitance can work well. The capacitance derating with DC voltage must be considered.

CSTR capacitor C_{CSTR}:

The CSTR capacitor is used to store energy transfer it to SYS load when power supply on IN pin is plug out. SYS voltage can hold a longer time if larger CSTR capacitor is used. The capacitance is calculated as:

$$C_{CSTR} = \frac{2 \times V_{SYS} \times I_{SYS} \times t_{HOLD}}{V_{CSTR}^{\ 2} - V_{SYS}^{\ 2}}$$

where C_{CSTR} is capacitance of CSTR capacitor, V_{SYS} is programmed SYS voltage, I_{SYS} is SYS load current, t_{HOLD} is desired SYS voltage hold time after IN is plug out, and V_{CSTR} is programmed CSTR voltage.

Inductor L:

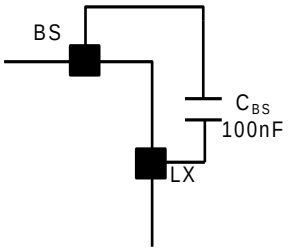
Choose the inductance to provide the desired ripple current. If ripple current equals to 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where Fsw is the switching frequency; $I_{OUT,MAX}$ is the maximum SYS load current; V_{out} is programmed SYS output voltage and $V_{IN,MAX}$ is programmed CSTR voltage.

External Bootstrap Cap

This capacitor provides the gate driver voltage for internal high side MOSFET. A 100nF low ESR ceramic capacitor connected between BS pin and LX pin is recommended.



Input Load Switch Current Limit

Connect a resistor between ILIM and GND to program input load switch current limit. The resistance can be calculated as:

$$R_{ILIM} = \frac{9600}{I_{LIM}}$$

where I_{LIM} is desired current limit value.

Boost Inductor Peak Current Limit

Connect a resistor between ICHG and GND to program boost inductor peak current limit. The resistance can be calculated as:

$$R_{ICHG} = \frac{150000}{I_{PEAK}}$$

where I_{PEAK} is desired boost peak current.

In order to charge the CSTR capacitor to the desired value, it is recommended to program the boost peak current at a proper value. Here is the recommended boost peak current and program resistor calculate formula:

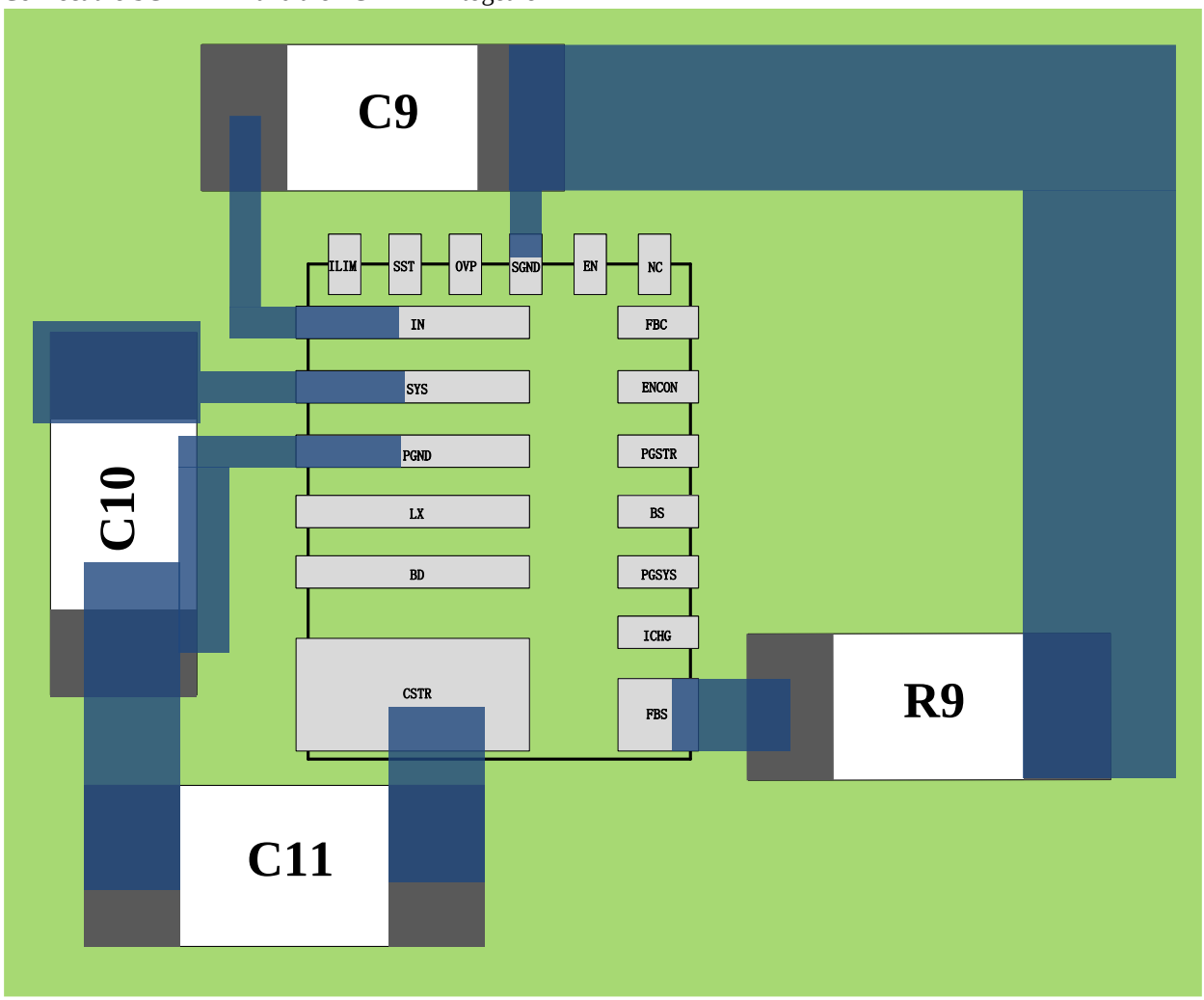
$$I_{peak\_cal} \geq \frac{1}{2} \times \frac{(V_{CSTR\_max} - V_{IN\_min}) \times T_{min\,on\_max}}{L_{min}}$$

where I_{peak_cal} is the calculated boost peak current; V_{CSTR_max} is the maximum CSTR voltage; V_{IN_min} is the minimum input voltage; T_{minon_max} is the maximum high side MOSFET minimum turn on time (160ns); L_{min} is the minimum inductance. Considering the 20% tolerance of the boost peak current program value, the selected ICHG resistance should be chosen as:

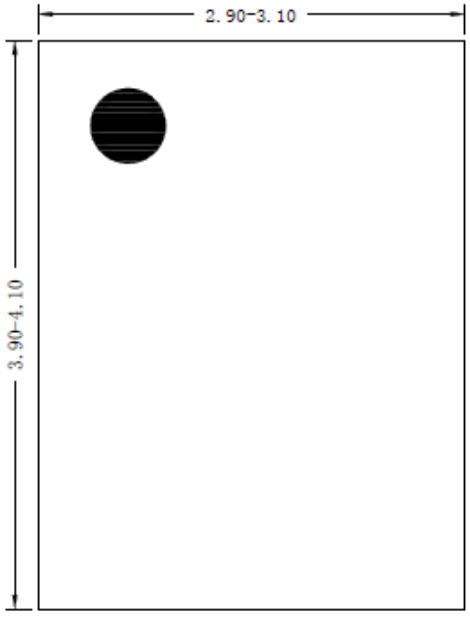
$$R_{ICHG\_sel} = \frac{150000 \times 80\%}{I_{peak\_cal}}$$

PCB Layout Guideline

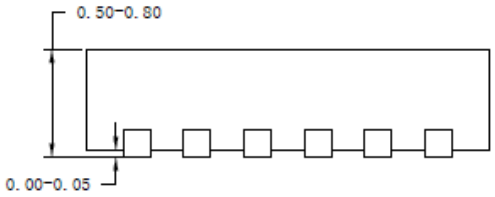
Put C9,C10,C11,R9 as close as possible to the IC
Connect the SGND PIN and the PGND PIN together



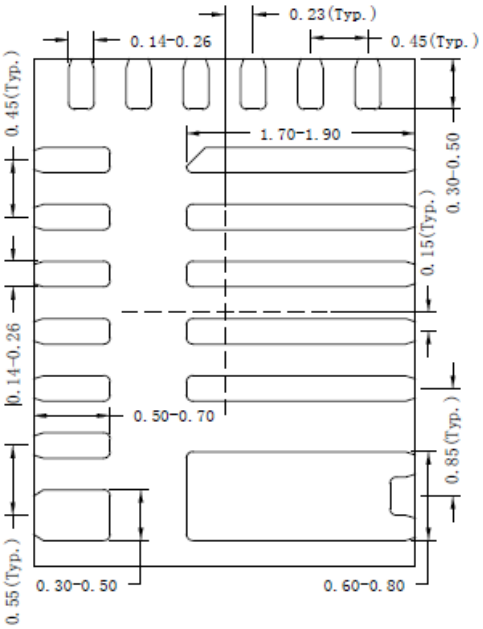
QFN3x4-19-B Package Outline Drawing



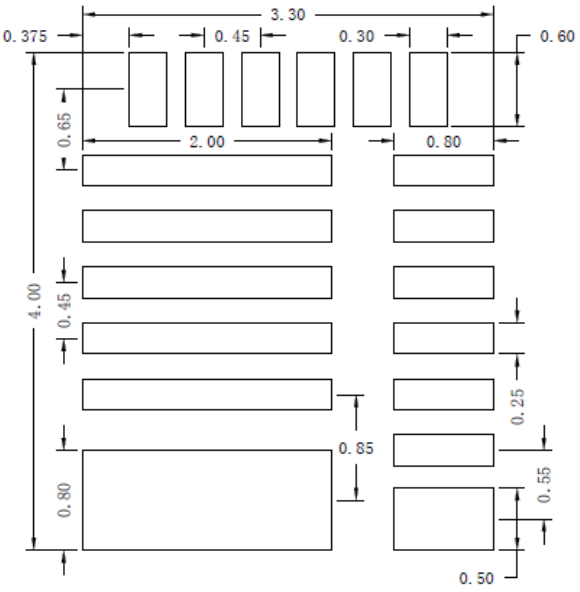
Top view



Side view



Bottom view

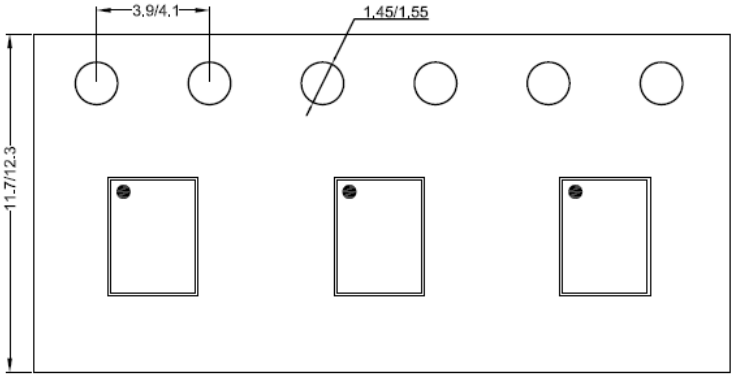


Recommended PCB layout
(Reference only)

Notes: **All dimension in MM and exclude mold flash & metal burr.**

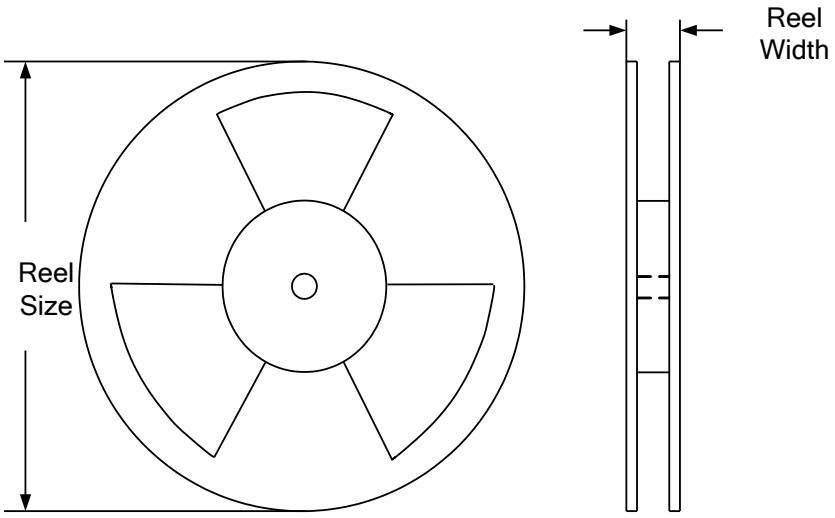
Taping & Reel Specification

1. QFN3x4 taping orientation



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Reel width(mm)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3x4	12	8	13"	12.4	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change	Pages Changed
Aug.24, 2015	Revision 0.9	Initial risk production release.	-
Mar.19, 2025	Revision 1.0	Initial production release.	-

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