SY70301
Quad-Output PMIC

General Description

The SY70301 is a high efficiency, quad-output, synchronous buck regulator that operates over a wide input voltage range of 2.5V to 5.5V. It features a total of four integrated power stages: two that can deliver continuous output current of up to 6A, and two that can deliver continuous output current of up to 4A. This flexibility allows the device to work for a wide range of applications that require high power and multiple outputs.

The SY70301 uses constant on-time (COT) and instant PWM control scheme to achieve fast transient response and loop stabilization. Seamless DCM/CCM transitions maximize efficiency at either heavy or light load. During startup and voltage changes, the device controls the output slew rate to minimize output voltage overshoot and inrush current.

The SY70301 supplies undervoltage lockout (UVLO) along with overvoltage (OVP), overcurrent (OCP), and overtemperature (OTP), protection to ensure reliable system operation.

In addition to the standard interrupt and chip enable, the SY70301 also supports I²C communication protocol.

The SY70301 is available in a QFN4.5mm×5mm-30 package.

Features

- 2.5V to 5.5V Wide Input Voltage Range
- Four Output Channels: Two with 6A Output Current per Channel; Two with 4A Output Current per Channel
- Low IQ in Low Power Mode
- COT Control Achieves Fast Transient Performance
- I²C Programmable Output Voltages from 0.6V to 3.7V
- ±1.0% Output Accuracy
- Independent Dynamic Voltage Scaling (DVS) for Each Output
- Status Feedback with Interrupt Pin
- Reliable OTP/UVP/OVP Protection
- Compact Package: QFN4.5×5-30

Applications

- Smartphones, Tablets
- FPGA and ASIC Power
- Industrial MPU Power

Typical Application

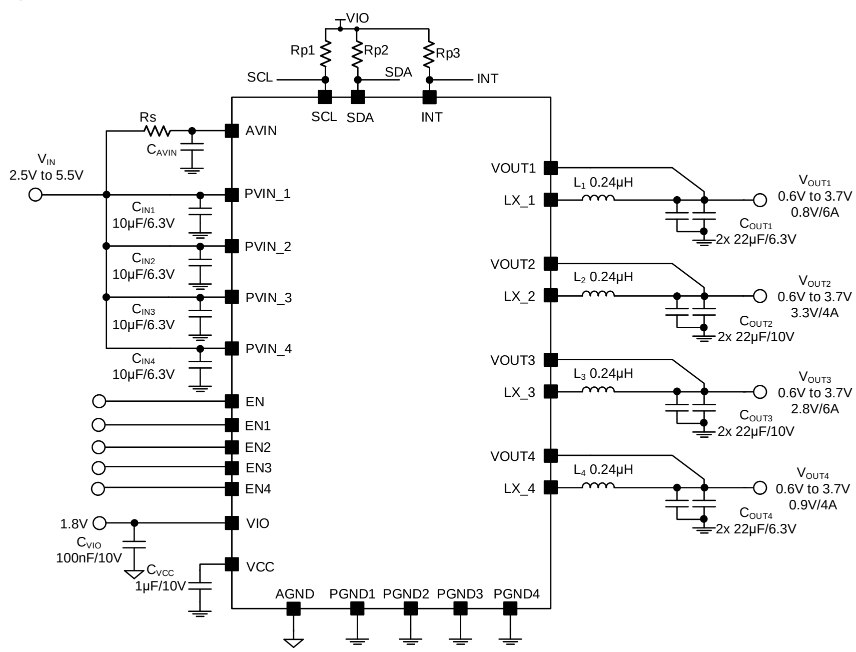


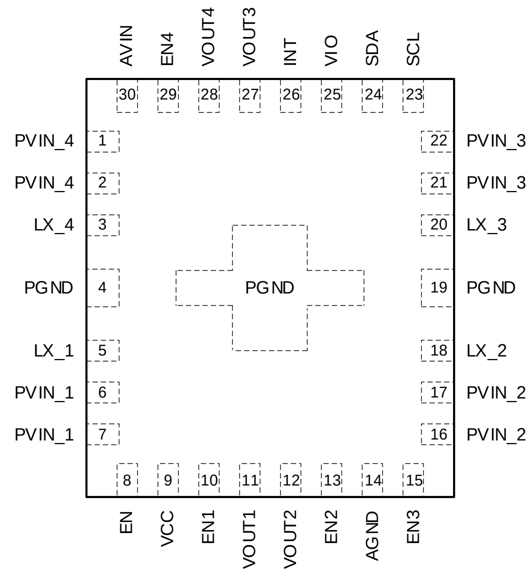
Figure 1. 4-Phase Single Output

Ordering Information

Part Number	Package Type	Top Mark
SY70301WBQ	QFN4.5×5-30 RoHS-Compliant and Halogen-Free	**FRG*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



(QFN4.5×5-30)

Pin Description

Pin No	Pin Name	Type (Note 1)	Description
1, 2	PVIN_4	PS	Power supply for Power Stage 4
3	LX_4	A/O	Switching node for Power Stage 4
4, 19, 31	PGND	G	Power ground
5	LX_1	A/O	Switching node for Power Stage 1
6, 7	PVIN_1	PS	Power supply for Power Stage 1
8	EN	D/I	Global enable pin. Tie to GND to disable the PMIC or tie to VIN to enable the PMIC.
9	VCC	A/O	Internal 2.7V LDO output. Power supply for the internal analog and digital control circuits. Decouple this pin to the AGND pin with at least a 1µF ceramic capacitor.
10	EN1	D/I	VOUT1 enable pin, logic high enable
11	VOUT1	A/I	Output voltage sense for Output 1
12	VOUT2	A/I	Output voltage sense for Output 2
13	EN2	D/I	VOUT2 enable pin, logic high enable
14	AGND	G	Analog ground
15	EN3	D/I	VOUT3 enable pin, logic high enable
16, 17	PVIN_2	PS	Power supply for Power Stage 2
18	LX_2	A/O	Switching node for Power Stage 2
20	LX_3	A/O	Switching node for Power Stage 3
21, 22	PVIN_3	PS	Power supply for Power Stage 3
23	SCL	D/I	I^2C clock pin
24	SDA	D/I/O	I^2C data pin
25	VIO	PS	IO supply voltage for digital communications. SDA/SCL should be pulled up to VIO voltage with a pullup resistor. Normally connected to 1.8V supply.
26	INT	D/O	Interrupt output pin

27	VOUT3	A/I	Remote output voltage sense for Output 3
28	VOUT4	A/I	Remote output voltage sense for Output 4
29	EN4	D/I	VOUT4 enable pin, logic high enable
30	AVIN	PS	Analog supply voltage, 2.5V to 5.5V

Note 1: A: Analog Pin, D: Digital Pin, G: Ground Pin, PS: Power Supply Pin, I: Input Pin, O: Output Pin

Block Diagram

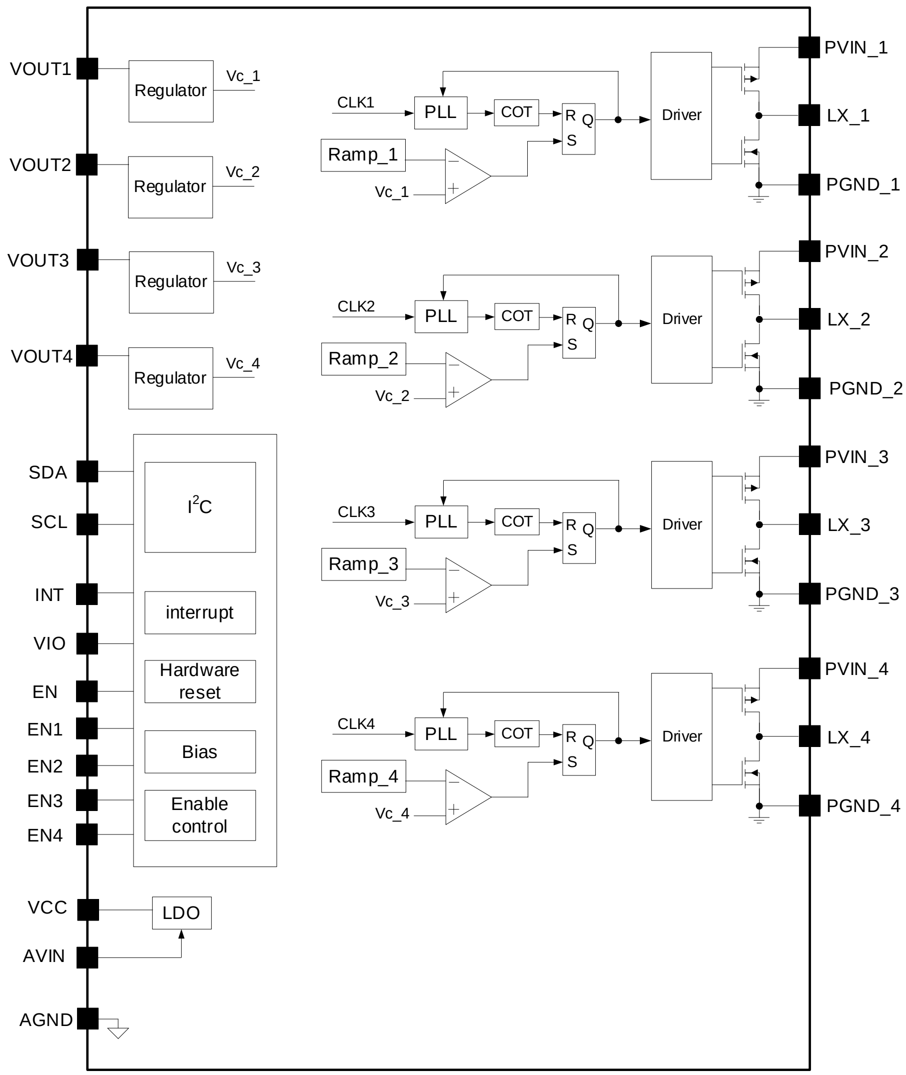


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 2)	Min	Max	Unit
PVIN, AVIN	-0.3	6	V
LX	-0.3 (-2 for <40ns, -3 for <10ns)	PVIN + 0.3	
VIO, EN, SCL, SDA	-0.3	AVIN + 0.3	
OUT	-0.3	6	
Other PINs	-0.3	6	
Junction Temperature		150	°C
Lead Temperature (Soldering, 10s)		260	
Ambient Temperature	-40	105	
Storage Temperature	-65	150	
ESD Susceptibility			
HBM (Human Body Model)	2000		V
CDM (Charge Device Model) All Pins	500		
Latch-Up	200		mA

Thermal Information

Parameter (Note 3)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	26	°C/W
θ_{JC_TOP} Junction-to-Case Top Thermal Resistance	8	
P_D Power Dissipation T_A = 25°C	5	W

Recommended Operating Conditions

Parameter (Note 4)	Min	Max	Unit
PVIN, AVIN	2.5	5.5	V
VIO	1.7	AVIN	
Ambient Temperature	-40	105	°C
Junction Temperature	-40	125	

Electrical Characteristics

(T_A = -40°C–85°C, AVIN/PVIN = 3.3V, unless otherwise specified.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Supply	Supply Voltage	AVIN, PVIN		2.5		5.5	V
	AVIN + PVIN Supply Current		EN1 = EN2 = EN3 = EN4 = 0		30		µA
	AVIN + PVIN Supply Current		VIN = 3.3V, EN1 = EN2 = EN3 = EN4 = VIN, All buck on, no switching, DCM		300		µA
	UVLO Rising Threshold	V_{UVLOR}	Rising	2.52	2.60	2.67	V
	UVLO Falling Threshold	V_{UVLOF}	Falling	2.28	2.34	2.40	V
	Input OVP Rising Threshold	V_{OVPR}	Rising	5.95	6.1	6.25	V
	Input OVP Falling Hysteresis	V_{OVPHYS}			200		mV
	System Delay Time for Turn-On	t_{SYS}			1.4		ms
	System Delay Time Accuracy			-20		20	%
Power Stage	Output Voltage	V_{OUT}	CH1		0.8		V
			CH2		3.3		
			CH3		2.8		
			CH4		0.9		
	VOUT Voltage Range	V_{OUT}		0.6		3.7	V
	VOUT Step Size	V_{STEP}	$V_{OUT} \leq 2.6V$		10		mV
			$V_{OUT} > 2.6V$		20		mV
	VOUT Accuracy	V_{ACC}	CCM, T_A = -40°C to +85°C	-1		1	%
	DVS Default Slew Rate		DVS up, 32/16/8/4/2/1mV/µs		32		mV/µs
			DVS down, 32/16/8/4/2/1mV/µs		8		mV/µs
	DVS Slew Rate Accuracy	V_{DVS}	Default DVS up = 32mV/µs Default DVS down = 8mV/µs	-15		15	%
	Soft-Start Slew Rate		CH1, 2.5/5/10/20mV/µs selectable		2.5		mV/µs
			CH2, 2.5/5/10/20mV/µs selectable		10		mV/µs
			CH3, 2.5/5/10/20mV/µs selectable		10		mV/µs
			CH4, 2.5/5/10/20mV/µs selectable		2.5		mV/µs
	Soft-Start Slew Rate Accuracy	t_{SS}	Slew Rate = 20mV/µs	-15		15	%
	Switching Frequency	f_{SW}			1.8		MHz
	Maximum Output Current	I_{OUT}	CH1/CH3	6			A
			CH2/CH4	4			A
	Top FET R_{ON}	$R_{DS(ON)\_T}$	PVIN = 3.3V		26		mΩ
	Bottom FET R_{ON}	$R_{DS(ON)\_B}$	PVIN = 3.3V		9		mΩ
	Output Discharge Resistance	R_{DIS}	Output disabled		125		Ω
Protection Characteristics	High Side Switch Current Limit	I_{PLMT}	CH1/CH3, T_A = 25°C	8.5		10.5	A
			CH2/CH4, T_A = 25°C	6.5		8.5	
	Low Side Switch Current Limit	I_{VLMT}	CH1/CH3, T_A = 25°C	6		8	A
			CH2/CH4, T_A = 25°C	4		6	

Parameter			Symbol	Test Conditions		Min	Typ	Max	Unit
		Low Side Switch Negative Current Limit	I_{NLMT}	CH1/CH3	T_A = 25°C	-4.2		-2.4	A
				CH2/CH4					
		Thermal Warning Threshold	T_{WN}	Typical = +109°C		-10		10	%
		Thermal Warning Hysteresis	T_{WNHYS}	Typical = +15°C		-10		10	%
		Thermal Shutdown Temperature	T_{SD}	Typical = +155°C		-10		10	%
		Thermal Shutdown Hysteresis	T_{SDHYS}	Typical = +15°C		-10		10	%
		Output OVP Threshold	V_{TH_OVP}			116	126	136	$\%V_{SET}$
		Output UVP Threshold	V_{TH_UVP}			30	40	50	$\%V_{SET}$
		Output OCP Threshold	V_{TH_OCP}			70	80	90	$\%V_{SET}$
IO PINs	EN	Low Level Input Voltage	V_{ENIL}					0.4	V
		High Level Input Voltage	V_{ENIH}			1.2			V
	VIO Pin	Power Supply Voltage				1.7	1.8	AVIN	V
		Supply Current						1	µA
	SCL, SDA	Low Level Input Voltage	V_{I2CIL}					0.3 × VIO	V
		High Level Input Voltage	V_{I2CIH}			0.7 × VIO			V
	Serial Interfaces	I^2C Frequency Capability	f_{I2C}					3.4	MHz

Note 2: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

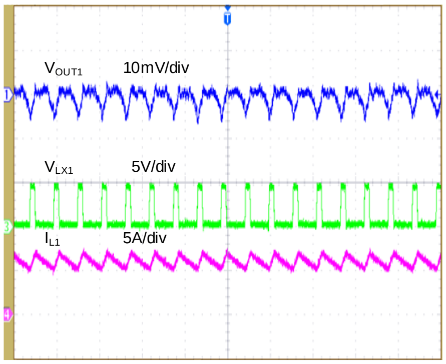
Note 3: θ_{JA} is measured in the natural convection at T_A = 25°C according to JESD51-2, and the PCB is built as a Silergy test board. θ_{JC_TOP} is measured according to JESD51-14

Note 4: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

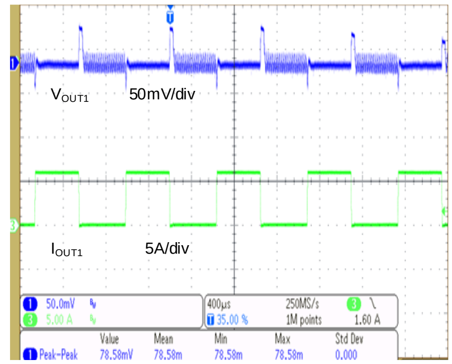
(T_A = 25°C, unless otherwise noted.)

Buck1 Waveform
(V_{IN}=5V, V_{OUT}=0.8V, I_{OUT}=6A, L=0.24μH, C_{OUT}=2x22μF)



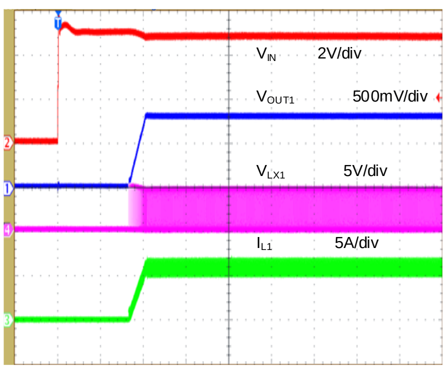
Time (1μs/div)

Buck1 Load Transient
(V_{IN}=5V, V_{OUT}=0.8V, I_{OUT}=0~6A, L=0.24μH, C_{OUT}=2x22μF)



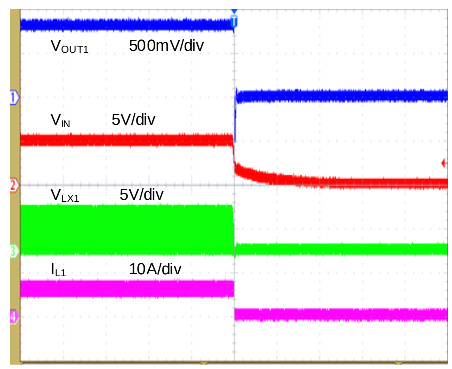
Time (400μs/div)

Buck1 Power On
(V_{IN}=5V, V_{OUT}=0.8V, I_{OUT}=6A, L=0.24μH, C_{OUT}=2x22μF)



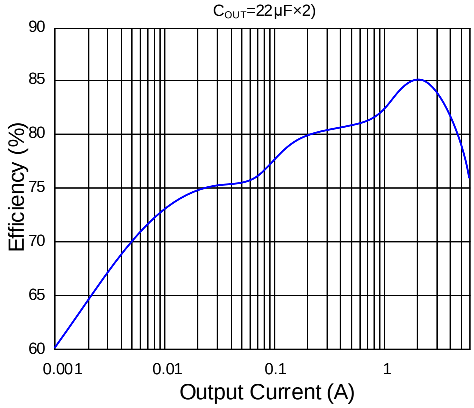
Time (800μs/div)

Buck1 Power Off
(V_{IN}=5V, V_{OUT}=0.8V, I_{OUT}=6A, L=0.24μH, C_{OUT}=2x22μF)

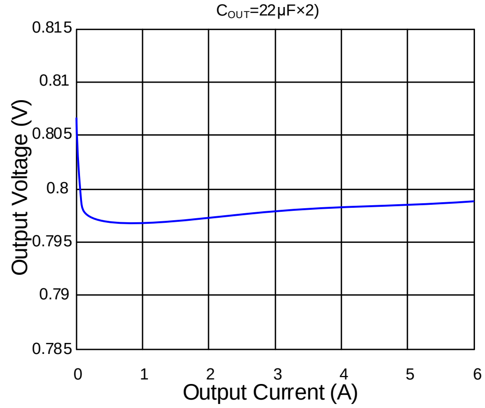


Time (800μs/div)

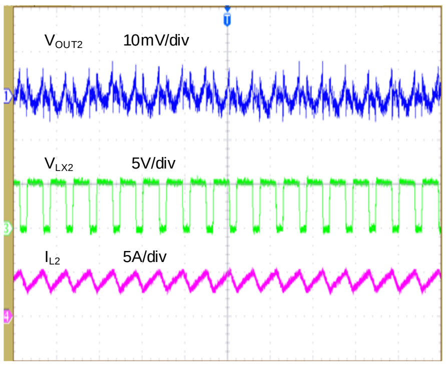
Buck1 Efficiency
(V_{IN}=5V, V_{OUT}=0.8V, L=0.24μH/DFE201610E-R24M, C_{OUT}=22μF×2)



Buck1 Load Regulation
(V_{IN}=5V, V_{OUT}=0.8V, L=0.24μH/DFE201610E-R24M, C_{OUT}=22μF×2)

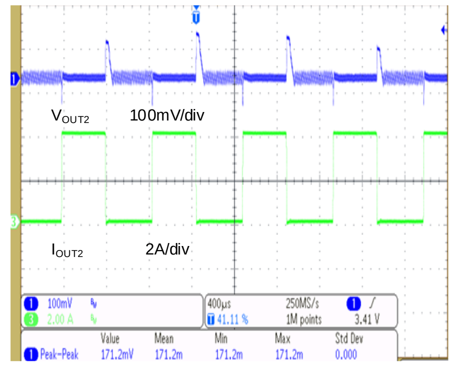


Buck2 Waveform
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=4A, L=0.24μH, C_{OUT}=2x22μF)



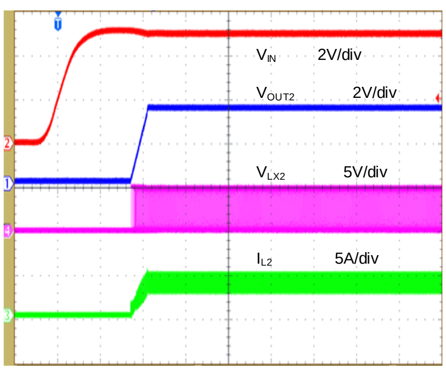
Time (1μs/div)

Buck2 Load Transient
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0~4A, L=0.24μH, C_{OUT}=2x22μF)



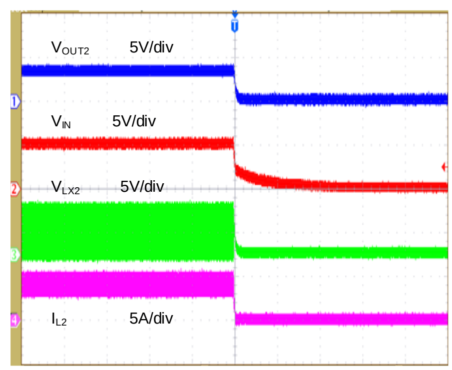
Time (400μs/div)

Buck2 Power On
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=4A, L=0.24μH, C_{OUT}=2x22μF)



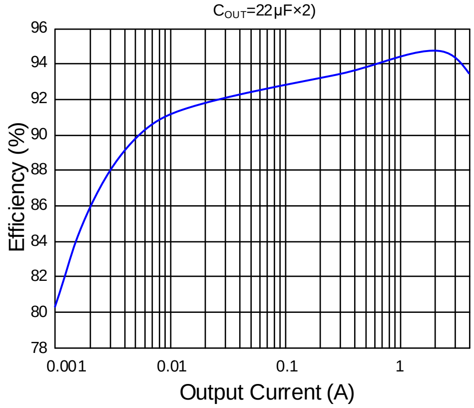
Time (800μs/div)

Buck2 Power Off
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=4A, L=0.24μH, C_{OUT}=2x22μF)

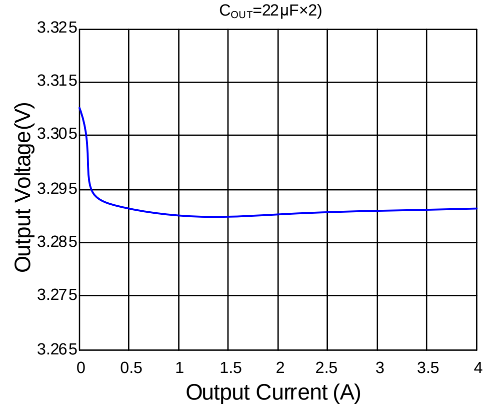


Time (800μs/div)

Buck2 Efficiency
(V_{IN}=5V, V_{OUT}=3.3V, L=0.24μH/DFE201610E-R24M, C_{OUT}=22μF×2)

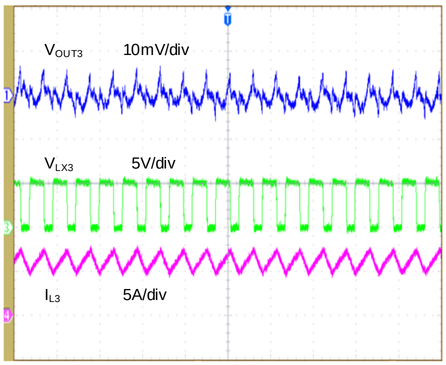


Buck2 Load Regulation
(V_{IN}=5V, V_{OUT}=3.3V, L=0.24μH/DFE201610E-R24M, C_{OUT}=22μF×2)



Buck3 Waveform

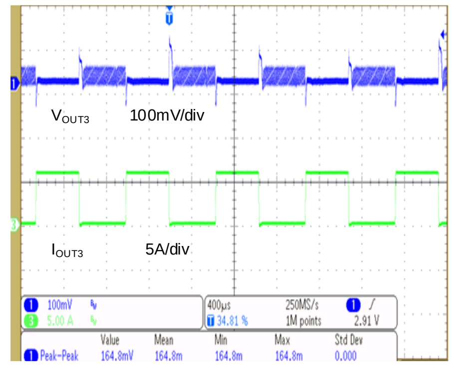
(V_{IN}=5V, V_{OUT}=2.8V, I_{OUT}=6A, L=0.24μH, C_{OUT}=2x22μF)



Time (1μs/div)

Buck3 Load Transient

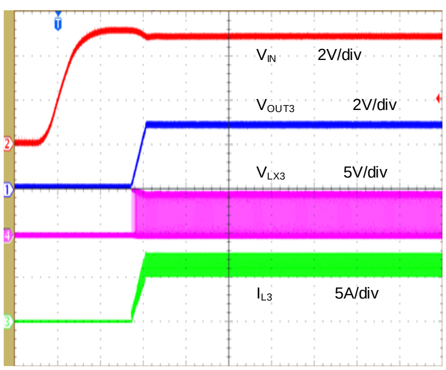
(V_{IN}=5V, V_{OUT}=2.8V, I_{OUT}=0~6A, L=0.24μH, C_{OUT}=2x22μF)



Time (400μs/div)

Buck3 Power On

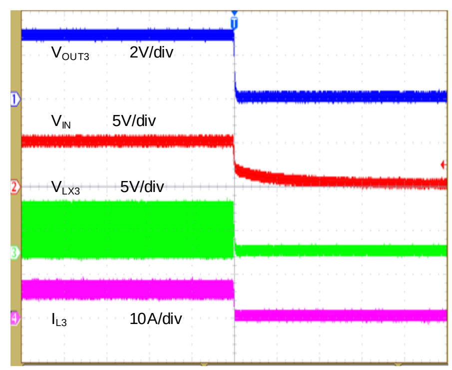
(V_{IN}=5V, V_{OUT}=2.8V, I_{OUT}=6A, L=0.24μH, C_{OUT}=2x22μF)



Time (800μs/div)

Buck3 Power Off

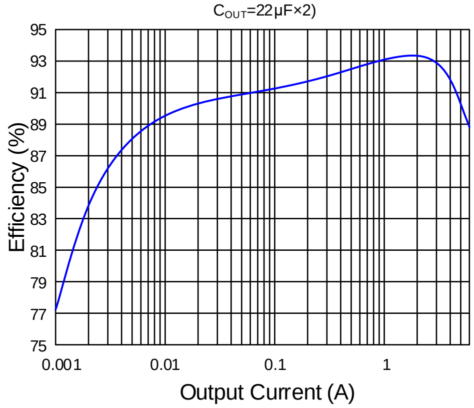
(V_{IN}=5V, V_{OUT}=2.8V, I_{OUT}=6A, L=0.24μH, C_{OUT}=2x22μF)



Time (800μs/div)

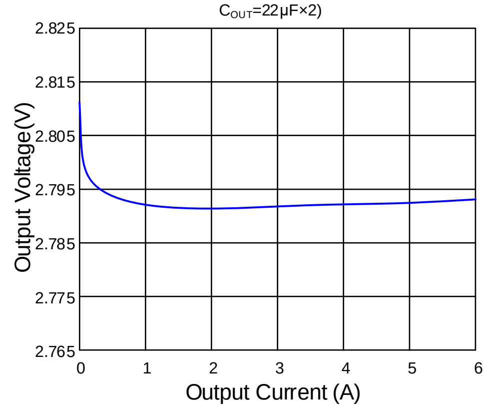
Buck3 Efficiency

(V_{IN}=5V, V_{OUT}=2.8V, L=0.24μH/DFE201610E-R24M, C_{OUT}=22μF×2)

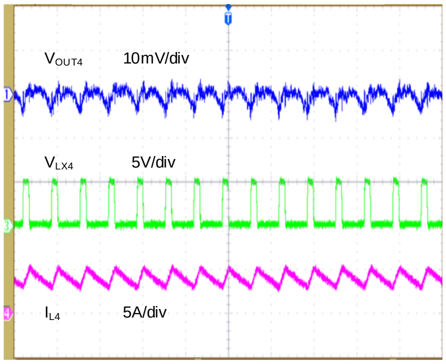


Buck3 Load Regulation

(V_{IN}=5V, V_{OUT}=2.8V, L=0.24μH/DFE201610E-R24M, C_{OUT}=22μF×2)

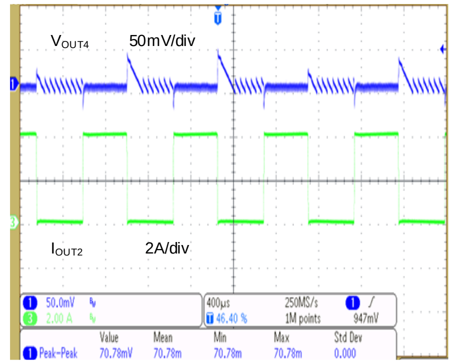


Buck4 Waveform
(V_{IN}=5V, V_{OUT}=0.9V, I_{OUT}=4A, L=0.24μH, C_{OUT}=2x22μF)



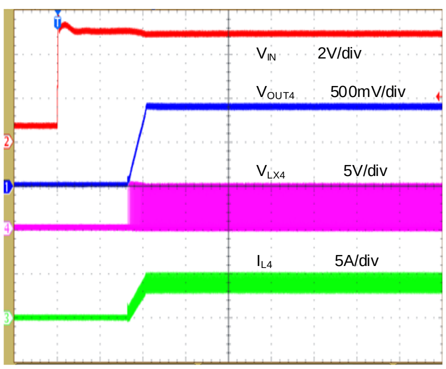
Time (1μs/div)

Buck4 Load Transient
(V_{IN}=5V, V_{OUT}=0.9V, I_{OUT}=0~4A, L=0.24μH, C_{OUT}=2x22μF)



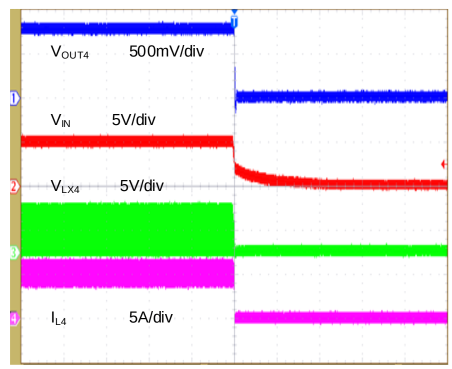
Time (400μs/div)

Buck4 Power On
(V_{IN}=5V, V_{OUT}=0.9V, I_{OUT}=4A, L=0.24μH, C_{OUT}=2x22μF)



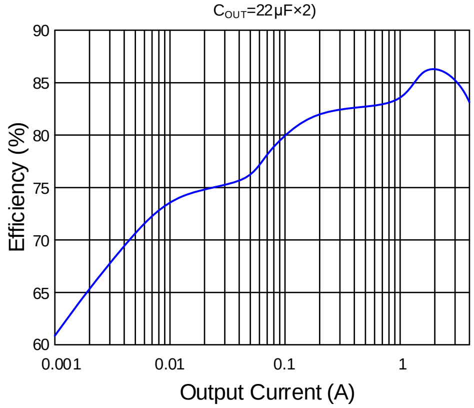
Time (800μs/div)

Buck4 Power Off
(V_{IN}=5V, V_{OUT}=0.9V, I_{OUT}=4A, L=0.24μH, C_{OUT}=2x22μF)

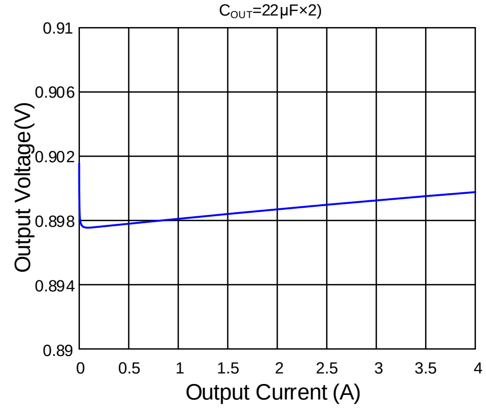


Time (800μs/div)

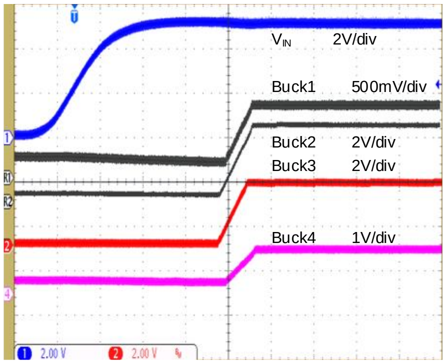
Buck4 Efficiency
(V_{IN}=5V, V_{OUT}=0.9V, L=0.24μH/DFE201610E-R24M,
C_{OUT}=22μF×2)



Buck4 Load Regulation
(V_{IN}=5V, V_{OUT}=0.9V, L=0.24μH/DFE201610E-R24M,
C_{OUT}=22μF×2)

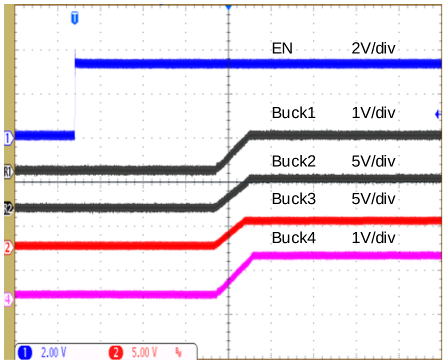


Power On Sequence
(V_{IN}=5V)



Time (400μs/div)

EN On Sequence
(V_{IN}=5V)



Time (400μs/div)

Detailed Description

The SY70301 is a high efficiency, quad-output, synchronous buck regulator that operates over a wide input voltage range of 2.5V to 5.5V. It features a total of four integrated power stages: two that can deliver continuous output current of up to 6A, and two that can deliver continuous output current of up to 4A. This flexibility allows the device to work for a wide range of applications that require high power and multiple outputs. Each of the power stages operates using a quasi-fixed operating frequency of 1.8MHz.

Constant On-Time and Ripple-Based Control Strategy

SY70301 uses a constant on-time, instant PWM architecture to achieve fast transient response for applications and high efficiency at light loads. The device uses a ripple-based control strategy, in which a virtual replica of the inductor current signal is synthesized internally and combined with the feedback voltage. When the sum voltage is lower than the reference voltage generated by a DAC, the bottom MOSFET turns off and the top MOSFET turns on for a fixed period of time (constant t_{ON}). t_{ON} is internally calculated according to the input voltage, output voltage, and desired switching frequency (f_{SW}):

$$t_{ON} = \frac{V_{OUT}/V_{IN}}{f_{SW}}$$

During each switching cycle, the top MOSFET turns off after a period of t_{ON} and the lower MOSFET turns on.

Minimum and Maximum Duty Cycle

In COT architecture, there is no limitation for operating the part at a low duty cycle because when the on-time is close to the minimum on-time, the switching frequency is reduced as needed to always ensure proper operation. The device can support a maximum duty cycle of up to 100% across the entire operating temperature range of -40˚C–85˚C.

Output Voltage Setting and DVS

The output voltage can be programmed using the 8-bit register BUCK1_DVS0CFG1. The corresponding output voltage of the DAC code is shown in Table 1. For more details, see register BUCK1_DVS0CFG1.

The ramp-up slew rate BUCKx_RSPUP [2:0] bits and the ramp-down slew rate BUCKx_RSPDN [2:0] bits in the BUCKx_RSPCFG1 register set the slew rates (DVS speed) in BUCKx during normal DVS transition. For more details, see register BUCK1_RSPCFG.

Table 1. Register Code vs. Setting VOUT

DAC Code	Vo/V	DAC Code	Vo/V	DAC Code	Vo/V	DAC Code	Vo/V
0000 0000	0.6	0100 0001	1.25	1000 0010	1.9	1100 0011	2.55
0000 0001	0.61	0100 0010	1.26	1000 0011	1.91	1100 0100	2.56
0000 0010	0.62	0100 0011	1.27	1000 0100	1.92	1100 0101	2.57
0000 0011	0.63	0100 0100	1.28	1000 0101	1.93	1100 0110	2.58
0000 0100	0.64	0100 0101	1.29	1000 0110	1.94	1100 0111	2.59
0000 0101	0.65	0100 0110	1.3	1000 0111	1.95	1100 1000	2.6
0000 0110	0.66	0100 0111	1.31	1000 1000	1.96	1100 1001	2.62
0000 0111	0.67	0100 1000	1.32	1000 1001	1.97	1100 1010	2.64
0000 1000	0.68	0100 1001	1.33	1000 1010	1.98	1100 1011	2.66
0000 1001	0.69	0100 1010	1.34	1000 1011	1.99	1100 1100	2.68
0000 1010	0.7	0100 1011	1.35	1000 1100	2	1100 1101	2.7
0000 1011	0.71	0100 1100	1.36	1000 1101	2.01	1100 1110	2.72
0000 1100	0.72	0100 1101	1.37	1000 1110	2.02	1100 1111	2.74
0000 1101	0.73	0100 1110	1.38	1000 1111	2.03	1101 0000	2.76
0000 1110	0.74	0100 1111	1.39	1001 0000	2.04	1101 0001	2.78
0000 1111	0.75	0101 0000	1.4	1001 0001	2.05	1101 0010	2.8
0001 0000	0.76	0101 0001	1.41	1001 0010	2.06	1101 0011	2.82

DAC Code	Vo/V	DAC Code	Vo/V	DAC Code	Vo/V	DAC Code	Vo/V
0001 0001	0.77	0101 0010	1.42	1001 0011	2.07	1101 0100	2.84
0001 0010	0.78	0101 0011	1.43	1001 0100	2.08	1101 0101	2.86
0001 0011	0.79	0101 0100	1.44	1001 0101	2.09	1101 0110	2.88
0001 0100	0.8	0101 0101	1.45	1001 0110	2.1	1101 0111	2.9
0001 0101	0.81	0101 0110	1.46	1001 0111	2.11	1101 1000	2.92
0001 0110	0.82	0101 0111	1.47	1001 1000	2.12	1101 1001	2.94
0001 0111	0.83	0101 1000	1.48	1001 1001	2.13	1101 1010	2.96
0001 1000	0.84	0101 1001	1.49	1001 1010	2.14	1101 1011	2.98
0001 1001	0.85	0101 1010	1.5	1001 1011	2.15	1101 1100	3
0001 1010	0.86	0101 1011	1.51	1001 1100	2.16	1101 1101	3.02
0001 1011	0.87	0101 1100	1.52	1001 1101	2.17	1101 1110	3.04
0001 1100	0.88	0101 1101	1.53	1001 1110	2.18	1101 1111	3.06
0001 1101	0.89	0101 1110	1.54	1001 1111	2.19	1110 0000	3.08
0001 1110	0.9	0101 1111	1.55	1010 0000	2.2	1110 0001	3.1
0001 1111	0.91	0110 0000	1.56	1010 0001	2.21	1110 0010	3.12
0010 0000	0.92	0110 0001	1.57	1010 0010	2.22	1110 0011	3.14
0010 0001	0.93	0110 0010	1.58	1010 0011	2.23	1110 0100	3.16
0010 0010	0.94	0110 0011	1.59	1010 0100	2.24	1110 0101	3.18
0010 0011	0.95	0110 0100	1.6	1010 0101	2.25	1110 0110	3.2
0010 0100	0.96	0110 0101	1.61	1010 0110	2.26	1110 0111	3.22
0010 0101	0.97	0110 0110	1.62	1010 0111	2.27	1110 1000	3.24
0010 0110	0.98	0110 0111	1.63	1010 1000	2.28	1110 1001	3.26
0010 0111	0.99	0110 1000	1.64	1010 1001	2.29	1110 1010	3.28
0010 1000	1	0110 1001	1.65	1010 1010	2.3	1110 1011	3.3
0010 1001	1.01	0110 1010	1.66	1010 1011	2.31	1110 1100	3.32
0010 1010	1.02	0110 1011	1.67	1010 1100	2.32	1110 1101	3.34
0010 1011	1.03	0110 1100	1.68	1010 1101	2.33	1110 1110	3.36
0010 1100	1.04	0110 1101	1.69	1010 1110	2.34	1110 1111	3.38
0010 1101	1.05	0110 1110	1.7	1010 1111	2.35	1111 0000	3.4
0010 1110	1.06	0110 1111	1.71	1011 0000	2.36	1111 0001	3.42
0010 1111	1.07	0111 0000	1.72	1011 0001	2.37	1111 0010	3.44
0011 0000	1.08	0111 0001	1.73	1011 0010	2.38	1111 0011	3.46
0011 0001	1.09	0111 0010	1.74	1011 0011	2.39	1111 0100	3.48
0011 0010	1.1	0111 0011	1.75	1011 0100	2.4	1111 0101	3.5
0011 0011	1.11	0111 0100	1.76	1011 0101	2.41	1111 0110	3.52
0011 0100	1.12	0111 0101	1.77	1011 0110	2.42	1111 0111	3.54
0011 0101	1.13	0111 0110	1.78	1011 0111	2.43	1111 1000	3.56
0011 0110	1.14	0111 0111	1.79	1011 1000	2.44	1111 1001	3.58
0011 0111	1.15	0111 1000	1.8	1011 1001	2.45	1111 1010	3.6
0011 1000	1.16	0111 1001	1.81	1011 1010	2.46	1111 1011	3.62
0011 1001	1.17	0111 1010	1.82	1011 1011	2.47	1111 1100	3.64
0011 1010	1.18	0111 1011	1.83	1011 1100	2.48	1111 1101	3.66
0011 1011	1.19	0111 1100	1.84	1011 1101	2.49	1111 1110	3.68
0011 1100	1.2	0111 1101	1.85	1011 1110	2.5	1111 1111	3.7

DAC Code	Vo/V	DAC Code	Vo/V	DAC Code	Vo/V	DAC Code	Vo/V
0011 1101	1.21	0111 1110	1.86	1011 1111	2.51		
0011 1110	1.22	0111 1111	1.87	1100 0000	2.52		
0011 1111	1.23	1000 0000	1.88	1100 0001	2.53		
0100 0000	1.24	1000 0001	1.89	1100 0010	2.54		

Power Sequencing

Power-Up Operation and Enable Logic

When input voltage rises above the UVLO rising threshold, the chip is enabled internally, key biasing circuits power up, and OTP configuration registers are loaded. When the EN pin turn-on signal is detected, the buck enters forced CCM mode and starts a power-up sequence at a specified slew rate, as shown in Figure 3.

Figure 5 illustrates the two mechanisms for enabling the SY70301 buck converters:

- EN pin
- Software EN bit: BUCKx_EN_DVS in register BUCKx_DVSxCFG0

The slew rate of each buck during its soft-start can be configured using register BUCKx_SLEWCTRL. The software EN bit default value is 1, so each channel is I²C enabled by default.

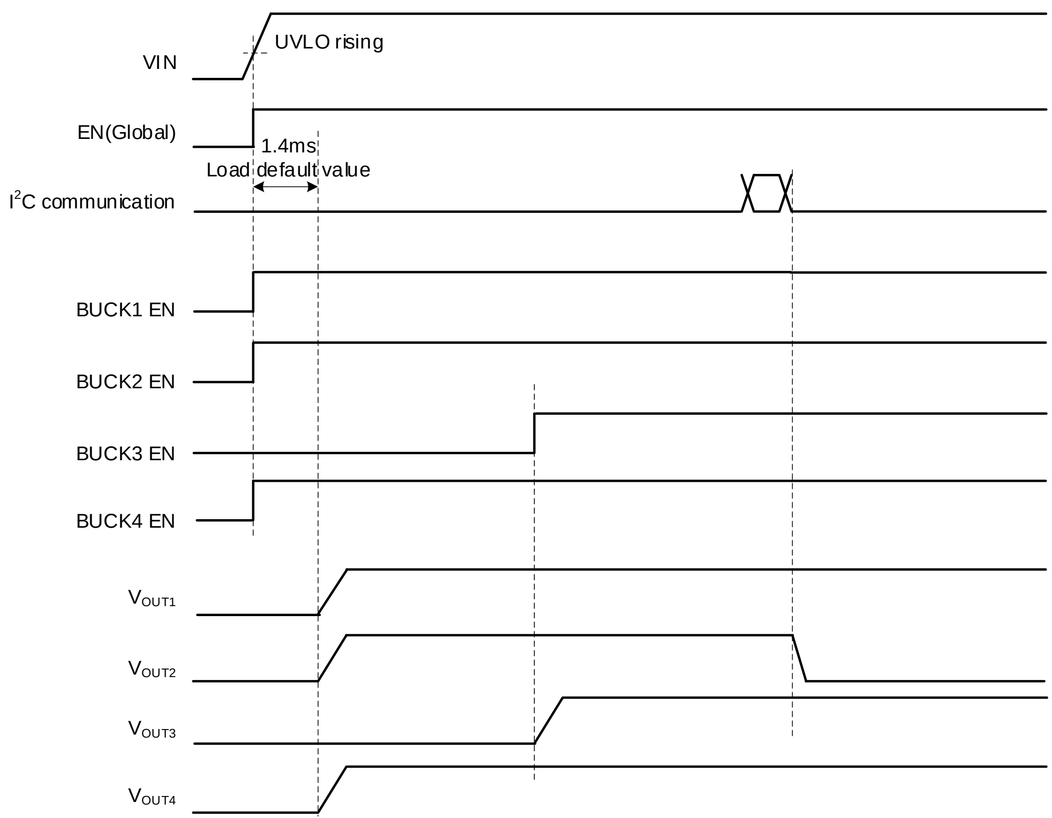


Figure 3. Power-Up Sequencing

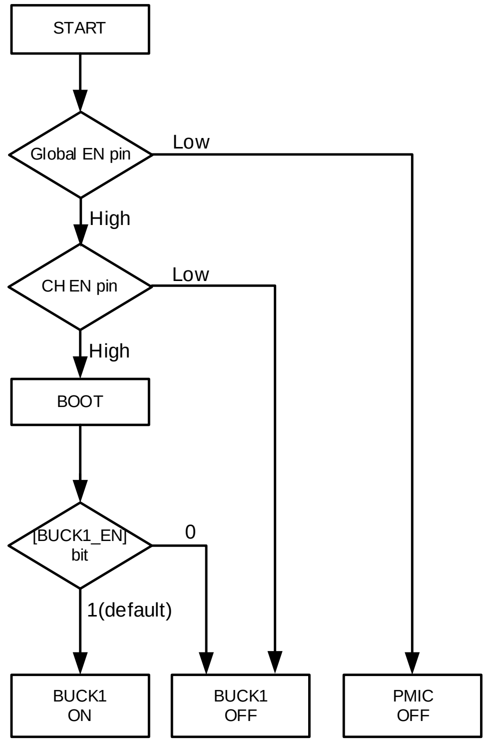


Figure 4. Enable Logic (Buck 1 Example)

Shutdown Operation

To trigger the channel shutdown operation, pull the EN pin low or set the bit BUCKx_EN_DVS in register BUCKx_DVSxCFG0 to 0. When the turn-off signal is detected, the buck turns off the high-side switch and turns on the low-side switch until the inductor current reaches zero. A discharge resistor enabled by bit VOUT_DISCHARGE_EN in register BUCKx_CFG0 can be used to pull down the output.

PFM/PWM Operation

The converter can be operated in either forced PWM mode or automatic PFM/PWM mode, selected by register BUCKx_DVS0CFG0. In forced PWM mode, the converter always operates in forced continuous conduction mode, even at light load. The advantage is that the converter operates with a fixed frequency that allows simple filtering of the switching frequency for noise-sensitive applications. The disadvantage of forced PWM mode is that efficiency is lower than PFM efficiency during light loads. In automatic PFM/PWM mode, the converter operates in regulated frequency PWM mode at moderate to heavy loads and in PFM mode during light loads. This maintains high efficiency over a wide load current.

Protection Features

The SY70301 has integrated overcurrent (OCP), overvoltage (OVP), undervoltage (UVP), and overtemperature (OTP) protection features, as shown in Table 2.

Table 2. Protection Features

Protection	Threshold	Deglitch Time	Operation
Thermal Shutdown	Rising: 155°C Falling: 140°C	-	Controlled by FLT_OT_CTRL Shut down when temperature > 155°C Restart when temperature < 140°C
Thermal Warning	Rising: 109°C Falling: 94°C	-	Thermal warning bit
Output OCP	80% of V_{SET}	200µs	Latch-off or hiccup mode
Output OVP	126% of V_{SET}	2µs	Stop switching when V_{OUT} > 126% of V_{SET} Resume switching when V_{OUT} < 126% of V_{SET}
Output UVP	40% of V_{SET}	10µs	Controlled by corresponding FLT_BUCKx_CTRL Latch-off or hiccup mode (default hiccup)
Input OVP	6.1V	4µs	Shut down when V_{IN} > 6.1V, restart when V_{IN} < 5.9V

Overtemperature Protection

The SY70301 provides thermal warning and thermal shutdown protection. If the junction temperature exceeds 109°C, the thermal warning bit FLT_TEMP_DIE is set to 1. The bit can be reset to 0 after an I²C read if the temperature drops below 94°C. The thermal warning function is activated once the global EN pin is pulled high.

As the temperature increases, the device enters thermal shutdown if the junction temperature exceeds 155°C (typ.). In this mode, the high side switch and low side switch are both turned off. When the junction temperature falls below 140°C (typ.), the buck is re-enabled automatically, as shown in Figure 5.

Overtemperature protection can be disabled by register FLT_OT_CTRL.

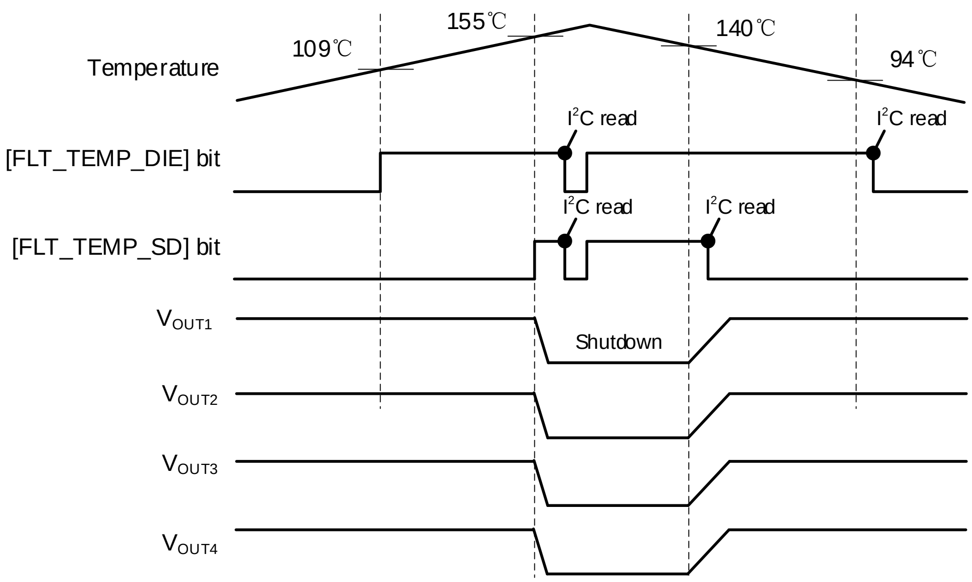


Figure 5. Thermal Warning and Thermal Shutdown

Overcurrent Protection Mode

The SY70301 features a cycle-by-cycle current limit to protect the device against overcurrent. When the current in the high-side MOSFET reaches its current limit, the high side MOSFET is turned off and the low side MOSFET is turned on. The regulator continues to limit the current on a cycle-by-cycle basis. As the load current increases, the output voltage drops. As soon as the output voltage drops below 80% of V_{SET} for a duration of 200µs, the buck is turned off for a period of soft-start time × 7, then restarted. If the overload condition remains, the buck is turned off for another period of soft-start time × 7. This restart will repeat until the overload condition is removed. Overcurrent fault detection is disabled during the normal power-up, shutdown, and DVS periods. See Figure 6.

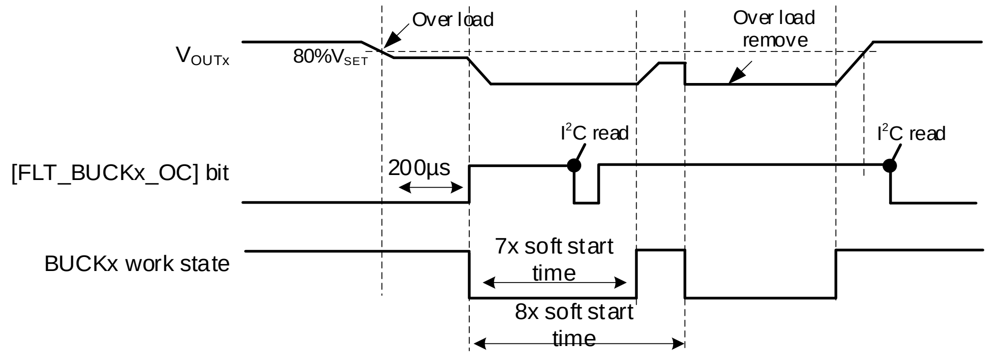


Figure 6. Overcurrent Protection

Output Overvoltage/Undervoltage Protection

The SY70301 protects against output overvoltage (OV) and undervoltage (UV) fault conditions. When the output voltage reaches 126% of V_{SET} for a duration of 2µs, the buck converter enters no-switching mode. Both high side and low side MOSFETS are turned off when a zero crossing is detected. The buck resumes normal operation when the output voltage drops below 126% of V_{SET}. Output OV fault detection is disabled during the normal power-up, shutdown, and DVS periods. See Figure 7.

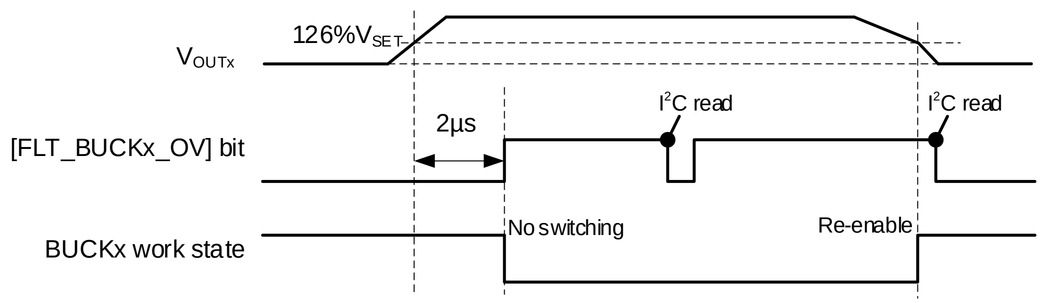


Figure 7. Output OV Protection

When the output voltage drops below 40% of V_{SET} for 10µs, the buck is turned off. The SY70301 provides hiccup and latch-off protection modes, selected by register FLT_BUCKx_CTRL. If latch-off mode is selected, the buck will not re-enable after a UV event, as shown in Figure 8. The latched state can only be cleared by cycling the PVIN/AVIN pins or by cycling the EN pin. If UV hiccup mode is selected, the buck restarts after a period of soft-start time × 7, as shown in Figure 9. This restart will repeat until the UV condition is removed. Output UV fault detection is disabled during the normal power-up, shutdown, and DVS periods.

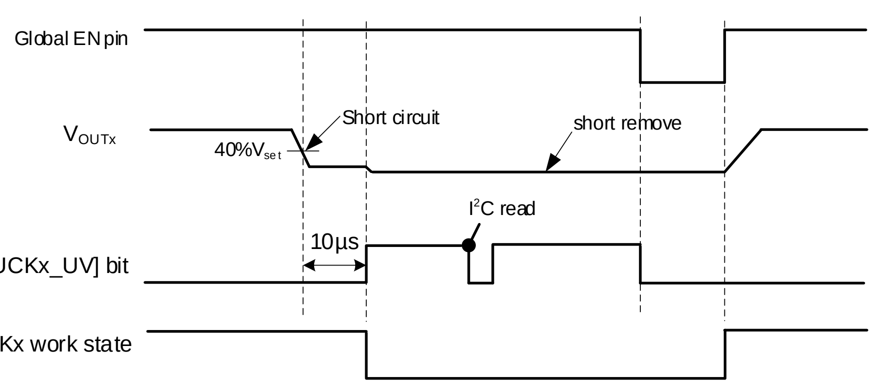


Figure 8. UV Protection: Latch-Off Mode

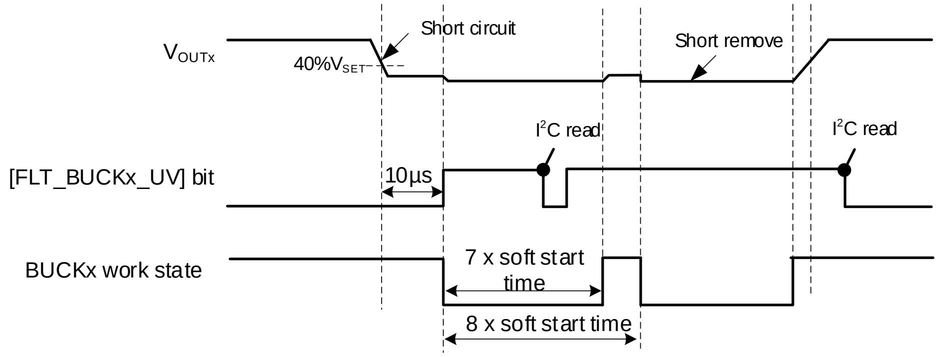


Figure 9. UV Protection: Hiccup Mode

Input Overvoltage Protection

The SY70301 provides overvoltage (OV) fault detection to protect the input, as shown in Figure 10. If PVIN exceeds 6.1V, all channels are turned off. The OV protection hysteresis is 200mV. When PVIN decreases to 5.9V, all channels restart. Input OV fault detection is activated once the global EN pin is pulled high.

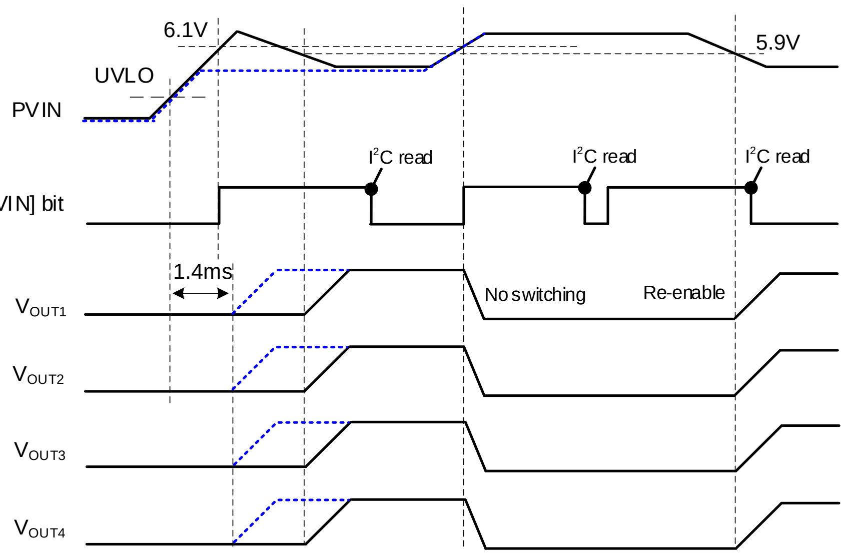


Figure 10. Input OV Protection

Interrupt Pin

The SY70301 can alert the host when a fault has occurred through an IRQ interrupt request signal. This signal has configurable masking options and is connected to a configurable interrupt (INT) pin that is set internally as an active-low, open-drain output.

When a fault occurs, the corresponding fault record bit is set to 1 until the fault is cleared. When the fault is cleared, the corresponding fault record bit is set to 0 after it is read.

When a fault occurs and the corresponding fault record is not masked, the INT pin is pulled low. Once all fault records are cleared, the INT pin is released to high impendace. Figure 11 shows the interrupt tree structure.

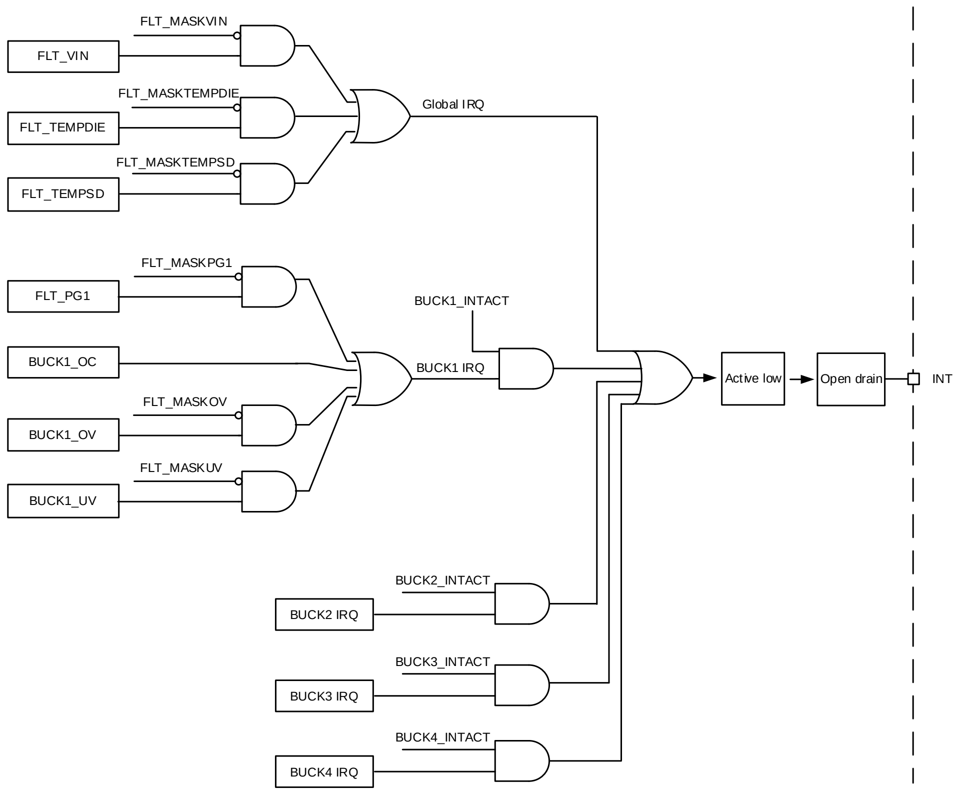


Figure 11. Interrupt Tree

Input Overvoltage Interrupt

The SY70301 provides a FLT_VIN bit in register FLT_RECORDTEMP to indicate an input OV fault. If the input voltage is higher than the OV protection threshold, the bit is set to 1 and the INT pin is pulled low, as shown in Figure 12. The bit can be reset to 0 after it is read if the OV protection state is cleared. This interrupt can be masked by bit FLT_MASKVIN in register FLT_MASKTEMP.

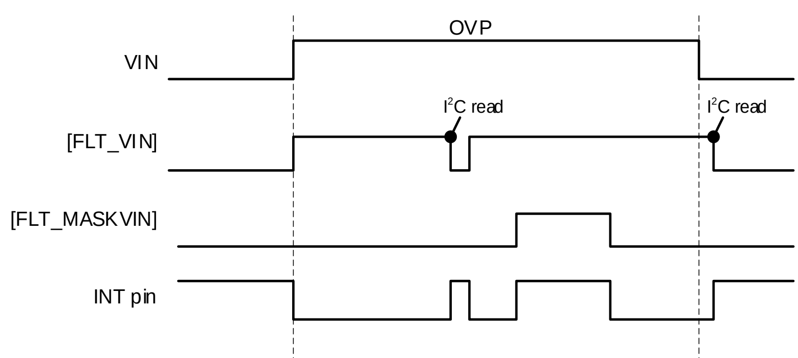


Figure 12. Input OV Protection Interrupt

Temperature Interrupt

The SY70301 provides a thermal warning record bit FLT_TEMP_DIE in register FLT_RECORDTEMP. If the temperature of the device is higher than 109°C, the bit is set to 1 and the INT pin is pulled low, as shown in Figure 13. The bit can be reset to 0 after it is read if the temperature drops below 94°C. This interrupt can be masked by bit FLT_MASKTEMP_DIE in register FLT_MASKTEMP.

The SY70301 also provides an overtemperature protection bit FLT_TEMP_SD in register FLT_RECORDTEMP. If the temperature of the device is higher than 155°C, the bit is set to 1 and the INT pin is pulled low, as shown in Figure 14. The bit can be reset to 0 after it is read if the temperature drops below 140°C. This interrupt can be masked by bit FLT_MASKTEMP_SD in register FLT_MASKTEMP.

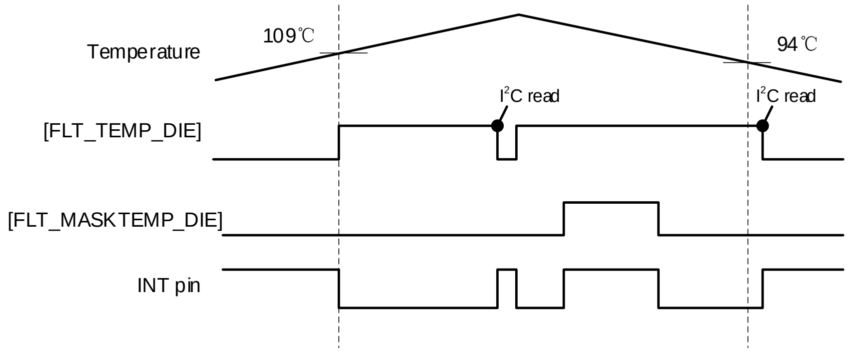


Figure 13. Thermal Warning Interrupt

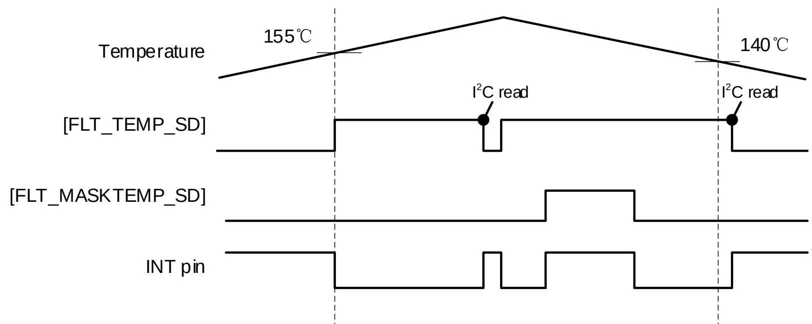


Figure 14. Thermal Shutdown Interrupt

Fault Power Good Interrupt

The SY70301 provides a bit to indicate power good state for each buck: FLT_PGx in register FLT_RECORDBUCKx. If the output voltage is detected between 90% and 110% of V_{SET}, the bit is set to 0, and if the output voltage is out of range, the bit is set to 1. The bit can be reset to 0 after it is read if the fault state is clear. This interrupt can be masked by bit FLT_MASKPGx in register FLT_MASKBUCKx. Power good fault detection is disabled during the normal power-up, shutdown, and DVS periods.

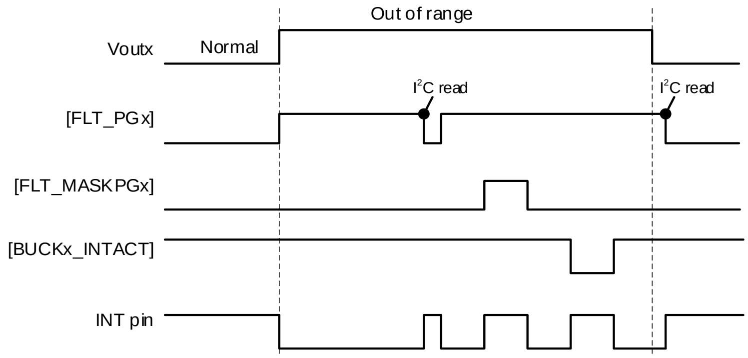


Figure 15. Fault Power Good Interrupt

Overcurrent Interrupt

The SY70301 provides a bit to indicate an overcurrent state: FLT_BUCK1_OC in register FLT_RECORDBUCKx. If an overcurrent state is detected, the bit is set to 1. The bit can be reset to 0 after it is read if the fault state is clear. This interrupt can only be masked by bit BUCKx_INTACT in register FLT_MASKBUCKx.

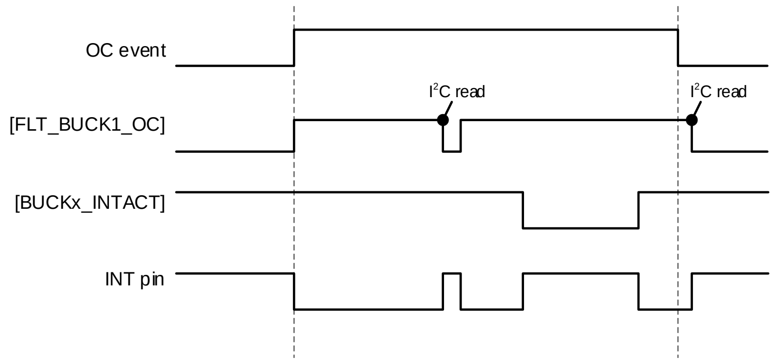


Figure 16. Input OC Protection Interrupt

Overvoltage Interrupt

The SY70301 provides a bit to indicate an overvoltage state: FLT_BUCKx_OV in register FLT_RECORDBUCKx. If an overvoltage state is detected, the bit is set to 1. The bit can be reset to 0 after it is read if the fault state is clear. This interrupt can be masked by bits FLT_BUCKx_MASKOV and BUCKx_INTACT in register FLT_MASKBUCKx.

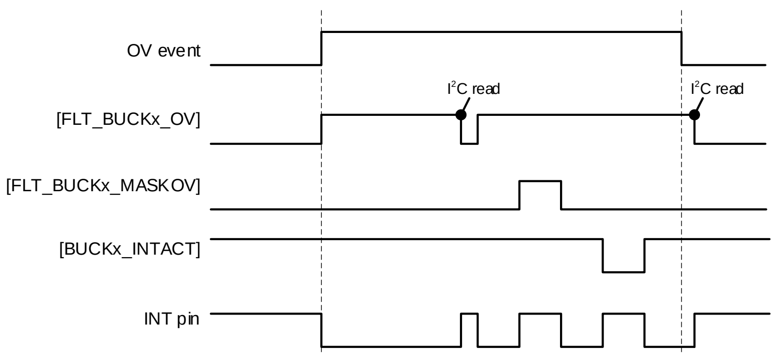


Figure 17. Input OV Protection Interrupt Function

Undervoltage Interrupt

The SY70301 provides a bit to indicate an undervoltage state: FLT_BUCKx_UV in register FLT_RECORDBUCKx. If an undervoltage state is detected, the bit is set to 1. The bit can be reset to 0 after it is read if the fault state is clear. This interrupt can be masked by bits FLT_BUCKx_MASKUV and BUCKx_INTACT in register FLT_MASKBUCKx.

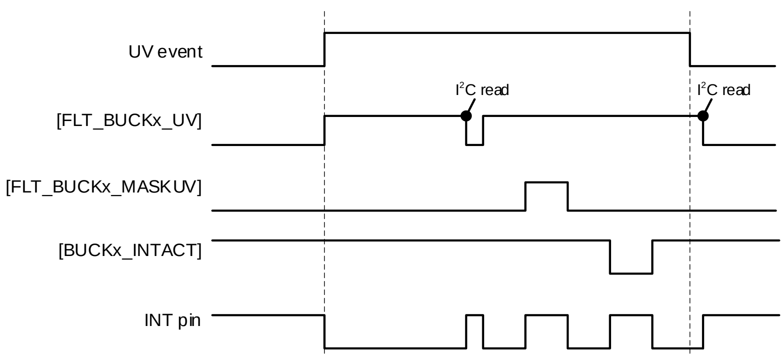


Figure 18. Input UV Protection Interrupt Function

Interrupt Condition during Power Sequencing

Buck fault (PG, OC, OV, UV) detection is blocked during the normal power-up, shutdown, and DVS periods.

When the buck is shut down by cycling the global EN pin, the fault record registers FLT_RECORDTEMP and FLT_RECORDBUCKx reset to default value.

Shutting down the buck using the software EN bit will not change the fault record registers FLT_RECORDTEMP and FLT_RECORDBUCKx.

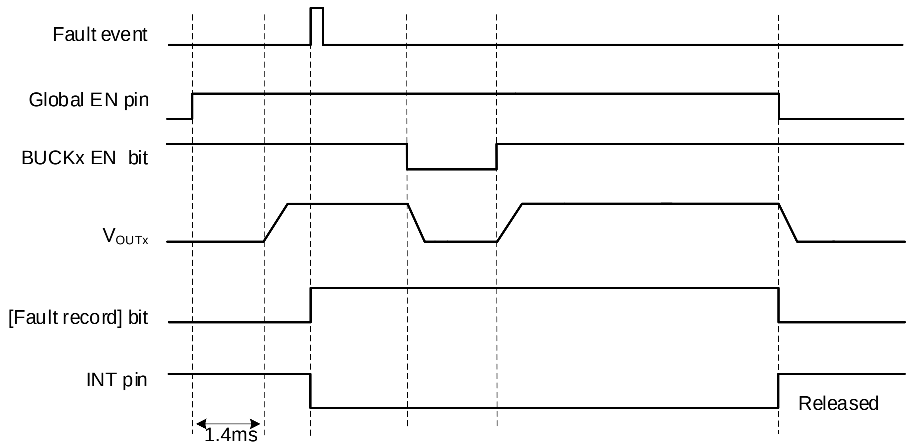


Figure 19. Interrupt during Power Sequencing

Application Information

The following paragraphs provide information on selecting the external components for each of the buck converters, to match the application requirements.

Input Capacitor C_{INX}

For the best performance, select typical X5R or better grade ceramic capacitors with a 6.3V or higher rating, and at least 10μF capacitance. The capacitor should be placed as close as possible to the corresponding pin on the device, while also minimizing the loop area formed by C_{INx} and the IN/GND pins.

When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability, and high RMS current rating over a wide temperature and voltage range.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current. The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1 - D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 10µF X5R capacitor is sufficient for each of the buck converters in most applications.

Output Inductor L_X

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT} / V_{IN,MAX})}{f_{sw} \times I_{OUT,MAX} \times 0.4}$$

where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY81057 has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Use an inductor with DCR less than 20mΩ to achieve good overall efficiency.

Output Capacitor C_{OUTX}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting C_{OUT}. For the best performance, use two X5R or better grade ceramic capacitors with a 10V rating, and capacitance of at least 22µF for each converter output.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed:

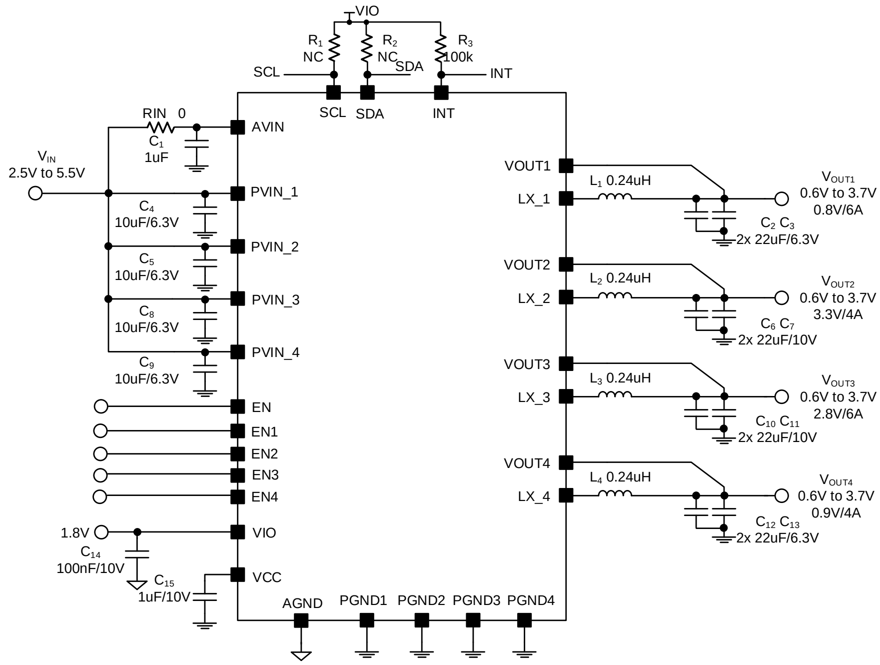
The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔIL) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, consider both.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The measured capacitive ripple might be higher than the theoretical value because the effective capacitance for ceramic capacitors decreases with the voltage across its terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Application Schematic



BOM List

Reference Designator	Description	Part Number	Manufacturer
U_1	PMIC	SY70301WBQ	Silergy
C_1	1µF/10V, 0603, X5R	GRM155C81A105KA12	Murata
C_4, C_5, C_8, C_9,	10µF/6.3V, 0603, X5R	GRM188D70J106MA73	Murata
C_2, C_3, C_{12}, C_{13}	22µF/6.3V, 0603, X5R	GRM188C80G226ME15	Murata
C_6, C_7, C_{10}, C_{11}	22µF/10V, 0603, X5R	GRM187R61A226ME15	Murata
L_1, L_2, L_3 ,L_4	0.24µH, 2016, 16m, 6.8A	DFE201610E-R24M	Murata
R_1, R_2	NC		
R_3	100kΩ, 0603		
R_{IN}	0Ω, 0603		

Layout Design

Follow these PCB layout guidelines for optimal performance:

- To achieve a higher efficiency and better noise immunity, place capacitor C close to the IC.
- To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A reasonable number of vias are suggested to be placed underneath the ground pad to enhance thermal performance.
- Place the decoupling capacitor of PVIN1 as close as possible to the PVIN1 pin and PGND1 pins, and minimize the loop area formed by the input capacitors, input pins, and PGND pins.
- Place the inductor as close as possible to the chip while keeping the trace short. To improve noise immunity and reduce parasitic inductance and resistance, minimize the PCB copper area associated with the LX pin.
- To minimize the impact of the switching noise, avoid routing the feedback lines (VOUT) close to LX(s) or other high-frequency signal lines (SCL/SDA) as much as possible.

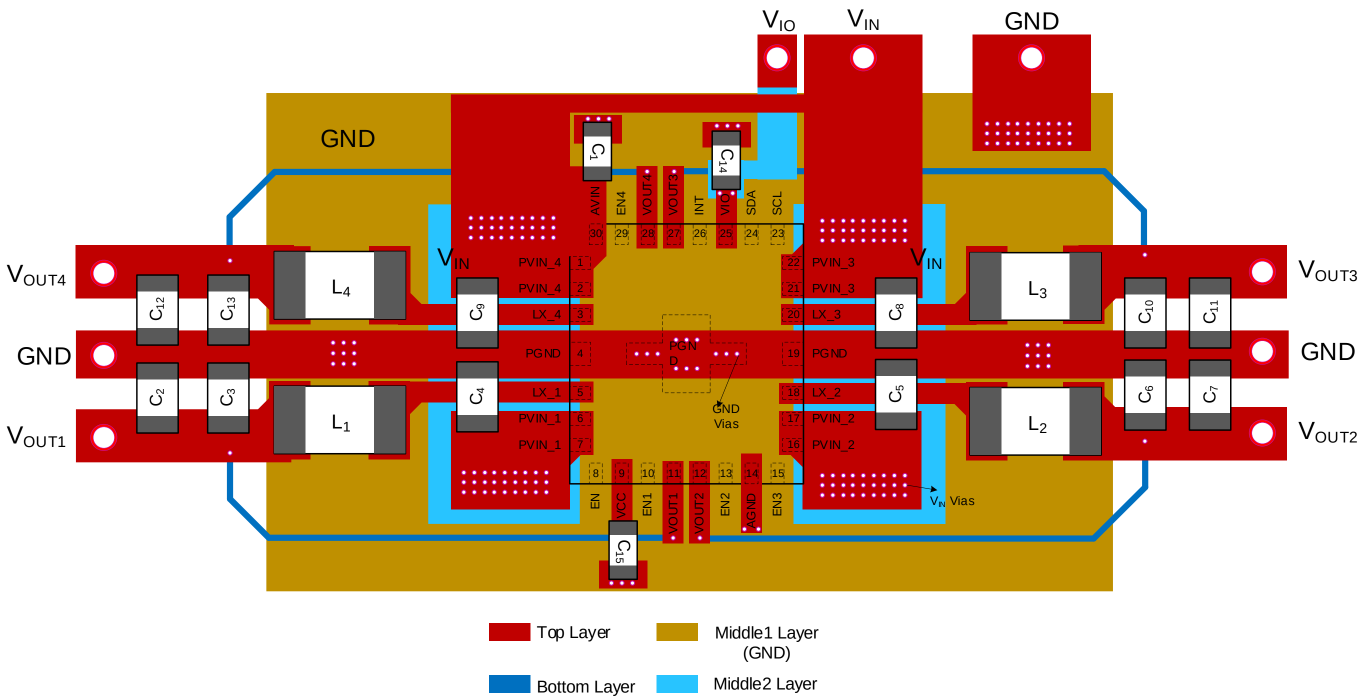


Figure 20. Suggested PCB Layout

I²C Communication Interface

The I²C interface is a simple, bidirectional 2-wire bus protocol consisting of the Serial Clock Control (SCL) and the Serial Data Signal (SDA). The SY70301 hosts a peripheral I²C interface that supports data speeds up to 3.4Mbps. SCL is an input to the SY70301 and is driven by the controller, whereas SDA is bidirectional. The SY70301 has an open-drain output to transmit data on SDA. An external pullup resistor must be placed on the serial data line to pull the drain output high during data transmission.

The default address of the SY70301 is set to 0x1E(0011110x) by internal MTP.

I²C Timing Spec Table

Characteristics	Symbol	Units	Standard Mode		Fast Mode		High-Speed Mode	
			Min	Max	Min	Max	Min	Max
Pullup Voltage	VPU	V	1.7V to VIO					
SCL Clock Frequency	f_{SCL}	kHz	0 to 100kHz		0 to 400kHz		0 to 3.4MHz	
Hold Time for Repeated START Condition	$t_{HD;STA}$	ms	4		0.6		0.16	
Low Period of the SCL Clock	t_{LOW}	ms	4.7		1.3		0.16	
High Period of the SCL Clock	t_{HIGH}	ms	4		0.6		0.06	
Setup Time for Repeated START Condition	$t_{SU;STA}$	ms	4.7		0.6		0.16	
DATA IN Hold Time	$t_{HD;DI}$	ns	0	3450	0	900	0	70
DATA OUT Hold Time	$t_{HD;DO}$	ns		70		70		70
Data Setup Time	$t_{SU;DAT}$	ns	250		100		10	
Rise Time of both SDA and SCL Signals	t_R	ns		1000	5	300	5	40
Fall Time of both SDA and SCL Signals	t_F	ns		300	5	300	5	40
Setup Time for STOP Condition	$t_{SU;STO}$	ms	4		0.6		0.16	
Bus Free Time between STOP and START Conditions	t_{BUF}	ms	4.7		1.3			
Capacitive Load for Each Bus Line	C_B	pF		400		400		100

START and STOP Conditions

The SY70301 is controlled via an I²C compatible interface. The START condition is a high-to-low transition of the SDA line while SCL is high. The STOP condition is a low-to-high transition on the SDA line while SCL is high. A STOP condition must be sent before each START condition. The I²C host always generates the START and STOP conditions.

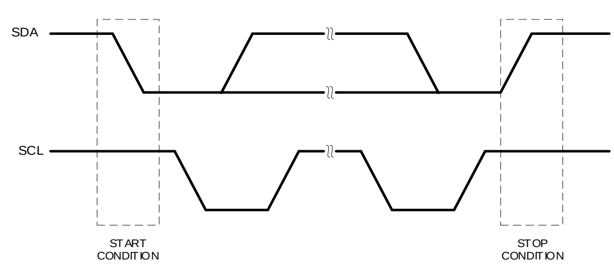


Figure 21. I2C Timing

Data Validity

The data on the SDA line must be stable during the high period of the SCL, unless generating a START or STOP condition. The high or low state of the data line can only change when the clock signal on the SCL line is low.

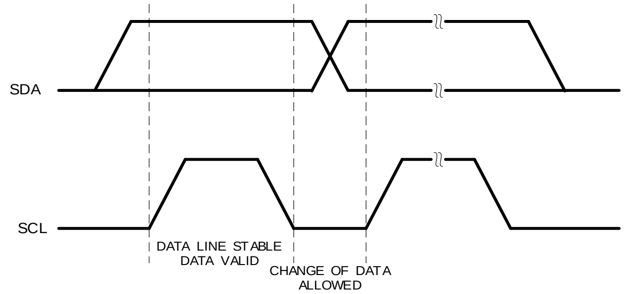


Figure 22. Data Validity

Acknowledge

Each address and data transmission uses nine clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the host sends seven peripheral address bits and an $R/\overline{W}$ bit during the next eight clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the host and the peripheral to acknowledge receipt of register addresses and data.

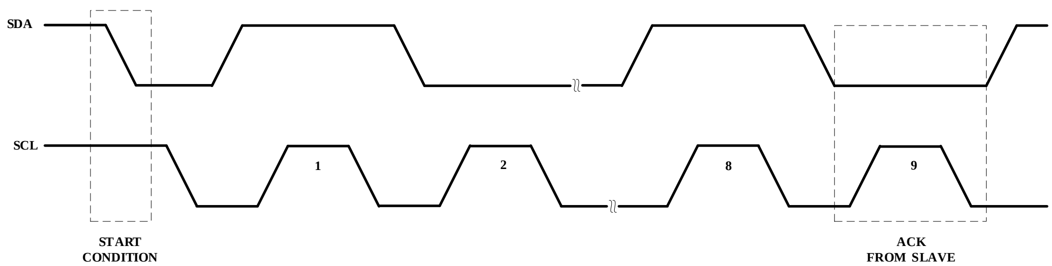


Figure 23. Acknowledge

Data Transactions

All transactions start with a control byte sent from the I²C host device. The control byte begins with a START condition, followed by seven bits of peripheral address (0011110x) for the device (this address can be changed if necessary) followed by the eighth ($R/\overline{W}$) bit. The $R/\overline{W}$ bit is 0 for a write or 1 for a read. If any peripheral devices on the I²C bus recognize their address, they will acknowledge by pulling the SDA line low for the last clock cycle in the control byte. If no peripherals exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition. Once the control byte is sent, and the device acknowledges it, the second byte sent by the host must be a register address byte. The register address byte tells the device which registers the host will write or read. Once the device receives a register address byte, it responds with an Acknowledge.

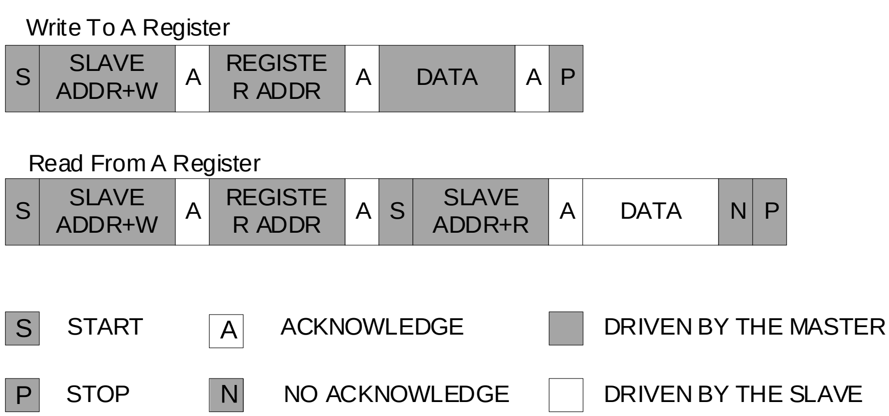


Figure 24. Data Transactions

Register Map

Register Address Map

No.	Address	Register	No.	Address	Register
1	0x01	IO_CHIPNAME	25	0x5B	BUCK3_RAMP
2	0x02	IO_CHIPVERSION	26	0x5F	BUCK3_CFG0
3	0x0F	IO_SOFTRESET	27	0x62	BUCK3_DVS0CFG1
4	0x13	FLT_RECORDTEMP	28	0x63	BUCK3_DVS0CFG0
5	0x14	FLT_RECORDBUCK1	29	0x6E	BUCK3_RSPCFG
6	0x15	FLT_RECORDBUCK3	30	0x6F	BUCK3_SLEWCTRL
7	0x16	FLT_RECORDBUCK2	31	0x75	BUCK2_RAMP
8	0x17	FLT_RECORDBUCK4	32	0x79	BUCK2_CFG0
9	0x30	FLT_OT_CTRL	33	0x7C	BUCK2_DVS0CFG1
10	0x32	FLT_MASKTEMP	34	0x7D	BUCK2_DVS0CFG0
11	0x33	FLT_MASKBUCK1	35	0x88	BUCK2_RSPCFG
12	0x34	FLT_MASKBUCK3	36	0x89	BUCK2_SLEWCTRL
13	0x35	FLT_MASKBUCK2	37	0x8F	BUCK4_RAMP
14	0x36	FLT_MASKBUCK4	38	0x93	BUCK4_CFG0
15	0x37	FLT_BUCK1_CTRL	39	0x96	BUCK4_DVS0CFG1
16	0x38	FLT_BUCK3_CTRL	40	0x97	BUCK4_DVS0CFG0
17	0x39	FLT_BUCK2_CTRL	41	0xA2	BUCK4_RSPCFG
18	0x3A	FLT_BUCK4_CTRL	42	0xA3	BUCK4_SLEWCTRL
19	0x3E	BUCK1_RAMP			
20	0x42	BUCK1_CFG0			
21	0x48	BUCK1_DVS0CFG1			
22	0x49	BUCK1_DVS0CFG0			
23	0X54	BUCK1_RSPCFG			
24	0X55	BUCK1_SLEWCTRL			

Register Description

IO_CHIPNAME				
Register Address:		0x01		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:0	11111111	CHIPNAME	R	Manufacturer Identification

IO_CHIPVERSION				
Register Address:		0x02		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:0	00000000	CHIPVERSION	R	Version Number Identification

IO_SOFTRESET				
Register Address:		0x0F		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:1	0000 000	-	-	-
0	0	SOFTRESET	R/W	Reset All Registers and Reload from OTP: 0: Do nothing 1: Reset and bit cleared

FLT_RECORDTEMP				
Register Address:		0x13		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	FLT_VIN	R	VIN OVP Occurred Record (Cleared when read) 0: No fault, less than threshold. 1: Fault, greater than threshold, send interrupt request
6:3	0000	-	-	-
2	0	FLT_TEMP_DIE	R	Overtemperature Record For Die (109°C) (Cleared when read) 0: No fault, less than threshold. 1: Fault, greater than threshold, send interrupt request
1	0	FLT_TEMP_SD	R	Overtemperature Shutdown Record (150°C) (Cleared when read) 0: No fault, less than threshold. 1: Fault, greater than threshold, send interrupt request
0	0	-	-	-

FLT_RECORDBUCK1				
Register Address:		0x14		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	FLT_PG1	R	Output Good for Buck 1 0: 110% of V_{SET} > VOUT1 > 90% of V_{SET} 1: VOUT1 is out of range, send interrupt request
6	0	FLT_BUCK1_OC	R	Overcurrent for Buck 1 (Cleared when read) 0: No fault, less than threshold. 1: Fault, greater than threshold, send interrupt request
5	0	FLT_BUCK1_OV	R	Overvoltage for Buck 1 (Cleared when read) 0: No fault, less than threshold. 1: Fault, greater than threshold, send interrupt request
4	0	FLT_BUCK1_UV	R	Undervoltage for Buck 1 (Cleared when read) 0: No fault, less than threshold. 1: Fault, greater than threshold, send interrupt request
3-0	0000	-	-	-

FLT_RECORDBUCK3				
Register Address:		0x15		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	FLT_PG3	R	Refer to FLT_RECORDBUCK1
6	0	FLT_BUCK3_OC	R	
5	0	FLT_BUCK3_OV	R	
4	0	FLT_BUCK3_UV	R	
3-0	0000	-	-	

FLT_RECORDBUCK2				
Register Address:		0x16		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	FLT_PG2	R	Refer to FLT_RECORDBUCK1
6	0	FLT_BUCK2_OC	R	
5	0	FLT_BUCK2_OV	R	
4	0	FLT_BUCK2_UV	R	
3-0	0000	-	-	

FLT_RECORDBUCK4				
Register Address:		0x17		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	FLT_PG4	R	Refer to FLT_RECORDBUCK1
6	0	FLT_BUCK4_OC	R	
5	0	FLT_BUCK4_OV	R	
4	0	FLT_BUCK4_UV	R	
3-0	0000	-	-	

FLT_OT_CTRL				
Register Address:		0x30		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:4	0000	-	-	-
3	0	FLT_OT_CTRL	R/W	Overtemperature Shutdown Mode 0: Shutdown and auto recover 1: Do nothing
2:0	000	-	-	-

FLT_MASKTEMP				
Register Address:		0x32		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	FLT_MASKVIN	R/W	Mask IRQ for VIN OVP 0: Pass IRQ to INT pin 1: Mask IRQ
6:3	000	-	-	-
2	0	FLT_MASKTEMP_DIE	R/W	Mask IRQ for Hot Die 0: Pass IRQ to INT pin 1: Mask IRQ
1	0	FLT_MASKTEMP_SD	R/W	Mask IRQ for Thermal Shutdown 0: Pass IRQ to INT pin 1: Mask IRQ
0	0	-	-	-

FLT_MASKBUCK1				
Register Address:		0x33		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	FLT_BUCK1 _MASKPG	R/W	Mask IRQ for FLT_PG1 0: Pass IRQ to INT pin 1: Mask IRQ
6	0	BUCK1_INTACT	R/W	Enable or Disable Buck1 INT Function 0: Disable 1: Enable Metal change available for the default value
5	0	FLT_BUCK1 _MASKOV	R/W	Mask IRQ for FLT_BUCK1_OV 0: Pass IRQ to INT pin 1: Mask IRQ
4	0	FLT_BUCK1 _MASKUV	R/W	Mask IRQ for FLT_BUCK1_UV 0: Pass IRQ to INT pin 1: Mask IRQ
3:0	0000	-	-	-

FLT_MASKBUCK3				
Register Address:		0x34		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	FLT_BUCK3 _MASKPG	R/W	Refer to FLT_MASKBUCK1
6	0	BUCK3_INTACT	R/W	
5	0	FLT_BUCK3 _MASKOV	R/W	
4	0	FLT_BUCK3 _MASKUV	R/W	
3:0	0000	-	-	

FLT_MASKBUCK2				
Register Address:		0x35		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	FLT_BUCK2 _MASKPG	R/W	Refer to FLT_MASKBUCK1
6	0	BUCK2_INTACT	R/W	
5	0	FLT_BUCK2 _MASKOV	R/W	
4	0	FLT_BUCK2 _MASKUV	R/W	
3:0	0000	-	-	

FLT_MASKBUCK4				
Register Address:		0x36		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	FLT_BUCK4 _MASKPG	R/W	Refer to FLT_MASKBUCK1
6	0	BUCK4_INTACT	R/W	
5	0	FLT_BUCK4 _MASKOV	R/W	
4	0	FLT_BUCK4 _MASKUV	R/W	
3:0	0000	-	-	

FLT_BUCK1_CTRL				
Register Address:		0x37		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:4	0000	-	-	-
3	1	FLT_BUCK1_CTRL	R/W	Protection Mode For UV 0: UV Shutdown and latch off 1: UV Hiccup
2:0	000	-	-	-

FLT_BUCK3_CTRL				
Register Address:		0x38		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:4	0000	-	-	Refer to FLT_BUCK1_CTRL
3	1	FLT_BUCK3_CTRL	R/W	
2:0	000	-	-	

FLT_BUCK2_CTRL				
Register Address:		0x39		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:4	0000	-	-	Refer to FLT_BUCK1_CTRL
3	1	FLT_BUCK2_CTRL	R/W	
2:0	000	-	-	

FLT_BUCK4_CTRL				
Register Address:		0x3A		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:4	0000	-	-	Refer to FLT_BUCK1_CTRL
3	1	FLT_BUCK4_CTRL	R/W	
2:0	000	-	-	

BUCK1_RAMP				
Register Address:		0x3E		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	-	-	-
6	1	FCCM_DVS_UP	R/W	Work Mode when DVS Up 0: Controlled by WORK_MODE bit 1: Forced PWM
5:3	00 0	-	-	-
2	1	FCCM_DVS_DN	R/W	Work Mode when DVS Down 0: Controlled by WORK_MODE bit 1: Forced PWM
1:0	00	-	-	-

BUCK1_CFG0				
Register Address:		0x42		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:1	0000 000	-	-	-
0	1	VOUT_DISCHARGE_EN	R/W	Enable Discharge Resistor when Shut Down 0:.Disable 1: Enable

<table>
<tr><th colspan="5">BUCK1_DVS0CFG1</th></tr>
<tr><td colspan="2">Register Address:</td><td>0x48</td><td></td><td></td></tr>
<tr><th>Bits</th><th>Default</th><th>Signal Name</th><th>R/W</th><th>Description</th></tr>
<tr><td>7:0</td><td>0x14</td><td>BUCK1_DVS0</td><td>R/W</td><td>8-bit DAC[7:0] value to generate VOUT for DVS Configuration
<table>
<tr><td>DAC</td><td>Vo/V</td><td>DAC</td><td>Vo/V</td></tr>
<tr><td>0000 0000</td><td>0.6</td><td>1100 1000</td><td>2.6</td></tr>
<tr><td>0000 0001</td><td>0.61</td><td>1100 1001</td><td>2.62</td></tr>
<tr><td>…</td><td>…</td><td>…</td><td>…</td></tr>
<tr><td>1100 0110</td><td>2.58</td><td>1111 1110</td><td>3.68</td></tr>
<tr><td>1100 0111</td><td>2.59</td><td>1111 1111</td><td>3.70</td></tr>
</table></td></tr>
</table>

BUCK1_DVS0CFG0				
Register Address:		0x49		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:6	00	-	-	-
5	0	WORK_MODE	R/W	Buck 1 Work Mode 0: Automatic PFM/PWM 1: Forced PWM
4:1	0000	-	-	-
0	1	BUCK1_EN	R/W	Enable Buck1 0: Disable, VOUT1 = 0 1: Enable

<table>
<tr><th colspan="5">BUCK1_RSPCFG</th></tr>
<tr><td colspan="2">Register Address:</td><td>0x54</td><td></td><td></td></tr>
<tr><th>Bits</th><th>Default</th><th>Signal Name</th><th>R/W</th><th>Description</th></tr>
<tr><td>7</td><td>0</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>6:4</td><td>001</td><td>BUCK1_RSPUP</td><td>R/W</td><td>
<table>
<tr><td></td><td>Ramp-Up Speed mV/µs</td></tr>
<tr><td>001</td><td>32</td></tr>
<tr><td>011</td><td>16</td></tr>
<tr><td>100</td><td>8</td></tr>
<tr><td>101</td><td>4</td></tr>
<tr><td>110</td><td>2</td></tr>
<tr><td>111</td><td>1</td></tr>
</table></td></tr>
<tr><td>3</td><td>0</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>2:0</td><td>100</td><td>BUCK1_RSPDN</td><td>R/W</td><td>
<table>
<tr><td></td><td>Ramp-Down Speed mV/µs</td></tr>
<tr><td>001</td><td>32</td></tr>
<tr><td>011</td><td>16</td></tr>
<tr><td>100</td><td>8</td></tr>
<tr><td>101</td><td>4</td></tr>
<tr><td>110</td><td>2</td></tr>
<tr><td>111</td><td>1</td></tr>
</table></td></tr>
<tr><td>3:0</td><td>0000</td><td>-</td><td>-</td><td>-</td></tr>
</table>

<table>
<tr><th colspan="5">BUCK1_SLEWCTRL</th></tr>
<tr><td colspan="2">Register Address:</td><td>0x55</td><td></td><td></td></tr>
<tr><th>Bits</th><th>Default</th><th>Signal Name</th><th>R/W</th><th>Description</th></tr>
<tr><td>7:6</td><td>00</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>5:4</td><td>11</td><td>BUCK1_POWERUP</td><td>R/W</td><td><table><tr><td></td><td>Power-Up Speed mV/μs</td></tr><tr><td>00</td><td>20</td></tr><tr><td>01</td><td>10</td></tr><tr><td>10</td><td>5</td></tr><tr><td>11</td><td>2.5</td></tr></table></td></tr>
<tr><td>3:0</td><td>0000</td><td>-</td><td>-</td><td>-</td></tr>
</table>

<table>
<tr><th colspan="5">BUCK3_RAMP</th></tr>
<tr><td colspan="2">Register Address:</td><td>0x5B</td><td></td><td></td></tr>
<tr><th>Bits</th><th>Default</th><th>Signal Name</th><th>R/W</th><th>Description</th></tr>
<tr><td>7</td><td>0</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>6</td><td>1</td><td>FCCM_DVS_UP</td><td>R/W</td><td>Work Mode when DVS Up
0: Controlled by WORK_MODE bit
1: Forced PWM</td></tr>
<tr><td>5:3</td><td>00 0</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>2</td><td>1</td><td>FCCM_DVS_DN</td><td>R/W</td><td>Work Mode when DVS Down
0: Controlled by WORK_MODE bit
1: Forced PWM</td></tr>
<tr><td>1:0</td><td>00</td><td>-</td><td>-</td><td>-</td></tr>
</table>

<table>
<tr><th colspan="5">BUCK3_CFG0</th></tr>
<tr><td colspan="2">Register Address:</td><td>0x5F</td><td></td><td></td></tr>
<tr><th>Bits</th><th>Default</th><th>Signal Name</th><th>R/W</th><th>Description</th></tr>
<tr><td>7:1</td><td>0000 000</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>0</td><td>1</td><td>VOUT_DISCHARGE_EN</td><td>R/W</td><td>Enable Discharge Resistor when Shut Down
0: Disable
1: Enable</td></tr>
</table>

<table>
<tr><th colspan="5">BUCK3_DVS0CFG1</th></tr>
<tr><td colspan="2">Register Address:</td><td>0x62</td><td></td><td></td></tr>
<tr><th>Bits</th><th>Default</th><th>Signal Name</th><th>R/W</th><th>Description</th></tr>
<tr><td>7:0</td><td>0xD2</td><td>BUCK3_DVS0</td><td>R/W</td><td>8-bit DAC[7:0] value to generate VOUT for DVS Configuration<table><tr><td>DAC</td><td>V_O/V</td><td>DAC</td><td>V_O/V</td></tr><tr><td>0000 0000</td><td>0.6</td><td>1100 1000</td><td>2.6</td></tr><tr><td>0000 0001</td><td>0.61</td><td>1100 1001</td><td>2.62</td></tr><tr><td>…</td><td>…</td><td>…</td><td>…</td></tr><tr><td>1100 0110</td><td>2.58</td><td>1111 1110</td><td>3.68</td></tr><tr><td>1100 0111</td><td>2.59</td><td>1111 1111</td><td>3.70</td></tr></table></td></tr>
</table>

<table>
<tr><th colspan="5">BUCK3_DVS0CFG0</th></tr>
<tr><td colspan="2">Register Address:</td><td>0x63</td><td></td><td></td></tr>
<tr><th>Bits</th><th>Default</th><th>Signal Name</th><th>R/W</th><th>Description</th></tr>
<tr><td>7:6</td><td>00</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>5</td><td>0</td><td>WORK_MODE</td><td>R/W</td><td>Buck 3 Work Mode
0: Automatic PFM/PWM
1: Forced PWM</td></tr>
<tr><td>4:1</td><td>0000</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>0</td><td>1</td><td>BUCK3_EN</td><td>R/W</td><td>Enable Buck 3
0: Disable
1: Enable</td></tr>
</table>

<table>
<tr><th colspan="5">BUCK3_RSPCFG</th></tr>
<tr><td colspan="2">Register Address:</td><td>0x6E</td><td></td><td></td></tr>
<tr><th>Bits</th><th>Default</th><th>Signal Name</th><th>R/W</th><th>Description</th></tr>
<tr><td>7</td><td>0</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>6:4</td><td>001</td><td>BUCK3_RSPUP</td><td>R/W</td><td><table><tr><td></td><td>Ramp-Up Speed mV/µs</td></tr><tr><td>001</td><td>32</td></tr><tr><td>011</td><td>16</td></tr><tr><td>100</td><td>8</td></tr><tr><td>101</td><td>4</td></tr><tr><td>110</td><td>2</td></tr><tr><td>111</td><td>1</td></tr></table></td></tr>
<tr><td>3</td><td>0</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>2:0</td><td>100</td><td>BUCK3_RSPDN</td><td>R/W</td><td><table><tr><td></td><td>Ramp-Down Speed mV/µs</td></tr><tr><td>001</td><td>32</td></tr><tr><td>011</td><td>16</td></tr><tr><td>100</td><td>8</td></tr><tr><td>101</td><td>4</td></tr><tr><td>110</td><td>2</td></tr><tr><td>111</td><td>1</td></tr></table></td></tr>
</table>

<table>
<tr><th colspan="5">BUCK3_SLEWCTRL</th></tr>
<tr><td colspan="2">Register Address:</td><td>0x6F</td><td></td><td></td></tr>
<tr><th>Bits</th><th>Default</th><th>Signal Name</th><th>R/W</th><th>Description</th></tr>
<tr><td>7:6</td><td>00</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>5:4</td><td>01</td><td>BUCK3_POWERUP</td><td>R/W</td><td><table><tr><td></td><td>Power-Up Speed mV/µs</td></tr><tr><td>00</td><td>20</td></tr><tr><td>01</td><td>10</td></tr><tr><td>10</td><td>5</td></tr><tr><td>11</td><td>2.5</td></tr></table></td></tr>
<tr><td>3:0</td><td>0000</td><td>-</td><td>-</td><td>-</td></tr>
</table>

BUCK2_RAMP				
Register Address:		0x75		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	-	-	-
6	1	FCCM_DVS_UP	R/W	Work Mode when DVS Up 0: Controlled by WORK_MODE bit 1: Forced PWM
5:3	00 0	-	-	-
2	1	FCCM_DVS_DN	R/W	Work Mode when DVS Down 0: Controlled by WORK_MODE bit 1: Forced PWM
1:0	00	-	-	-

BUCK2_CFG0				
Register Address:		0x79		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:1	0000 000	-	-	-
0	1	VOUT_DISCHARGE_EN	R/W	Enable Discharge Resistor when Shut Down 0:.Disable 1: Enable

BUCK2_DVS0CFG1				
Register Address:		0x7C		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:0	0xEB	BUCK2_DVS0	R/W	8-bit DAC [7:0] value to generate VOUT for DVS Configuration 0

DAC	Vo/V	DAC	Vo/V
0000 0000	0.6	1100 1000	2.6
0000 0001	0.61	1100 1001	2.62
…	…	…	…
1100 0110	2.58	1111 1110	3.68
1100 0111	2.59	1111 1111	3.70

BUCK2_DVS0CFG0				
Register Address:		0x7D		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:6	00	-	-	-
5	0	WORK_MODE	R/W	Buck 2 Work Mode 0: Automatic PFM/PWM 1: Forced PWM
4:1	0000	-	-	-
0	1	BUCK2_EN	R/W	Enable Buck 2 0: Disable 1: Enable

BUCK2_RSPCFG				
Register Address:		0x88		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	-	-	-
6:4	001	BUCK2_RSPUP	R/W	Ramp-Up Speed mV/µs: 001 = 32; 011 = 16; 100 = 8; 101 = 4; 110 = 2; 111 = 1
3	0	-	-	-
2:0	100	BUCK2_RSPDN	R/W	Ramp-Down Speed mV/µs: 001 = 32; 011 = 16; 100 = 8; 101 = 4; 110 = 2; 111 = 1

BUCK2_SLEWCTRL				
Register Address:		0x89		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:6	00	-	-	-
5:4	01	BUCK2_POWERUP	R/W	Power-Up Speed mV/µs: 00 = 20; 01 = 10; 10 = 5; 11 = 2.5
3:0	0000	-	-	-

BUCK4_RAMP				
Register Address:		0x8F		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	-	-	-
6	1	FCCM_DVS_UP	R/W	Work Mode when DVS Up 0: Controlled by WORK_MODE bit 1: Forced PWM
5:3	00 0	-	-	-
2	1	FCCM_DVS_DN	R/W	Work Mode when DVS Down 0: Controlled by WORK_MODE bit 1: Forced PWM
1:0	00	-	-	-

BUCK4_CFG0				
Register Address:		0x93		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:1	0000 000	-	-	-
0	1	VOUT_DISCHARGE_EN	R/W	Enable Discharge Resistor when Shut Down 0:.Disable 1: Enable

BUCK4_DVS0CFG1				
Register Address:		0x96		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:0	0x1E	BUCK4_DVS0	R/W	8-bit DAC[7:0] value to generate VOUT for DVS Configuration 0 DAC / Vo/V / DAC / Vo/V: 0000 0000 / 0.6 / 1100 1000 / 2.6 0000 0001 / 0.61 / 1100 1001 / 2.62 … / … / … / … 1100 0110 / 2.58 / 1111 1110 / 3.68 1100 0111 / 2.59 / 1111 1111 / 3.70

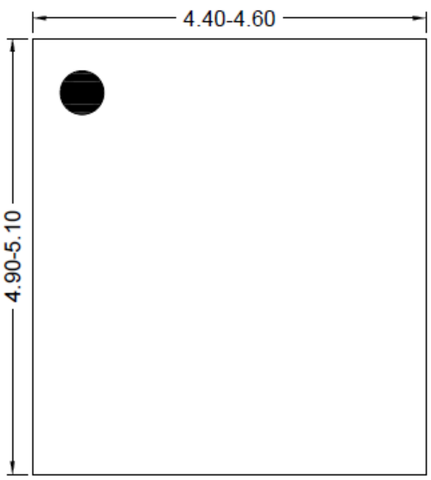
DAC	Vo/V	DAC	Vo/V
0000 0000	0.6	1100 1000	2.6
0000 0001	0.61	1100 1001	2.62
…	…	…	…
1100 0110	2.58	1111 1110	3.68
1100 0111	2.59	1111 1111	3.70

BUCK4_DVS0CFG0				
Register Address:		0x97		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:6	00	-	-	-
5	0	WORK_MODE	R/W	Buck 4 Work Mode 0: Automatic PFM/PWM 1: Forced PWM
4:1	0000	-	-	-
0	1	BUCK4_EN	R/W	Enable Buck 4 0: Disable 1: Enable

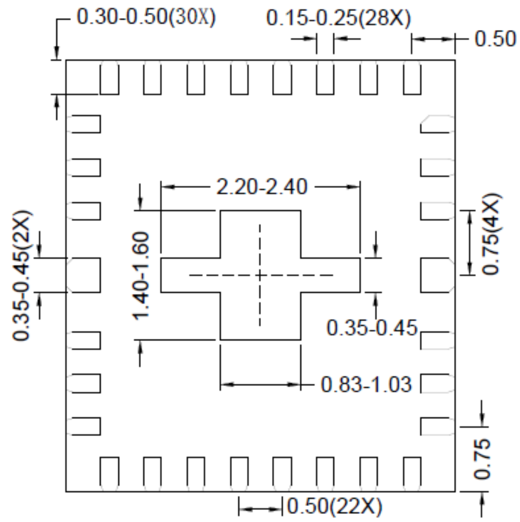
BUCK4_RSPCFG				
Register Address:		0xA2		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7	0	-	-	-
6:4	001	BUCK4_RSPUP	R/W	DVS Up Speed mV/µs: 001: 32 011: 16 100: 8 101: 4 110: 2 111: 1
3	0	-	-	-
2:0	100	BUCK4_RSPDN	R/W	DVS Down Speed mV/µs: 001: 32 011: 16 100: 8 101: 4 110: 2 111: 1

BUCK4_SLEWCTRL				
Register Address:		0xA3		
Bits	**Default**	**Signal Name**	**R/W**	**Description**
7:6	00	-	-	-
5:4	11	BUCK4_POWERUP	R/W	Power-Up Speed mV/µs: 00: 20 01: 10 10: 5 11: 2.5
3:0	0000	-	-	-

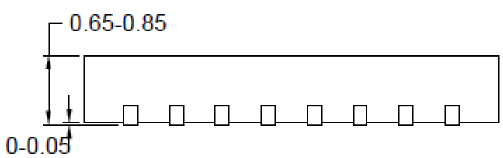
QFN4.5×5-30 Package Outline Drawing



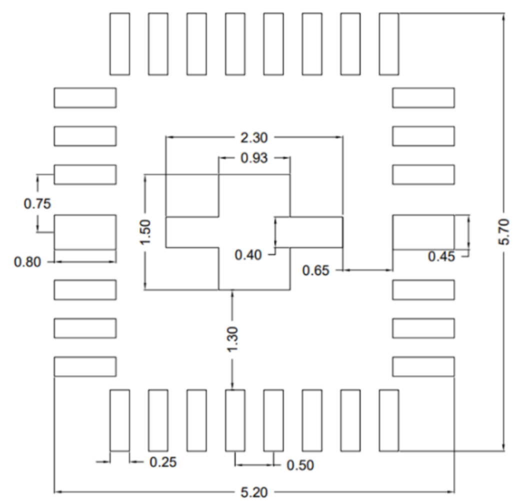
Top View



Bottom View



Side View



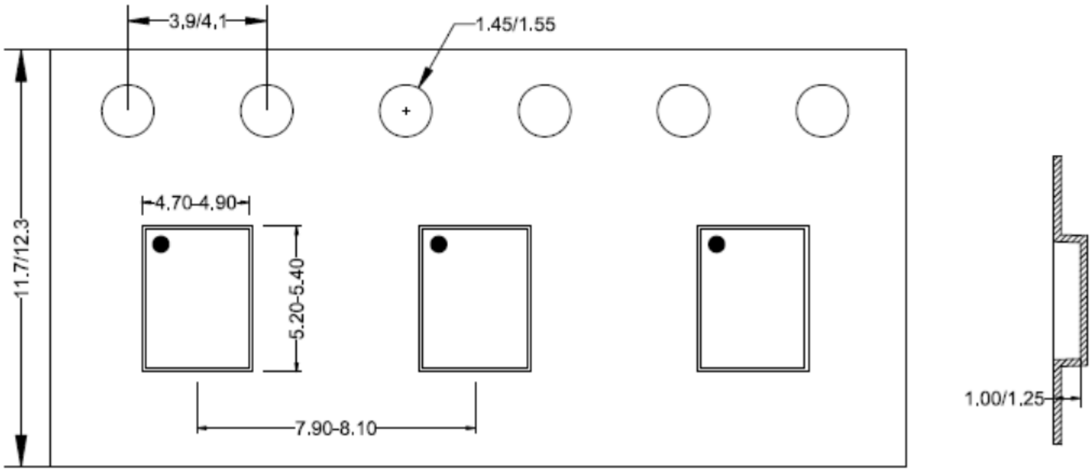
Recommended PCB Layout (reference only)

Notes: *All dimensions are in millimeters and exclude mold flash and metal burr.*

Tape and Reel Specification

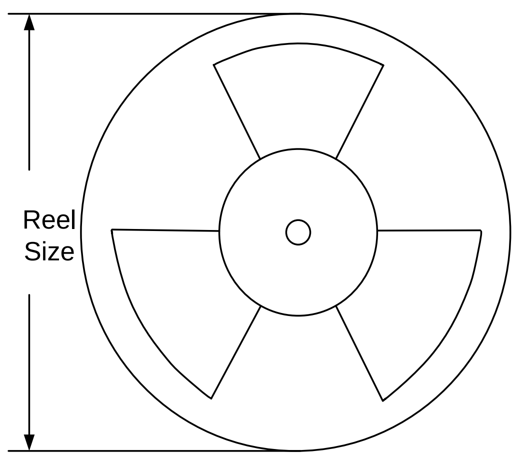
Tape Dimensions and Pin 1 Orientation

QFN4.5×5-30



Feeding Direction

Reel Dimensions



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Trailer * Length(mm)	Leader * Length (mm)	Qty per Reel (pcs)
QFN4.5×5-30	12	8	13	400	400	5000

All Dimension are nominal

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
Nov. 07, 2024	Revision 1.0	Initial Release	-

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