SY70501

Triple, Low Quiescent Current, High-Current, High Efficiency Synchronous Buck Converters with Integrated Load Switch

General Description

The SY70501 is designed for LPDDR5/LPDDR5X.It integrates 3 high efficiency synchronous Buck and a low R_{ON} load-switch (LSW). The device incorporates protections such as Undervoltage Lockout Protection (UVLO), Over-Current Protection (OCP), Undervoltage Protection (UVP), Overvoltage Protection (OVP), Over-Temperature Protection (OTP) and power-good (PG) monitor. Additionally, the SY70501 controller supports soft-start and shutdown with special sequence and can satisfy JEDEC JESID209-SA requirements.

All Buck regulators support PFM mode for light load efficiency and soft-start with pre-bias voltage. All Buck regulators adopts constant on-time (COT) control to achieve fast transient performance and excellent loop stability. All Buck regulators support 600kHz and 900kHz switching frequency controlled by an external resistor, R_{MODE}.

Current limit value of VDD2H and the slew rate of VDDQ can be controlled by R_{MODE}.

The output voltage of VDDQ is controlled by the level of VDDQ_VID pin.

The SY70501 can be controlled by EN and VDDQ_EN pin and it is flexible.

The SY70501 is available in QFN3×4-23 package.

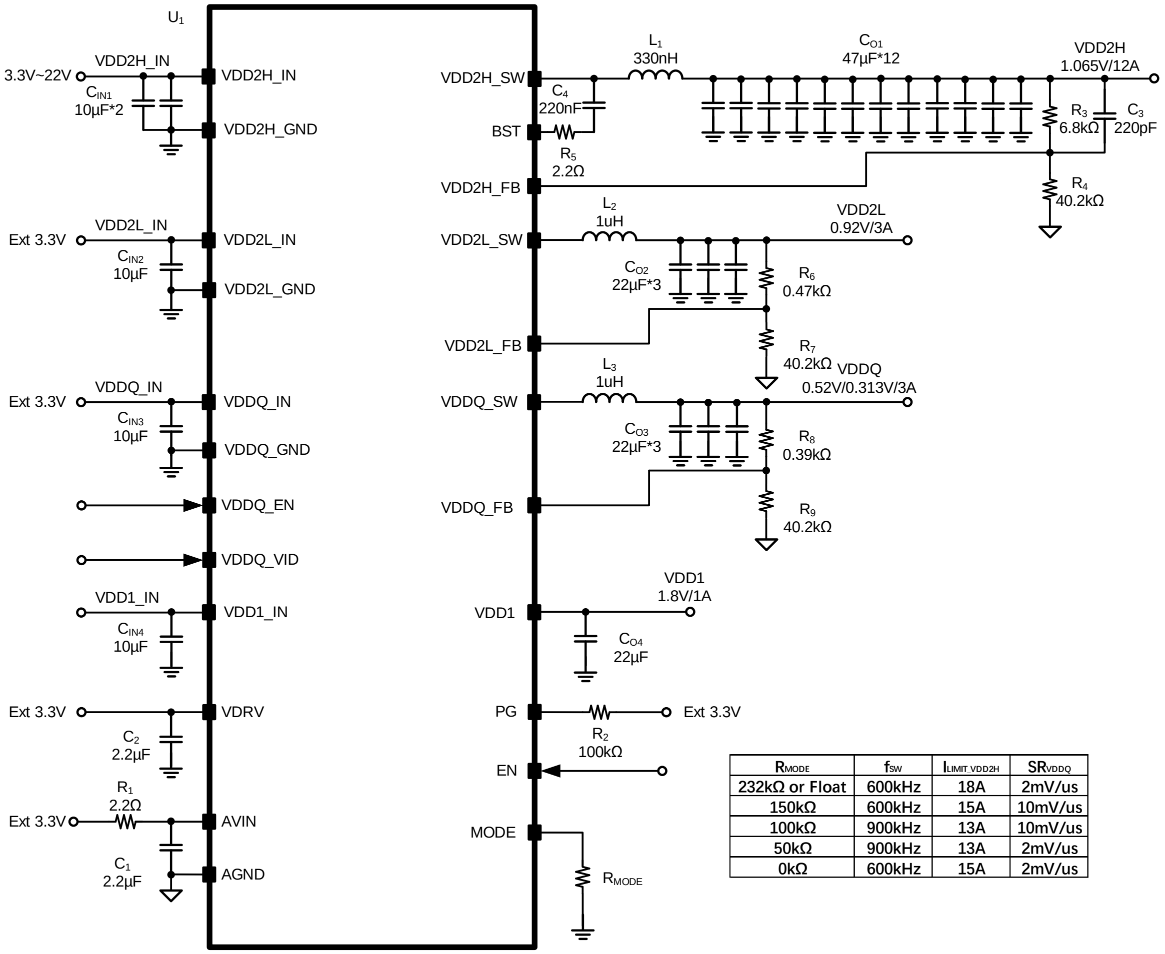
Features

- One-Chip Power Solution for LPDDR5/LPDDR5X with 3 Buck converters(VDD2H/VDD2L/VDDQ) and one Load Switch (VDD1)
- VDD2H_IN Wide Input Voltage Range: 3.15V~22V
- VDD2H Output Voltage: 1.065V (V_{REF_VDD2H}=0.91V)
- VDD2H Output Current: up to 12A, Peak 18A
- VDD2H/VDD2L/VDDQ Switching Frequency: 600kHz (R_{MODE} 0Ω/150kΩ/232kΩ), 900kHz (R_{MODE} 50kΩ/ 100kΩ)
- VDD2H Low R_{ON}: High-side 13.5mΩ, Low-side 6mΩ
- VDD2L/VDDQ Input Voltage 1.7~3.5V
- VDD2L Output Voltage: 0.91V
- VDDQ Output Voltage: 0.515V/0.31V Controlled by VDDQ_VID
- VDD2L/VDDQ Output Current: 3A
- VDD2L/VDDQ R_{ON}: High-side 70mΩ, Low-side 30mΩ
- COT Control for Fast Transient Response
- VDD1 Output Voltage: 1.8V
- VDD1 Output Current: up to 1A, Peak 3A
- VDD1 Low R_{ON}: 25mΩ
- Auto PWM/PFM Mode to Achieve High-Efficiency
- PG Pin Indicates the Output Voltages are Ready for All Channels
- Internal Soft-start and Soft Shutdown with Special Sequence Compliant with JEDEC Requirements
- Output Discharge
- Undervoltage lockout (UVLO), Over-Current Protection (OCP), Undervoltage Protection (UVP), Overvoltage Protection (OVP), Over-Temperature Protection (OTP)
- VDD2H supports Ultra-Sonic Mode(USM)
- Compact Package: QFN3×4-23
- MSL Rating: MSL3

Applications

- Laptop Computers
- Servers
- Networking Systems
- High-Performance Computer Platforms

Typical Application



R_{MODE}	f_{SW}	I_{LIMIT_VDD2H}	SR_{VDDQ}
232kΩ or Float	600kHz	18A	2mV/us
150kΩ	600kHz	15A	10mV/us
100kΩ	900kHz	13A	10mV/us
50kΩ	900kHz	13A	2mV/us
0kΩ	600kHz	15A	2mV/us

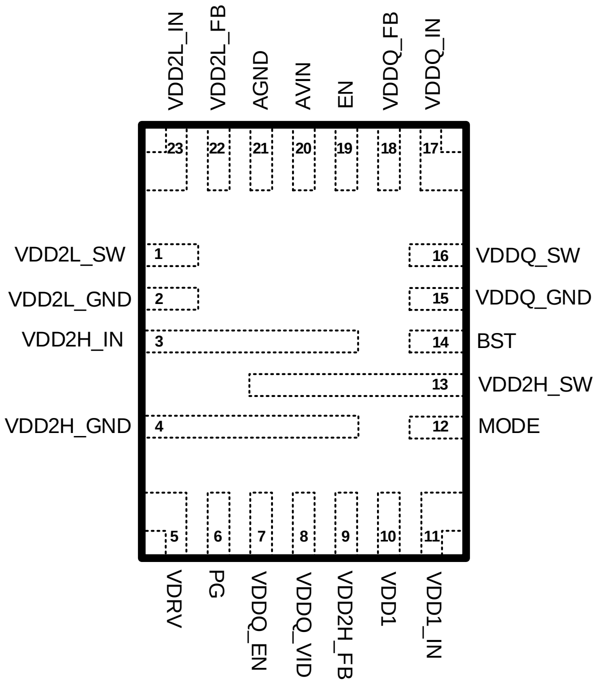
Figure 1. Schematic Diagram

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY70501TDQ	QFN3x4-23 RoHS-Compliant and Halogen-Free	**AAUCxyz**

x = year code, y = week code, z = lot number code

Pinout (top view)



(QFN3x4-23)

Pin Description

Pin Number	Pin Name	Pin Description
1	VDD2L_SW	Switch node of VDD2L.Connect this pin to the inductor using short, wide and multi-layer PCB traces to minimum wiring resistance.
2	VDD2L_GND	Power ground of VDD2L.Connect this pin to ground side of PVIN decouple cap and the ground layer of PCB using wide PCB traces and multiple vias.
3	VDD2H_IN	Power input of VDD2H. Connect this pin to a 3.15V to 22V power supply. Place two 10µF decouple ceramic caps to the VDD2H_IN and VDD2H_GND as close as possible. Connect this pin to PVIN cap using wide PCB traces and multiple vias.
4	VDD2H_GND	Power ground of VDD2H.Connect this pin to ground side of PVIN decouple cap and the ground layer of PCB using wide PCB traces and multiple vias.
5	VDRV	External 3.3V input for driver voltage. Decouple the VDRV pin and PGND with a minimum 2.2µF ceramic capacitor.
6	PG	Power good indicator (Open drain output). Connect this pin to a pull up source with a 100kΩ resistor. It is pulled up when the output of all active channels with the range of PG threshold voltage. It is pulled low when any one channel over the range of PG threshold voltage.
7	VDDQ_EN	VDDQ enable control. The VDDQ_EN pin is a digital input that enables or disables the VDDQ regulator. When both VDDQ_EN and EN high, the VDDQ regulator turns on with a specific sequence. When VDDQEN low or EN low, the VDDQ turns off. VDDQ_EN pin is pulled low internally by resistor.
8	VDDQ_VID	VDDQ output voltage control. Pull VDDQ_VID high, VDDQ VREF = 0.515V; Pull VDDQ_VID low, VDDQ VREF = 0.31V. VDDQ_VID is pulled high to AVIN internally by resistor.
9	VDD2H_FB	FB pin of VDD2H. The output voltage can be adjusted by changing the ratio of FB resistor. Keep FB trace far away from SW and other noisy nodes as it is sensitive.
10	VDD1	Power output of 1.8V load switch. Decouple the VDD1 pin by placing a minimum 22µF ceramic capacitor as close to the pin as possible.

11	VDD1_IN	Power input of VDD1. Connect the VDD1_IN pin to a 1.8V power supply. Decouple the VDD1_IN pin by placing a minimum 10µF ceramic capacitor.
12	MODE	Mode selection. The MODE pin selects switching frequency, high side and low side current limit of VDD2H, and the VDDQ DVS/Soft Start/Soft Shutdown slew rate by changing R_{MODE} (0Ω, 50kΩ, 100kΩ, 150kΩ, 232kΩ / Float).
13	VDD2H_SW	Switch node of VDD2H. Connect this pin to the inductor using short, wide and multi-layer PCB traces to minimum wiring resistance.
14	BST	Bootstrap. The high side MOS driver voltage of VDD2H is pumped external, a 220 nF ceramic capacitor between the VDD2H_SW and BST pins is connected.
15	VDDQ_GND	Power ground of VDDQ. Connect this pin to ground side of PVIN decouple cap and the ground layer of PCB using wide PCB traces and multiple vias.
16	VDDQ_SW	Switch node of VDDQ. Connect this pin to the inductor using short, wide and multi-layer PCB traces to minimum wiring resistance.
17	VDDQ_IN	Power input of VDDQ. Connect this pin to a 1.7V to 3.5V power supply. Place a 10µF decouple ceramic cap to the VDDQ_IN and VDDQ_GND as close as possible. Connect this pin to PVIN cap using wide PCB traces and multiple vias.
18	VDDQ_FB	FB pin of VDDQ. The output voltage can be adjusted by changing the ratio of FB resistor. Keep FB trace far away from SW and other noisy nodes as it is sensitive.
19	EN	Enable pin of whole chip. The EN pin is a digital input that enables or disables the chip. When EN high, the VDD1, VDD2H, VDD2L, VDDQ channels turn on with a specific sequence. When EN low, all channels turn off with sequence. EN pin is pulled low internally by resistor.
20	AVIN	External AVIN input. The AVIN pin supplies power for the logic controller and reference voltage. Decouple with a minimum 2.2µF ceramic cap as close to AVIN and AGND as possible. Series a 2.2Ω resistor to Ext 3.3V to filter input noise of switching frequency generated by Buck channel.
21	AGND	Analog ground. Connect AGND pin to a clean ground point.
22	VDD2L_FB	FB pin of VDD2L. The output voltage can be adjusted by changing the ratio of FB resistor. Keep FB trace far away from SW and other noisy nodes as it is sensitive.
23	VDD2L_IN	Power input of VDD2L. Connect this pin to a 1.7V to 3.5V power supply. Place a 10µF decouple ceramic cap to the VDD2L_IN and VDD2L_GND as close as possible. Connect this pin to PVIN cap using wide PCB traces and multiple vias.

Block Diagram

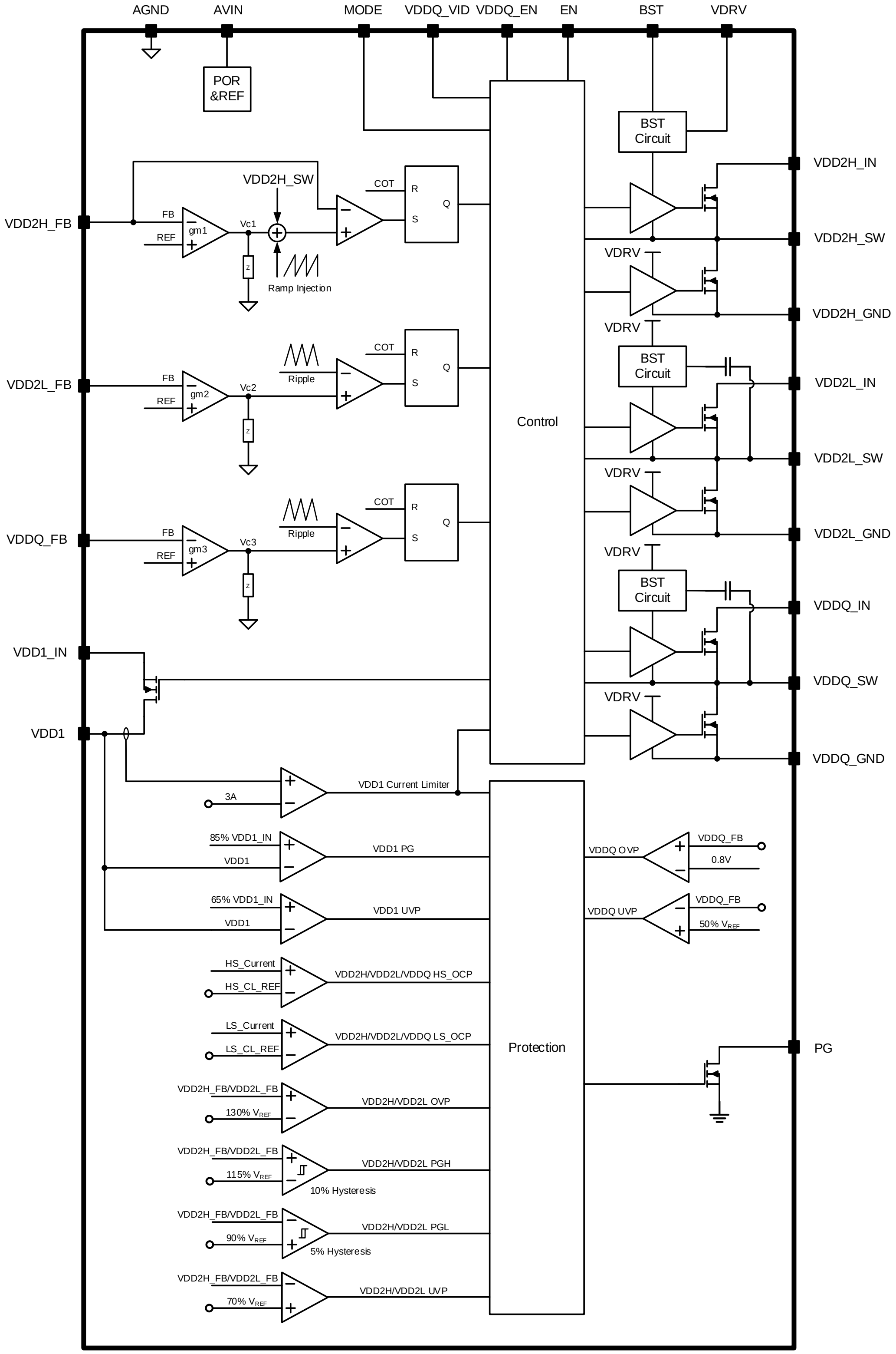


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VDD2H_IN		+25	V
VDD2H_SW	-0.3(-3.6V for <25ns)	+25(+28V for 25ns)	
BST		VDD2H_SW+4V	
VDD2L_IN		+4	
VDD2L_SW	-0.3 (-3.6V for <25ns)	+4(+9V for 10ns)	
VDDQ_IN		+4	
VDDQ_SW	-0.3 (-3.6V for <25ns)	+4(+9V for 10ns)	
Other PINs	-0.3	+4	
Junction Temperature Range		150	°C
Lead Temperature (Soldering, 10 sec.)		260	
Storage Temperature Range	-55	150	

ESD Ratings

Characteristic	Condition	Value	Unit
Electro Discharge	Human Body Model (HBM), Per ANSI/ESDA/JEDEC JS-001 (Latest Ver.)	±2000	V
	Charged Device Model (CDM), Per ANSI/ESDA/JEDEC JS-002 (Latest Ver.)	±750	

Latch-up

Characteristic	Pin Name	Condition	Value	Unit
External Input Pins(1)	EN,VDDQ_EN,VDDQ_VID	E-Test, I-Test / 1.5 X V_{MAXSUP}(2)	4	V
Power Input Pins(1)	VDD2H_IN	MSV(3) (Guarantee Level)	25	
	VDD2L_IN,VDDQ_IN		4	
	VDD1_IN		4	
All Other Pins(1)	VDRV,AVIN	1.5x VDD or MSV(3) (Guarantee Level)	4	

(1) JEDEC document JESD78F states that Signal-Pin-Test (External Input Pins) and Supply-Test (Power Input Pins) can accurately determine the latch-up sensitivity level.
(2) V_{MAXSUP}: It is the maximum supply voltage at which a supply is specified to operate in conformance with the applicable device specification.
(3) MSV: Maximum Stress Voltage.

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	17	°C/W
θ_{JC_TOP} Junction-to-Case(Top) Thermal Resistance	13.3	
θ_{JC_BOTTOM} Junction-to-Case(Bottom) Thermal Resistance	5.4	
θ_{JB} Junction-to-Board Thermal Resistance	7.2	
P_D Power Dissipation @ T_A = 25°C	7.3	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VDD2H_IN	3.15	22	V
VDD2L_IN	1.7	3.5	
VDDQ_IN	1.7	3.5	
VDD1_IN	1.6	2.0	
AVIN	3.15	3.5	
VDRV	3.15	3.5	
Junction Temperature	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{VDD2H_IN}= 12V, V_{AVIN} = 3.3V, V_{EN} = V_{DDQEN} = 2V, R_{MODE} = 0Ω, T_J = 25°C, unless otherwise noted.) (**Note 4**)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Input Supply (V_{VDD2H_IN})	Input Voltage Range	V_{VDD2H_IN}		3.15	12	22	V
	UVLO Rising Threshold	V_{UVLOR_VDD2H}		2.9	3.0	3.1	V
	UVLO Hysteresis	V_{UVLOR_HYS}			300		mV
Input Supply (V_{VDD2L_IN})	Input Voltage Range	V_{VDD2L_IN}		1.7	3.3	3.5	V
	UVLO Rising Threshold	V_{UVLOR_VDD2L}		1.55	1.6	1.65	V
	UVLO Hysteresis	V_{UVLOR_HYS}			200		mV
Input Supply (V_{VDDQ_IN})	Input Voltage Range	V_{VDDQ_IN}		1.7	3.3	3.5	V
	UVLO Rising Threshold	V_{UVLOR_VDDQ}		1.55	1.6	1.65	V
	UVLO Hysteresis	V_{UVLOR_HYS}			200		mV
Input Supply (V_{VDD1_IN})	Input Voltage Range	V_{VDD1_IN}		1.6	1.8	2.0	V
	UVLO Rising Threshold	V_{UVLOR_VDD1}		1.45	1.5	1.55	V
Driver Supply (V_{VDRV})	Input Voltage Range	V_{VDRV}		3.15	3.3	3.5	V
	UVLO Rising Threshold	V_{UVLOR_VDRV}		2.9	3.0	3.1	V
	UVLO Hysteresis	V_{UVLOR_HYS}			200		mV
AVIN Supply (V_{AVIN})	Input Voltage Range	V_{AVIN}		3.15	3.3	3.5	V
	UVLO Rising Threshold	V_{UVLOR_AVIN}		2.9	3.0	3.1	V
	UVLO Hysteresis	V_{UVLOR_HYS}			200		mV
Supply Current	AVIN supply current, all rails active	I_{AVIN}	V_{EN} = 2V, V_{VDDQ_EN} = 2V, V_{VDD1_IN} = 1.8V, V_{VDD2L_IN} = 3.3V, V_{VDDQ_IN} = 3.3V, no switching		107		µA
	AVIN supply current, VDD2H active only	I_{AVIN_VDD2H}	V_{EN} = 2V, V_{VDDQ_EN} = 0V, V_{VDD1_IN} = 0V, V_{VDD2L_IN} = 0V, V_{VDDQ_IN} = 0V, no switching		65		µA
	AVIN supply current, VDD2H and VDD1 active	$I_{AVIN\_VDD2H\_VDD1}$	V_{EN} = 2V, V_{VDDQ_EN} = 0V, V_{VDD1_IN} = 1.8V, V_{VDD2L_IN} = 0V, V_{VDDQ_IN} = 0V, no switching		67		µA
	AVIN supply current, VDD2H and VDD2L active	$I_{AVIN\_VDD2H\_VDD2L}$	V_{EN} = 2V, V_{VDDQ_EN} = 0V, V_{VDD1_IN} = 0V, V_{VDD2L_IN} = 3.3V, V_{VDDQ_IN} = 0V, no switching		85		µA
	AVIN supply current, VDD2H and VDDQ active	$I_{AVIN\_VDD2H\_VDDQ}$	V_{EN} = 2V, V_{VDDQ_EN} = 2V, V_{VDD1_IN} = 0V, V_{VDD2L_IN} = 0V, V_{VDDQ_IN} = 3.3V, no switching		84		µA
	AVIN shutdown current	I_{AVIN_SDN}	V_{EN} = 0V, no switching			2	µA

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
	VDRV shutdown current	I_{VDRV_SDN}	V_{EN} = 0V, no switching			1	µA
Enable Input Pin (EN)	High-Level Rising Threshold Voltage	V_{THR_EN}		1.1	1.2	1.3	V
	Hysteresis	V_{EN_HYS}			100		mV
	EN pin current	$I_{\_EN}$	V_{VDDQ_EN} 2V			5	µA
			V_{VDDQ_EN} 0V			1	µA
Enable Input Pin (VDDQ_EN)	High-Level Rising Threshold Voltage	$V_{THR\_VDDQ\_EN}$		1.1	1.2	1.3	V
	Hysteresis	$V_{VDDQ\_EN\_HYS}$			100		mV
	VDDQ_EN pin current	$I_{\_VDDQ\_EN}$	V_{VDDQ_EN} 2V			5	µA
			V_{VDDQ_EN} 0V			1	µA
Input Pin (VDDQ_VID)	VDDQ_VID low voltage threshold	$V_{VDDQ\_VID\_LOW}$				0.45	V
	VDDQ_VID high voltage threshold	$V_{VDDQ\_VID\_HIGH}$		0.7			V
Power Good Monitor Pin(PG)	Logic Level Low	V_{OL_PG}	I_{Sink}=4mA			0.4	V
	PG high to low delay	t_{PGTD_H-L}			20		us
	PG low to high delay	t_{PGTD_L-H}			2		us
	EN low to PG low	t_{PGTD_ENL-L}				1	us
Power Good Threshold Voltage(VDD2H)	Power Good Upper Threshold Rising	$V_{VDD2H\_PG\_TUR}$	% of V_{REF_VDD2H}		115		%
	Power Good Upper Threshold Falling	$V_{VDD2H\_PG\_TUF}$			105		
	Power Good Lower Threshold Rising	$V_{VDD2H\_PG\_TLR}$			95		
	Power Good Lower Threshold Falling	$V_{VDD2H\_PG\_TLF}$			90		
Power Good Threshold Voltage(VDD2L)	Power Good Upper Threshold Rising	$V_{VDD2L\_PG\_TUR}$	% of V_{REF_VDD2L}		115		%
	Power Good Upper Threshold Falling	$V_{VDD2L\_PG\_TUF}$			105		
	Power Good Lower Threshold Rising	$V_{VDD2L\_PG\_TLR}$			95		
	Power Good Lower Threshold Falling	$V_{VDD2L\_PG\_TLF}$			90		
Power Good Threshold Voltage(VDDQ)	Power Good Lower Threshold Falling	$V_{VDDQ\_PG\_TLF}$	% of V_{REF_VDDQ}		50		%
Power Good Threshold Voltage(VDD1)	Power Good Lower Threshold Rising	$V_{VDD1\_PG\_TLR}$	% of VDD1_IN		85		%
	Power Good Lower Threshold Falling	$V_{VDD1\_PG\_TLF}$			65		
Over-voltage protection (OVP) threshold	Over-voltage protection threshold of VDD2H	V_{OVP_VDD2H}	% of V_{REF}	125	130	135	%
	Over-voltage protection threshold of VDD2L	V_{OVP_VDD2L}		125	130	135	
	Over-voltage protection threshold of VDDQ	V_{OVP_VDDQ}		0.75	0.8	0.85	V
Under-voltage protection (UVP) threshold	Under-voltage protection threshold of VDD2H	V_{UVP_VDD2H}	% of V_{REF}	65	70	75	%
	Under-voltage protection threshold of VDD2L	V_{UVP_VDD2L}		65	70	75	

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
	Under-voltage protection threshold of VDDQ	V_{UVP_VDDQ}		45	50	55	
	Under-voltage protection threshold of VDD1	V_{UVP_VDD1}	% of VDD1_IN		65		
Mode Source Current		I_{MODE}		9	10	11	µA
Timing Characteristics	Soft-start Time for VDD1	t_{SS_VDD1}	EN high to VDD1 ready (85%)		0.47		ms
	Soft-start Time for VDD2H	t_{SS_VDD2H}	VDD1 ready to VDD2H ready (95%)		1.5		ms
	Soft-start Time for VDD2L	t_{SS_VDD2L}	VDD2H ready to VDD2L ready (95%)		1.1		ms
	Soft-start Time for VDDQ	t_{SS_VDDQ}	VDD2L ready to VDDQ ready, R_{MODE} = 0Ω/50kΩ/232kΩ, VDDQVID = High		0.4		ms
			VDD2L ready to VDDQ ready, R_{MODE} = 100kΩ/150kΩ, VDDQVID =High		0.11		ms
	Shutdown Delay Time for VDD1	$t_{SD\_DELAY\_VDD1}$	EN low to VDD1 off		5.96		ms
	Soft-shutdown Time for VDD2H	t_{SSD_VDD2H}	EN off to VDD2H drop to 0.2V		2.48		ms
	Soft-shutdown Time for VDD2L	t_{SSD_VDD2L}	EN off to VDD2L drop to 0.2V		0.98		ms
	Soft-shutdown Time for VDDQ	t_{SSD_VDDQ}	EN/VDDQ_EN low to VDDQ drop to 0.2V ,R_{MODE} = 0Ω/50kΩ/232kΩ, VDDQVID = High		0.37		ms
			EN/VDDQ_EN low to VDDQ drop to 0.2V ,R_{MODE} = 100kΩ/150kΩ, VDDQVID =High		0.08		ms
Overtemperature Protection (OTP)	Thermal Shutdown Temperature	T_{SD}	Thermal shutdown threshold		150		°C
	Thermal shutdown hysteresis	T_{SD_HYS}	Thermal shutdown hysteresis		25		°C

Power Converters

(V_{VDD2H_IN}= 12V, V_{AVIN} = 3.3V, V_{EN} = V_{DDQEN} = 2V, R_{MODE} = 0Ω, T_J = 25°C, unless otherwise noted.)

Parameter			Symbol	Condition	Min.	Typ.	Max.	Unit
VDD2H Synchronous Buck Converter	Output Voltage Default Value		V_{VDD2H}	R_3=6.8kΩ, R_4=40.2kΩ		1.065		V
	Internal Ref Voltage		V_{REF_VDD2H}		0.9	0.91	0.92	V
	Current	Continuous Output Current	I_{CC_VDD2H}		12			A
		Low Side Current Limit	$I_{LIMIT\_VDD2H\_LS}$	R_{MODE}=0Ω/150kΩ	14	15	16.5	A
		Low Side Current Limit	$I_{LIMIT\_VDD2H\_LS}$	R_{MODE}=50kΩ/100kΩ		13		A
		Low Side Current Limit	$I_{LIMIT\_VDD2H\_LS}$	R_{MODE}=232kΩ		18		A
	High Side FET Ron		$R_{ON\_HS\_VDD2H}$	NFET switch (VDD2H_IN to VDD2H_SW) , T_J=25°C		13.5		mΩ
	Low Side FET Ron		$R_{ON\_LS\_VDD2H}$	NFET switch (VDD2H_SW to GND) , T_J=25°C		6		mΩ
	High Side FET		$I_{AV\_VDD2H\_HS}$	V_{DD}=50V, L=100uH		16		A
			$E_{AV\_VDD2H\_HS}$			12.8		mJ

Parameter			Symbol	Condition	Min.	Typ.	Max.	Unit
	Low Side FET		$I_{AV\_VDD2H\_LS}$			25		A
			$E_{AV\_VDD2H\_LS}$			31.25		mJ
	Switch leakage		SW_{LKG_VDD2H}	V_{EN}=0V,V_{VDD2H_SW}=0V		0	1	µA
	Discharge Resistance		R_{DIS_VDD2H}	@100mA and 25°C		20		Ω
	Switching Frequency(CCM)		f_{SW_VDD2H}	R_{MODE}=0Ω/150kΩ/232kΩ or Float	500	600	700	kHz
				R_{MODE}=50kΩ/100kΩ		900		kHz
	Output Line Regulation		V_{VDD2H_LIR}	Ref Test Condition: V_{VDD2H_IN}=12V,V_{VDD2H}=1.065V,I_{OUT}=6A VDD2H_IN Range:3.15V~22V	-1		+1	%
	Output Load Regulation		V_{VDD2H_LOR}	Ref Test Condition: V_{VDD2H_IN}=12V,V_{VDD2H}=1.065V,I_{OUT}=6A Load Range:0A~ I_{CC_MAX}	-1		+1.5	%
	Output Load Transient		V_{VDD2H_LTR}	V_{VDD2H_IN}=12V,V_{VDD2H}=1.065V,0→70% I_{CC_MAX} @2.5A/us	-5		+5	%
				V_{VDD2H_IN}=12V, V_{VDD2H}=1.065V,30% I_{CC_MAX}→100% I_{CC_MAX} @2.5A/us	-5		+5	%
	Min on time (**Note 5**)		$t_{ON\_MIN\_VDD2H}$			60		ns
	Min off time (**Note 5**)		$t_{OFF\_MIN\_VDD2H}$			100		ns
VDD2L Synchronous Buck Converter	Output Voltage Default Value		V_{VDD2L}			0.91		V
	Internal Ref Voltage		V_{REF_VDD2L}		0.9	0.91	0.92	V
	Current	Continuous Output Current	I_{CC_VDD2L}		3			A
		Low Side Current Limit	$I_{LIMIT\_VDD2L\_LS}$		3.5	4	4.5	A
	High Side FET Ron		$R_{ON\_HS\_VDD2L}$	NFET switch (VDD2L_IN to VDD2L_SW) , T_J=25°C		70		mΩ
	Low Side FET Ron		$R_{ON\_LS\_VDD2L}$	NFET switch (VDD2L_SW to GND) , T_J=25°C		30		mΩ
	Switch leakage		SW_{LKG_VDD2L}	V_{EN}=0V,V_{VDD2L_SW}=0V		0	1	µA
	Discharge Resistance		R_{DIS_VDD2L}	@100mA and 25°C		5		Ω
	Switching Frequency(CCM)		f_{SW_VDD2L}	R_{MODE}=0Ω/150kΩ/232kΩ or Float	500	600	700	kHz
				R_{MODE}=50kΩ/100kΩ		900		kHz
	Output Line Regulation		V_{VDD2L_LIR}	Ref Voltage Test Condition: V_{VDD2L_IN}=3.3V,V_{VDD2L}=0.91V,I_{OUT}=1.5A VDD2L_IN Range:1.7V~3.5V	-1		+1	%
	Output Load Regulation		V_{VDD2L_LOR}	Ref Voltage Test Condition: V_{VDD2L_IN}=3.3V,V_{VDD2L}=0.91V,I_{OUT}=1.5A Load Range:0A~ I_{CC_MAX}	-1		+1.5	%
	Min on time (**Note 5**)		$t_{ON\_MIN\_VDD2L}$			60		ns
	Min off time (**Note 5**)		$t_{OFF\_MIN\_VDD2L}$			100		ns
VDDQ Synchronous Buck Converter	Output Voltage Default Value		V_{VDDQ}			0.515		V
	Internal Ref Voltage		V_{REF_VDDQ}	VDDQ_VID High	0.51	0.515	0.52	V
				VDDQ_VID Low	0.305	0.31	0.315	V
	Current	Continuous Output Current	I_{CC_VDDQ}		3			A
		Low Side Current Limit	$I_{LIMIT\_VDDQ\_LS}$		4	4.5	5	A

Parameter			Symbol	Condition	Min.	Typ.	Max.	Unit
	High Side FET Ron		$R_{ON\_HS\_VDDQ}$	NFET switch (VDDQ_IN to VDD2L_SW), T_J=25°C		70		mΩ
	Low Side FET Ron		$R_{ON\_LS\_VDDQ}$	NFET switch (VDDQ_SW to GND) , T_J=25°C		30		mΩ
	Switch leakage		SW_{LKG_VDDQ}	V_{EN}=0V,V_{VDDQ_SW}=0V		0	1	µA
	Discharge Resistance		R_{DIS_VDDQ}	@100mA and 25°C		5		Ω
	Switching Frequency(CCM)		f_{SW_VDDQ}	R_{MODE}=0Ω/150kΩ/232kΩ or Float	500	600	700	kHz
				R_{MODE}=50kΩ/100kΩ		900		kHz
	Output Line Regulation		V_{VDDQ_LIR}	Ref Voltage Test Condition: V_{VDDQ_IN}=3.3V,V_{VDDQ}=0.515V/0.31V,I_{OUT}=1.5A VDDQ_IN Range:1.7V~3.5V	-1		+1	%
	Output Load Regulation		V_{VDDQ_LOR}	Ref Voltage Test Condition: V_{VDDQ_IN}=3.3V,V_{VDDQ}=0.515V,I_{OUT}=1.5A Load Range:0A~ I_{CC_MAX}	-1		+1.5	%
				Ref Voltage Test Condition: V_{VDDQ_IN}=3.3V,V_{VDDQ}=0.31V,I_{OUT}=1.5A Load Range:0A~ I_{CC_MAX}	-1		+2.5	%
	Min on time (**Note 5**)		$t_{ON\_MIN\_VDDQ}$			60		ns
	Min off time (**Note 5**)		$t_{OFF\_MIN\_VDDQ}$			100		ns
VDD1 Load Switch	FET Ron		R_{ON_VDD1}	T_J=25°C		25		mΩ
	Discharge Resistance		R_{DIS_VDD1}	@100mA and 25°C		1		kΩ
	Current	Continuous Output Current	I_{CC_VDD1}			1		A
		Fast Current Limit	$I_{LIMIT\_VDD1\_FAST}$			5		A
		Slow Current Limit	$I_{LIMIT\_VDD1\_SLOW}$		2.5	3	3.5	A

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a six-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

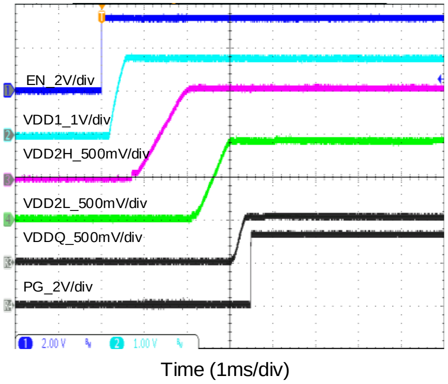
Note 4: Unless otherwise stated, limits are 100% production tested and guaranteed by statistical correlation at $T_A \cong T_J$ = 25°C.

Note 5: Guaranteed by design or statistical correlation and not production tested.

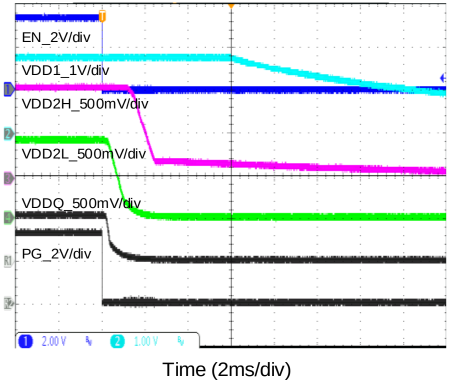
Note 6: GPIO pin (EN/VDDQ_EN/VDDQ_VID) voltage cannot exceed the voltage of AVIN.

Typical Performance Characteristics

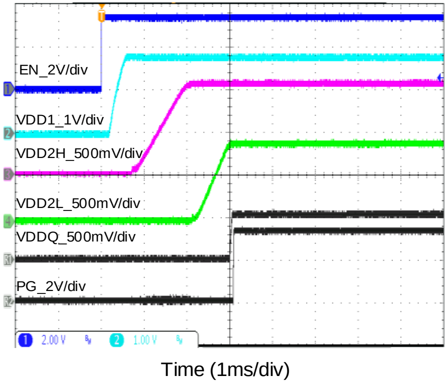
EN On Sequence
(VDD2H_IN 12V, AVIN/VDRV/VDD2L_IN/VDDQ_IN 3.3V,VDD1_IN 1.8V,VDDQ_VID high, R_{MODE}=232kohm(SR_{VDDQ} 2mV/us))



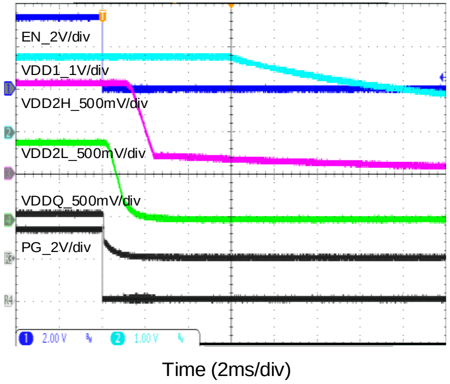
EN Off Sequence
(VDD2H_IN 12V, AVIN/VDRV/VDD2L_IN/VDDQ_IN 3.3V,VDD1_IN 1.8V,VDDQ_VID high, R_{MODE}=232kohm(SR_{VDDQ} 2mV/us))



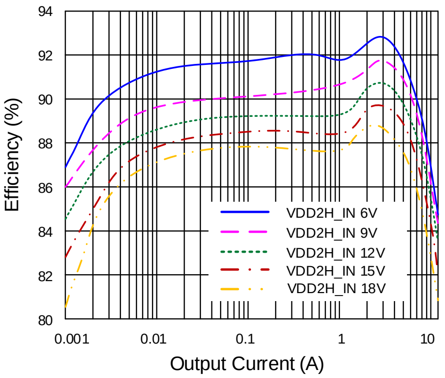
EN On Sequence
(VDD2H_IN 12V, AVIN/VDRV/VDD2L_IN/VDDQ_IN 3.3V,VDD1_IN 1.8V,VDDQ_VID high, R_{MODE}=100kohm(SR_{VDDQ} 10mV/us))



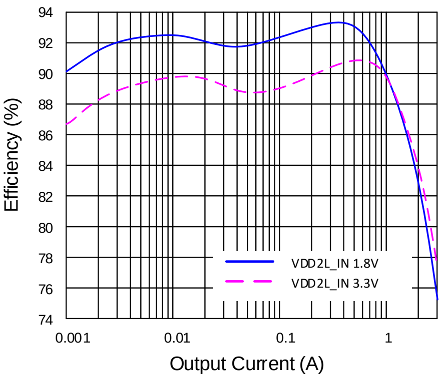
EN Off Sequence
(VDD2H_IN 12V, AVIN/VDRV/VDD2L_IN/VDDQ_IN 3.3V,VDD1_IN 1.8V,VDDQ_VID high, R_{MODE}=100kohm(SR_{VDDQ} 10mV/us))



Efficiency vs Output Load
(VDRV and AVIN 3.3V, VDD2H= 1.065V,f_{SW}=600kHz)

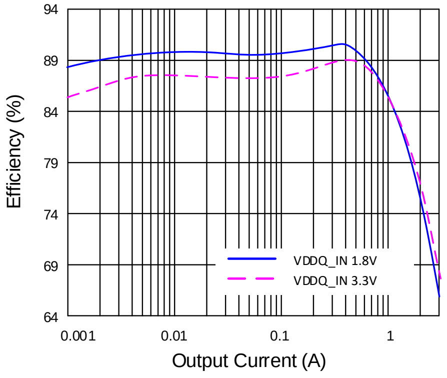


Efficiency vs Output Load
(VDRV and AVIN 3.3V, VDD2L=0.92V,f_{SW}=600kHz)



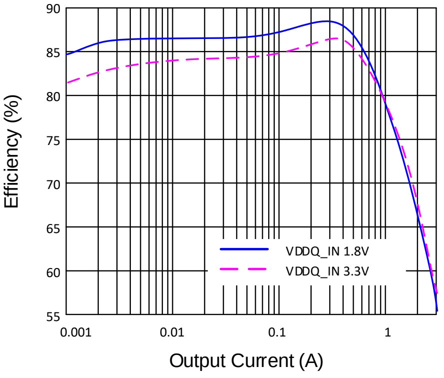
Efficiency vs Output Load

(VDRV and AVIN 3.3V, VDDQ=0.52V,f_{SW}=600kHz)



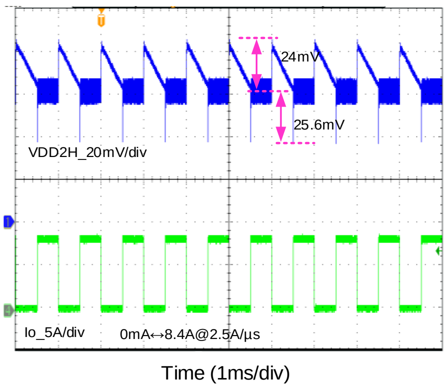
Efficiency vs Output Load

(VDRV and AVIN 3.3V, VDDQ=0.313V,f_{SW}=600kHz)



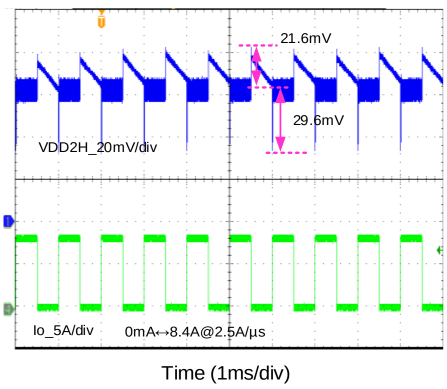
VDD2H Load Transient Response

(12V→1.065V,f_{SW} 600kHz)



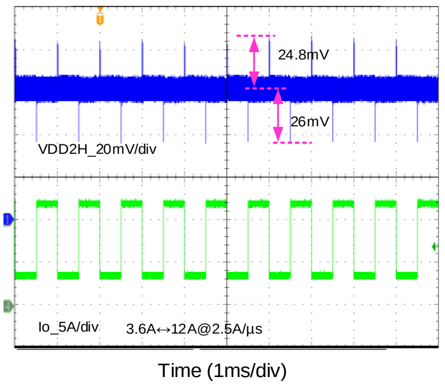
VDD2H Load Transient Response

(12V→1.065V,f_{SW} =900kHz)



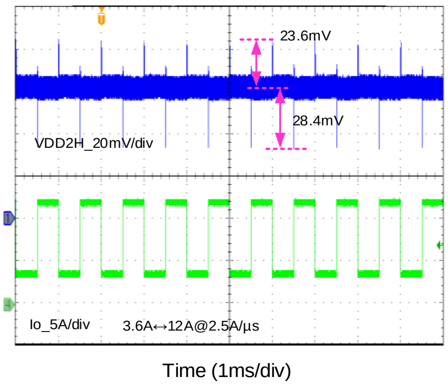
VDD2H Load Transient Response

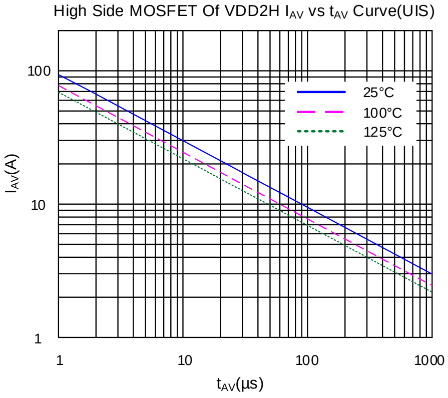
(12V→1.065V,f_{SW} 600kHz)

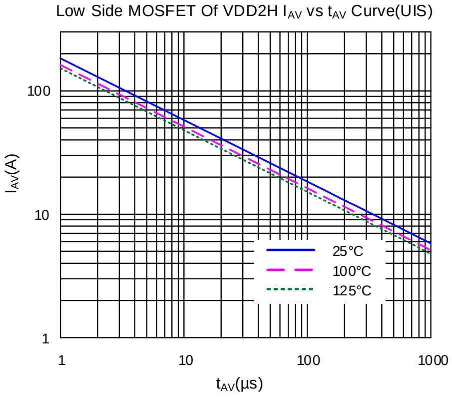


VDD2H Load Transient Response

(12V→1.065V,f_{SW} =900kHz)







Note: No Margin is reserved in the UIS Curve, Test data is based on FT Result.

Functional Description

EN Logic

The SY70501 uses two enable pins (EN and VDDQ_EN) to control power output. The EN pin controls all channels on or off, and VDDQ_EN pin only controls VDDQ rail operation. Table 1 shows the on/off logic for EN and VDDQ_EN. VDDQ is turned on when both EN and VDDQ_EN are driven high.

1) When EN is driven high or pull low, all channels will power on and off in sequence, and PG will switch to high-impedance state when the last channel soft-start is done, and pulled low when EN pin is driven low.
2) If VDDQ_EN is low before VDD2L exceeds 95% V_{REF_VDD2L}, PG pin will switch to high-impedance when VDD2L soft-start is done and VDDQ is off.
3) VDD2H,VDD2L and VDDQ will Soft Shutdown when EN pull low, and MOSFET will stop switching when the output voltage is lower than 200mV, and the discharge MOSFET is turned on. VDD1 output voltage will be discharged by internal discharge resistor when EN is driven low and VDD1 is turned off.

Table 1. EN and VDDQ_EN Logic

EN	VDDQ_EN	VDD2H	VDD2L	VDDQ	VDD1
High	High	ON	ON	ON	ON
High	Low	ON	ON	OFF	ON
Low	High/Low	OFF	OFF	OFF	OFF

EN On/Off Sequence

The EN pin is utilized to enable or disable the SY70501 device, with its default state being pulled low by an internal resistor. When the pin is set to a high state, the SY70501 device is enabled, whereas a low state disables the chip.

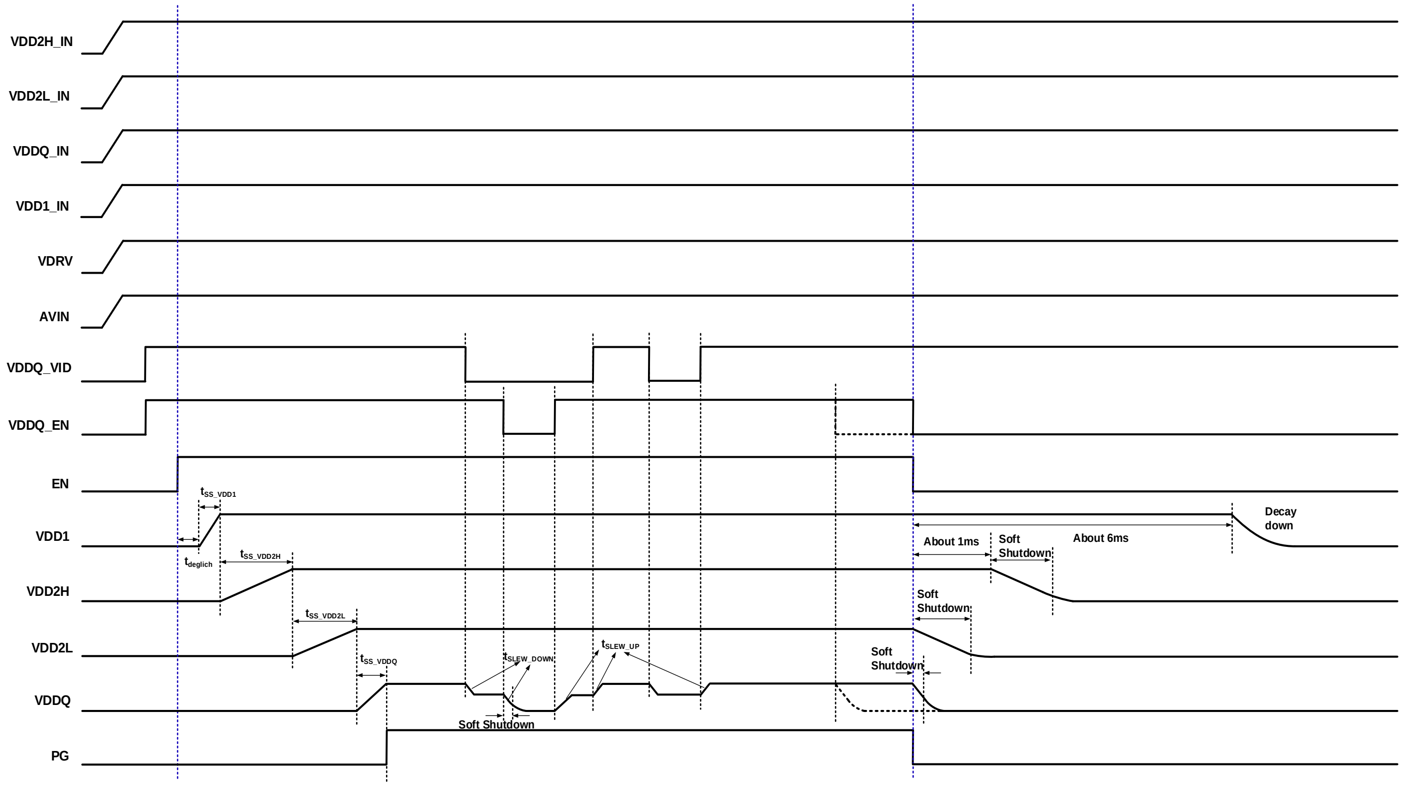


Figure 3. EN On/Off Output Sequencing

Mode Selection

The switching frequency of all the buck converters, current limit value of VDD2H and the VDDQ slew rate can be configured based on the R_{MODE} value.

1) When V_{VDRV}, V_{AVIN}, V_{VDD2H_IN} reach UVLO threshold voltage and the EN pin is pulled high, a one-shot signal followed by the POR signal are generated, and the Mode Selection circuit is enabled.
2) The detected MODE state is latched within 100us after POR signal is generated. After the MODE Selection is completed, the circuitry is turned off to save power.

Table 2 shows the MODE selection options.

Table 2. Mode Selection

R_{MODE}	f_{SW}	I_{LIMIT_VDD2H}	SR_{VDDQ}
232kΩ or Float	600kHz	18A	2mV/us
150kΩ	600kHz	15A	10mV/us
100kΩ	900kHz	13A	10mV/us
50kΩ	900kHz	13A	2mV/us
0kΩ	600kHz	15A	2mV/us

Soft-start and Soft Shutdown

1) The SY70501 controls the output slew-rate to minimize output voltage overshoot and inrush current during soft-start.
2) The device meets the JEDEC requirements for LPDDR5/LPDDR5X start-up and shutdown sequences by controlling EN and VDDQ_EN pins.
3) All buck converters support soft-start with pre-bias voltage. This is accomplished by keeping the high-side and low-side MOSFETs off until Vref exceeds the FB voltage.
4) All buck converters support soft shutdown when the EN pin is pulled low. The slew-rate of the soft shutdown is same as soft-start.
5) The soft-start and soft shutdown sequences are shown in Figure 3.

VDDQ Dynamic Voltage Scaling

The output voltage of VDDQ is controlled by the VDDQ_VID pin.

1) VDDQ_VID pin is pulled high internally.
2) DVS slew rate is same as the soft start slew rate shown in Table 2 and it is defined by R_{MODE}.
3) Fault detection is blanked during DVS.

VDDQ Voltage Control Logic is shown in Table 3.

Table 3. VDDQ Voltage Control Logic

VDDQ_EN	VDDQ_VID	V_{VDDQ}
High	High	0.515V
High	Low	0.31V
Low	High/Low	0V

Power-Good (PG) Logic

The PG pin is used as power good indicator and uses an open drain configuration. It is in high-impedance state when all the output channels are within the valid range. The pin is pulled low when the voltage of any channel falls below or goes above the thresholds (see EC table for the thresholds).

1) PG turns to high impedance after 2us when the output voltage of all active channels is within the valid range during the soft-start period.

   PG is pulled low after 20us when the output voltage of any active channel is outside of the valid range.

2) Fault detection is active once the channel startup ends, and blanked during the normal power-up, shut down and DVS transitions (VDDQ).

3) In case of a PG fault, the channel which ramp up after PG fault channel is shut down immediately. The shutdown channel will ramp up again when PG fault is removed and the device is enabled.

4) If any of the VDD1, VDD2L or VDDQ channels is not used, PG indicates the correct status for the active channels.

5) After soft-start is completed, PG remains high even if VDDQ_EN turns off the VDDQ channel.

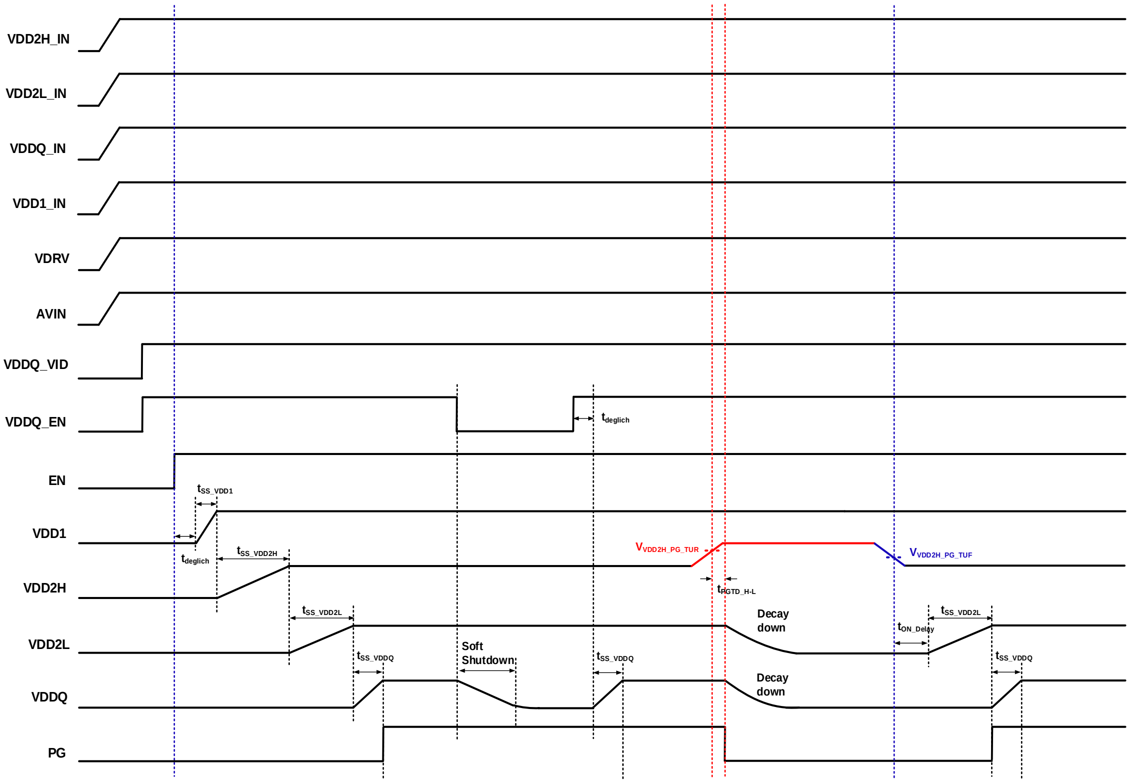


Figure 4. PG Logic

PG Status during Fault Events	Channel				
PG Fault Channel	VDD1	VDD2H	VDD2L	VDDQ	PG
VDD2H	ON	ON	OFF	OFF	Low
VDD2L	ON	ON	ON	OFF	Low
VDDQ	ON	ON	ON	ON	Low

OCP Protection

Each converter has a current limit function. All buck converters integrate current limit control for the high-side and low-side MOSFETs during operation, using separate current-sense circuits. The high-side MOSFET is turned off when $I_L > I_{LIMIT\_HS}$, and the low-side MOSFET is not allowed to be turned-off until $I_L < I_{LIMIT\_LS}$. Figure 5 shows the OCP logic.

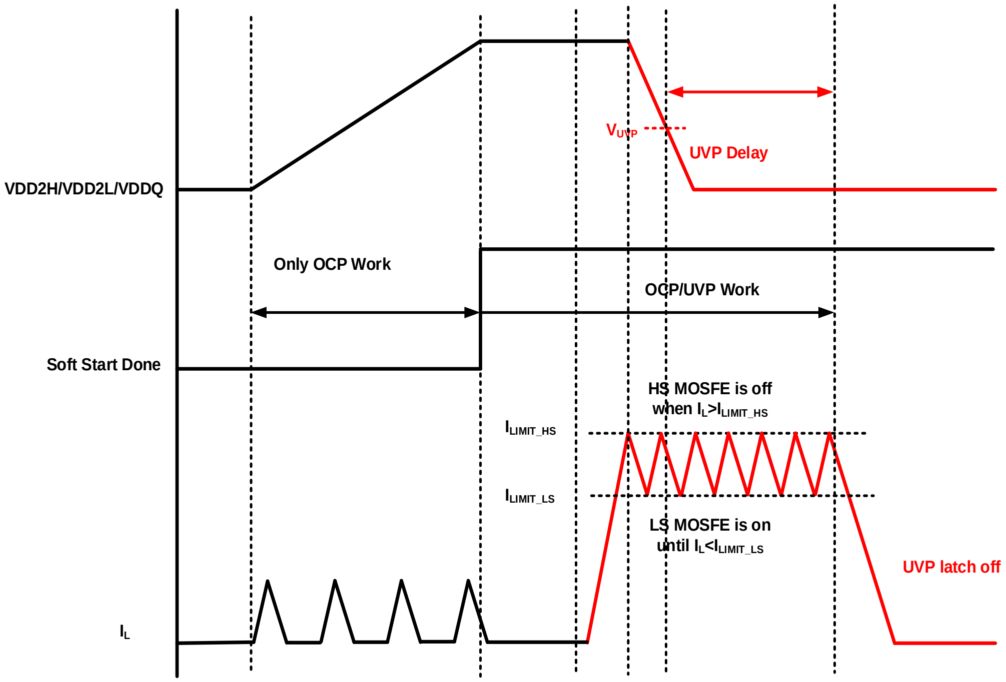


Figure 5. Buck OCP Logic

VDD1 provides a current limit function. When the current flow through the MOSFET exceeds 5A current limit ($I_{LIMIT\_VDD1\_FAST}$), the current limit loop starts regulating the gate voltage to keep the current flow through MOSFET below 3A. When V_{VDD1}< V_{UVP_VDD1}, and UVP fault happens, VDD1 turns off and PG is pulled low, while the discharge Resistor is turned on.

Figure 6 shows VDD1 OCP logic.

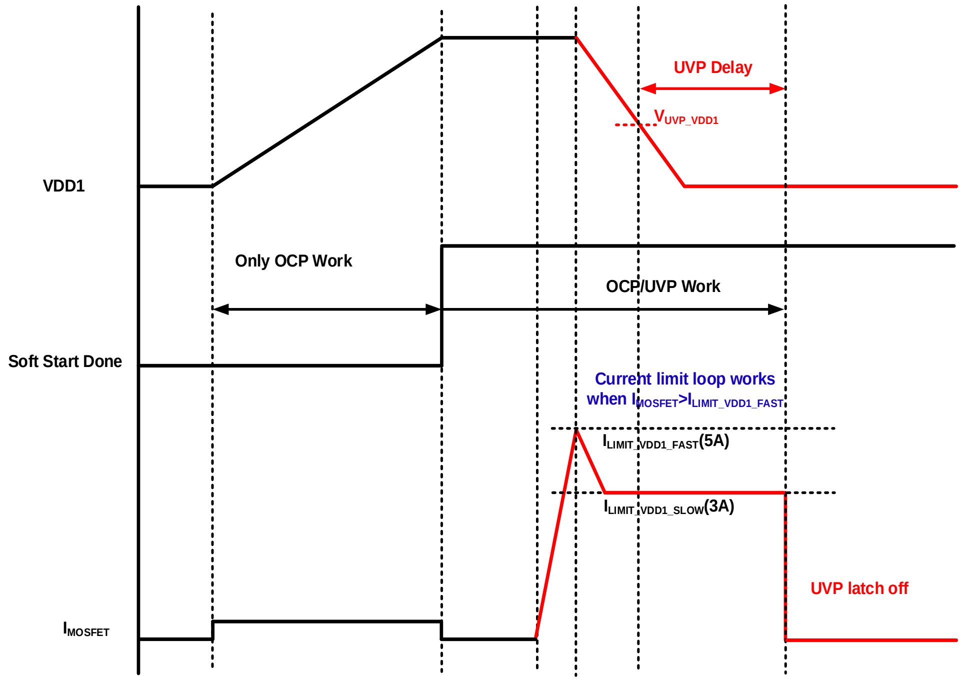


Figure 6. VDD1 OCP Logic

UVP Protection

The SY70501 supports output undervoltage protection. The output voltage will fall when OCP is triggered. When the voltage drops below the UVP threshold, the converter will latch in the off state.

1) If VDD2H, VDD2L or VDDQ UVP faults happen, the VDD1 rail stays turned on, but all the other channels are latched in the off state.
2) If VDD1 UVP fault happens, all channel are latched off and PG is pulled low.
3) For VDD1, when UVP happens, the converter is turned off immediately, then the discharge resistor is enabled to discharge the output voltage.
4) For all the buck channels, when an UVP event is detected, the high-side MOSFET can't be turned on again, and the low-side MOSFET will turn off when zero crossing is detected. The corresponding discharge resistor is turned on to discharge output voltage.

The Figure 7 and Figure 8 show VDD2H and VDD1 UVP operation.

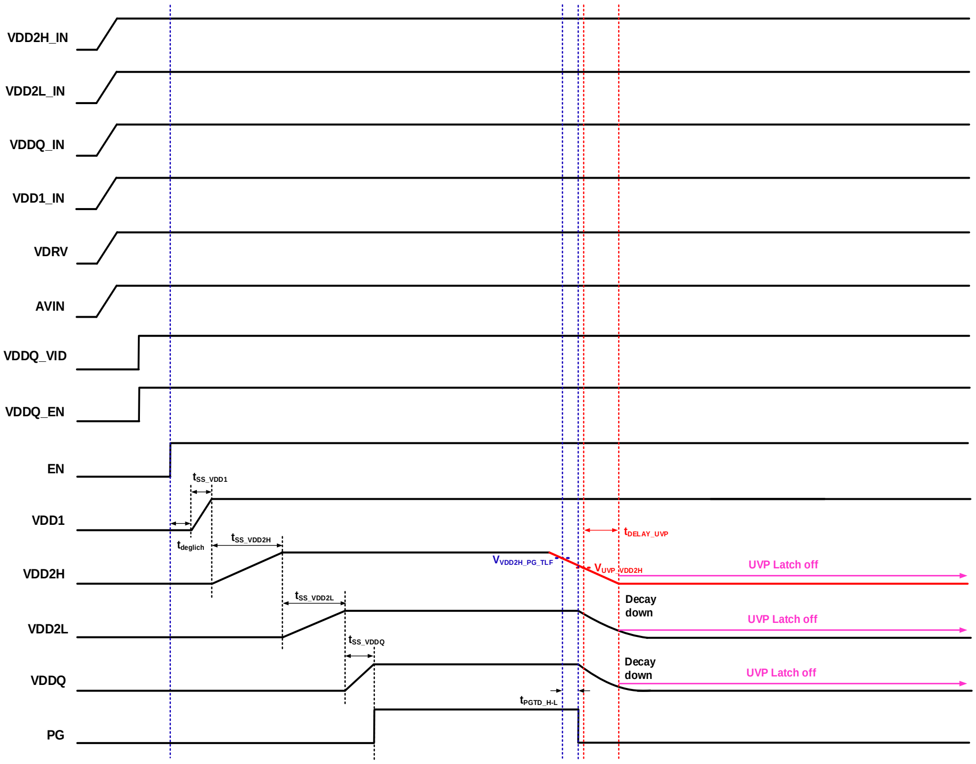


Figure 7. VDD2H UVP Protection

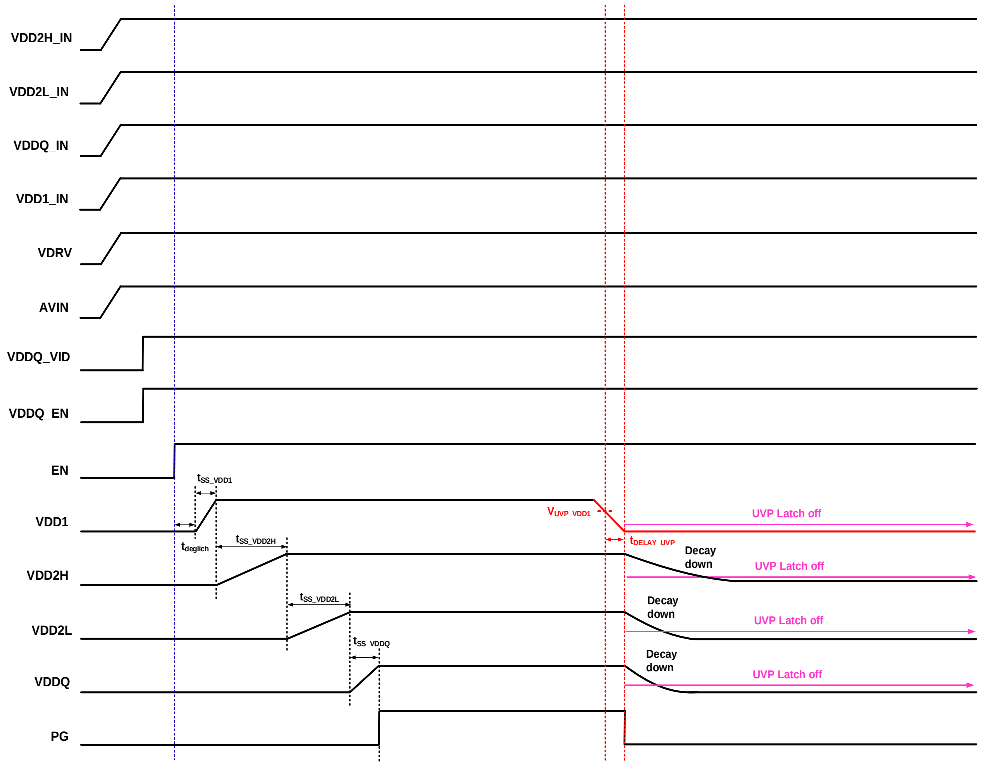


Figure 8. VDD1 UVP Protection

Temperature Shutdown (TSD) Protection Logic

1) If the temperature rises above 150°C, the device will turn off all the channels, VDD2H/VDD2L/VDDQ will turn off with soft shutdown and the PG pin will be pulled low.

2) When T_J falls down below 125°C, the device exits the protection state, and all channels will start-up again using the start-up delays for sequencing. The PG pin will switch to high-impedance when all the voltages are within the normal operating range.

The Figure 9 shows TSD logic.

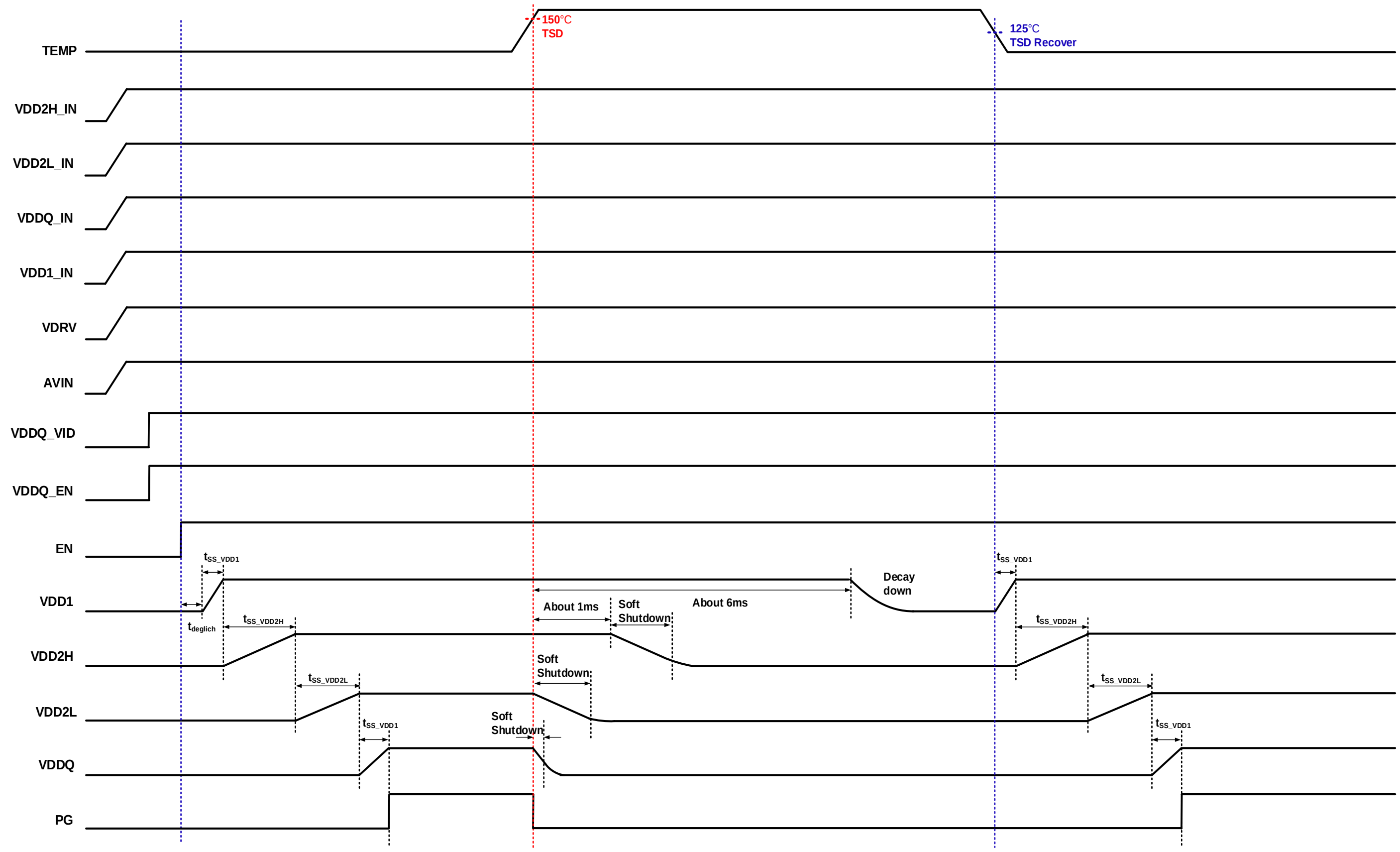


Figure 9. TSD Logic

Output OVP

If any of the VDD2H/VDD2L/VDDQ rails exceeds their OVP threshold voltage, the device will turn off all of the channels except VDD1, and PG pin will be pulled low. The converters will stay off and PG pin kept low even if the output OVP fault is removed. The Figure 10 shows VDD2H Output after an OVP event.

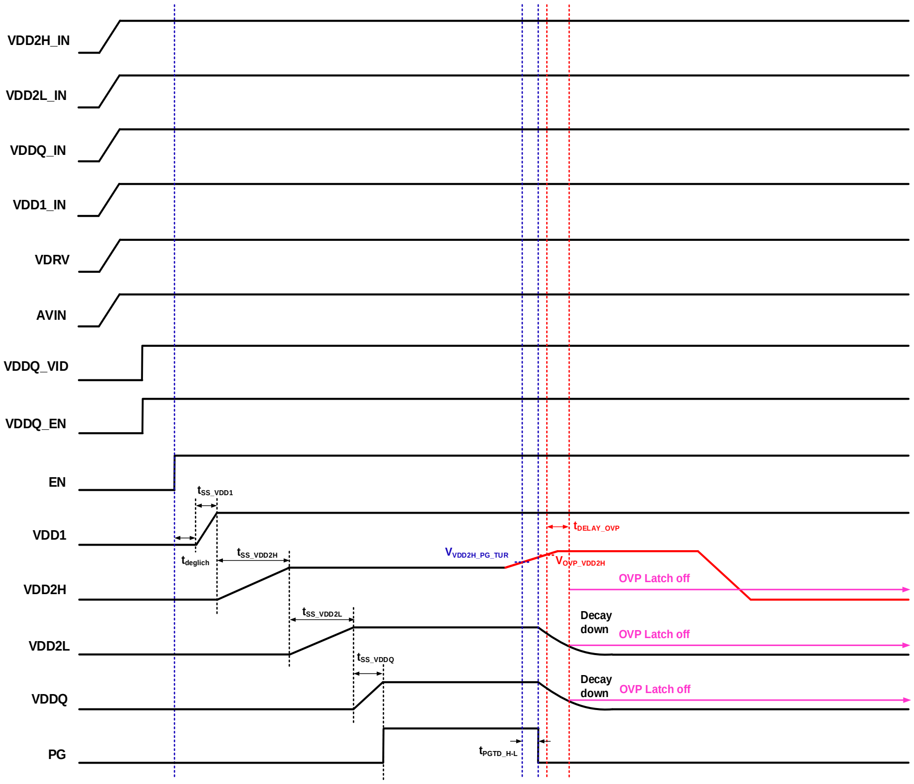


Figure 10. VDD2H Output OVP Operation

UVLO Protection

All input power pins support under voltage lockout protection, including VDD2H_IN(3V), VDD2L_IN(1.6V), VDDQ_IN(1.6V), VDD1_IN(1.5V), AVIN(3V) and VDRV(3V). The AVIN, VDRV, VDD2H_IN and VDDQ are use non-latched protection, while VDD2L_IN, VDD1_IN use latched-off protection.

The SY70501 can turn on using the start-up sequence only when VDD2H_IN, VDRV, AVIN exceed their UVLO thresholds and EN pin is pulled high.

When VDDQ_IN falls and becomes lower than the UVLO threshold voltage, VDDQ is shut down but the PG pin stays high-impedance. Once VDDQ_IN goes above the UVLO threshold voltage, VDDQ rail starts ramping up.

The Figure 11 shows VDD2L UVLO operation. Figure 12 and Figure 13 show VDDQ UVLO operation.

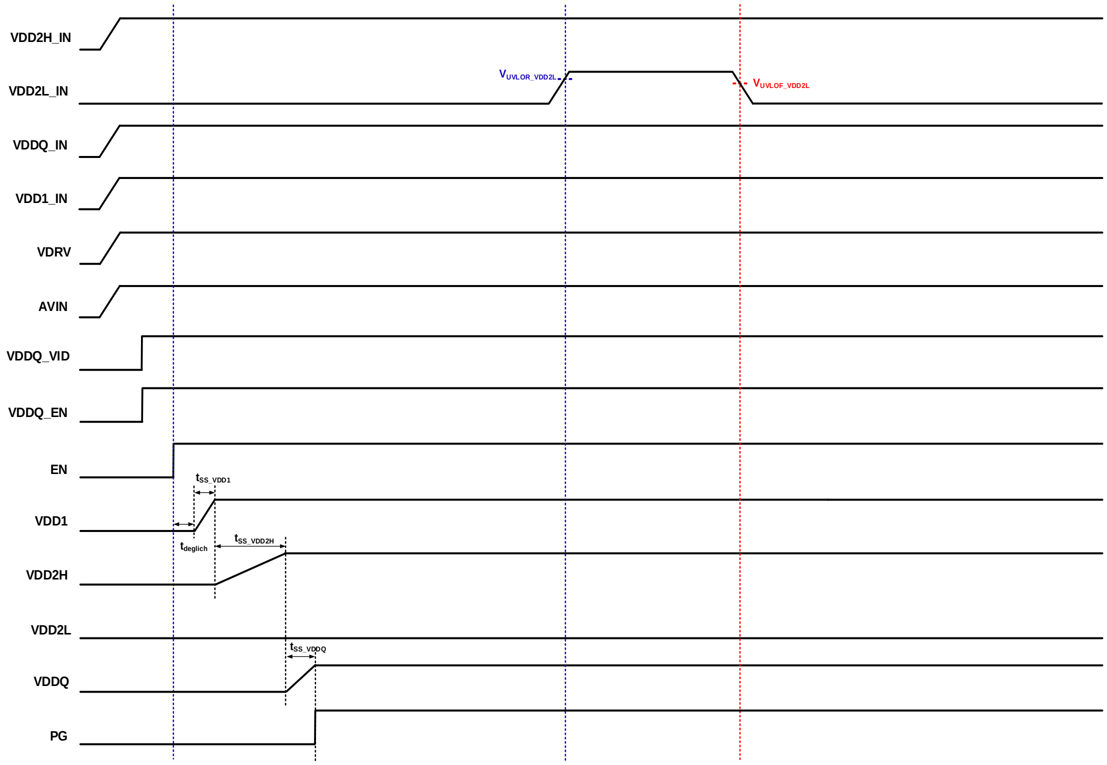


Figure 11. VDD2L UVLO Operation (Latch)

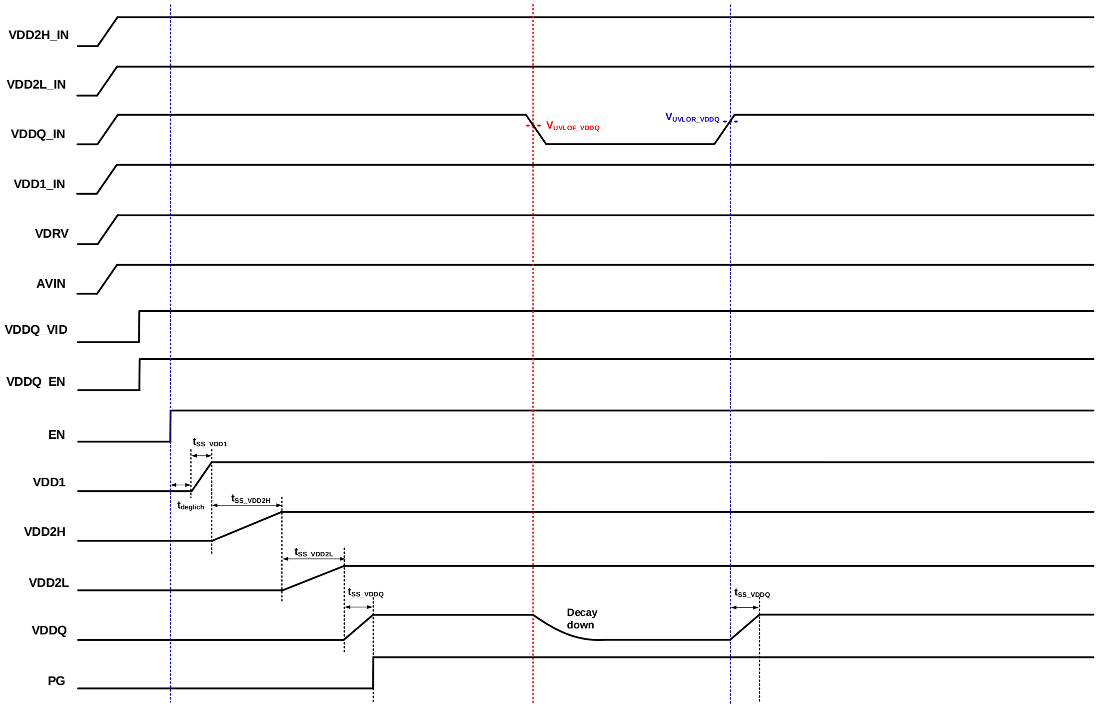


Figure 12. VDDQ UVLO Operation (Non-Latch, VDDQ UVLO fault after PG pull high)

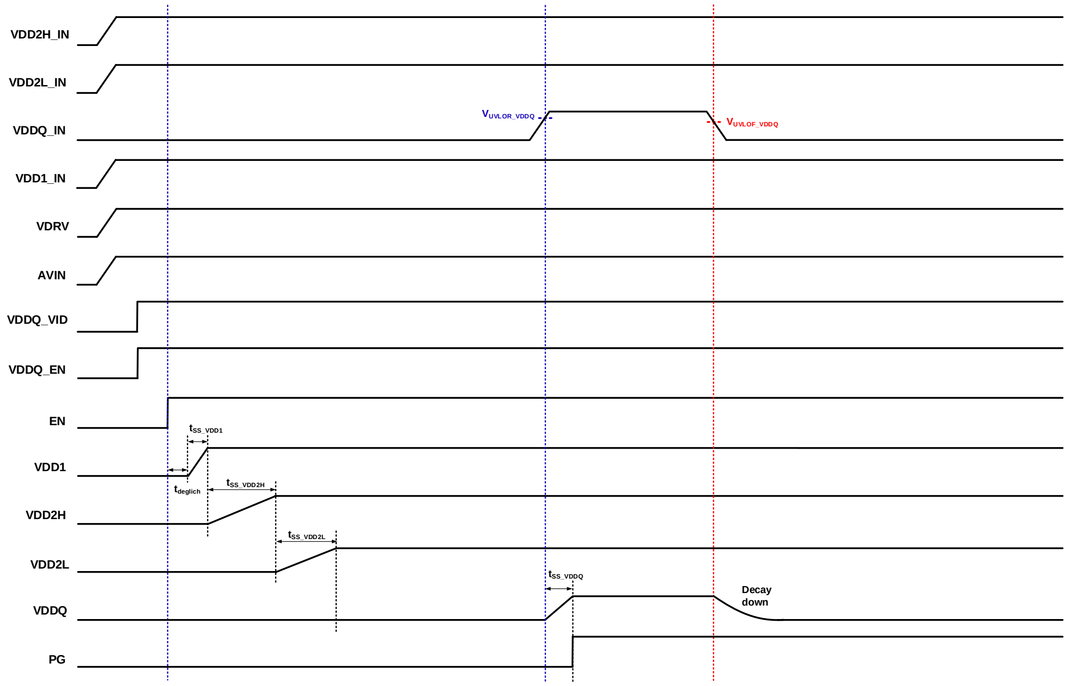


Figure 13. VDDQ UVLO Operation (Non-Latch, VDDQ UVLO fault before VDD2L PG ok)

Increasing the UVLO threshold voltage for VDD2H_IN can be achieved by adjusting the ratio of R_{UP1} and R_{DOWN1}. The new UVLO threshold can be calculated using the following equation:

$$V_{UVLOR}=\frac{\left(R_{UP1}+R_{DOWN1}\right)\cdot V_{THR\_EN}}{R_{DOWN1}}>V_{UVLOR\_VDD2H}$$

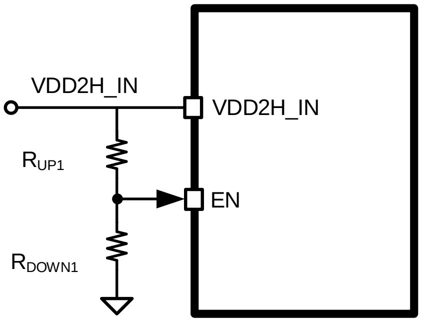


Figure 14. Circuit for Adjusting the VDD2H UVLO Threshold Voltage

Discharge Function

The SY70501 integrates discharge circuits for all channels. The discharge circuits turn on when UVP, OCP, OVP, UVLO, TSD fault happen or the EN pin is pulled low, except the period during VDD2H, VDD2L and VDDQ soft shutdown.

Application Information

Feedback Resistor and Feed-forward Capacitor Selection

Choose R_{UP2} and R_{DOWN2} to program the proper output voltage. Choose large resistance values for both R_H and R_L to minimize power consumption under light loads. For these rails V_{OUT} can be calculated using the following equation:

$$V_{OUT}=\frac{\left(R_{UP2}+R_{DOWN2}\right)\cdot V_{FB}}{R_{DOWN2}}$$

Where $V_{FB}=V_{REF}$. C_{FF} is used to improve load transient performance and phase margin. Using an optimal C_{FF} value is important for loop stability.

$$C_{FF}=\frac{1}{2\pi\times f_c\times R_{UP2}}$$

Where fc is the crossover frequency without C_{FF}.

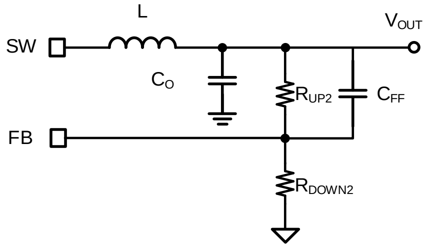


Figure 15. Output Voltage Adjustment Reference Circuit

Input Capacitor Selection

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply and to reduce EMI. When selecting an input capacitor, select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. Systems that are powered by long wires may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum, or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS}=I_{OUT}\times\sqrt{D\times(1-D)}$$

The worst-case condition occurs at D = 0.5, resulting in

$$I_{CIN\_RMS\_MAX}=\frac{I_{OUT}}{2}$$

For simplicity, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification. Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated as follows:

$$V_{CIN\_RIPPLE} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at D = 0.5, resulting in

$$V_{CIN\_RIPPLE\_MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. Place the ceramic input capacitors as close to the IN and GND pins as possible.

Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. Selecting a low inductor value will help reduce size and cost and enhance transient response, but will increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low value inductors may help reduce DC losses and increase efficiency. Higher inductor values tend to have higher DCR for the same size, and slow transient response.

A reasonable compromise between size, efficiency, and transient response can be obtained by selecting a ripple current (ΔIL) approximately 20%–50% of the desired full output load current. Start calculating the approximate inductor value by selecting the input and output voltages, the operating frequency (f_{SW}), the maximum output current ($I_{OUT,MAX}$) and estimating a ΔI_L as some percentage of that current.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current (ΔI_L) and required peak current inductor current I_{L_PEAK} according to the following equations:

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L_1}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{\Delta I_L}{2}$$

Select an inductor with a saturation current higher than I_{L_PEAK}.

For maximum efficiency, select an inductor with a low DCR that meets the inductance, size, and cost targets. Low loss ferrite materials should be considered.

Output Capacitor C_{OUT} Selection

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady-state ripple and transient requirements must be taken into consideration when selecting this capacitor. Ceramic and POS types are most often selected due to their small size and low cost.

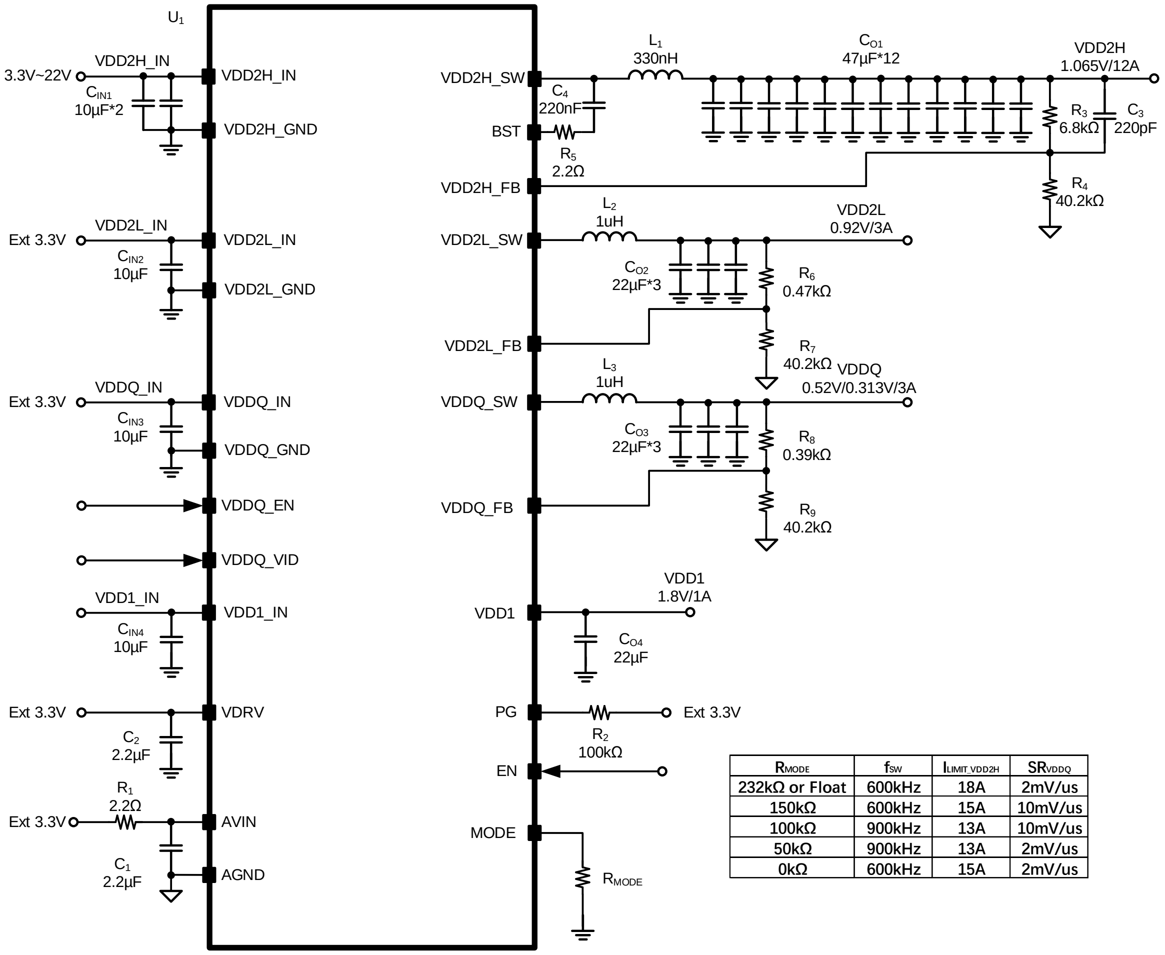
Output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitors ESR (ESR ripple) as well as the stored charge (capacitive ripple). When estimating the total ripple, both should be considered.

$$V_{RIPPLE\_ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE\_CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Using ceramic capacitors connected in parallel is recommended for a typical application.

Application Schematic



R_{MODE}	f_{SW}	I_{LIMIT_VDD2H}	SR_{VDDQ}
232kΩ or Float	600kHz	18A	2mV/us
150kΩ	600kHz	15A	10mV/us
100kΩ	900kHz	13A	10mV/us
50kΩ	900kHz	13A	2mV/us
0kΩ	600kHz	15A	2mV/us

BOM List

Reference Designator	Description	Part Number	Manufacturer	Qty
U_1	PMIC	SY70501TDQ	SILERGY	1
L_1	330nH,15%,2.6mΩ,25.2A	SPM6550CT-R33L	TDK	1
L_2,L_3	1uH,20%,30mΩ,5.1A	TMS322512ALM-1R0MTAA	TDK	2
C_{IN1}	10µF,20%,25V,X5R,0603(in)	C1608X5R1E106M080AC	TDK	2
C_{IN2},C_{IN3}, C_{IN4}	10µF,20%,6.3V,X5R,0603(in)	C1608X5R0J106M080AB	TDK	3
C_{O2},C_{O3},C_{O4}	22µF,20%,6.3V,X5R,0603(in)	C1608X5R0J226M080AC	TDK	7
C_{O1}	47µF,20%,6.3V,X5R,0805(in)	C2012X5R0J476M125AC	TDK	12
C_1, C_2	2.2µF,20%,6.3V,X5R,0402(in)	C1005X5R0J225M050BC	TDK	2
C_3	220pF,5%,50V,NP0,0402(in)	C1005NP01H221JT00F	TDK	1
C_4	220nF,10%,6.3V,X5R,0402(in)	C1005X5R0J224KT00F	TDK	1
R_1, R_5	2.2Ω,1%,1/16W,0402(in)	RT0402FRE072R2L	YAGEO	2
R_2	100kΩ,1%,1/16W,0402(in)	RT0402FRE07100KL	YAGEO	1
R_3	6.8kΩ,1%,1/16W,0402(in)	RT0402FRE076K8L	YAGEO	1
R_4, R_7, R_9	40.2kΩ,1%,1/16W,0402(in)	RT0402FRE0740K2L	YAGEO	3

Reference Designator	Description	Part Number	Manufacturer	Qty
R_6	0.47kΩ,1%,1/16W,0402(in)	RC0402FR-07470RL	YAGEO	1
R_8	0.39kΩ,1%,1/16W,0402(in)	RC0402FR-07390RL	YAGEO	1
R_{MODE}	0Ω/50kΩ/100kΩ/150kΩ/232kΩ, 1%,1/16W,0402(in)	RC0402FR-070RL/ RC0402FR-0750KL/ RT0402FRE07100KL/ RC0402FR-07150KL/ RC0402FR-07232KL	YAGEO	1

Layout Design

Follow the PCB layout guidelines below for optimal performance and thermal dissipation.

Buck Converters

- **Input Capacitors:** Place the input capacitor near the PVIN and PGND pins, minimizing the loop formed by these connections. Connect the input capacitor to the PVIN and PGND pins using a wide copper traces.
- **Inductors and Output Capacitors:**
  1) The inductor need to be placed as close as possible to the device keeping the switch node small enough for best EMI performance.
  2) The copper traces from SW pin to inductor and inductor to C_{OUT} must be thick/short enough to minimize the PCB DCR loss.
  3) Guarantee the C_{OUT} ground pins to the PGND pin connections are short and wide, to minimize the ground loop.

LSW

- **Input Capacitors and Output Capacitors:**
  1) Place the input capacitor very close to PVIN and the output capacitor very close to VOUT, in order to minimize PCB Layout (ESL and ESR).
  2) Keep the C_{IN} and C_{OUT} ground sides far away from PGND to minimize ground noise.

Common

- **Feedback Network and Output Lines:** Avoid routing the feedback lines near switching nodes or other high-frequency signals as they are noise-sensitive. The feedback connections should be routed as differential pairs to the output capacitor on a separate layer and connected near the load to achieve better accuracy and load transient response. The feedback wires which connect FB pin and the node between R_{UP2} and R_{DOWN2} should be short as it is high-Z and sensitive.
- **Analog Power/VDRV Power Supply Loop:**
  1) Place AVIN decoupling capacitor as close as possible to the AVIN and AGND pins.
  2) Connect AGND pin to a quiet ground point where no IR drop occurs.
  3) Place VDRV decoupling capacitor as close as possible to the VDRV and PGND pins.
- **SW Connection:** Keep SW area small to prevent excessive EMI, while providing wide copper traces to minimize parasitic resistance and inductance.
- **GND Vias:** Place adequate number of vias on the GND layer around the device and exposed pad for better thermal performance..

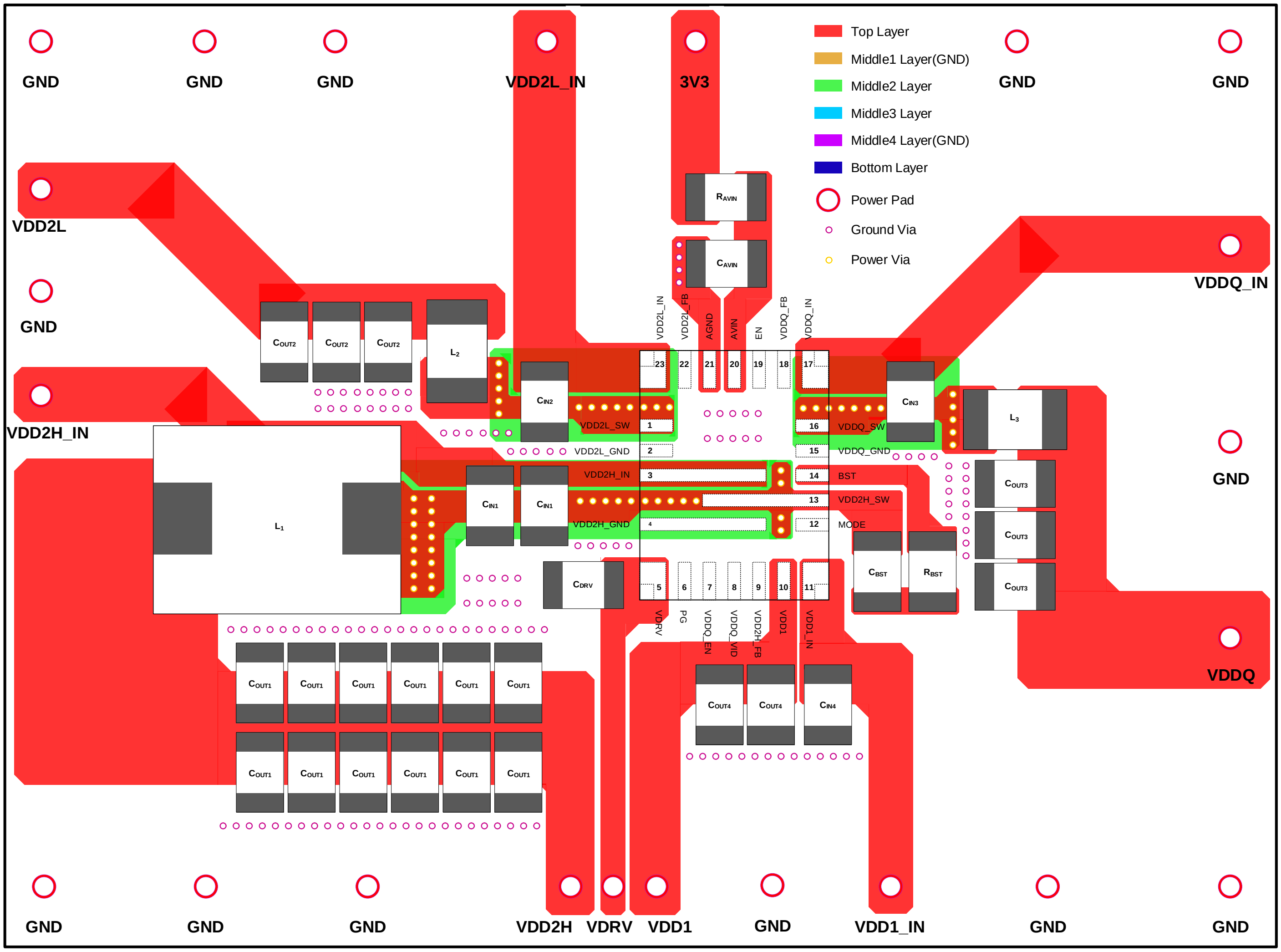
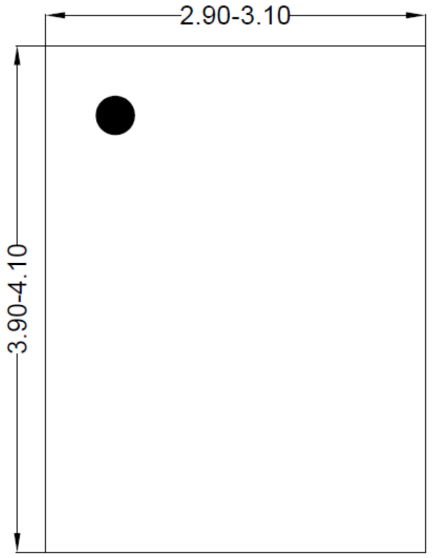
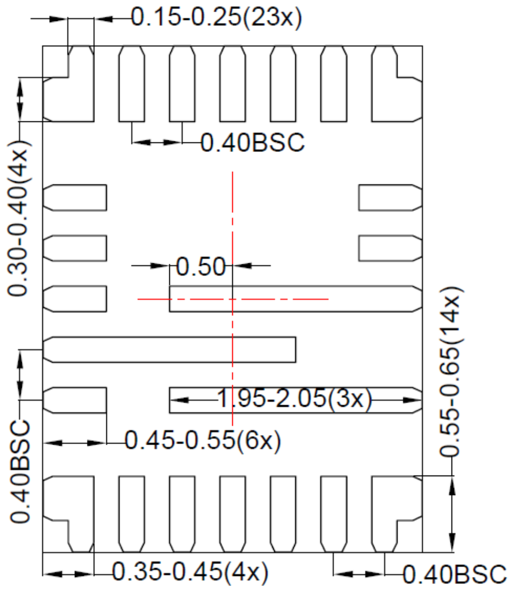


Figure 16. Recommended PCB Layout

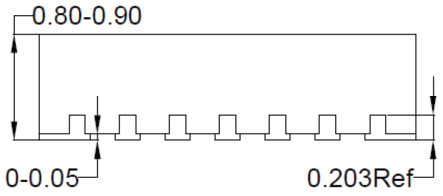
QFN3x4-23 Package Outline Drawing



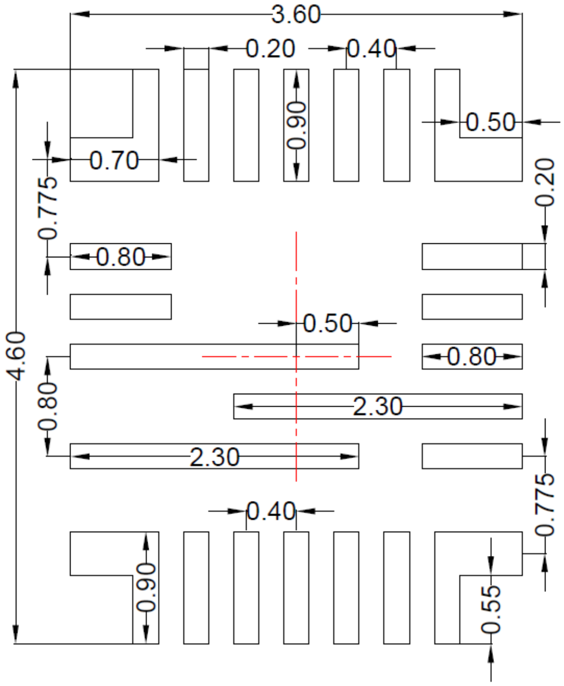
Top view



Bottom view



Front view



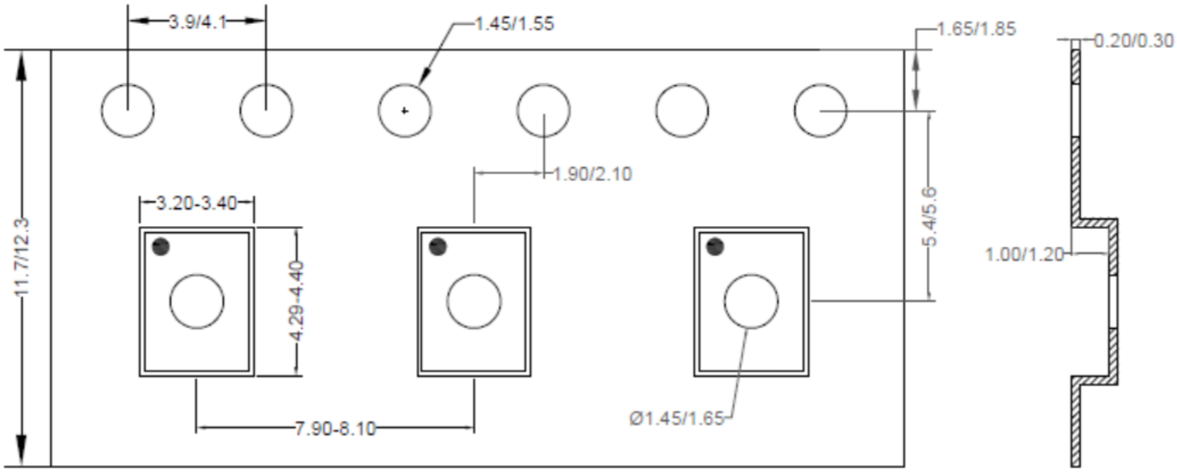
**Recommended PCB layout
(Reference Only)**

Notes:

1. All dimension in millimeter and exclude mold flash & metal burr.

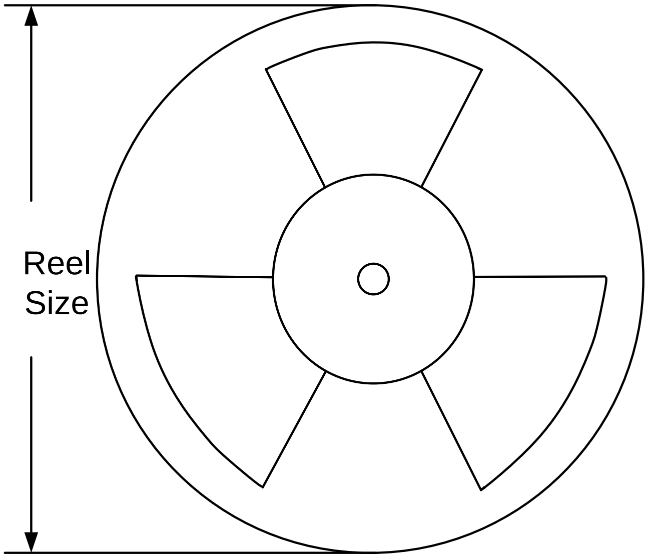
2. The center line refers to the chip body center.

Tape and Reel Information



Direction of feed →

Reel Dimensions



Package Types	Tape Width (mm)	Pocket Pitch (mm)	Reel Size (Inch)	Trailer * Length (mm)	Leader * Length (mm)	Qty per Reel (pcs)
QFN3×4	12	8	13"	400	400	5000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
Mar.31, 2026	Revision 1.0	Initial release.	-
May.07, 2026	Revision 1.0a	Add GPIO pin voltage limit in Note 6.	P11

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. **Applications.** Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale.** Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license.** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com