SY70202M

High Efficiency, High Integration PMIC for SSD Systems

General Description

The SY70202M is an SSD PMIC composed of four synchronous buck regulators and two independent LDOs. Buck 1, LDO 1, and LDO 2 operate in power load switch mode (PLSW), and Buck 4 operates in LDO mode, which can be configured using GPIOx pins.

Other configurable options include output voltage, startup time, system level sequencing, sleep mode, DPSLP mode (deep sleep), and operating mode. Each channel provides a wide voltage range to support DVS (Dynamic Voltage Scaling) through the I²C interface. The buck converters are designed to use very small inductors.

The SY70202M is available in a CSP 2.6mm×2.6mm -36 ball package.

Key Features

- Wide Input Voltage Range
  - V_{IN} = 2.8V to 3.7V
- Channel 1 Synchronous Buck:
  - 4A Maximum Output Current Capability
  - 1.6V to 3.0V Programmable, 25mV Step
  - PLSW Mode or Buck Mode Selection
- Channel 2 Synchronous Buck:
  - 2A Maximum Output Current Capability
  - 0.9V to 2.0V Programmable, 10mV Step
- Channel 3 Synchronous Buck:
  - 4A Maximum Output Current Capability
  - 0.5V to 1.2V Programmable, 10mV Step
- Channel 4 Synchronous Buck:
  - 2A Maximum Output Current Capability
  - 0.9V to 2.0V Programmable, 50mV Step
  - Buck Mode or LDO Mode Selection
- Channel 5 LDO1:
  - 0.4A Maximum Output Current Capability
  - 1.0V to 2.7V Programmable, 50mV Step
  - PLSW Mode or LDO Mode Selection
- Channel 6 LDO2:
  - 0.4A Maximum Output Current Capability
  - 1.0V to 2.7V Programmable, 50mV Step
  - PLSW Mode or LDO Mode Selection
- I²C Interface up to 3.4MHz
- Auto PWM/PFM or Forced PWM Controlled by I²C Interface
- Output Voltage Level of Each Channel Controlled by I²C Interface
- Reliable Protections:
  - Input/Output Overvoltage Protection (OVP)
  - Short-Circuit Protection (SCP)
  - Overtemperature Protection (OTP)
- Compact Package: CSP2.6×2.6-36
- MSLRating: MSL 1

Applications

- Solid State Drives
- Microcontroller Based Designs

Simplified Typical Application

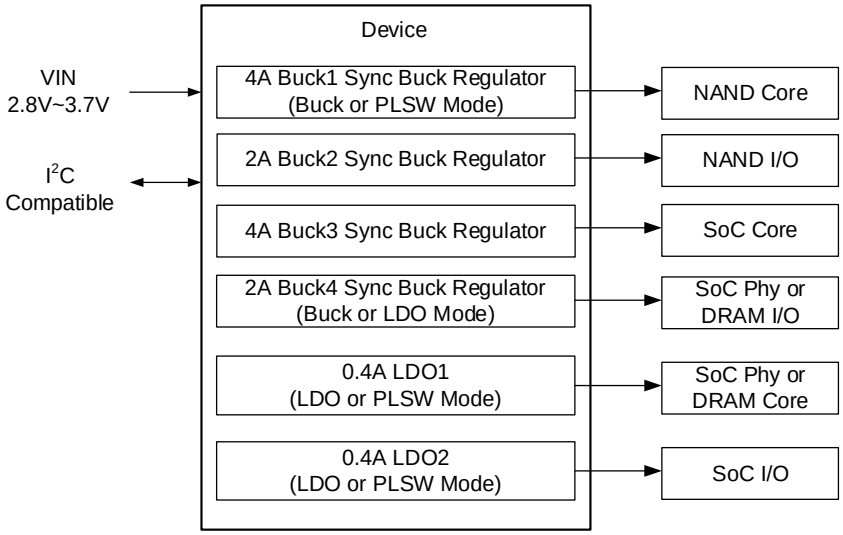
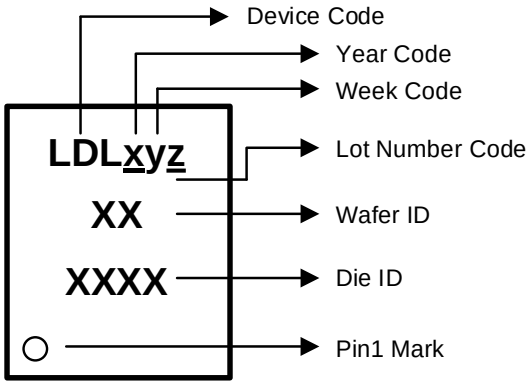


Figure 1. Simplified Application Circuit

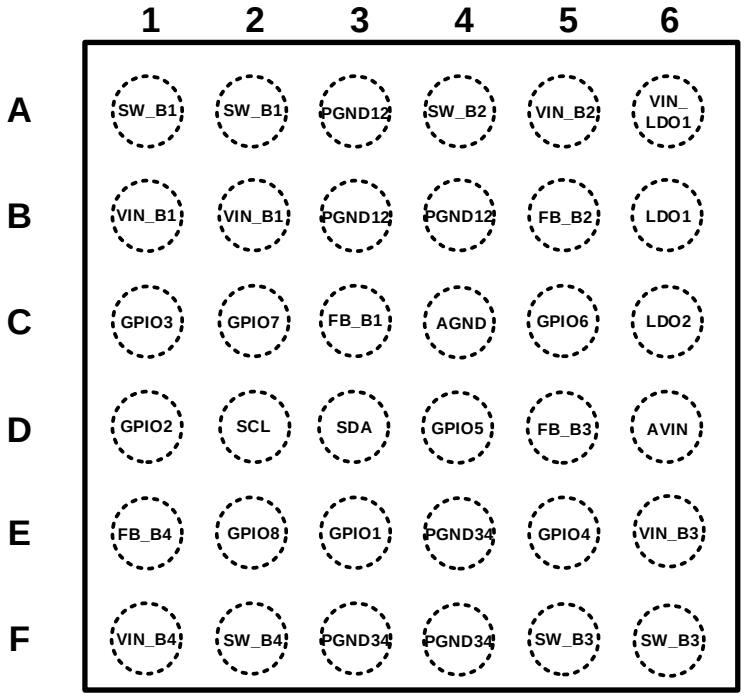
Ordering Information

Ordering Part Number	Package Type
SY70202MVTS	CSP2.6×2.6-36 RoHS-Compliant, Halogen-Free

Marking Diagram



Pinout (top view)



(CSP2.6×2.6-36)

Pin Descriptions

Pin Number	Pin Name	Pin Description
A1, A2	SW_B1	Switch pin for Buck 1 Regulator
A3, B3, B4	PGND12	Dedicated power ground for Buck 1 and Buck 2 regulators
A4	SW_B2	Switch pin for Buck 2 Regulator
A5	VIN_B2	Dedicated V_{IN} power input for Buck 2 Regulator
A6	VIN_LDO1	Dedicated V_{IN} power input for LDO Regulator
B1, B2	VIN_B1	Dedicated V_{IN} power input for Buck 1 Regulator
B5	FB_B2	Feedback for Buck 2 Regulator. Connect to the Buck 2 output capacitor.

B6	LDO1	Output for LDO 1 Regulator (leave unconnected if LDO is not used and disabled)
C1	GPIO3	General purpose input
C2	GPIO7	Configurable general-purpose input/open-drain output
C3	FB_B1	Feedback for Buck 1 Regulator. Connect to the Buck 1 output capacitor.
C4	AGND	Analog Ground. Connects to the other ground pins on the device with a Kelvin connection.
C5	GPIO6	General purpose input
C6	LDO2	Output for LDO 2 Regulator (leave unconnected if LDO is not used and disabled)
D1	GPIO2	General purpose input
D2	SCL	I^2C clock input
D3	SDA	I^2C data input and open-drain output
D4	GPIO5	Configurable general-purpose input/open drain output
D5	FB_B3	Feedback for Buck 3 Regulator. Connect to the Buck 3 output capacitor.
D6	AVIN	Analog input supply. This is also the pin that is monitored for VIN OVP.
E1	FB_B4	Feedback for Buck 4 Regulator. Connect to the Buck 4 output capacitor.
E2	GPIO8	General purpose input
E3	GPIO1	General purpose open-drain output
E4, F3, F4	PGND34	Dedicated power ground for Buck 3 and Buck 4 Regulators
E5	GPIO4	General purpose input
E6	VIN_B3	Dedicated VIN power input for Buck 3 Regulator
F1	VIN_B4	Dedicated VIN power input for Buck 4 Regulator
F2	SW_B4	Switch pin for Buck 4 Regulator
F5, F6	SW_B3	Switch pin for Buck 3 Regulator

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
All Pins to GND	-0.3	6	V
Junction Temperature Range		150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature Range	-55	150	
ESD Susceptibility			
HBM (Human Body Model)	±2000		V
CDM (Charged Device Model)	±500		
Latch-up	±200		mA

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	24	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	4	
P_D Power Dissipation T_A = 25°C	4.17	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Supply Input Voltage, VIN	2.8	3.7	V
Junction Temperature Range	-40	125	°C
Ambient Temperature Range	-40	85	

Block Diagram

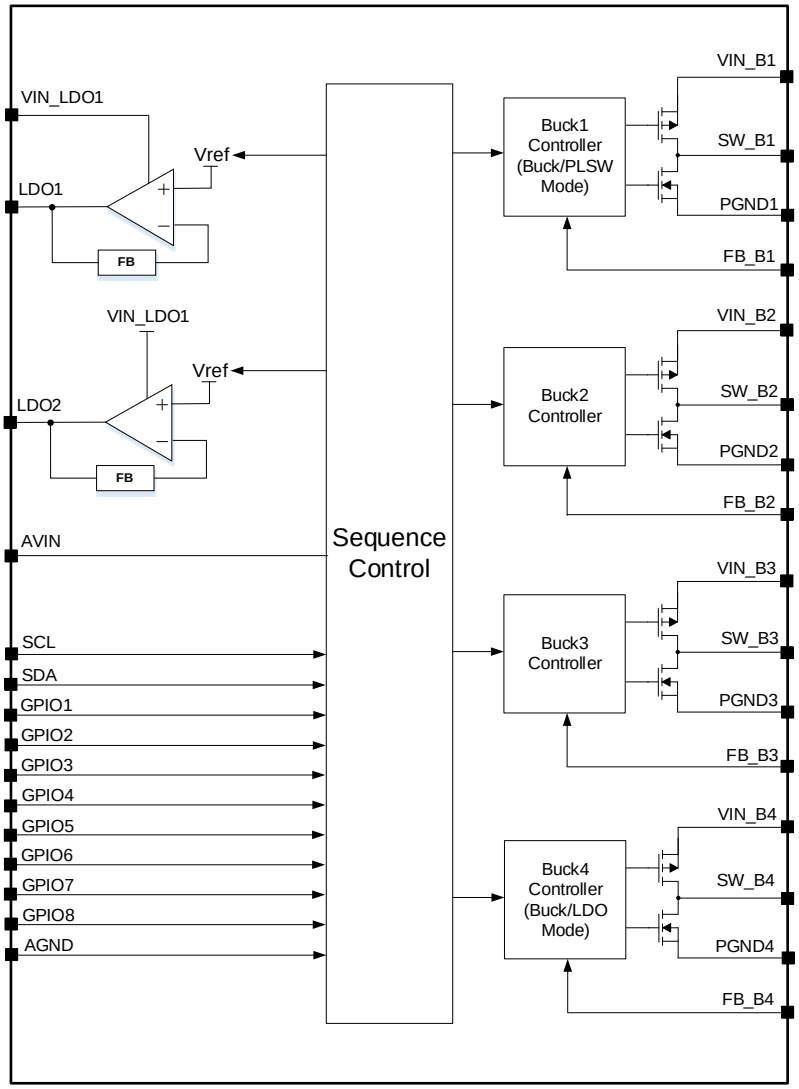


Figure 2. Block Diagram

Electrical Characteristics

(V_{IN} = 3.3V, T_A = 25°C, unless otherwise specified. (Note 4))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Digital I/O	GPIOs Output Low (Open-Drain)	V_{OL}	I_{OL} = 1mA	-	-	0.35	V
	GPIOs Input Low (GPIO2/3/4)	V_{IO_LOW}		-	-	0.35	V
	GPIOs Input Low (GPIO5/6/7/8)	V_{IO_LOW}		-	-	0.55	V
	GPIOs Input High (GPIO2/3/4/5/6/7/8)	V_{IO_HIGH}		1.19	-	-	V
System Control	Supply Input Voltage	V_{IN}		2.8	-	3.7	V
	UVLO Threshold Rising	$V_{UVLO,RISING}$		2.5	2.6	2.7	V
	UVLO Hysteresis	$V_{UVLO,HYS}$	(Note 5)	-	100	-	mV
	Operating Supply Current		All regulators disabled (Note 5)	-	20	-	µA
	Operating Supply Current		All regulators enabled but no load (Note 5)	-	120	-	µA
	VIN OV Shutdown Threshold Rising	$V_{IN\_OVP\_R}$	(Note 5)	-	3.9	-	V
	VIN OV Shutdown Threshold Falling	$V_{IN\_OVP\_F}$	(Note 5)	-	3.6	-	V
	VIN OVP Deglitch Time		(Note 5)		5		µs
	Thermal Shutdown	$T_{OTP,RISING}$	Temperature rising (Note 5)	-	155	-	°C
	Thermal Shutdown Hysteresis	$T_{OTP,HYS}$	(Note 5)	-	15	-	°C
	Startup Delay after Initial AVIN	$T_{SYS,ON}$		-	1	1.5	ms
	OV/UV Retry Time		Channel off time (Note 5)	-	10	-	ms
nIRQ (SYSWARN)	System Warning (SYSWARN) Falling Threshold	$V_{SYSWARN}$	(Note 5)	-	2.9	-	V
	System Warning (SYSWARN) Accuracy	$V_{SYSWARN,ACC}$		-3.5	-	3.5	%
	System Monitor (SYSWARN) Hysteresis	$V_{SYSWARN,HYS}$	(Note 5)	-	50	-	mV
Buck 1	Output Voltage Range	V_{OUT1}	Controllable by I^2C interface, 25mV steps	1.6	-	3.0	V
	Output Voltage Accuracy	ΔV_{OUT1_PWM}	PWM mode operation at T_A = 25°C, V_{OUT} = default	-1	-	1	%
			PWM mode operation at T_J = -40°C to 125°C, V_{OUT} = Default	-2	-	2	%
		ΔV_{OUT1_PFM}	PFM mode operation, I_{OUT} = 1mA at T_J = -40°C to 125°C, V_{OUT} = Default	-2.0	-	2.5	%
	Supply Current, Standby	I_{VIN_B1}	Regulator only, no load (Note 5)	-	22	-	µA
			Regulator only, no load at sleep (GPIO8) = low (Note 5)	-	10	-	µA
			Regulator disable	-	0.1	1	µA

	Switching Frequency	F_{OSC1}	(Note 5)	-	2	-	MHz
	High Side FET Current Limit	I_{LIM1_HS}		5.6	-	-	A
	Maximum Output DC Load Current	I_{OUT1}		4	-	-	A
	Internal Soft-Start Time	T_{SS1}	B1_SST = 0. 10% to 90% of V_{NOM} (Note 5)	-	250	-	µs
			B1_SST = 1. 10% to 90% of V_{NOM} (Note 5)	-	500	-	µs
	Discharge Resistor	R_{DIS1}	(Note 5)	-	4.4	-	Ω
	OVP Threshold	V_{OVP1}		115	120	125	%
	OVP Hysteresis	$V_{OVP1,HYS}$	(Note 5)	-	5	-	%
	OVP Deglitch Time	t_{OVP1}	(Note 5)	-	10	-	µs
	Short-Circuit Protection Threshold	V_{SCP1}	(Note 5)	-	30	-	%
	Short-Circuit Protection Deglitch Time	t_{SCP1}	(Note 5)	-	50	-	µs
Buck 1 in PLSW Mode	Output Voltage Range	V_{OUT}		2.8	3.3	3.7	V
	Load Switch Current Limit	I_{LIM1_HS}	Shut down after deglitch time and stays off for off-time	3.1	4.5	5.8	A
	Load Switch Current Shutdown Deglitch Time	t_{LIM1_HS}	(Note 5)	-	200	-	µs
	Load Switch Current Shutdown Off-Time		(Note 5)	-	10	-	ms
	Internal Soft-Start Time	T_{SS1}	B1_SST = 0. 10% to 90% of V_{NOM}(Note 5)	-	250	-	µs
			B1_SST = 1. 10% to 90% of V_{NOM}(Note 5)	-	500	-	µs
	Short-Circuit Protection Threshold	V_{SCP1}	(Note 5)	-	80	-	$\%V_{IN}$
	Short-Circuit Protection Deglitch Time	t_{SCP1}	(Note 5)	-	50	-	µs
Buck 2	Output Voltage Range	V_{OUT2}	Controllable by I^2C interface in 10mV steps	0.9	-	2.0	V
	Output Voltage Accuracy	ΔV_{OUT2_PWM}	PWM mode operation at T_A = 25°C, V_{OUT} = default	-1	-	1	%
			PWM mode operation at T_J = -40°C to 125°C, V_{OUT} = default	-2	-	2	%
		ΔV_{OUT2_PFM}	PFM mode operation, I_{OUT} = 1mA at T_J = -40°C to 125°C, V_{OUT} = default	-2.0	-	2.5	%
	Supply Current, Standby	I_{VIN_B2}	Regulator only, no load (Note 5)	-	22	-	µA
			Regulator only, no load at sleep (GPIO8) = low (Note 5)	-	10	-	µA
			Regulator disable	-	0.1	1	µA
	Switching Frequency	F_{OSC2}	(Note 5)	-	2	-	MHz
	High Side FET Current Limit	I_{LIM2_HS}		3.6	-	-	A
	Maximum Output DC Load Current	I_{OUT2}		2	-	-	A

	Internal Soft-Start Time	T_{SS2}	B2_SST = 0. 10% to 90% of V_{NOM} (Note 5)	-	250	-	µs
			B2_SST = 1. 10% to 90% of V_{NOM} (Note 5)	-	500	-	µs
	Discharge Resistor	R_{DIS2}	(Note 5)	-	9.4	-	Ω
	OVP Threshold	V_{OVP2}		115	120	125	%
	OVP Hysteresis	$V_{OVP2,HYS}$	(Note 5)	-	5	-	%
	OVP Deglitch Time	t_{OVP2}	(Note 5)	-	10	-	µs
	Short-Circuit Protection Threshold	V_{SCP2}	(Note 5)	-	30	-	%
	Short-Circuit Protection Deglitch Time	t_{SCP2}	(Note 5)	-	50	-	µs
Buck 3	Output Voltage Range	V_{OUT3}	Controllable by I^2C interface in 10mV steps	0.5	-	1.2	V
	Output Voltage Accuracy	ΔV_{OUT3_PWM}	PWM mode operation at T_A = 25°C, V_{OUT} = default	-1	-	1	%
			PWM mode operation at T_J = -40°C to 125°C, V_{OUT} = default	-2	-	2	%
		ΔV_{OUT3_PFM}	PFM mode operation, I_{OUT} = 1mA at T_J = -40°C to 125°C, V_{OUT} = default	-2.0	-	2.5	%
	Supply Current, Standby	I_{VIN_B3}	Regulator Only, No Load (Note 5)	-	22	-	µA
			Regulator only, no load at sleep (GPIO8) = low (Note 5)	-	10	-	µA
			Regulator disable	-	0.1	1	µA
	Switching Frequency	F_{OSC3}	(Note 5)	-	2	-	MHz
	High Side FET Current Limit	I_{LIM3_HS}		5.6	-	-	A
	Maximum Output DC Load Current	I_{OUT3}		4	-	-	A
	Internal Soft-Start Time	T_{SS3}	B3_SST = 0. 10% to 90% of V_{NOM} (Note 5)	-	250	-	µs
			B3_SST = 1. 10% to 90% of V_{NOM} (Note 5)	-	500	-	µs
	Discharge Resistor	R_{DIS3}	(Note 5)		9.4	-	Ω
	OVP Threshold	V_{OVP3}		115	120	125	%
	OVP Hysteresis	$V_{OVP3,HYS}$	(Note 5)	-	5	-	%
	OVP Deglitch Time	t_{OVP3}	(Note 5)	-	10	-	µs
	Short-Circuit Protection Threshold	V_{SCP3}	(Note 5)	-	30	-	%
	Short-Circuit Protection Deglitch Time	t_{SCP3}	(Note 5)	-	50	-	µs
Buck 4	Output Voltage Range	V_{OUT4}	Controllable by I^2C interface in 50mV steps	0.9	-	2.0	V
	Output Voltage Accuracy	ΔV_{OUT4_PWM}	PWM mode operation at T_A = 25°C, V_{OUT} = default	-1	-	1	%
			PWM mode operation at T_J = -40°C to 125°C, V_{OUT} = default	-2	-	2	%

		ΔV_{OUT4_PFM}	PFM mode operation, I_{OUT} = 1mA at T_J = -40°C to 125°C, V_{OUT} = default	-2.0	-	2.5	%
	Supply Current, Standby	I_{VIN_B4}	Regulator only, no load (Note 5)	-	22	-	μA
			Regulator only, no load at sleep (GPIO8) = low (Note 5)	-	10	-	μA
			Regulator disable	-	0.1	1	μA
	Switching Frequency	F_{OSC4}	(Note 5)	-	2	-	MHz
	High Side FET Current Limit	I_{LIM4_HS}		3.6	-	-	A
	Maximum Output DC Load Current	I_{OUT4}		2	-	-	A
	Internal Soft-Start Time	T_{SS4}	B4_SST = 0. 10% to 90% of V_{NOM} (Note 5)	-	250	-	μs
			B4_SST = 1. 10% to 90% of V_{NOM} (Note 5)	-	500	-	μs
	Discharge Resistor	R_{DIS4}	(Note 5)	-	9.4	-	Ω
	OVP Threshold	V_{OVP4}		115	120	125	%
	OVP Hysteresis	$V_{OVP4,HYS}$	(Note 5)	-	5	-	%
	OVP Deglitch Time	t_{OVP4}	(Note 5)	-	10	-	μs
	Short-Circuit Protection Threshold	V_{SCP4}	(Note 5)	-	30	-	%
	Short-Circuit Protection Deglitch Time	t_{SCP4}	(Note 5)	-	50	-	μs
Buck 4 in LDO Mode	Output Voltage Range	$V_{OUT\_B4\_LDO}$	Controllable by I^2C interface in 50mV steps	0.9	-	2.0	V
	Output Current	$I_{OUT\_B4\_LDO}$	V_{IN_B4} = 2.8V to 3.7V	0.4	-	-	A
	Output Voltage Accuracy	$\Delta V_{OUT\_B4\_LDO}$	T_A = 25°C, V_{IN_B4}-$V_{OUT\_B4\_LDO}$ > 0.4V	-1	-	1	%
			T_J = -40°C to 125°C V_{IN_B4} - $V_{OUT\_B4\_LDO}$ > 0.4V	-2	-	2	%
	Supply Current	I_{VIN_B4}	Regulator enable, no load (Note 5)	-	10	-	μA
			Regulator disable	-	0	1	μA
	Internal Soft-Start Time	$T_{SS\_B4\_LDO}$	B4_SST = 0. 10% to 90% of V_{NOM} (Note 5)	-	250	-	μs
			B4_SST = 1. 10% to 90% of V_{NOM} (Note 5)	-	500	-	μs
	OVP Threshold	$V_{OVP\_B4\_LDO}$		115	120	125	%
	OVP Hysteresis	V_{OVP_HYS}	(Note 5)	-	5	-	%
	OVP Deglitch Time	$t_{OVP\_B4\_LDO}$	(Note 5)	-	10	-	μs
	Dropout Voltage	$V_{DV\_B4\_LDO}$	I_{LDO1} = 150mA, V_{IN_B4} > 2.8V	-	-	200	mV
			I_{LDO1} = 300mA, V_{IN_B4} > 2.8V	-	-	400	mV
	Discharge Resistor	$R_{DIS\_B4\_LDO}$	(Note 5)	-	9.4	-	Ω
	Current Limit	$I_{LIM\_B4\_LDO}$		400	500	600	mA
	Current Shutdown Deglitch Time	$t_{LIM\_B4\_LDO}$	(Note 5)	-	200	-	μs
	Short-Circuit Protection Threshold	$V_{SCP\_B4\_LDO}$	(Note 5)	-	60	-	%
	Short-Circuit Protection	$t_{SCP\_B4\_LDO}$	(Note 5)	-	50	-	μs

	Deglitch Time						
LDO 1	LDO1 Input Voltage Range	V_{IN_LDO1}	LDO Mode	2.8	-	3.7	V
	LDO1 Output Voltage Range	V_{OUT_LDO1}	Controllable by I^2C interface in 50mV steps	1.0	-	2.7	V
	Output Current	I_{OUT_LDO1}	V_{IN_LDO1} = 2.8V to 3.7V	0.4	-	-	A
	Output Voltage Accuracy	ΔV_{OUT_LDO1}	T_A = 25°C, V_{OUT} = default V_{IN_LDO1} - V_{OUT_LDO1} > 0.4V	-1	-	1	%
			T_J = -40°C to 125°C, V_{OUT} = default V_{IN_LDO1}-V_{OUT_LDO1} > 0.4V	-2	-	2	%
	Supply Current	I_{VIN_LDO1}	Regulator Enable, No Load (Note 5)	-	10	-	µA
			Regulator Disable	-	0	1	µA
	Internal Soft-Start Time	T_{SS_LDO1}	LDO1_SST = 0. 10% to 90% of V_{NOM} (Note 5)	-	200	-	µs
			LDO1_SST = 1. 10% to 90% of V_{NOM} (Note 5)	-	360	-	µs
	OVP Threshold	V_{OVP_LDO1}		115	120	125	%
	OVP Hysteresis	$V_{OVP\_LDO1,HYS}$	(Note 5)	-	5	-	%
	OVP Deglitch Time	t_{OVP_LDO1}	(Note 5)	-	10	-	µs
	Dropout Voltage	V_{DV_LDO1}	I_{LDO1} = 400mA, V_{IN_LDO1} > 2.8V	-	-	400	mV
	Discharge Resistor	R_{DIS_LDO1}	(Note 5)	-	20	-	Ω
	Current Limit	I_{LIM_LDO1}		400	500	600-	mA
	Current Shutdown Deglitch Time	t_{LIM_LDO1}	(Note 5)	-	200	-	µs
	Short Circuit Protection Threshold	V_{SCP_LDO1}	(Note 5)	-	60	-	%
	Short Circuit Protection Deglitch Time	t_{SCP_LDO1}	(Note 5)	-	50	-	µs
LDO 1 in PLSW Mode	LDO1 Input Voltage Range	V_{IN_LDO1}	PLSW mode	2.8	-	3.7	V
	Supply Current	I_{VIN_LDO1}	PLSW mode (Note 5)	-	12	-	µA
			Load switch disabled	-	0	1	µA
	Internal Soft-Start Time	T_{SS_LDO1}	10% to 90% of V_{NOM} (Note 5)	-	200	-	µs
	Load Switch Current Limit	I_{LIM_HS}	PLSW mode	400	500	600	mA
	Load Switch Current Shutdown Deglitch Time	t_{LIM_HS}	(Note 5)	-	200	-	µs
	Load Switch Current Shutdown Off-Time		(Note 5)	-	10	-	ms
	Short-Circuit Protection Threshold	$V_{SCP,LDO1}$	(Note 5)	-	60	-	%
	Short-Circuit Protection Deglitch Time	$t_{SCP,LDO1}$	(Note 5)	-	50	-	µs
LDO 2	LDO 2 Input Voltage Range	V_{IN_LDO1}	LDO mode	2.8	-	3.7	V
	LDO 2 Output Voltage Range	V_{OUT_LDO2}	Controllable by I^2C interface in 50mV steps	1.0	-	2.7	V
	Output Current	I_{OUT_LDO2}	V_{IN_LDO1} = 2.8V to 3.7V	0.4	-	-	A
	Output Voltage Accuracy	ΔV_{OUT_LDO2}	T_A = 25°C, V_{OUT} = default V_{IN_LDO1}-V_{OUT_LDO2} > 0.4V	-1	-	1	%
			T_J = -40°C to 125°C, V_{OUT} = default V_{IN_LDO1} - V_{OUT_LDO2} > 0.4V	-2	-	2	%

	Supply Current	I_{VIN_LDO2}	Regulator enable, no load (Note 5)	-	10	-	μA
			Regulator disable	-	0	1	μA
	Internal Soft-Start Time	T_{SS_LDO2}	LDO2_SST = 0.10% to 90% of V_{NOM} (Note 5)	-	200	-	μs
			LDO2_SST = 1.10% to 90% of V_{NOM} (Note 5)	-	360	-	μs
	OVP Threshold	V_{OVP_LDO2}		115	120	125	%
	OVP Hysteresis	$V_{OVP\_LDO2,HYS}$	(Note 5)	-	5	-	%
	OVP Deglitch Time	t_{OVP_LDO2}	(Note 5)	-	10	-	μs
	Dropout Voltage	V_{DV_LDO2}	I_{LDO2} = 400mA, V_{IN_LDO1} > 2.8V	-	-	400	mV
	Discharge Resistor	R_{DIS_LDO2}	(Note 5)	-	20	-	Ω
	Current Limit	I_{LIM_LDO2}		400	500	600	mA
	Current Shutdown Deglitch Time	t_{LIM_LDO2}	(Note 5)	-	200	-	μs
	Short-Circuit Protection Threshold	V_{SCP_LDO2}	(Note 5)	-	60	-	%
	Short-Circuit Protection Deglitch Time	t_{SCP_LDO2}	(Note 5)	-	50	-	μs
LDO 2 in PLSW Mode	LDO 2 Input Voltage Range	V_{IN_LDO1}	PLSW mode	2.8	-	3.7	V
	Supply Current	I_{VIN_LDO1}	PLSW mode (Note 5)	-	12	-	μA
			Load switch disabled	-	0	1	μA
	Internal Soft-Start Time	T_{SS_LDO2}	10% to 90% of V_{NOM} (Note 5)	-	200	-	μs
	Load Switch Current Limit	I_{LIM_HS}		400	500	600	mA
	Load Switch Current Shutdown Deglitch Time	t_{LIM_HS}	(Note 5)	-	200	-	μs
	Load Switch Current Shutdown Off-Time		(Note 5)	-	10	-	ms
	Short-Circuit Protection Threshold	$V_{SCP,LDO2}$	(Note 5)	-	60	-	%
	Short Circuit Protection Deglitch Time	$t_{SCP,LDO2}$	(Note 5)	-	50	-	μs

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on Silergy EVB.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

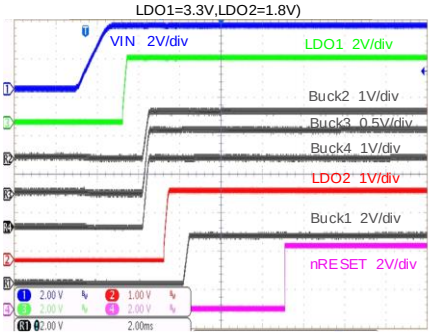
Note 5: Guaranteed by design or statistical correlation and not production tested.

Typical Performance Characteristics

(T_A = 25°C)

Power On Sequence

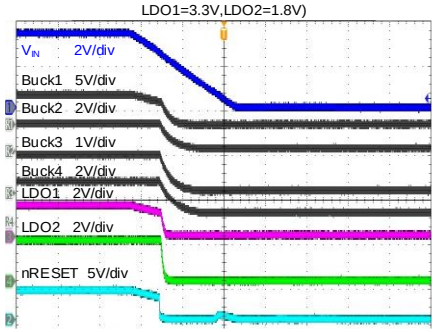
(V_{IN}=3.3V,V_{OUT1}=2.5V,V_{OUT2}=1.2V,V_{OUT3}=0.82V,V_{OUT4}=1.8V, LDO1=3.3V,LDO2=1.8V)



Time (2ms/div)

Power Off Sequence

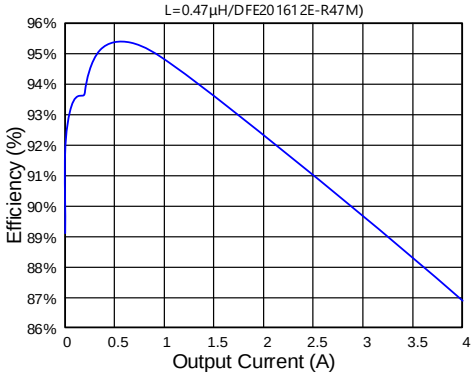
(V_{IN}=3.3V,V_{OUT1}=2.5V,V_{OUT2}=1.2V,V_{OUT3}=0.82V,V_{OUT4}=1.8V, LDO1=3.3V,LDO2=1.8V)



Time (400µs/div)

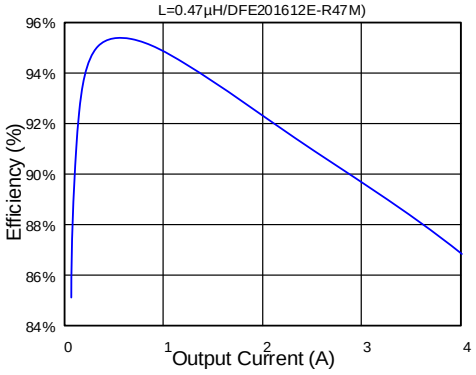
Efficiency vs. Load Current

(V_{IN}=3.3V, Buck1=2.5V, C_{OUT}=22µF, I_{OUT}=0~4A, PFM, L=0.47µH/DFE201612E-R47M)



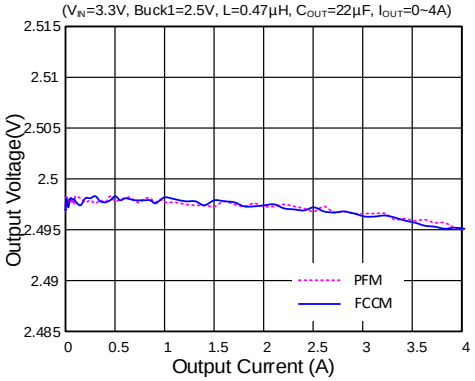
Efficiency vs. Load Current

(V_{IN}=3.3V, Buck1=2.5V, C_{OUT}=22µF, I_{OUT}=0~4A, FCCM, L=0.47µH/DFE201612E-R47M)



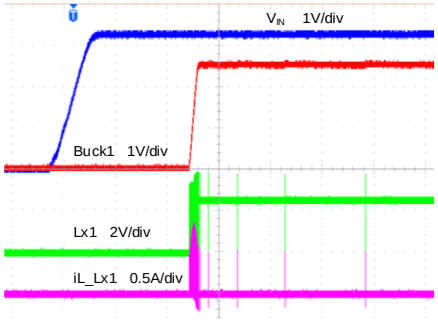
Output Voltage vs. Load Current

(V_{IN}=3.3V, Buck1=2.5V, L=0.47µH, C_{OUT}=22µF, I_{OUT}=0~4A)



Buck1 Power On

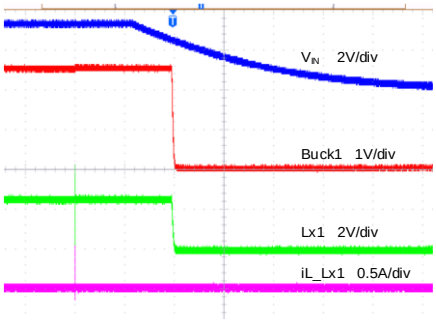
(V_{IN}=3.3V, V_{OUT}=2.5V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A)



Time (1ms/div)

Buck1 Power Off

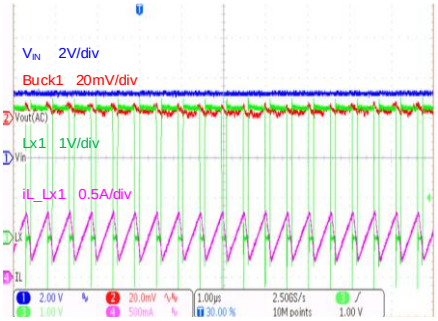
(V_{IN}=3.3V, V_{OUT}=2.5V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A)



Time (1ms/div)

Buck1 Waveforms，FCCM Mode

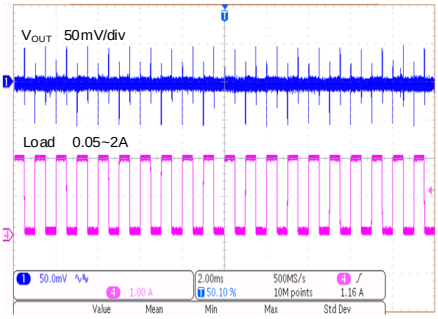
(V_{IN}=3.3V, V_{OUT}=2.5V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0.5A)



Time (1μs/div)

Buck1 Load Transient

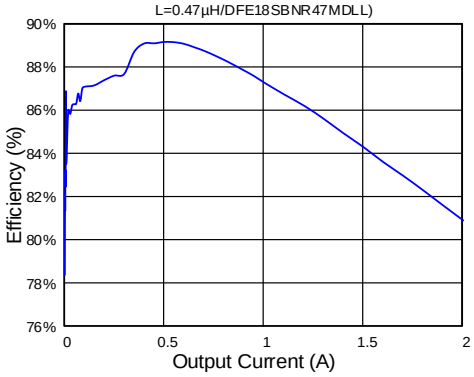
(V_{IN}=3.3V, V_{OUT}=2.5V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0.05~2A(9.75μs), FCCM)



Time (2ms/div)

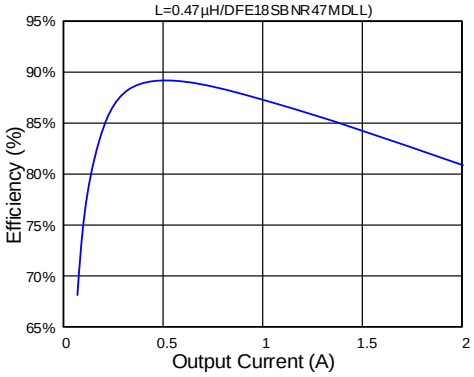
Efficiency vs. Load Current

(V_{IN}=3.3V, Buck2=1.2V, C_{OUT}=22μF, I_{OUT}=0~2A, PFM, L=0.47μH/DFE18SBNR47MDLL)



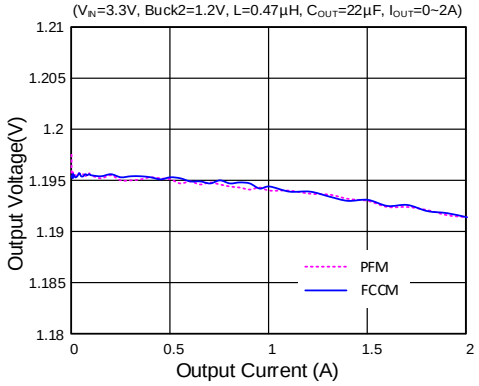
Efficiency vs. Load Current

(V_{IN}=3.3V, Buck2=1.2V, C_{OUT}=22μF, I_{OUT}=0~2A, FCCM, L=0.47μH/DFE18SBNR47MDLL)



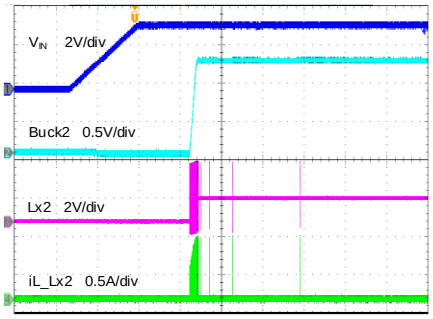
Output Voltage vs. Load Current

(V_{IN}=3.3V, Buck2=1.2V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0~2A)



Buck2 Power On

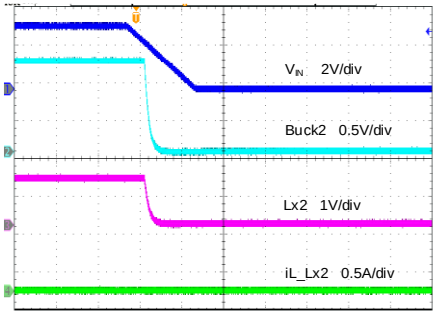
(V_{IN}=3.3V, V_{OUT}=1.2V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A)



Time (2ms/div)

Buck2 Power Off

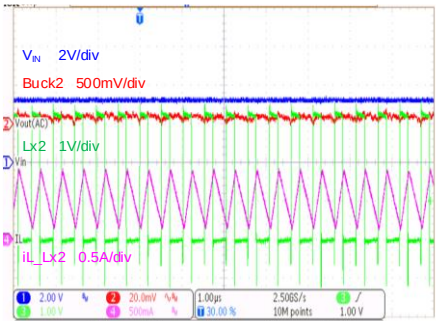
(V_{IN}=3.3V, V_{OUT}=1.2V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A)



Time (2ms/div)

Buck2 Waveforms，FCCM Mode

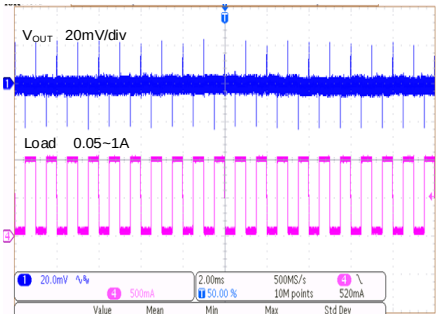
(V_{IN}=3.3V, V_{OUT}=1.2V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0.5A)



Time (1μs/div)

Buck2 Load Transient

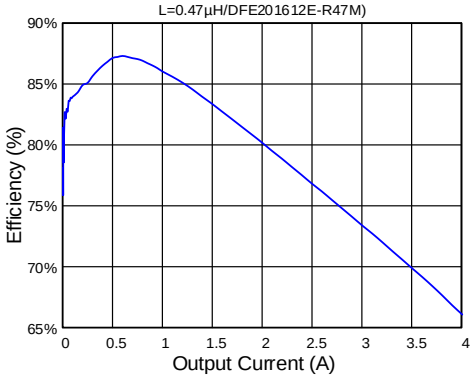
(V_{IN}=3.3V, V_{OUT}=1.2V, L=0.47μH, C_{OUT}=22μF,
I_{OUT}=0.05~1A(4.75μs), FCCM)



Time (2ms/div)

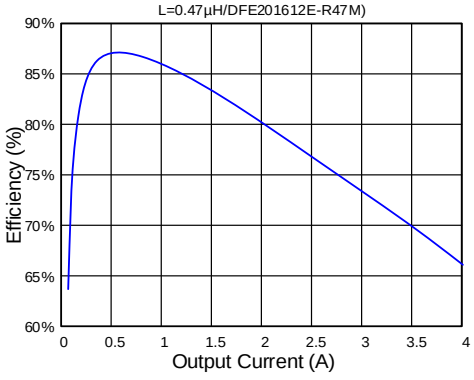
Efficiency vs. Load Current

(V_{IN}=3.3V, Buck3=0.8V, C_{OUT}=22μF, I_{OUT}=0~4A, PFM, L=0.47μH/DFE201612E-R47M)



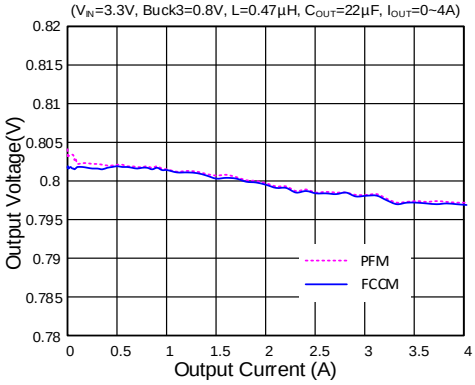
Efficiency vs. Load Current

(V_{IN}=3.3V, Buck3=0.8V, C_{OUT}=22μF, I_{OUT}=0~4A, FCCM, L=0.47μH/DFE201612E-R47M)



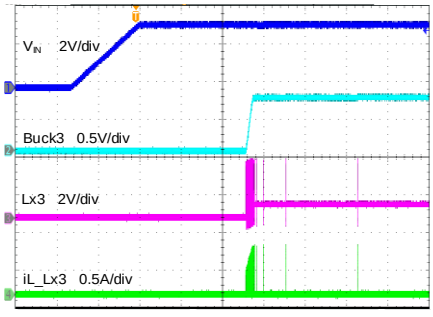
Output Voltage vs. Load Current

(V_{IN}=3.3V, Buck3=0.8V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0~4A)



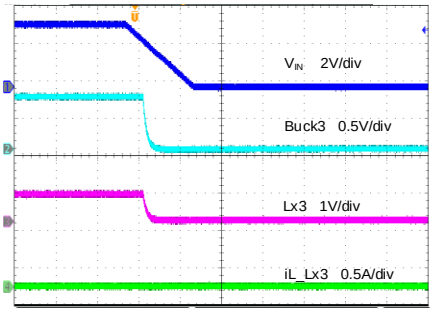
Buck3 Power On

(V_{IN}=3.3V, V_{OUT}=0.8V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A)



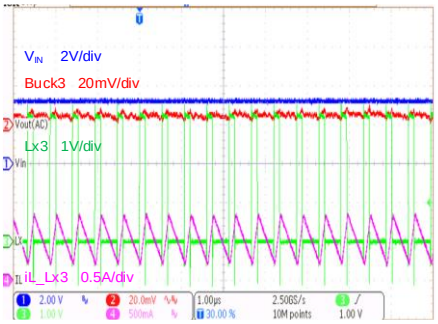
Buck3 Power Off

(V_{IN}=3.3V, V_{OUT}=0.8V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A)



Buck3 Waveforms，FCCM Mode

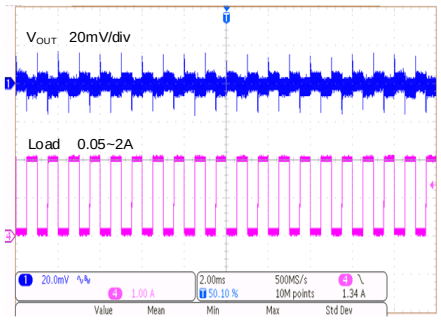
(V_{IN}=3.3V, V_{OUT}=0.8V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0.5A)



Time (1μs/div)

Buck3 Load Transient

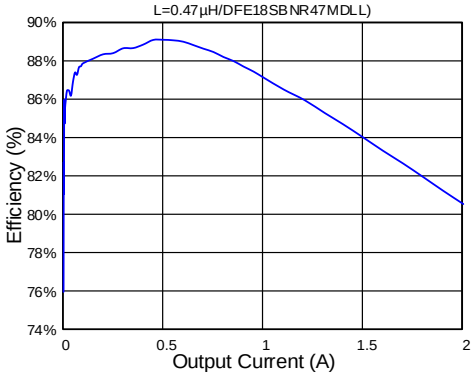
(V_{IN}=3.3V, V_{OUT}=0.8V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0.05~2A(9.75μs), FCCM)



Time (2ms/div)

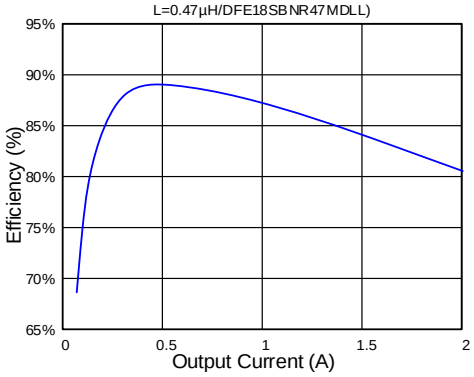
Efficiency vs. Load Current

(V_{IN}=3.3V, Buck4=1.2V, C_{OUT}=22μF, I_{OUT}=0~2A, PFM, L=0.47μH/DFE18SBNR47MDLL)



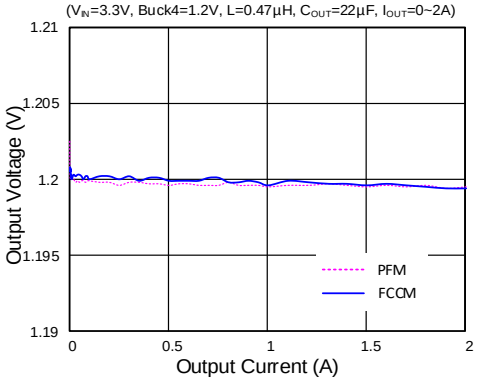
Efficiency vs. Load Current

(V_{IN}=3.3V, Buck4=1.2V, C_{OUT}=22μF, I_{OUT}=0~2A, FCCM, L=0.47μH/DFE18SBNR47MDLL)



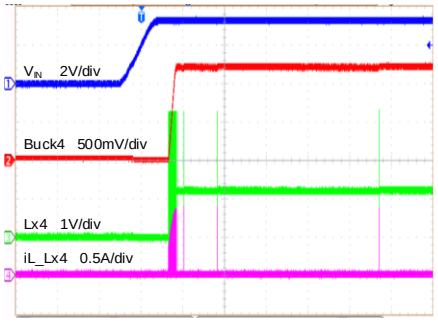
Output Voltage vs. Load Current

(V_{IN}=3.3V, Buck4=1.2V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0~2A)



Buck4 Power On

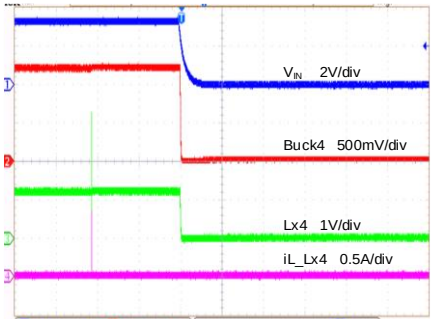
(V_{IN}=3.3V, V_{OUT}=1.2V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A)



Time (2ms/div)

Buck4 Power Off

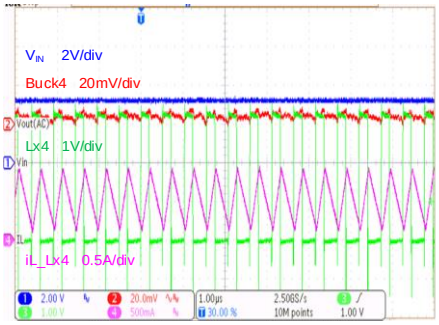
(V_{IN}=3.3V, V_{OUT}=1.2V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0A)



Time (10ms/div)

Buck4 Waveforms，FCCM Mode

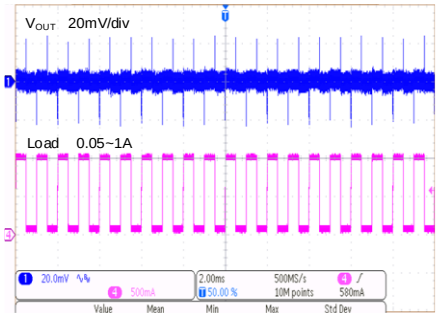
(V_{IN}=3.3V, V_{OUT}=1.2V, L=0.47μH, C_{OUT}=22μF, I_{OUT}=0.5A)



Time (1μs/div)

Buck4 Load Transient

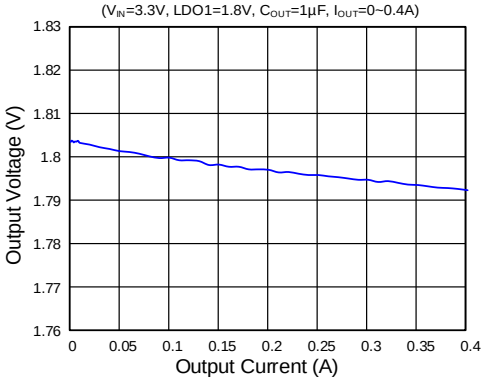
(V_{IN}=3.3V, V_{OUT}=1.2V, L=0.47μH, C_{OUT}=22μF,
I_{OUT}=0.05~1A(4.75μs), FCCM)



Time (2ms/div)

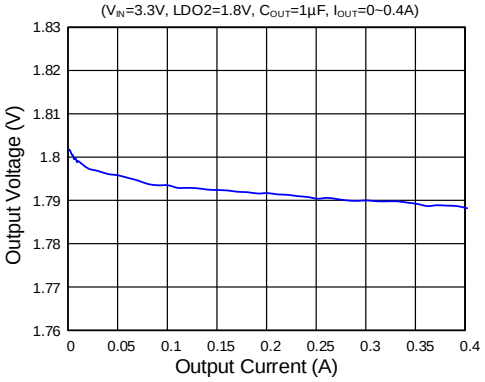
Output Voltage vs. Load Current

(V_{IN}=3.3V, LDO1=1.8V, C_{OUT}=1μF, I_{OUT}=0~0.4A)



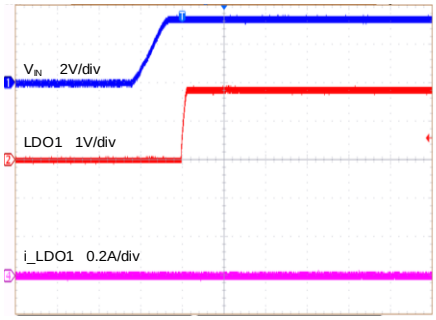
Output Voltage vs. Load Current

(V_{IN}=3.3V, LDO2=1.8V, C_{OUT}=1μF, I_{OUT}=0~0.4A)



LDO1 Power On

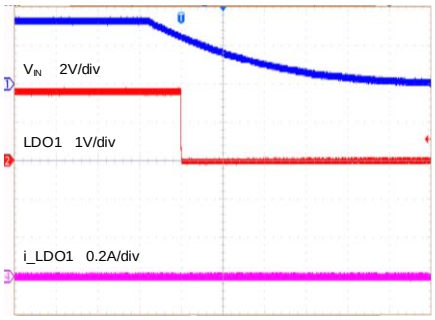
(V_{IN}=3.3V, V_{OUT}=1.8V, C_{OUT}=1μF, I_{OUT}=0A)



Time (2ms/div)

LDO1 Power Off

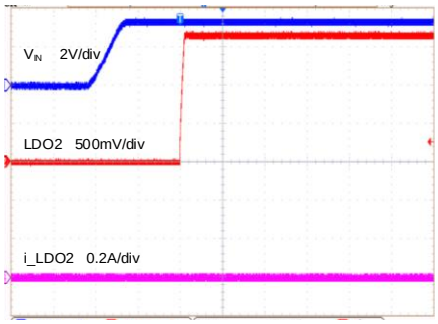
(V_{IN}=3.3V, V_{OUT}=1.8V, C_{OUT}=1μF, I_{OUT}=0A)



Time (2ms/div)

LDO2 Power On

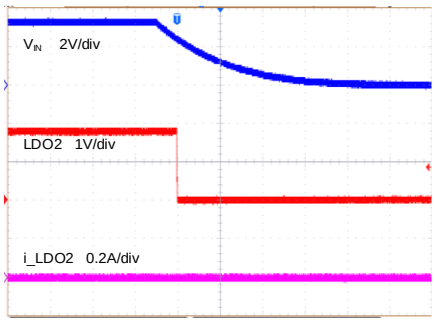
(V_{IN}=3.3V, V_{OUT}=1.8V, C_{OUT}=1μF, I_{OUT}=0A)



Time (2ms/div)

LDO2 Power Off

(V_{IN}=3.3V, V_{OUT}=1.8V, C_{OUT}=1μF, I_{OUT}=0A)



Time (2ms/div)

Typical Application

GPIO2 = Floating, GPIO3 = High, GPIO4 = High

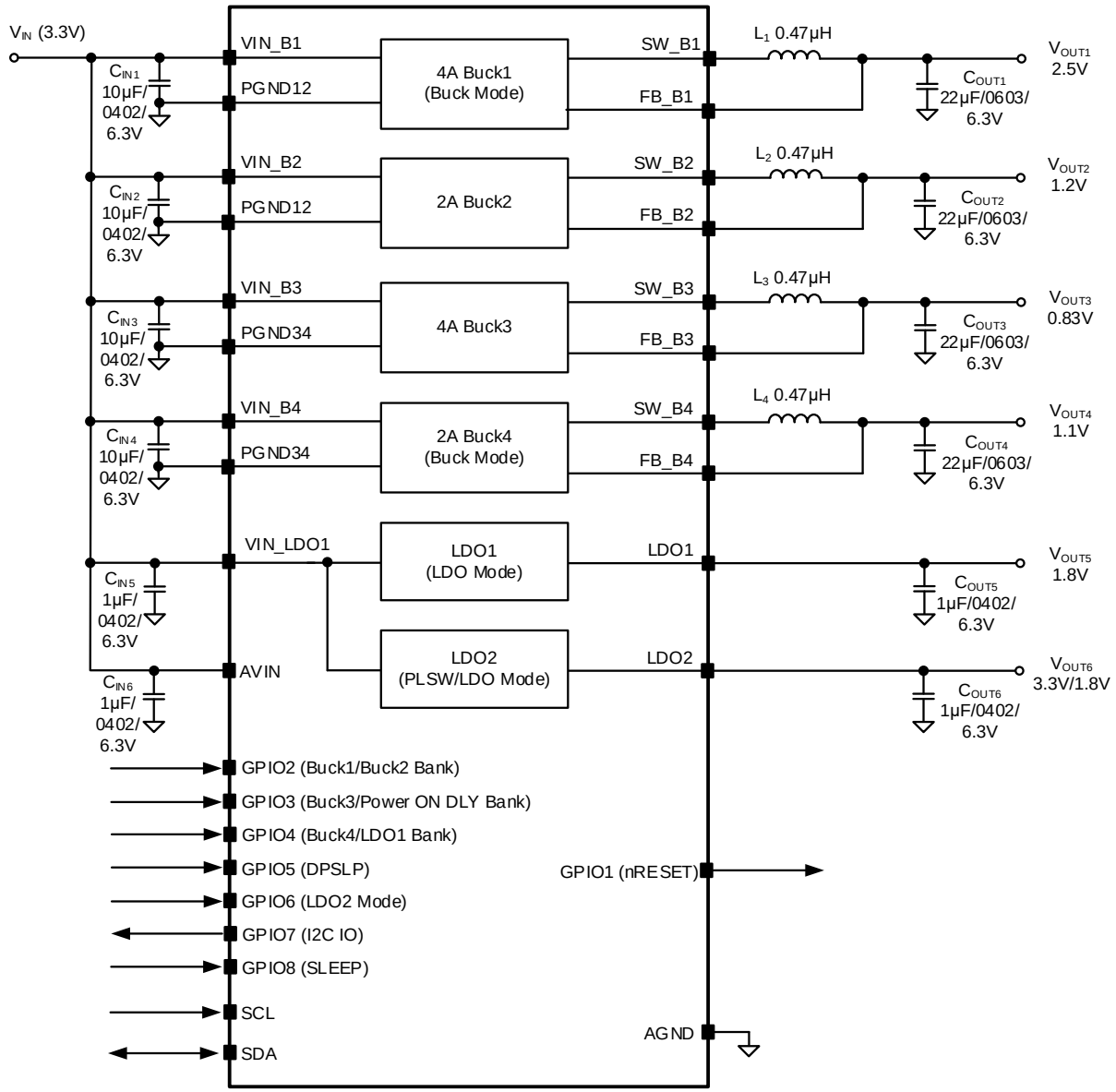


Figure 3. Application Circuit for Application A

Note: Buck 1 I_{OUT} > 2.5A, C_{OUT} = 22µF/0603/6.3V x 2

GPIO2 = Floating, GPIO3 = Floating, GPIO4 = Floating

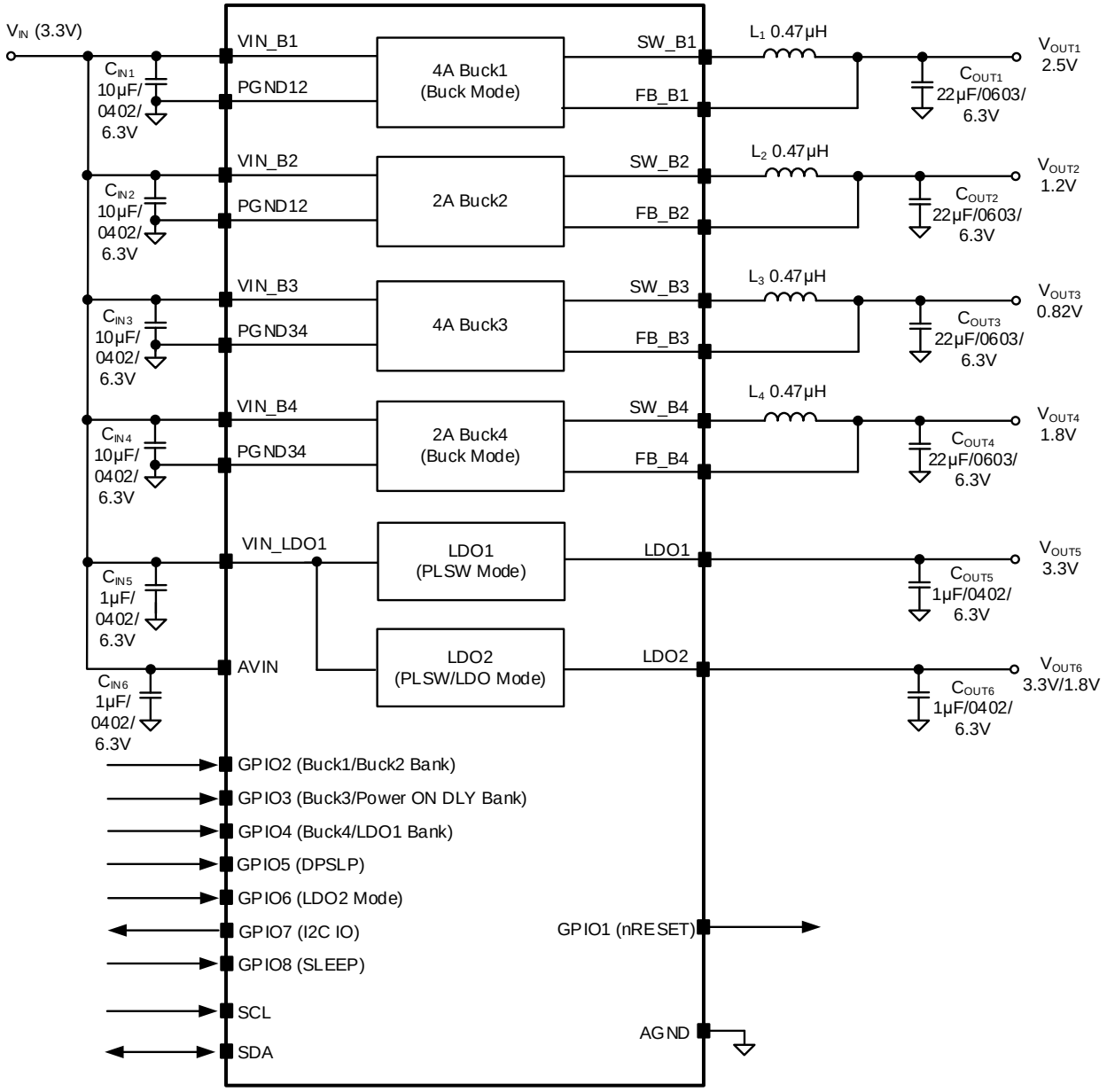


Figure 4. Application Circuit for Application B

Note: Buck 1 I_{OUT} > 2.5A, C_{OUT} = 22µF/0603/6.3V x 2

GPIO2 = Floating, GPIO3 = Low, GPIO4 = Low

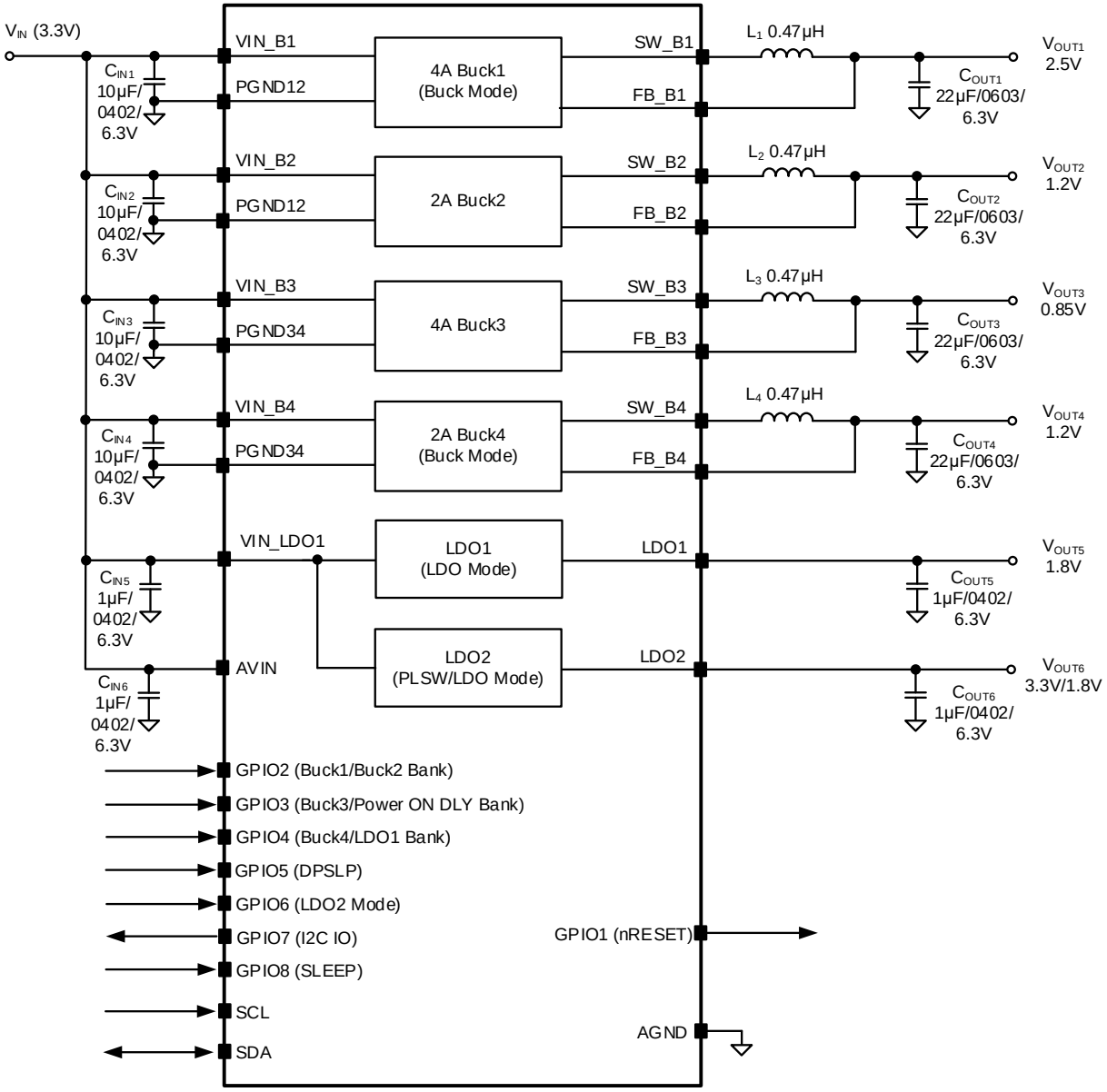


Figure 5. Application Circuit for Application C

Note: Buck 1 I_{OUT} > 2.5A, C_{OUT} = 22uF/0603/6.3V x 2

GPIO2 = High, GPIO3 = Floating, GPIO4 = Floating

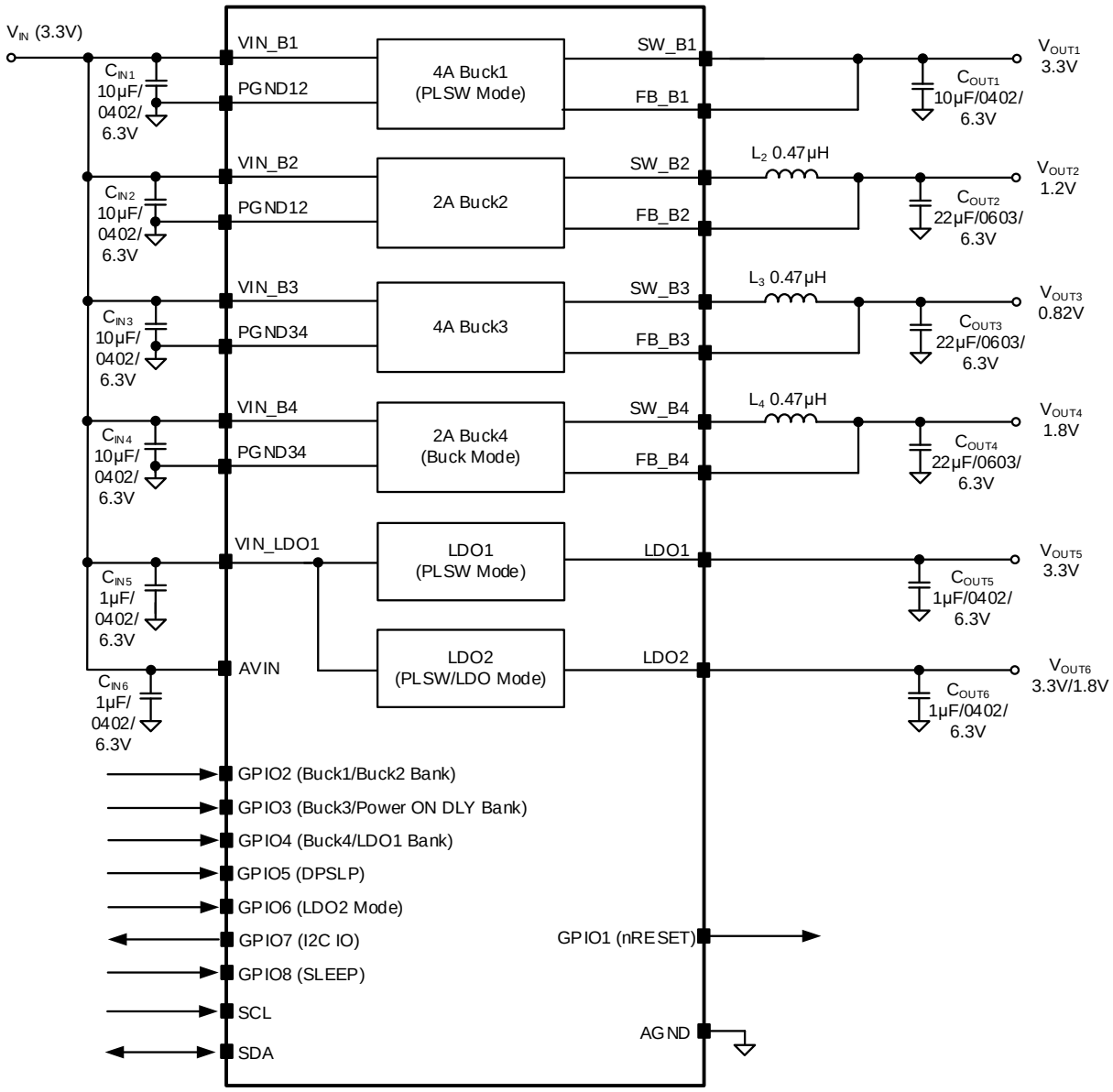


Figure 6. Application Circuit for Application D

Note: Buck 1 I_{OUT} > 2.5A, C_{OUT} = 22uF/0603/6.3V x 2

Power On/Off Sequence

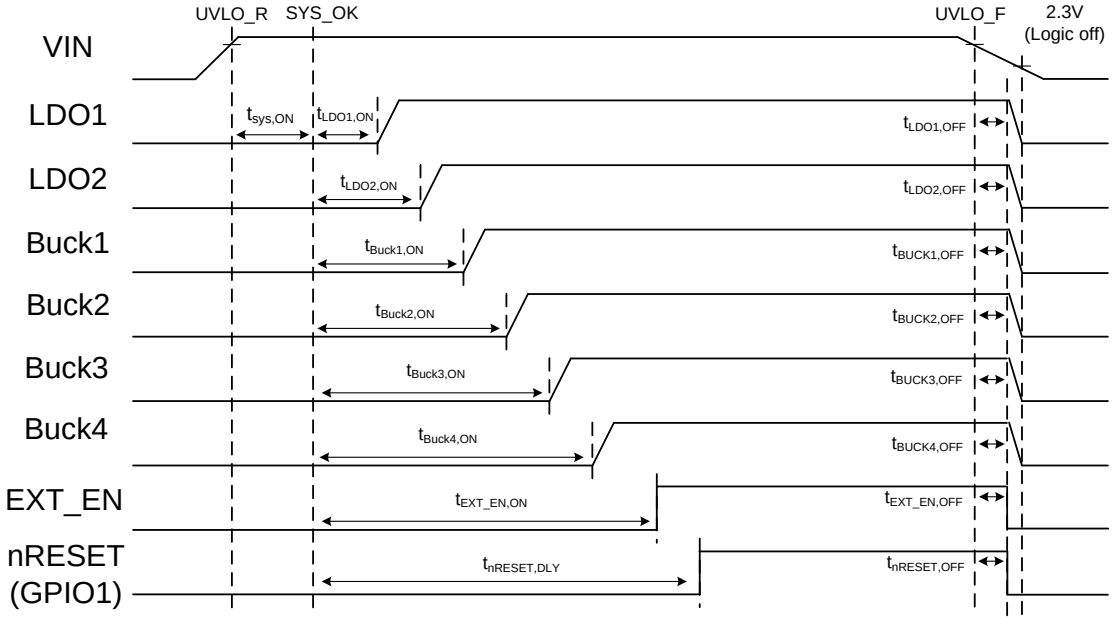


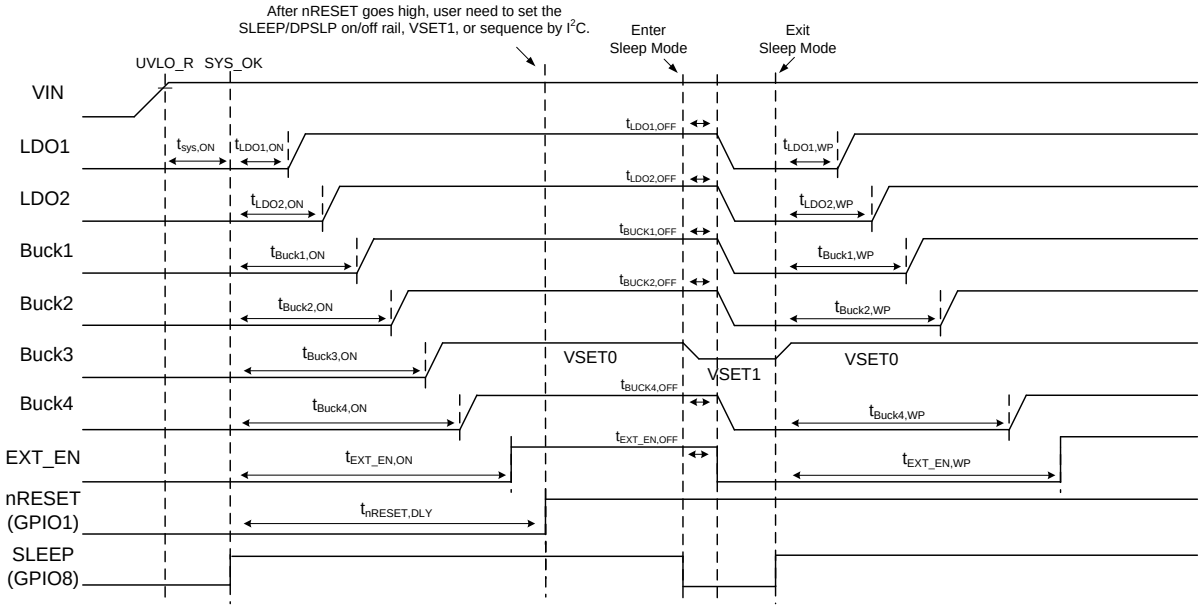
Figure 7. Power-On/Off Sequence

Power-on delay time: $t_{LDO1,ON}$/ $t_{LDO2,ON}$/ $t_{BUCK1,ON}$/ $t_{BUCK2,ON}$/ $t_{BUCK3,ON}$/$t_{BUCK4,ON}$/$t_{EXT\_EN,ON}$ = 0–7.5ms, 0.5ms/step.

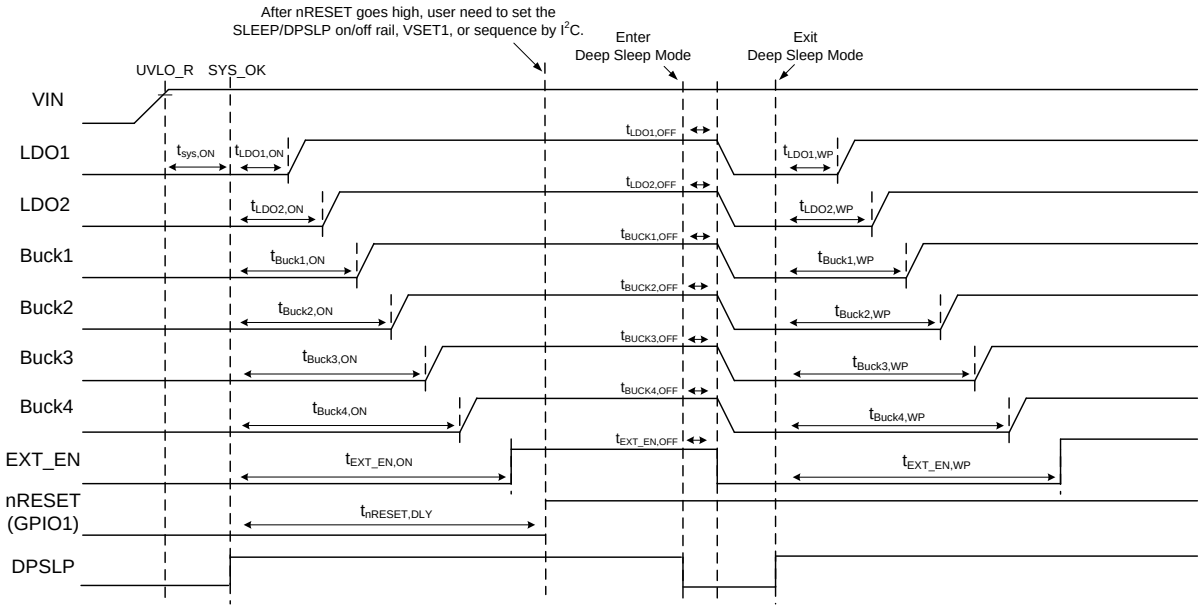
Power-off delay time: $t_{LDO1,OFF}$/$t_{LDO2,OFF}$/$t_{BUCK1,OFF}$/ $t_{BUCK2,OFF}$/$t_{BUCK3,OFF}$/$t_{BUCK4,OFF}$/$t_{EXT\_EN,OFF}$/$t_{NRESET,OFF}$ = 0ms, 0.25ms, 0.5ms, or 1ms.

nRESET delay time: $t_{NRESET,DLY}$ = 0.5ms, 1ms, 2ms, 4ms, 8ms, or 16ms.

SLEEP and DPSLE Sequence



(a)



(b)

Figure 8. Power-On/Off Sequence
(a) Enter/Exit Sleep Mode and (b) Enter/Exit Deep Sleep Mode

Wake up delay time: $t_{LDO1,WP}$/ $t_{LDO2,WP}$/$t_{BUCK1,WP}$/$t_{BUCK2,WP}$/$t_{BUCK3,WP}$/$t_{BUCK4,WP}$/$t_{EXT\_EN,WP}$ = 0–1.5ms, 0.5ms/step.

Functional Description

Table 1. Buck and LDO Overview

	Output Program Range	Output Program Step	Mode	I_{OUT} Max	HS Current Limit	Discharge Resistor	Soft-Start Time
Buck 1	1.6-3.0V	25mV	Buck or PLSW	4.0A	5.6A	4.4Ω	250/500μs
Buck 2	0.9-2.0V	10mV	Buck	2.0A	3.6A	9.4Ω	250/500μs
Buck 3	0.5-1.2V	10mV	Buck	4.0A	5.6A	9.4Ω	250/500μs
Buck 4	0.9-2.0V	50mV	Buck or LDO	2.0A	3.6A	9.4Ω	250/500μs
LDO 1	1.0-2.7V	50mV	LDO or PLSW	0.4A	LDO, PLSW: 0.5A	20Ω	200/360μs
LDO 2	1.0-2.7V	50mV	LDO or PLSW	0.4A	LDO, PLSW: 0.5A	20Ω	200/360μs

Power Sequence

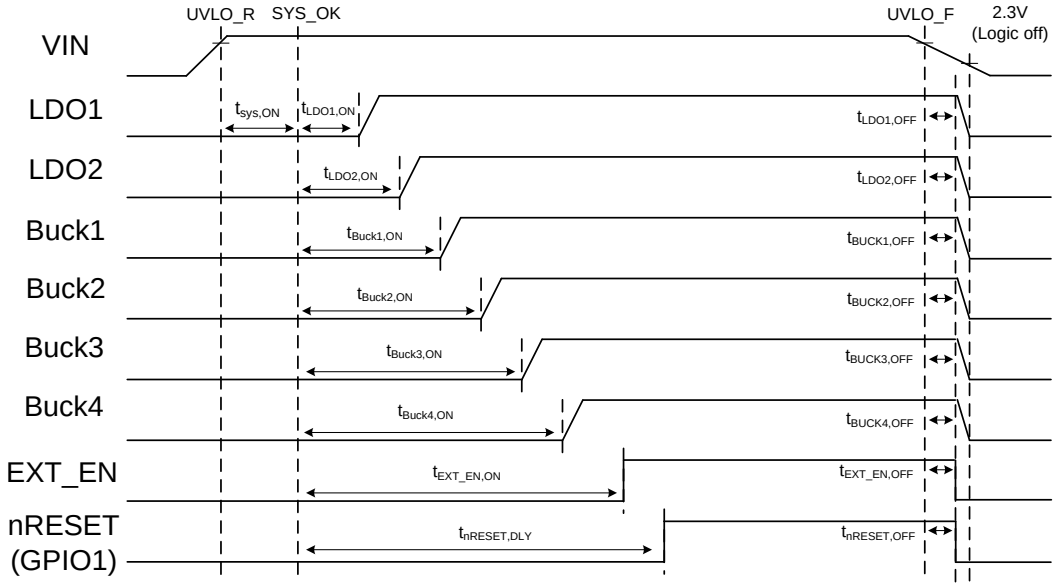


Figure 9. V_{IN} Power-On/Off Sequence

(1) When V_{IN} exceeds the UVLO rising threshold, each channel will start after the system delay $t_{SYS,ON}$ (typ = 1ms). During the system delay, the device will detect the GPIO2/3/4 status to define each channel's default setting (operating mode, output voltage, power-on delay, etc.). The power-on delay time can be set from 0ms to 7.5ms (0.5ms/step) to provide a different power sequence as required by the application. If V_{IN} is lower than the UVLO falling threshold, all channels will be turned off after the delay time. The power-off delay time can be set to 0ms, 0.25ms, 0.5ms, or 1ms.

(2) nRESET and EXT_EN are open-drain outputs. They are high impedance after a delay time that starts when V_{IN} exceeds the UVLO rising threshold. The delay time of nRESET can be set from 0.5ms to 16ms, and the delay time of EXT_EN can be set from 0ms to 7.5ms (0.5ms/step). nRESET and EXT_EN will be pulled low immediately when any output is out of regulation or V_{IN} is lower than the UVLO falling threshold. nRESET remains high in sleep and deep sleep modes.

Undervoltage Lockout (UVLO)

Undervoltage lockout is achieved by detecting V_{IN} voltage. If the AVIN pin voltage exceeds $V_{IN,RISING}$ (2.6V typ.), all rails will start after a delay. When AVIN pin voltage is lower than $V_{IN,FALLING}$ (2.5V typ.), all rails are shut down after a delay. The UVLO hysteresis (0.1V typ.) is designed to prevent shutdown caused by supply transients.

External Enable (EXT_EN)

The SY70202M provides an external power supply enable function, EXT_EN, which is used to control an external regulator. If AVIN pin voltage exceeds $V_{IN,RISING}$ (2.6V typ.), EXT_EN will become high impedance after a fixed delay. When AVIN pin voltage is lower than $V_{IN,FALLING}$ (2.5V typ.) or if a fault occurs, EXT_EN will become low impedance after a fixed delay. EXT_EN can be set to enable or disable in sleep or deep sleep mode using bit [6] of registers 0x08h or 0x09h, respectively.

GPIOx Setting

The SY70202M has eight GPIO pins. Each GPIO can be programmed for a specific function to suit different applications. GPIO2, GPIO3, and GPIO4 are 3-level GPIOs that can be used to set the output voltage of the power rail and the power-on delay.

GPIO1

GPIO1 is an open-drain output used for the nRESET function, which also acts as a power-good indicator. This pin becomes high impedance after a fixed delay from power-on. It will be pulled low immediately when any output goes out of regulation, or when AVIN pin voltage falls below $V_{IN,FALLING}$. The input trigger of nRESET can be set to SYS_OK or Buck2_PG using bit [7] of register 0x14h.

Note: If the nRESET input trigger is set as Buck2_PG, the power-on delay time of Buck 2 must be longer than other power rails.

nRESET becomes high after all channels have turned on during the power-on sequence and the subsequent delay time expires.
If V_{IN} drops below the UVLO falling threshold and then recovers to exceed the UVLO rising threshold, the device will reset and restart with the default initial power-on sequence.

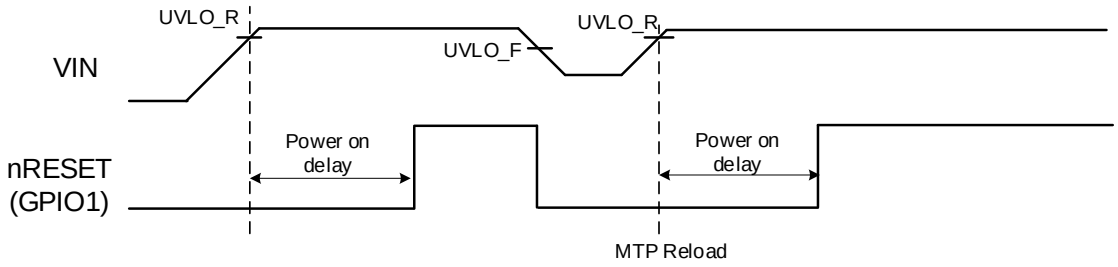


Figure 10. nRESET Logic when V_{IN} Drops below 2.3V

GPIO2

GPIO2 is an input pin used to select Buck 1 and Buck 2 output voltages. Buck 1 can be set to operate in buck or PLSW mode by the register B1_Mode. If Buck 1 is operating in buck mode, the output voltage can be set by the register B1_VSET. Buck 1 and Buck 2 have three configuration options, as shown in Table 2. The GPIO2 status must be set before UVLO and cannot be changed while the converter is running. Once the converter is running, buck operating mode and output voltage settings can only be changed using I^2C.

Table 2. GPIO2 Function Selection

GPIO2	Buck 1 Mode and Output Voltage	Buck 2 Output Voltage
High	B1_Mode = PLSW mode	B2_VSET = 1.2V
Floating	B1_Mode = buck mode, B1_VSET = 2.5V	B2_VSET = 1.2V
Low	B1_Mode = buck mode, B1_VSET = 2.9V	B2_VSET = 1.2V

GPIO3

GPIO3 is an input pin used to select Buck 3 output voltage and power-on delay options for each rail. Buck 3 has three configuration options, as shown in Table 3. The GPIO3 status must be set before UVLO and cannot be changed while the converter is running. After the converter is running, buck operating mode and output voltage settings can be changed using I^2C.

Table 3. GPIO3 Function Selection

GPIO3	Buck 3 Output Voltage	Power-On Delay
High	B3_VSET0 = 0.83V B3_VSET1 = 0.83V	Sequence A
Floating	B3_VSET0 = 0.82V B3_VSET1 = 0.82V	Sequence B
Low	B3_VSET0 = 0.85V B3_VSET1 = 0.85V	Sequence C

Table 4. Power-On Sequences

Rail	GPIO3 = High Sequence A	GPIO3 = Floating Sequence B	GPIO3 = Low Sequence C
Buck1	3.00ms	3.00ms	3.00ms
Buck2	4.00ms	1.00ms	4.00ms
Buck3	0.00ms	1.00ms	0.00ms
Buck4	2.00ms	1.00ms	1.00ms
LDO1	1.00ms	0.00ms	2.00ms
LDO2	3.50ms	2.00ms	2.00ms
EXT_EN	1.50ms	1.50ms	1.50ms
nRESET	Input trigger: SYS_OK, delay time = 8ms		

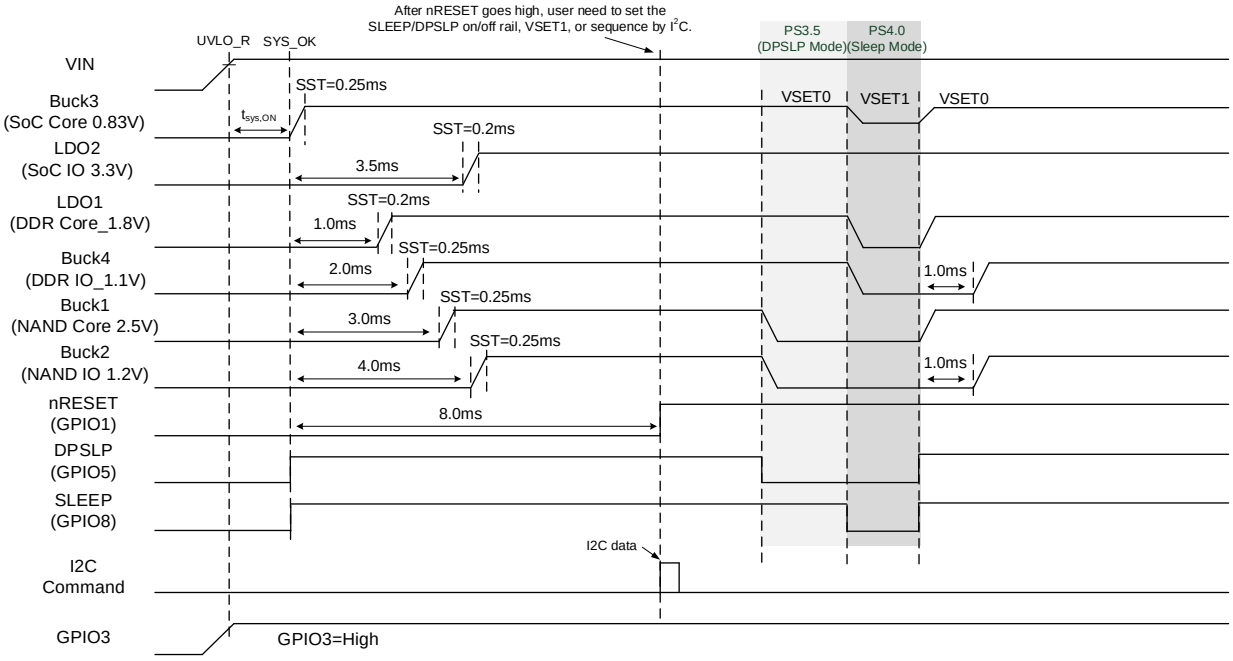


Figure 11. Power Sequence A

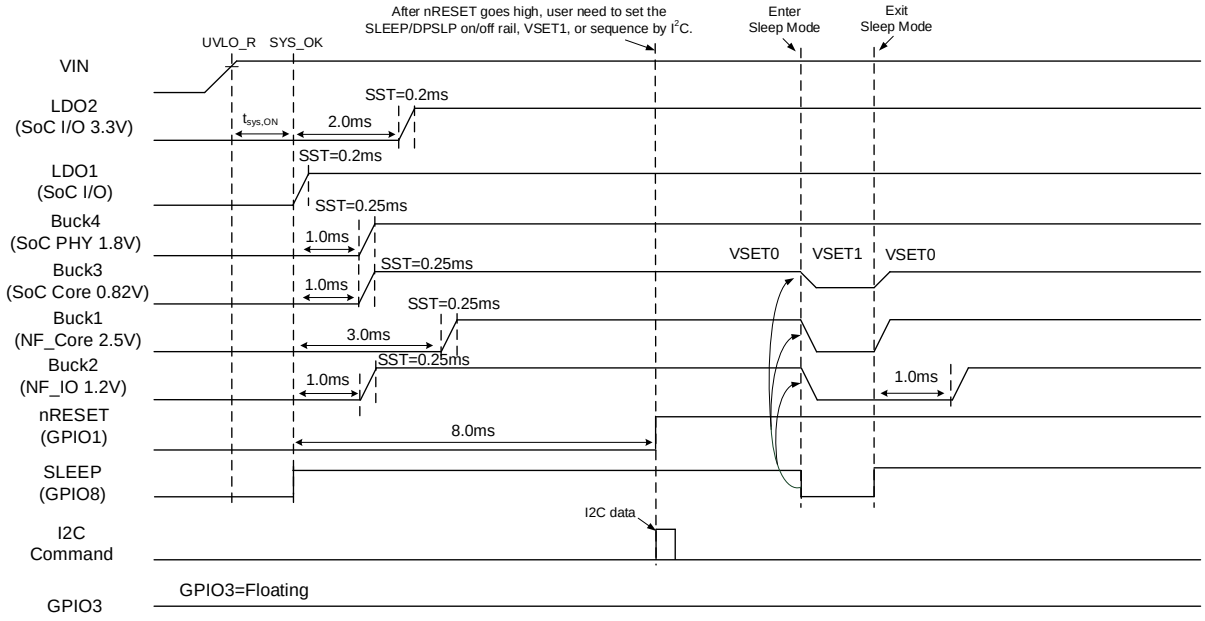


Figure 12. Power Sequence B

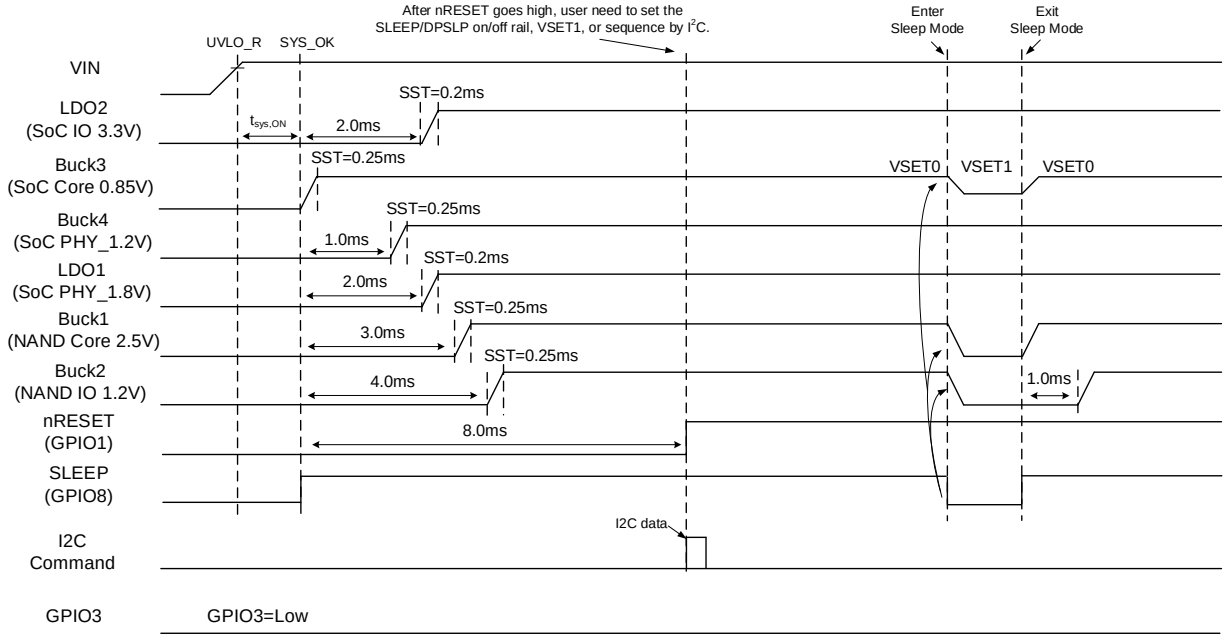


Figure 13. Power Sequence C

GPIO4

GPOI4 is an input pin used to select Buck 4 and LDO1 functions. Buck 4 can be set to operate in buck or LDO mode using the register B4_Mode. If Buck 4 is operating in buck mode, the output voltage can be set by register B4_VSET. LDO 1 can be set to operate in LDO or PLSW mode by the register LDO1_Mode. If LDO 1 is operating in LDO mode, the output voltage can be set by the register LDO1_VSET. Buck 4 and LDO 1 have three configuration options, as shown in Table 5. GPIO4 status must be set before UVLO and cannot be changed while the converter is running. After the converter is running, buck operating mode and output voltage settings can only be changed using I²C.

Table 5. GPIO4 Function Selection

GPIO4	Buck 4 Mode and Output Voltage	LDO 1 Mode and Output Voltage
High	DDR_SEL = 0 (DDR4):B4_Mode = buck mode, B4_VSET = 1.2V	DDR_SEL = 0 (DDR4): LDO1_Mode = LDO mode LDO1_VSET = 2.5V
	DDR_SEL = 1 (LPDDR4): B4_Mode = buck mode, B4_VSET = 1.1V	DDR_SEL = 1 (LPDDR4): LDO1_Mode = LDO mode LDO1_VSET = 1.8V
Floating	B4_Mode = buck Mode, B4_VSET = 1.8V	LDO1_Mode = PLSW
Low	B4_Mode = buck mode, B4_VSET = 1.2V	LDO1_Mode = LDO mode LDO1_VSET = 1.8V

GPIO5

GPIO5 can be configured as DPSLP mode input pin, nIRQ(SYSWARN) output pin, or I²C-controlled output pin using bits [7:6] of register 0x15h:

- **DPSLP mode**: Input pin. The DPSLP input is a level sensitive. If GPIO5 is pulled high (>1.2V), the device operates in ACTIVE mode; if the GPIO5 is pulled low (<0.55V), the device transitions to DPSLP mode.
- **I²C-controlled output**: GPIO5 can be configured as the I²C controlled open-drain output. The output can be selected as HIGH or LOW using bit [1] of register 0x15h.
- **nIRQ(SYSWARN) output**: GPIO5 can be configured as the nIRQ(SYSWARN) open-drain output. If AVIN < SYSWARN threshold (2.9V typ.), the device asserts the nIRQ interrupt, and GPIO5 will go low. The nIRQ pin only de-asserts when the fault condition is no longer present, and the corresponding fault bit is read via I²C.

GPIO5 function can be modified by I2C after nRESET goes high.

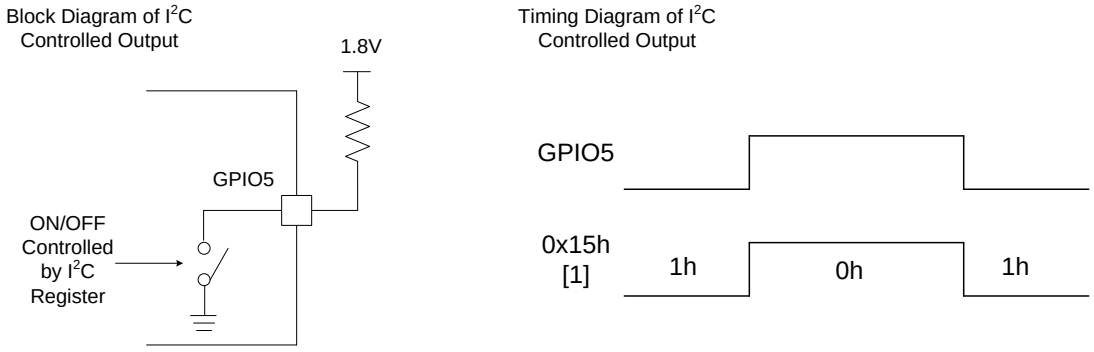


Figure 14. I²C Controlled Output Function Block Diagram and Timing

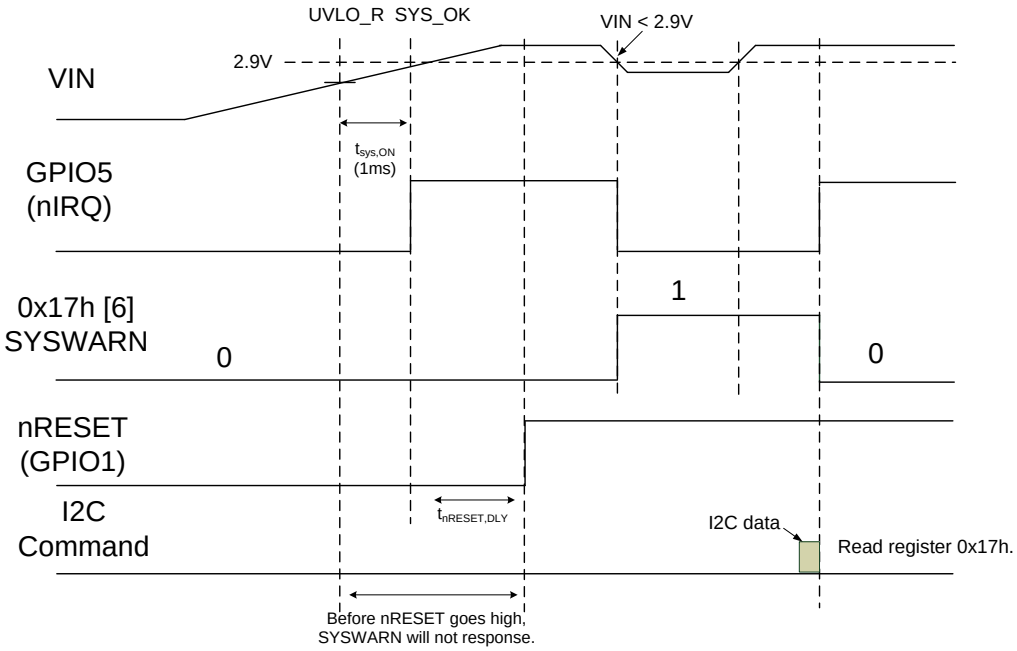


Figure 15. nIRQ (SYSWARN) Timing

GPIO6

GPIO6 is an Input pin used to select LDO 2 operating mode. If GPIO6 is pulled high, LDO 2 operates in LDO mode; if GPIO6 is pulled low, LDO 2 operates in PLSW mode. LDO 2 mode will be latched after the LDO 2 power-on delay.

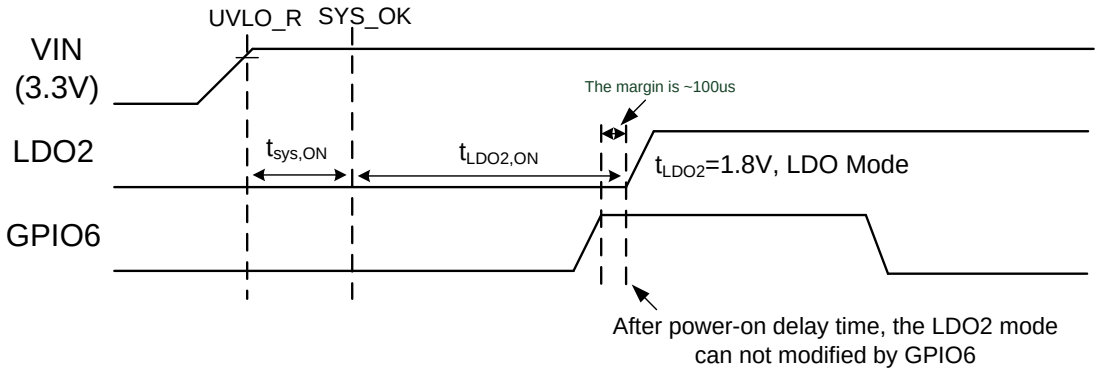


Figure 16. GPIO6 Function Timing

GPIO7

GPIO7 can be configured as an EXT_EN output pin, an I²C-controlled output pin, or a PWRDIS input pin using bits [5:4] of register 0x15h. GPIO7 function can be modified by I²C after nRESET goes high.

- **I²C-controlled output**: GPIO7 can be configured as a I²C controlled open-drain output. The output can be selected HIGH or LOW using bit [0] of register 0x15h.

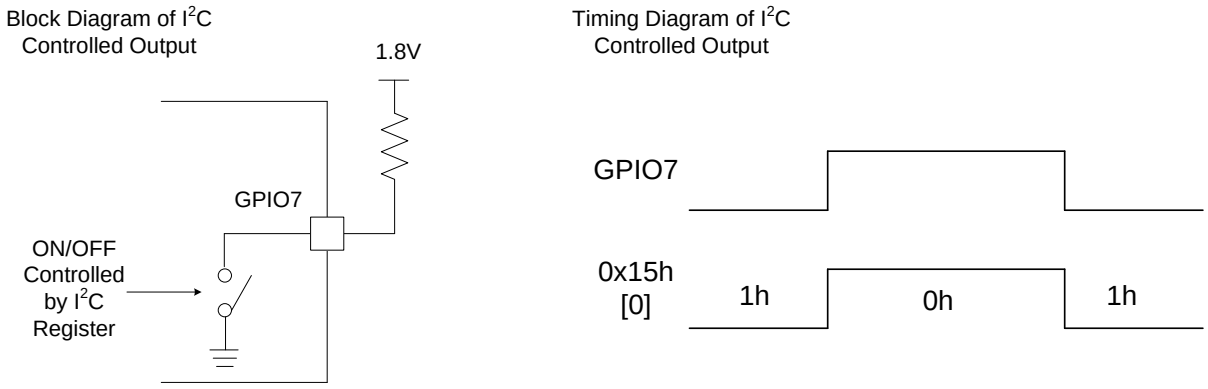


Figure 17. I²C-Controlled Output Function Block Diagram and Timing

- **PWRDIS input**: GPIO7 can be configured as the PWRDIS input. If GPIO7 is pulled high (>1.2V), all rails will be shut down; if GPIO7 is pulled low (<0.55V), all rails will power up with the power-on sequence. PWRDIS can be considered a global enable for the device. If PWRDIS is high during power-on, this will prevent the device from turning on and powering on the rails.

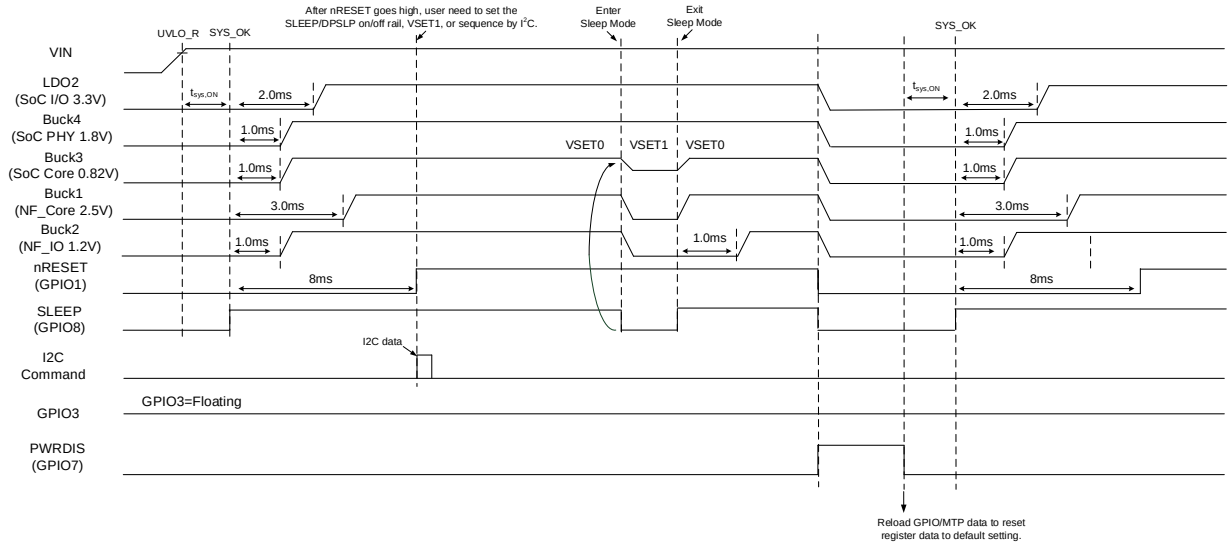


Figure 18. Timing for PWRDIS during Normal Operation

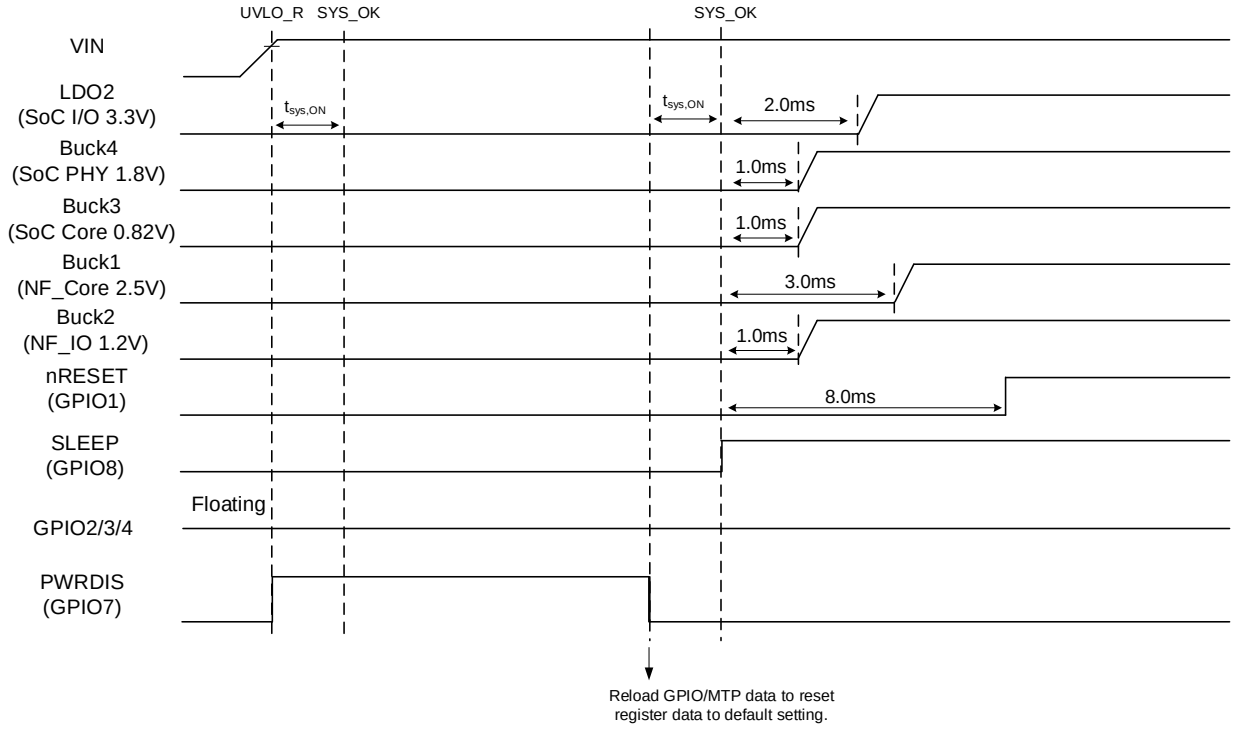


Figure 19. Timing for PWRDIS during V_{IN} Power-On

GPIO8

GPIO8 is an input pin used to control SLEEP state. The pin is level sensitive. If the GPIO8 is pulled high (>1.2V), the device operates in ACTIVE mode; if the GPIO8 is pulled low (<0.55V), the device operates in SLEEP mode.

GPIO Initial Status

Table 6 shows the initial status for the GPIO pins.

Table 6. GPIO Initial Status

GPIO	Function	Pin	Initial Status
GPIO1	nRESET	Open-drain output	NA
GPIO2	Buck 1 and Buck 2 bank	Input	Internal 1MΩ pull low
GPIO3	Buck 3 and power-on delay bank	Input	
GPIO4	Buck 4 and LDO 1 bank	Input	
GPIO5	DPSLP, I²C control output, or nIRQ(SYSWARN)	Input or open-drain output	NA
GPIO6	LDO 2 mode	Input	Internal 1MΩ pull low
GPIO7	EXT_EN, I²C control output, or PWRDIS	Input or open-drain output	PWRDIS: external 10kΩ pull low
GPIO8	Sleep	Input	Internal 1MΩ pull low

State Machine

The SY70202M state machine contains six states, shown in Figure 20.

In the RESET state, the device is waiting for the input voltage on V_{IN} to be within a valid range between VIN_UVLO and VIN OVP thresholds. In this state, all regulators are off.

The ACTIVE state is the normal operating mode when the input voltage is within the allowable range, all outputs are turned on, and no faults are present. When entering ACTIVE state from the RESET, THERMAL, or OV/SCP fault states, all regulators are powered following their power-up sequence. The regulators will not be sequenced when entering ACTIVE state from SLEEP or DPSLP states.

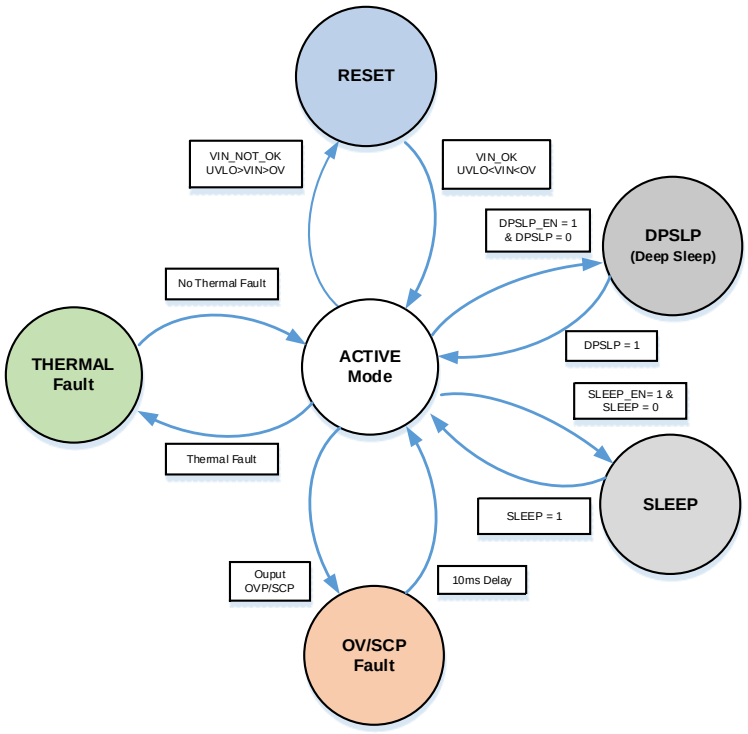


Figure 20. State Machine

Sleep Mode State

Each output can be programmed to be on or off in the sleep state. The regulators follow their programmed sequencing delay times when turning on or off as they exit or enter the SLEEP state. Bucks 1–4, LDO1,2, and EXT_EN can be programmed to turn off or turn on in SLEEP state by I²C. The device can enter SLEEP state via the I²C register SLEEP bit or by a GPIO input. Each individual regulator output can be programmed to be either on or off in SLEEP state. Buck 3 can also be programmed to regulate its VSET0 voltage, VSET1 voltage (DVS), or be turned off completely in SLEEP state.

shows the conditions to enter SLEEP state. Device I²C remains enabled in SLEEP state. The device exits the SLEEP state when the conditions to enter SLEEP state are no longer present.

Table 7. SLEEP Mode Truth Table

SLEEP	0x10h[1], SLEEP_EN	Result
0	1	SLEEP mode
1	1	ACTIVE mode

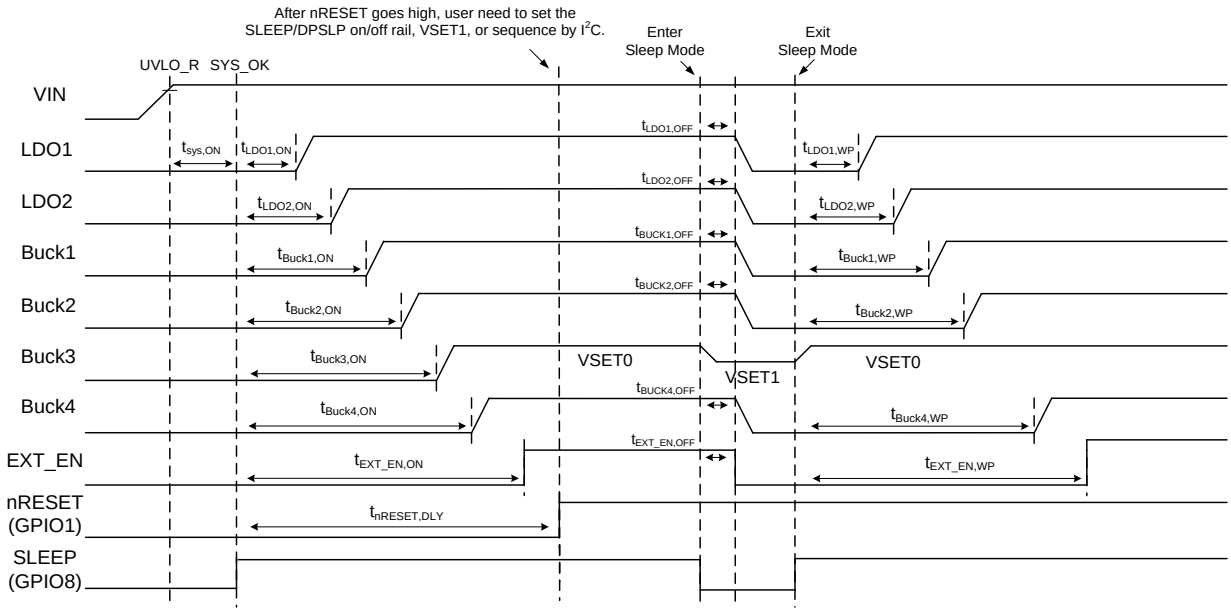


Figure 21. Sequence for Entering/Exiting SLEEP Mode

Power-on delay time: $t_{LDO1,ON}$/ $t_{LDO2,ON}$/ $t_{BUCK1,ON}$/ $t_{BUCK2,ON}$/ $t_{BUCK3,ON}$/ $t_{BUCK4,ON}$/$t_{EXT\_EN,ON}$ = 0–7.5ms, 0.5ms/step.

Power-off delay time: $t_{LDO1,OFF}$/ $t_{LDO2,OFF}$/ $t_{BUCK1,OFF}$/ $t_{BUCK2,OFF}$/ $t_{BUCK3,OFF}$/ $t_{BUCK4,OFF}$/$t_{EXT\_EN,OFF}$ = 0ms, 0.25ms, 0.5ms, or 1ms.

nRESET delay time: $t_{nRESET,DLY}$ = 0.5ms, 1ms, 2ms, 4ms, 8ms, or 16ms.

Wakeup delay time: $t_{LDO1,WP}$/ $t_{LDO2,WP}$/ $t_{BUCK1,WP}$/ $t_{BUCK2,WP}$/ $t_{BUCK3,WP}$/ $t_{BUCK4,WP}$/$t_{EXT\_EN,WP}$ = 0–1.5ms, 0.5ms/step.

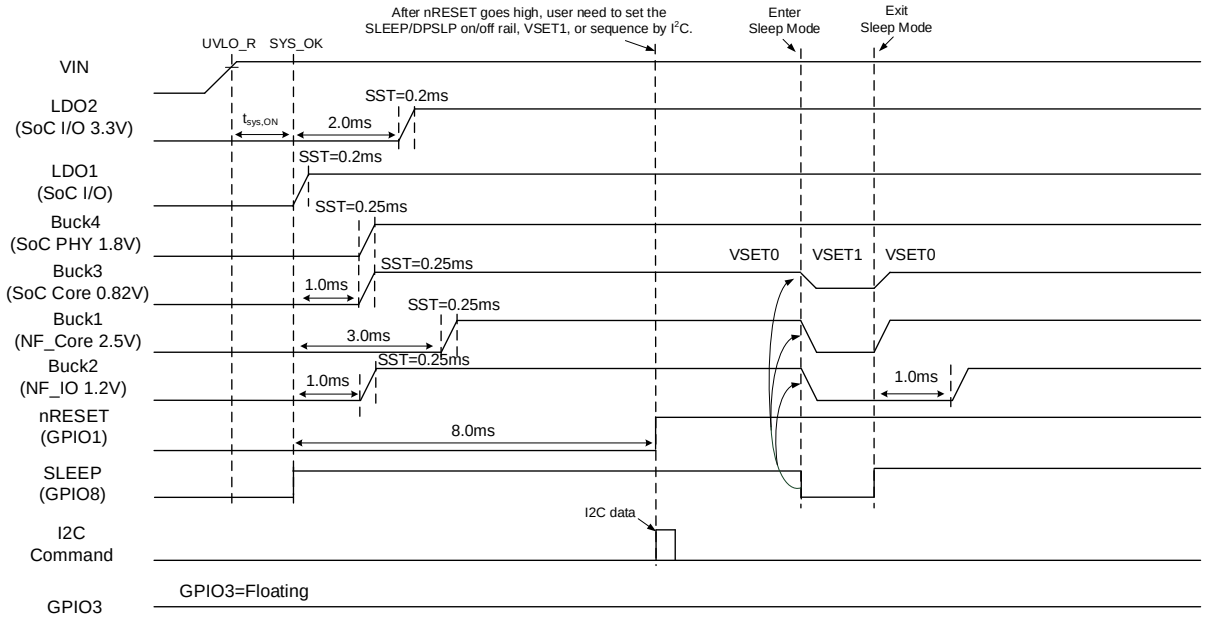


Figure 22. SLEEP Sequence for Power Sequence B

Deep Sleep (DPSLP) Mode State

The DPSLP state is another low-power operating mode similar to the SLEEP state. Each output can be programmed by an associated register to be on or off of during DPSLP state. The regulators follow their programmed sequencing delay times when turning on or off as they exit or enter the DPSLP state.

The device can enter DPSLP state via I²C register DPSLP_EN or the DPSLP GPIO pin. Table 8 shows the conditions to enter DPSLP state. Device I²C remains enabled in DPSLP state. The device exits the DPSLP state when the conditions to enter DPSLP state are no longer present.

Table 8. DPSLP Mode Truth Table

DPSLP	0x10h[0], DPSLP_EN	Result
0	1	Deep Sleep (DPSLP) mode
1	1	ACTIVE mode

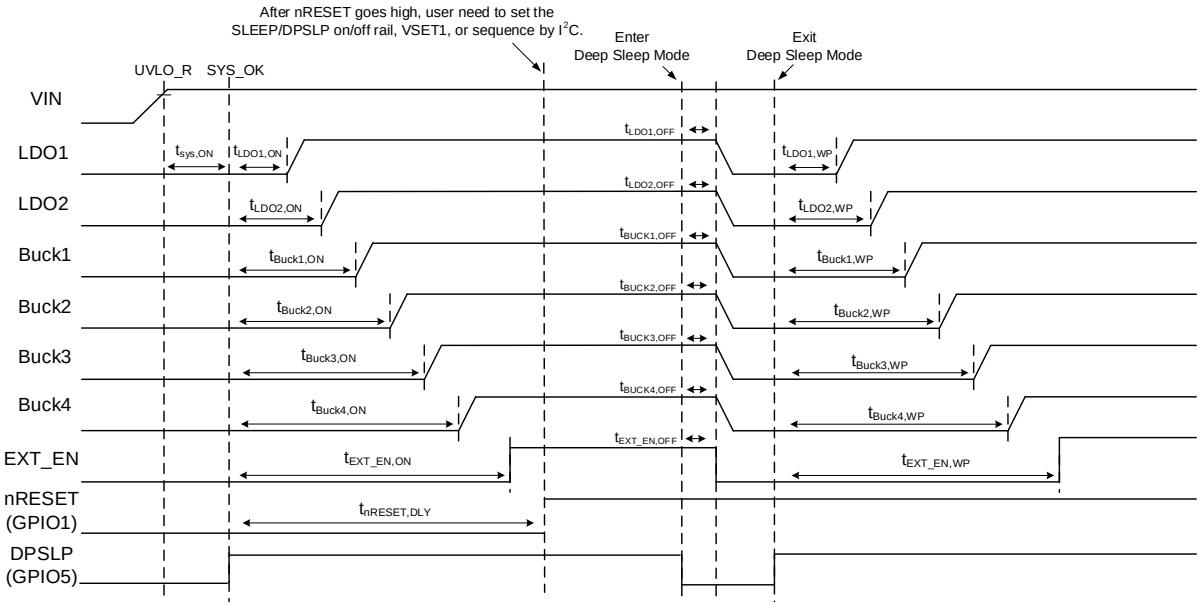


Figure 23. Conceptual of Sequence for Enter/Exit DPSLP Mode

Power-on delay time: $t_{LDO1,ON}$/ $t_{LDO2,ON}$/ $t_{BUCK1,ON}$/ $t_{BUCK2,ON}$/ $t_{BUCK3,ON}$/ $t_{BUCK4,ON}$/$t_{EXT\_EN,ON}$ = 0–7.5ms, 0.5ms/step.

Power-off delay time: $t_{LDO1,OFF}$/ $t_{LDO2,OFF}$/ $t_{BUCK1,OFF}$/ $t_{BUCK2,OFF}$/ $t_{BUCK3,OFF}$/ $t_{BUCK4,OFF}$/$t_{EXT\_EN,OFF}$ = 0ms, 0.25ms, 0.5ms, or 1ms.

nRESET delay time: $t_{nRESET,DLY}$ = 0.5ms, 1ms, 2ms, 4ms, 8ms, or 16ms.

Wakeup delay time: $t_{LDO1,WP}$/ $t_{LDO2,WP}$/ $t_{BUCK1,WP}$/ $t_{BUCK2,WP}$/ $t_{BUCK3,WP}$/ $t_{BUCK4,WP}$/$t_{EXT\_EN,WP}$ = 0–1.5ms, 0.5ms/step.

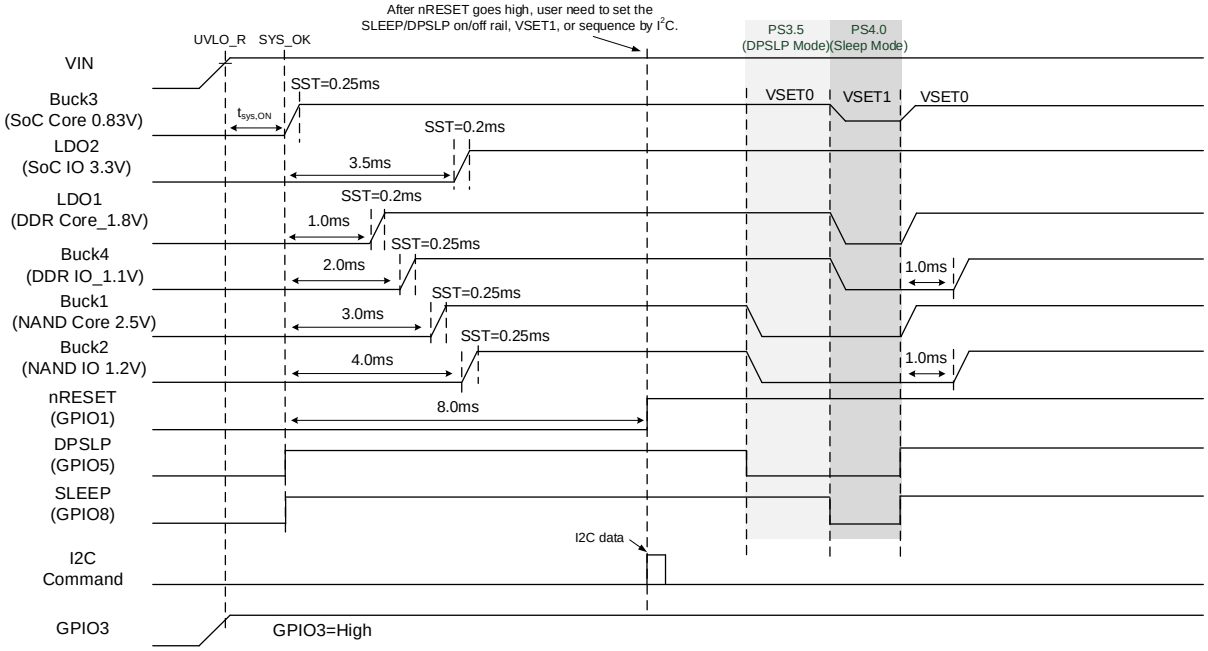


Figure 24. SLEEP and DPSLP Sequence for Power Sequence A

Fault-Protection Modes

The following sections and Table 9 describe the SY70202M fault-protection functions.

Table 9. Protection Functions Summary

Protection		Mechanism
V_{IN} Overvoltage Protection (VINOVP)		When VIN rises above 3.9V, the device shuts down and all the regulators are disabled. When V_{IN} decreases to 3.6V, the device restarts with the power-up sequence.
Overtemperature Protection (OTP)		When temperature exceeds 155°C, the device shuts down. When temperature decreases below 140°C, it restarts following the power-up sequence.
Output Overvoltage Protection (OVP)		When output voltage exceeds 125% of the target voltage for more than the 20µs deglitch time -the device shuts down for 10ms, then restarts following the power-up sequence.
Output Short-Circuit Protection (SCP)		Buck output voltage: <30% for more than 50µs deglitch time -the device shuts down for 10ms, then restarts following the power-up sequence. Buck 1 in PLSW mode: output voltage <80% with 50µs deglitch time -the device shuts down all functions for 10ms, then restarts following the power-up sequence. LDO: output voltage <60% of target for at least 50µs deglitch time -the device shuts down all functions for 10ms, then restarts with the power-up sequence.
Overcurrent Protection (OCP)	Buckx	Inductor current peak reaches current limit, and then maintain regulation.
	LDO	LDO current limit reached. If I_{OUT} = 0.5A for more than 200µs, the device shuts down for 10ms, then restarts with the power-up sequence.
	LDO 1/2 PLSW Mode	Load switch current limit reached. If I_{OUT} = 0.5A for more than 200µs, the device shuts down for 10ms, then restarts with the power-up sequence.
	Buck 1 PLSW Mode	Load switch current limit reached. If I_{OUT} = 4.5A for more than 200µs, the device shuts down all functions for 10ms, then restarts with the power-up sequence.

The device will reset to default settings after VINOVP, OTP, OVP, SCP, or OCP shutdown.

Output Overvoltage and Short-Circuit Protection

If an output overvoltage or short-circuit condition occurs, the device will be shut down without the power-off sequence for 10ms, then restart with the power-up sequence. If the short-circuit or overvoltage condition still exists in the ACTIVE state, the device will shut down again for 10ms then restart, repeating until the fault condition is removed.

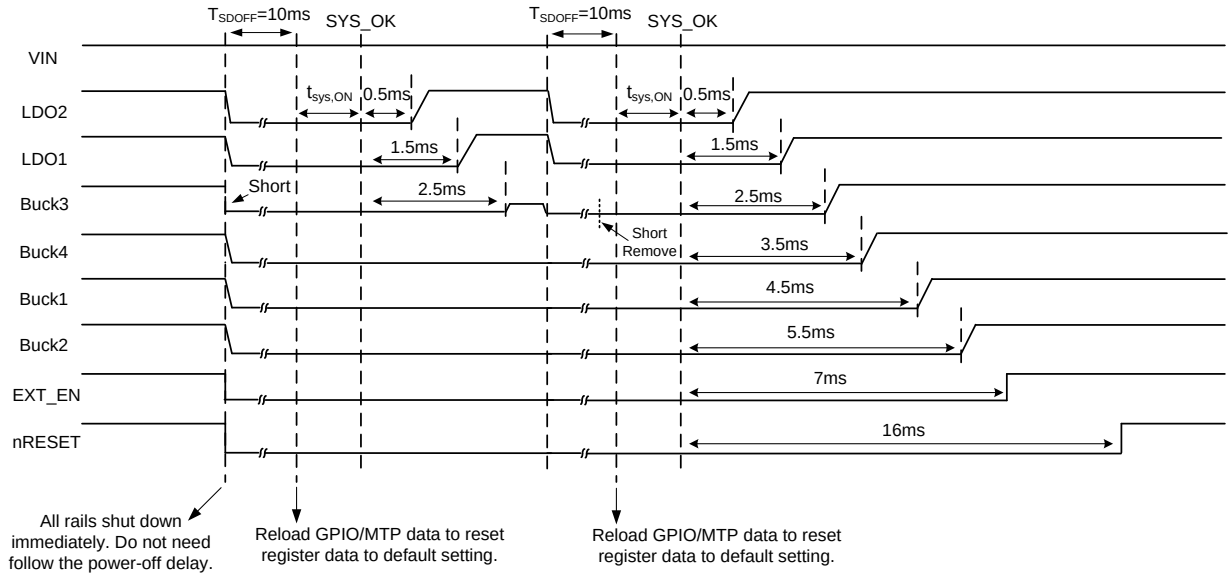


Figure 25. Buck 3 Output Short-Circuit Event in ACTIVE Mode

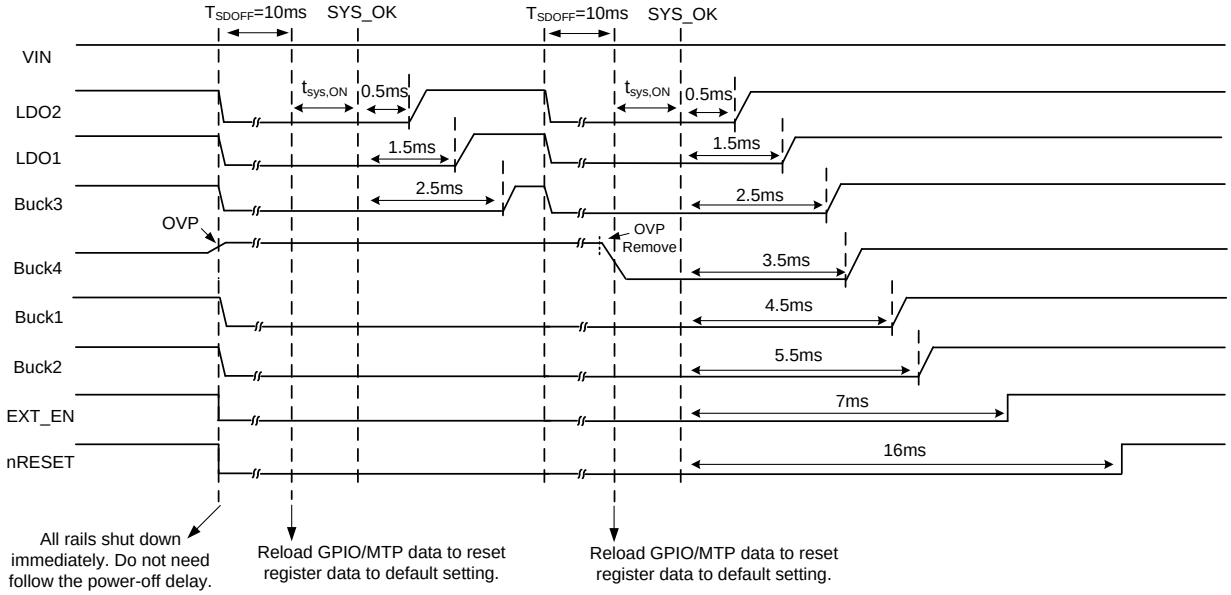


Figure 26. Buck 4 Output Overvoltage Event in ACTIVE Mode

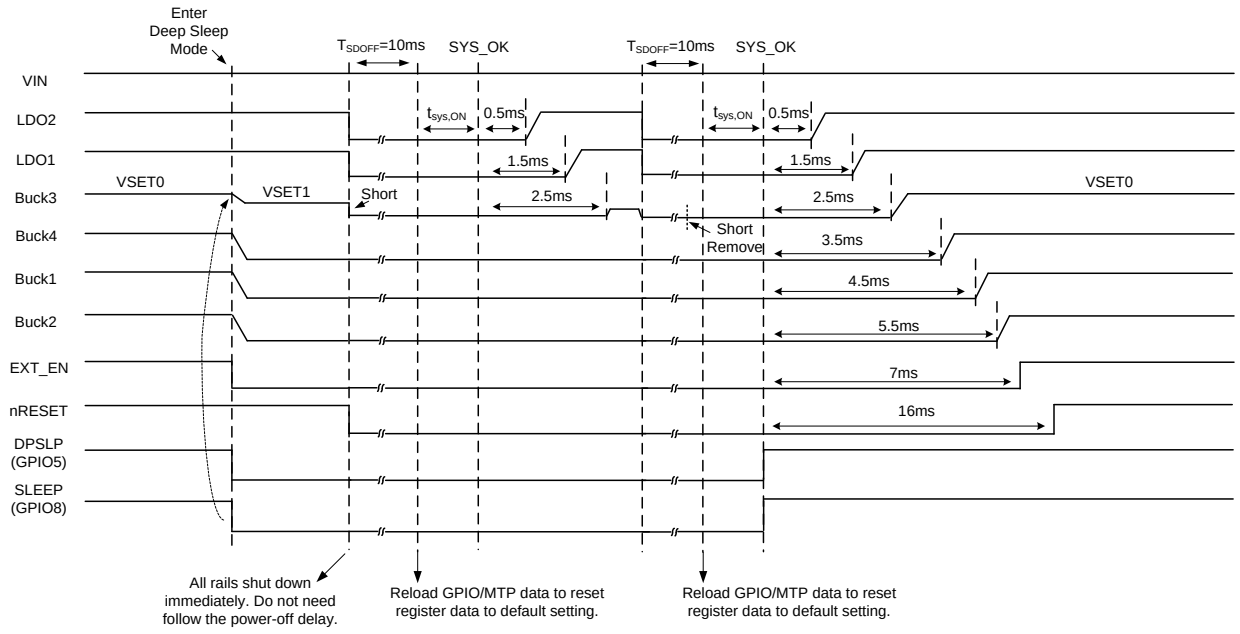


Figure 27. Buck 3 Output Short-Circuit Event in Deep Sleep Mode

Input Overvoltage Protection

The V_{IN} overvoltage protection (OVP) threshold is 3.9V. When V_{IN} exceeds 3.9V, all channels will be turned off. The OVP hysteresis is 0.3V. When V_{IN} decreases to 3.6V, all channels will restart with the power-on sequence.

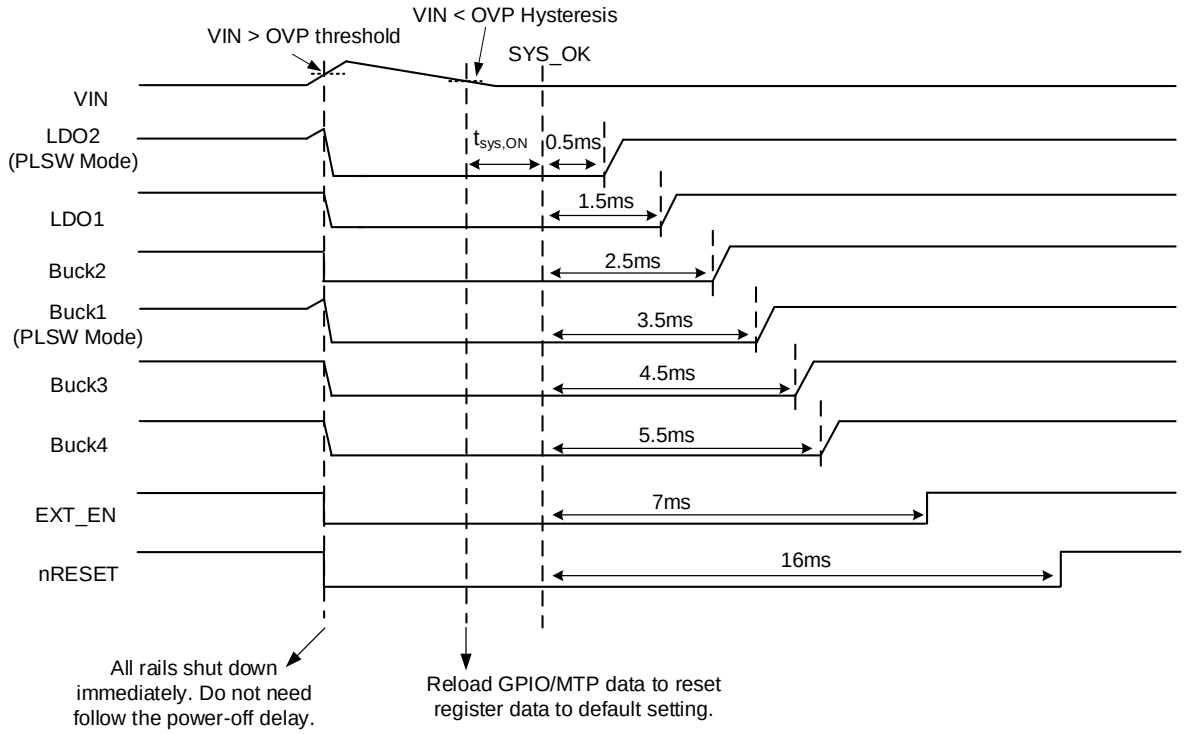


Figure 28. Input Overvoltage Protection

Output Current Limit

The buck converter limits the HS (high-side) switch current and LS (low-side) switch current during each switching cycle. This reduces the effective duty cycle and causes the output voltage to drop, potentially creating a short-circuit condition and causing the device to turn off all supplies off for 10ms then restart with the power-up sequence.

For the LDO, when the output current reaches the current limit threshold, the protection circuit will limit the output current. If the current limit is reached for 200μs, or if short-circuit is detected, the device will shut down for 10ms then restart with the power-up sequence.

For Buck1 operating as a load switch (PLSW mode), when the output current exceeds 4.5A, the protection will limit the current. If the current limit is reached for 200μs, the device will shut down for 10ms then restart with the power-up sequence.

Thermal Shutdown

Thermal shutdown is implemented to prevent damage caused by excessive heat and power dissipation. When the junction temperature exceeds 155°C, the device will be shut down without the power-off sequence. Once the temperature falls below 140°C, the device will automatically restart with the startup sequence, using the default configuration.

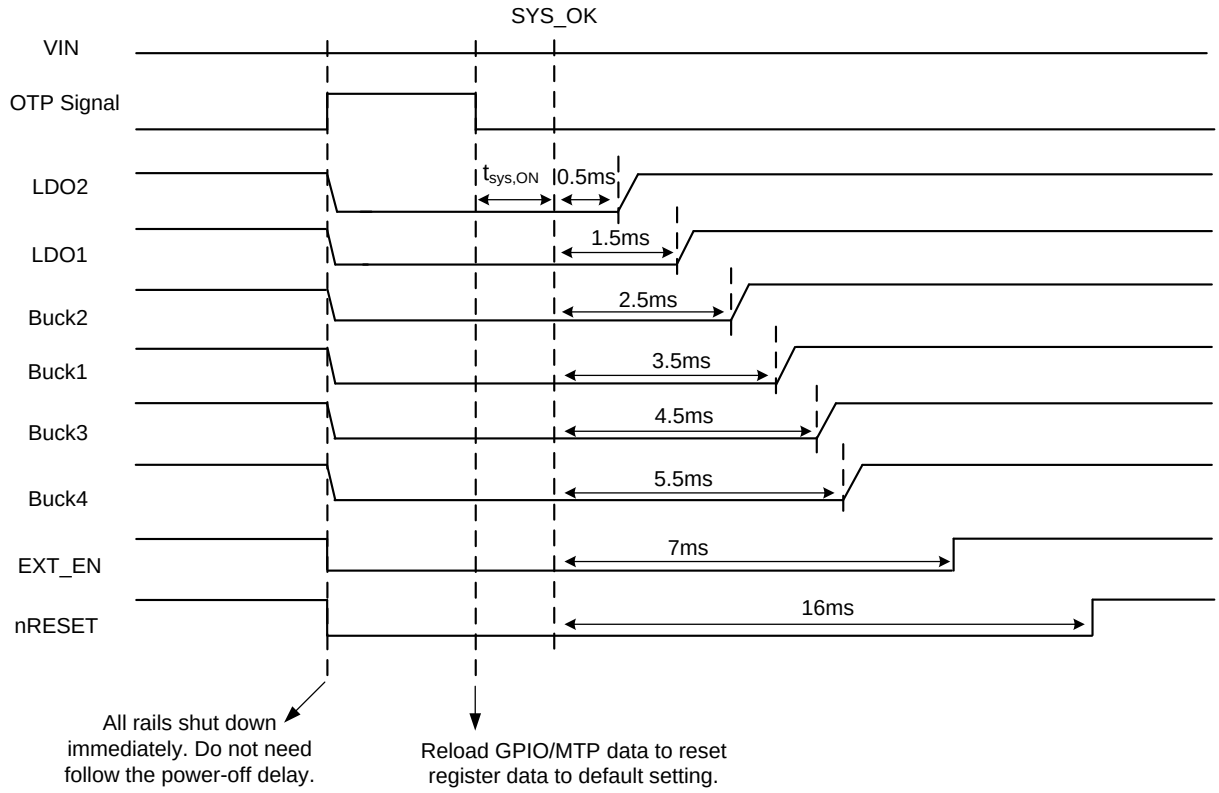


Figure 29. Overtemperature Protection

Application Information

The following paragraphs provide information on selecting the external components for each of the buck converters, to match the application requirements.

Input Capacitor C_{INX}

For the best performance, select typical X5R or better grade ceramic capacitors with a 6.3V or higher rating, and at least 10μF capacitance. The capacitor should be placed as close as possible to the corresponding pin on the device, while also minimizing the loop area formed by C_{INx} and the IN/GND pins.

When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability, and high RMS current rating over a wide temperature and voltage range.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current. The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 10μF X5R capacitor is sufficient for each of the buck converters in most applications.

Output Inductor L_X

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT}\left(1 - V_{OUT}/V_{IN,MAX}\right)}{f_{SW} \times I_{OUT,MAX} \times 0.4}$$

where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY70202M has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}\left(1 - V_{OUT}/V_{IN,MAX}\right)}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Use an inductor with DCR less than 20mΩ to achieve good overall efficiency.

Output Capacitor C_{OUTX}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting C_{OUT}. For the best performance, use two X5R or better grade ceramic capacitors with a 10V rating, and capacitance of at least 22μF for each converter output.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed:

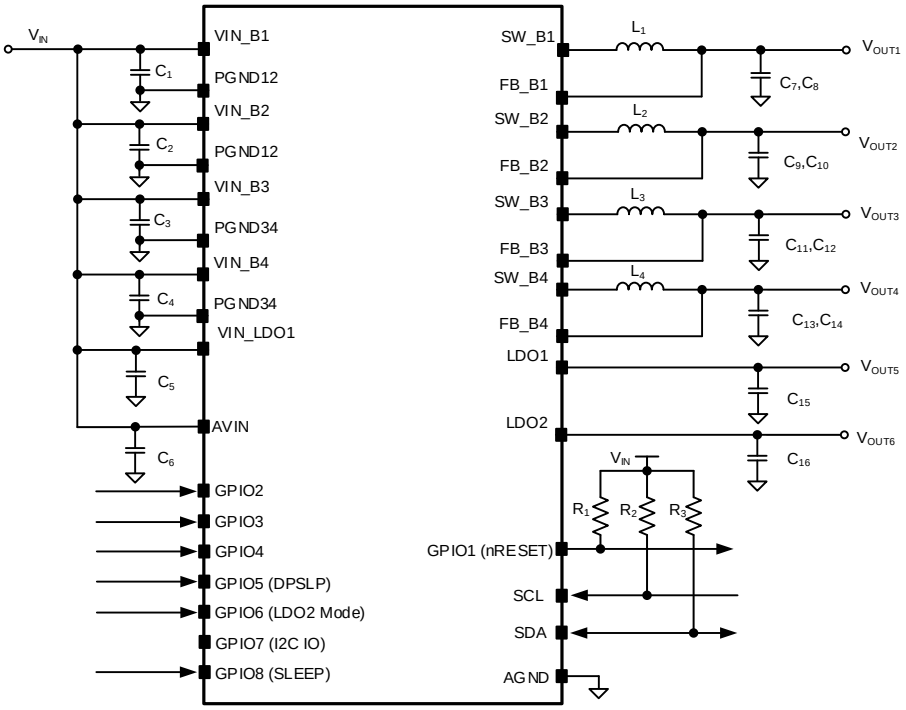
The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔIL) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, consider both.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The measured capacitive ripple might be higher than the theoretical value because the effective capacitance for ceramic capacitors decreases with the voltage across its terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Application Schematic



BOM List

Reference Designator	Description	Part Number	Manufacturer
U_1	PMIC	SY70202M	Silergy
L_1, L_3	0.47μH, 26mΩ, 4A 2016	DFE201612E-R47M	Murata
L_2, L_4	0.47μH,60mΩ,4A 1608	DFE18SBNR47MDLL	Murata
C_1, C_2, C_3, C_4	10μF/6.3V,0402, X5R	GRM155R60J106ME47D	Murata
C_5, C_6, C_{15}, C_{16}	1μF/6.3V, 0603, X6S	GRM033C80G105MEA2D	Murata
C_7, C_8, C_9, C_{10}, C_{11}, C_{12}, C_{13} ,C_{14}	22μF/6.3V,0603, X5R	GRM186R60J226ME15D	Murata
R_1	100kΩ,0603		
R_2, R_3	5.1kΩ, 0603		

Layout Design

Follow these PCB layout guidelines for optimal performance:

- Place C_{INX} C_{OUTX} and L as close as possible to the device to improve efficiency and provide better noise immunity.
- Maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance.
- Place the decoupling capacitor of VIN_B1 close to the VIN_B1 and PGND12 pins. Minimize the loop area formed by the input capacitors, input pins, and PGND pins. Apply the same principle of decoupling capacitor placement for all buck converters and LDOs.
- Minimize the PCB copper area associated with the LX pin to improve noise immunity.

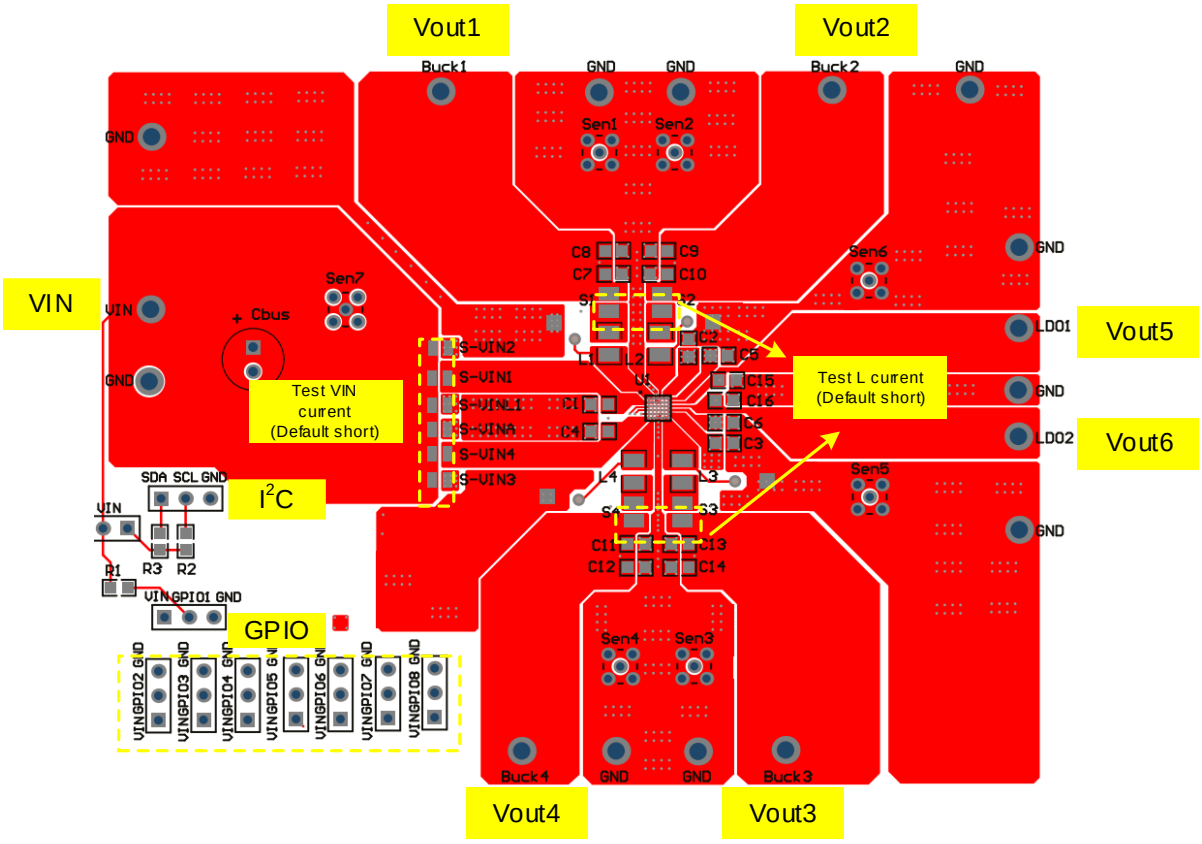


Figure 30. Suggested PCB Layout

I²C Compatible Interface

The SY70202M features an I²C compatible interface that allows the host to control the configuration and the output voltage level of all channels for the DVS function. The I²C interface supports clock speeds up to 3.4MHz and supports standard I²C commands. The host issues a special one-byte address to enter High Speed mode operating up to 3.4MHz.

All transactions start with a control byte sent from the I²C host device. The control byte begins with a START condition followed by seven bits of peripheral address, which is 0100101x for this device.

The I²C interface is fully functional once V_{IN} exceeds the UVLO threshold.

I²C Interface Timing

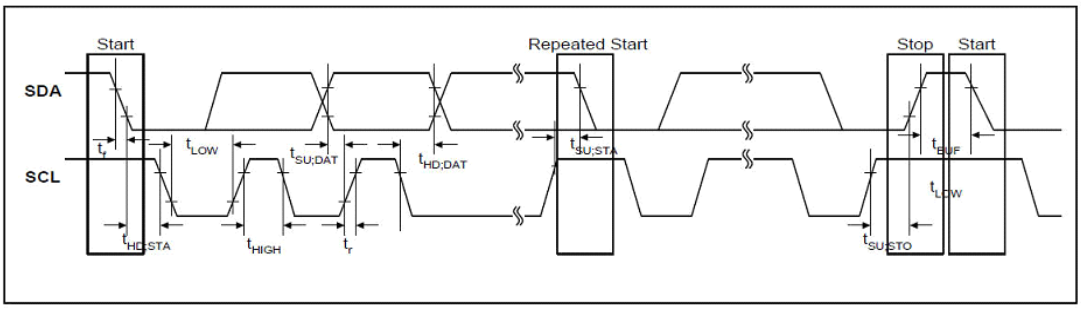


Figure 31. I²C Interface Timing

Table 10. I²C Electrical Characteristics

Characteristics	Symbol	Standard Mode		Fast Mode		High Speed Mode		Units
		Min	Max	Min	Max	Min	Max	
V_{IN} voltage	V_{IN}	3.3V						V
Pullup voltage	V_{PU}	1.7V to 3.6V						V
SCL clock frequency	f_{SCL}	0 to 100k		Hz		0 to 3.4M		Hz
Hold time (repeated) START condition	$t_{HD,STA}$	4	µs	0.6	µs	0.16	-	µs
LOW period of the SCL clock	t_{LOW}	4.7	µs	1.3	µs	0.16	-	µs
HIGH period of the SCL clock	t_{HIGH}	4	µs	0.6	µs	0.06	-	µs
Setup time for a repeated START condition	$t_{SU,STA}$	4.7	µs	0.6	µs	0.16	-	µs
DATA in hold time	$t_{HD;DI}$	0	ns	0	ns	0	70	ns
DATA out hold time	$t_{HD;DO}$		ns		ns		70	ns
Data setup time	$t_{SU;DAT}$	250	ns	100	ns	10	-	ns
Rise time of both SDA and SCL signals	t_R	-	ns	5	ns	5	40	ns
Fall time of both SDA and SCL signals	t_F	-	ns	5	ns	5	40	ns
Setup time for STOP condition	$t_{SU;STO}$	4	µs	0.6	µs	0.16	1	µs
Bus free time between STOP and START Conditions	t_{BUF}	4.7	-	1.3	-	-	-	µs
Capacitive load for each bus line	C_B	-	400	-	400	-	100	pF
Low Level Input Voltage	V_{IL}	-	0.4	-	0.4	-	0.4	V
High Level Input Voltage	V_{IH}	1.4	-	1.4	-	1.4	-	V

I²C Device Address

When communicating with multiple devices using the I²C interface, each device must have its own unique address

so the host can distinguish between the devices. The device peripheral address is 0x0100101x, where 'x' is the read/write control bit.

START and STOP Conditions

The START condition is a high-to-low transition of the SDA line while SCL is high. The STOP condition is a low-to-high transition on the SDA line while SCL is high. A STOP condition must be sent before each START condition. The I²C host always generates the START and STOP conditions.

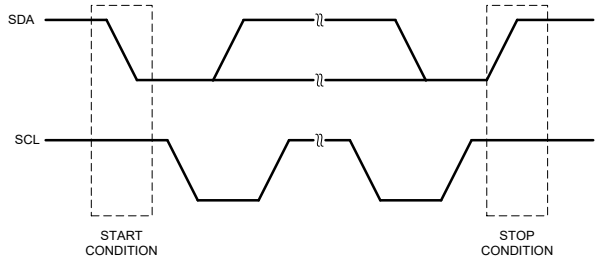


Figure 32. Start and Stop Conditions

Data Validity

The data on the SDA line must be stable during the high period of the SCL, unless generating a START or STOP condition. The high or low state of the data line can only change when the clock signal on the SCL line is low.

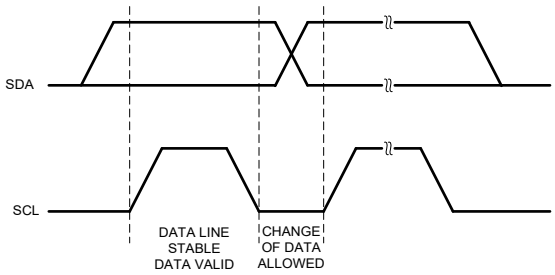


Figure 33. Data Validity

Acknowledge

Each address and data transmission uses nine clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the host sends seven peripheral address bits and an R/$\overline{W}$ bit during the next eight clock pulses. During the ninth clock pulse, the device that recognizes its address holds the data line low to acknowledge. The acknowledge bit is also used by both the host and peripheral to acknowledge receipt of register addresses and data.

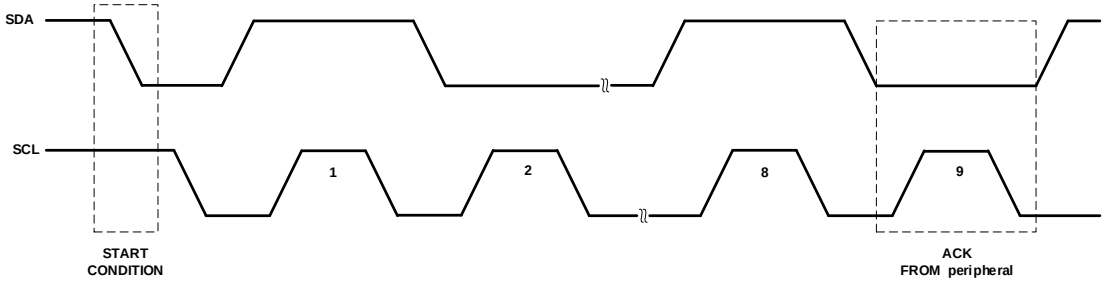


Figure 34. I²C Acknowledge

Table 11. PMIC I²C Protocol

Write operation	Start	Device address							R/W	ACK	Byte address	ACK	N-bytes DATA												ACK	STOP
		0	1	0	0	1	0	1	0	0	N-bytes address	0													0	
Read operation	Start	Device address							R/W	ACK	Byte address	ACK	Repeated Start	Device address							R/W	ACK	N-bytes DATA		ACK	STOP
		0	1	0	0	1	0	1	0	0	N-bytes address	0		0	1	0	0	1	0	1	1	0			1	

Data is written by the host from the address contained in the second byte and can continue for N subsequent addresses (ACK occurs after every byte) until the transaction is stopped. Data is read by the host from the address contained in the second byte and can continue for multiple bytes (ACK occurs after every byte) with the address being incremented on every byte being read.

Register Map

Register Map Summary

Address	D7	D6	D5	D4	D3	D2	D1	D0
0x00h	x	B1_Mode	B1_VSET					
0x01h	x	B2_VSET						
0x02h	x	B3_VSET0						
0x03h	x	B3_VSET1						
0x04h	x	DDR_SEL	B4_Mode	B4_VSET				
0x05h	x	LDO1_ Mode	LDO1_VSET					
0x06h	x	x	LDO2_VSET					
0x07h	x	x	LDO2_CH _EN	LDO1_CH_E N	Buck4_CH_ EN	Buck3_CH_ EN	Buck2_CH _EN	Buck1_CH_ EN
0x08h	B3_VID@ SLEEP_ EN	EXT_EN_SL EEP_ EN	LDO2_ SLEEP_ EN	LDO1_ SLEEP_ EN	Buck4_ SLEEP_ EN	Buck3_ SLEEP_ EN	Buck2_ SLEEP_ EN	Buck1_ SLEEP_ EN
0x09h	x	EXT_EN_DP SLP_ EN	LDO2_ DPSLP_ EN	LDO1_ DPSLP_ EN	Buck4_ DPSLP_ EN	Buck3_ DPSLP_ EN	Buck2_ DPSLP_ EN	Buck1_ DPSLP_ EN
0x0Ah	x	x	x	x	B4_PWM_ EN	B3_PWM_ EN	B2_PWM_ EN	B1_PWM_ EN
0x0Bh	x	x	LDO2_ SST	LDO1_ SST	B4_SST	B3_SST	B2_SST	B1_SST
0x0Ch	Buck1_Power OFF_ DLY		Buck2_Power OFF_ DLY		Buck3_Power OFF_ DLY		Buck4_Power OFF_ DLY	
0x0Dh	LDO1_Power OFF_ DLY		LDO2_Power OFF_ DLY		EXT_EN_Power OFF_ DLY		nRESET_Power OFF_ DLY	
0x0Eh	Buck1_Wake Up_ DLY		Buck2_Wake Up_ DLY		Buck3_Wake Up_ DLY		Buck4_Wake Up_ DLY	
0x0Fh	x	x	LDO1_Wake Up_ DLY		LDO2_Wake Up_ DLY		EXT_EN_Wake Up_ DLY	
0x10h	DIS_ OVUV	DIS_OTP	DIS_ VINOVP	x	x	x	SLEEP_ EN	DPSLP_ EN
0x11h	B1_Power ON_DLY				B2_Power ON_DLY			
0x12h	B3_Power ON_DLY				B4_Power ON_DLY			
0x13h	LDO1_Power ON_DLY				LDO2_Power ON_DLY			
0x14h	nRESET_ Input Trigger	nRESET_Power_ON_DLY			EXT_EN_ Power ON_DLY			
0x15h	GPIO5 function		GPIO7 function		x	GPIO6 Lock	GPIO5 Open drain	GPIO7 Open drain
0x34h	x	x	x	Vendor ID	CMI Version			

Fault Register Map

Address	D7	D6	D5	D4	D3	D2	D1	D0
0x16h	TSP	VIN_ OVP	LDO2_ OVP	LDO1_ OVP	Buck4_ OVP	Buck3_ OVP	Buck2_ OVP	Buck1_ OVP
0x17h	x	SYSWARN	LDO2_ UVP(SCP)	LDO1_ UVP(SCP)	Buck4_ UVP(SCP)	Buck3_ UVP(SCP)	Buck2_ UVP(SCP)	Buck1_ UVP(SCP)

Note: The fault bit is a latched status bit and remains asserted until read by I²C.

GPIO2 Register Map

Address	Register	Default GPIO2 High	Default GPIO2 Floating	Default GPIO2 Low	EEPROM Bit	Range	Resolution
0x00h	B1_Mode [6]	PLSW/01h	Buck/00h	Buck/00h	1bit	0 – Buck 1 operating in buck mode 1 – Buck 1 operating in PLSW mode	-
	B1_VSET [5:0]	2.5V/24h	2.5V/24h	2.9V/34h	6bits	Buck 1 output range is 1.6V-3.0V	25mV
0x01h	B2_VSET [6:0]	1.2V/1Eh	1.2V/1Eh	1.2V/1Eh	7bits	Buck 2 output range is 0.9V-2.0V	10mV

GPIO3 Register Map

Address	Register	Default GPIO3 High	Default GPIO3 Floating	Default GPIO3 Low	EEPROM Bit	Range	Resolution
0x02h	B3_VSET0 [6:0]	0.83V/21h	0.82V/20h	0.85V/23h	7bits	Buck 3 output range is 0.5V-1.2V	10mV
0x03h	B3_VSET1 [6:0]	0.83V/21h	0.82V/20h	0.85V/23h	7bits	Buck 3 output range is 0.5V-1.2V	10mV
0x11h	B1_Power ON_DLY [7:4]	3.0ms/06h	3.0ms/06h	3.0ms/06h	4bits	0000: 0ms, 0001: 0.5ms, …. 1110: 7.0ms, 1111: 7.5ms	0.5ms
	B2_Power ON_DLY [3:0]	4.0ms/08h	1.0ms/02h	4.0ms/08h	4bits	0000: 0ms, 0001: 0.5ms, …. 1110: 7.0ms, 1111: 7.5ms	0.5ms
0x12h	B3_Power ON_DLY [7:4]	0.0ms/00h	1.0ms/02h	0.0ms/00h	4bits	0000: 0ms, 0001: 0.5ms, …. 1110: 7.0ms, 1111: 7.5ms	0.5ms
	B4_Power ON_DLY [3:0]	2.0ms/04h	1.0ms/02h	1.0ms/02h	4bits	0000: 0ms, 0001: 0.5ms, …. 1110: 7.0ms, 1111: 7.5ms	0.5ms
0x13h	LDO1_Power ON_DLY [7:4]	1.0ms/02h	0.0ms/00h	2.0ms/04h	4bits	0000: 0ms, 0001: 0.5ms, …. 1110: 7.0ms, 1111: 7.5ms	0.5ms
	LDO2_Power ON_DLY [3:0]	3.5ms/07h	2.0ms/04h	2.0ms/04h	4bits	0000: 0ms, 0001: 0.5ms, …. 1110: 7.0ms, 1111: 7.5ms	0.5ms
0x14h	nRESET_ Input Trigger [7]	SYS_OK/01h	SYS_OK/01h	SYS_OK/01h	1bit	0: Buck2_PG 1: SYS_OK	-
	nRESET_ Power ON_ DLY [6:4]	8.0ms/04h	8.0ms/04h	8.0ms/04h	3bits	000: 0.5ms, 001: 1.0ms, 010: 2.0ms, 011: 4.0ms, 100: 8.0ms, 101: 16.0ms	-
	EXT_EN_ Power ON_ DLY [3:0]	1.5ms/03h	1.5ms/03h	1.5ms/03h	4bits	0000: 0ms, 0001: 0.5ms, …. 1110: 7.0ms, 1111: 7.5ms	0.5ms

GPIO4 Register Map

Address	Register	Default GPIO4 High	Default GPIO4 Floating	Default GPIO4 Low	EEPROM Bit	Range	Resolution
0x04h	DDR_SEL [6]	LPDDR4/ 01h	LPDDR4/ 01h	LPDDR4/ 01h	1bit	0 – DDR4 1 – LPDDR4	-
	B4_Mode [5]	Buck/00h	Buck/00h	Buck/00h	1bit	0 – Buck 4 operating in buck mode 1 – Buck 4 operating in LDO mode	-
	B4_VSET [4:0]	1.1V/04h	1.8V/12h	1.2V06h/	6bits	Buck 4 output range is 0.9V-2.0V	50mV
0x05h	LDO1_Mode [6]	LDO/00h	PLSW/01h	LDO/00h	1bit	00h: LDO Mode 01h: PLSW Mode	-
	LDO1_VSET [5:0]	1.8V/10h	1.8V/10h	1.8V/10h	6bits	LDO 1 output range is 1.0V-2.7V	50mV

Register Map

Address	Register	Default	EEPROM Bit	Range	Resolution
0x06h	LDO2_VSET [5:0]	1.8V/10h	6bits	LDO 2 output range is 1.0V-2.7V	50mV
0x07h	LDO2_CH_EN[5]	Enable/01h	1bit	0 – LDO 2 Disable 1 – LDO 2 Enable.	-
	LDO1_CH_EN[4]	Disable/00h	1bit	0 – LDO 1 Disable, 1 – LDO 1 Enable.	-
	Buck4_CH_EN[3]	Enable/01h	1bit	0 – Buck 4 Disable, 1 –Buck 4 Enable.	-
	Buck3_CH_EN[2]	Enable/01h	1bit	0 –Buck 3 Disable, 1 –Buck 3 Enable.	-
	Buck2_CH_EN[1]	Enable/01h	1bit	0 –Buck 2 Disable, 1 –Buck 2 Enable.	-
	Buck1_CH_EN[0]	Enable/01h	1bit	0 –Buck 1 Disable, 1 –Buck 1 Enable.	-
0x08h	B3_VID@SLEEP_ EN [7]	Enable/01h	1bit	0 – Buck 3 disable VID function; Buck 3 output keeps VSET0 when the IC enters Sleep mode 1 – Buck 3 enable VID function; Buck 3 output changes to VSET1 when the IC enters Sleep mode	-
	EXT_EN_SLEEP_ EN [6]	Stays on/00h	1bit	0 – EXT_EN stays on when the IC enters Sleep mode 1 – EXT_EN turns off when the IC enters Sleep mode	-
	LDO2_SLEEP_ EN [5]	Stays on/00h	1bit	0 – LDO 2 stays on when the IC enters Sleep mode 1 – LDO 2 turns off when the IC enters Sleep mode	-
	LDO1_SLEEP_ EN [4]	Stays on/00h	1bit	0 – LDO 1 stays on when the IC enters Sleep mode 1 – LDO 1 turns off when the IC enters Sleep mode	-
	Buck4_SLEEP_ EN [3]	Stays on/00h	1bit	0 – Buck 4 stays on when the IC enters Sleep mode 1 – Buck 4 turns off when the IC enters Sleep mode	-
	Buck3_SLEEP_ EN [2]	Stays on/00h	1bit	0 – Buck 3 stays on when the IC enters Sleep mode 1 – Buck 3 turns off when the IC enters Sleep mode	-
	Buck2_SLEEP_ EN [1]	Stays on/00h	1bit	0 – Buck 2 stays on when the IC enters Sleep mode 1 – Buck 2 turns off when the IC enters Sleep mode	-
	Buck1_SLEEP_ EN [0]	Stays on/00h	1bit	0 – Buck 1 stays on when the IC enters Sleep mode 1 – Buck 1 turns off when the IC enters Sleep mode	-

Address	Register	Default	EEPROM Bit	Range	Resolution
0x09h	EXT_EN_ DPSLP_EN [6]	Stays on/00h	1bit	0 – EXT_EN stays on when the device enters Deep Sleep mode 1 – EXT_EN turns off when the device enters Deep Sleep mode	-
	LDO2_ DPSLP_ EN [5]	Stays on/00h	1bit	0 – LDO 2 stays on when the device enters Deep Sleep mode 1 – LDO 2 turns off when the device enters Deep Sleep mode	-
	LDO1_ DPSLP_ EN [4]	Stays on/00h	1bit	0 – LDO 1 stays on when the device enters Deep Sleep mode 1 – LDO 1 turns off when the device enters Deep Sleep mode	-
	Buck4_ DPSLP_ EN [3]	Stays on/00h	1bit	0 – Buck 4 stays on when the device enters Deep Sleep mode 1 – Buck 4 turns off when the device enters Deep Sleep mode	-
	Buck3_ DPSLP_ EN [2]	Stays on/00h	1bit	0 – Buck 3 stays on when the device enters Deep Sleep mode 1 – Buck 3 turns off when the device enters Deep Sleep mode	-
	Buck2_ DPSLP_ EN [1]	Stays on/00h	1bit	0 – Buck 2 stays on when the device enters Deep Sleep mode 1 – Buck 2 turns off when the device enters Deep Sleep mode	-
	Buck1_ DPSLP_ EN [0]	Stays on/00h	1bit	0 – Buck 1 stays on when the device enters Deep Sleep mode 1 – Buck 1 turns off when the device enters Deep Sleep mode	-
0x0Ah	B4_PWM_EN [3]	LPM/00h	1bit	0 – Buck 4 enters LPM at light load 1 – Buck 4 forced into PWM at light load	-
	B3_PWM_EN [2]	LPM/00h	1bit	0 – Buck 3 enters LPM at light load 1 – Buck 3 forced into PWM at light load	-
	B2_PWM_EN [1]	LPM/00h	1bit	0 – Buck 2 enters LPM at light load 1 – Buck 2 forced into PWM at light load	-
	B1_PWM_EN [0]	LPM/00h	1bit	0 – Buck 1 enters LPM at light load 1 – Buck 1 forced into PWM at light load	-
0x0Bh	LDO2_SST [5]	200μs/00h	1bit	0 – LDO 2 SST = 200μs 1 – LDO 2 SST = 360μs	160μs
	LDO1_SST [4]	200μs/00h	1bit	0 – LDO 1 SST = 200μs 1 – LDO 1 SST = 360μs	160μs
	B4_SST [3]	250μs/00h	1bit	0 – Buck 4 SST = 250μs 1 – Buck 4 SST = 500μs	250μs
	B3_SST [2]	250μs/00h	1bit	0 – Buck 3 SST = 250μs 1 – Buck 3 SST = 500μs	250μs
	B2_SST [1]	250μs/00h	1bit	0 – Buck 2 SST = 250μs 1 – Buck 2 SST = 500μs	250μs
	B1_SST [0]	250μs/00h	1bit	0 – Buck 1 SST = 250μs 1 – Buck 1 SST = 500μs	250μs

Address	Register	Default	EEPROM Bit	Range	Resolution
0x0Ch	Buck1_Power OFF_ DLY [7:6]	0ms/00h	2bits	00: 0ms, 01: 0.25ms, 10: 0.5ms, 11: 1.0ms	-
	Buck2_Power OFF_ DLY [5:4]	0ms/00h	2bits	00: 0ms, 01: 0.25ms, 10: 0.5ms, 11: 1.0ms	-
	Buck3_Power OFF_ DLY [3:2]	0ms/00h	2bits	00: 0ms, 01: 0.25ms, 10: 0.5ms, 11: 1.0ms	-
	Buck4_Power OFF_ DLY [1:0]	0ms/00h	2bits	00: 0ms, 01: 0.25ms, 10: 0.5ms, 11: 1.0ms	-
0x0Dh	LDO1_ Power OFF_ DLY [7:6]	0ms/00h	2bits	00: 0ms, 01: 0.25ms, 10: 0.5ms, 11: 1.0ms	-
	LDO2_Power OFF_ DLY [5:4]	0ms/00h	2bits	00: 0ms, 01: 0.25ms, 10: 0.5ms, 11: 1.0ms	-
	EXT _EN _Power OFF_ DLY [3:2]	0ms/00h	2bits	00: 0ms, 01: 0.25ms, 10: 0.5ms, 11: 1.0ms	-
	nRESET_ Power OFF_ DLY [1:0]	0ms/00h	2bits	00: 0ms, 01: 0.25ms, 10: 0.5ms, 11: 1.0ms	-
0x0Eh	Buck1Wake Up_ DLY [7:6]	0ms/00h	2bits	00: 0ms, 01: 0.5ms, 10: 1.0ms, 11: 1.5ms	0.5ms
	Buck2_Wake Up_ DLY [5:4]	1ms/02h	2bits	00: 0ms, 01: 0.5ms, 10: 1.0ms, 11: 1.5ms	0.5ms
	Buck3_Wake Up_ DLY [3:2]	0ms/00h	2bits	00: 0ms, 01: 0.5ms, 10: 1.0ms, 11: 1.5ms	0.5ms
	Buck4_Wake Up_ DLY [1:0]	0ms/00h	2bits	00: 0ms, 01: 0.5ms, 10: 1.0ms, 11: 1.5ms	0.5ms
0x0Fh	LDO1_Wake Up_ DLY [5:4]	0ms/00h	2bits	00: 0ms, 01: 0.5ms, 10: 1.0ms, 11: 1.5ms	0.5ms
	LDO2_Wake Up_ DLY [3:2]	0ms/00h	2bits	00: 0ms, 01: 0.5ms, 10: 1.0ms, 11: 1.5ms	0.5ms
	EXT_EN_ Wake Up_ DLY [1:0]	0ms/00h	2bits	00: 0ms, 01: 0.5ms, 10: 1.0ms, 11: 1.5ms	0.5ms
0x10h	DIS_OVUV [7]	Enable/00h	1bit	0 – Enable hiccup mode or OVUVFLT state in ACTIVE mode 1 – Disable hiccup mode or OVUVFLT state in ACTIVE mode	-
	DIS_OTP [6]	Enable/00h	1bit	0 – Enable OTP 1 – Disable OTP	-
	DIS_VINOVP [5]	Enable/00h	1bit	0 – Enable VINOVP 1 – Disable VINOVP	-
	SLEEP_EN [1]	Enable/01h	1bit	0 – SLEEP mode is disabled 1 – SLEEP mode is enabled	-
	DPSLP_EN [0]	Enable/01h	1bit	0 – DPSLP mode is disabled 1 – DPSLP mode is enabled	-

Address	Register	Default	EEPROM Bit	Range	Resolution
0x15h	GPIO5 Function [7:6]	DPSLP/00h	2bits	00: DPSLP Input 01: I²C-controlled output 10: nIRQ(SYSWARN) output	-
	GPIO7 Function [5:4]	I²C IO/01h	2bits	00: EXT_EN Output. 01: I²C-controlled output 10: PWRDIS input	-
	GPIO6 Lock [2]	Lock/01h	1bit	0-GPIO6 status not locked and LDO 2 mode can be changed when GPIO6 status changes after power-on (not recommended due to triggering protection). 1-GPIO6 status lock and LDO mode will not change with GPIO6 status after power on.	-
	GPIO5 Open drain [1]	Turn off/00h	1bit	0 – Open-drain turn-off 1 – Open-drain turn-on	-
	GPIO7 Open drain [0]	Turn off/00h	1bit	0 – Open-drain turn-off 1 – Open-drain turn-on	-
0x34h	Vendor ID [4]	01h	1bit	01h	-
	CMI Version [3:0]	01h	4bits	01h	-

Fault Flag

Address	Register	Default	EEPROM Bit	Range	Resolution
0x16h	TSP [7]	Normal/00h	1bit	Thermal shutdown protection indicator 0: Normal (default) 1: Fault	-
	VIN_OVP [6]	Normal/00h	1bit	Input overvoltage protection indicator 0: Normal (default) 1: Fault	-
	LDO2_OVP [5]	Normal/00h	1bit	LDO 2 overvoltage protection indicator 0: Normal (default) 1: Fault	-
	LDO1_OVP [4]	Normal/00h	1bit	LDO 1 overvoltage protection indicator 0: Normal (default) 1: Fault	-
	Buck4_OVP [3]	Normal/00h	1bit	Buck 4 overvoltage protection indicator 0: Normal (default) 1: Fault	-
	Buck3_OVP [2]	Normal/00h	1bit	Buck 3 overvoltage protection indicator 0: Normal (default) 1: Fault	-
	Buck2_OVP [1]	Normal/00h	1bit	Buck 2 overvoltage protection indicator 0: Normal (default) 1: Fault	-
	Buck1_OVP [0]	Normal/00h	1bit	Buck 1 overvoltage protection indicator 0: Normal (default) 1: Fault	-
0x17h	SYSWARN [6]	Normal/00h	1bit	SYSWARN indicator 0: Normal (default) 1: Fault	-
	LDO2_UVP(SCP) [5]	Normal/00h	1bit	LDO 2 overload protection indicator 0: Normal (default) 1: Fault	-
	LDO1_UVP(SCP) [4]	Normal/00h	1bit	LDO 1 overload protection indicator 0: Normal (default)	-

				1: Fault	
	Buck4_UVP(SCP) [3]	Normal/00h	1bit	Buck 4 overload protection indicator 0: Normal (default) 1: Fault	-
	Buck3_UVP(SCP) [2]	Normal/00h	1bit	Buck 3 overload protection indicator 0: Normal (default) 1: Fault	-
	Buck2_UVP(SCP) [1]	Normal/00h	1bit	Buck 2 overload protection indicator 0: Normal (default) 1: Fault	-
	Buck1_UVP(SCP) [0]	Normal/00h	1bit	Buck 1 overload protection indicator 0: Normal (default) 1: Fault	-

Register Settings

Buck 1 Output Voltage Adjustment
Address – 0x00h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	B1_Mode	B1_VSET					
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck 1 Operating Mode B1 Mode [6]

Code	Buck 1 mode
00h	Buck 1 operating in buck mode
01h	Buck 1 operating in PLSW mode

Set Buck 1 Output Voltage VSET [5:0]
The output voltage is equal to B1_VSET × 0.025 + 1.6V.

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
00h	1.6V	10h	2V	20h	2.4V	30h	2.8V
01h	1.625V	11h	2.025V	21h	2.425V	31h	2.825V
02h	1.65V	12h	2.05V	22h	2.45V	32h	2.85V
03h	1.675V	13h	2.075V	23h	2.475V	33h	2.875V
04h	1.7V	14h	2.1V	24h	2.5V	34h	2.9V
05h	1.725V	15h	2.125V	25h	2.525V	35h	2.925V
06h	1.75V	16h	2.15V	26h	2.55V	36h	2.95V
07h	1.775V	17h	2.175V	27h	2.575V	37h	2.975V
08h	1.8V	18h	2.2V	28h	2.6V	38h	3V
09h	1.825V	19h	2.225V	29h	2.625V	-	-
0Ah	1.85V	1Ah	2.25V	2Ah	2.65V	-	-
0Bh	1.875V	1Bh	2.275V	2Bh	2.675V	-	-
0Ch	1.9V	1Ch	2.3V	2Ch	2.7V	-	-
0Dh	1.925V	1Dh	2.325V	2Dh	2.725V	-	-
0Eh	1.95V	1Eh	2.35V	2Eh	2.75V	-	-
0Fh	1.975V	1Fh	2.375V	2Fh	2.775V	-	-

Buck 2 Output Voltage Adjustment
Address – 0x01h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	B2_VSET						
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

The output voltage is equal to B2_VSET × 0.01 + 0.9V

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
00h	0.9V	17h	1.13V	2Eh	1.36V	45h	1.59V	5Ch	1.82V
01h	0.91V	18h	1.14V	2Fh	1.37V	46h	1.6V	5Dh	1.83V
02h	0.92V	19h	1.15V	30h	1.38V	47h	1.61V	5Eh	1.84V
03h	0.93V	1Ah	1.16V	31h	1.39V	48h	1.62V	5Fh	1.85V
04h	0.94V	1Bh	1.17V	32h	1.4V	49h	1.63V	60h	1.86V
05h	0.95V	1Ch	1.18V	33h	1.41V	4Ah	1.64V	61h	1.87V
06h	0.96V	1Dh	1.19V	34h	1.42V	4Bh	1.65V	62h	1.88V
07h	0.97V	1Eh	1.2V	35h	1.43V	4Ch	1.66V	63h	1.89V
08h	0.98V	1Fh	1.21V	36h	1.44V	4Dh	1.67V	64h	1.9V
09h	0.99V	20h	1.22V	37h	1.45V	4Eh	1.68V	65h	1.91V
0Ah	1V	21h	1.23V	38h	1.46V	4Fh	1.69V	66h	1.92V
0Bh	1.01V	22h	1.24V	39h	1.47V	50h	1.7V	67h	1.93V
0Ch	1.02V	23h	1.25V	3Ah	1.48V	51h	1.71V	68h	1.94V
0Dh	1.03V	24h	1.26V	3Bh	1.49V	52h	1.72V	69h	1.95V
0Eh	1.04V	25h	1.27V	3Ch	1.5V	53h	1.73V	6Ah	1.96V
0Fh	1.05V	26h	1.28V	3Dh	1.51V	54h	1.74V	6Bh	1.97V
10h	1.06V	27h	1.29V	3Eh	1.52V	55h	1.75V	6Ch	1.98V
11h	1.07V	28h	1.3V	3Fh	1.53V	56h	1.76V	6Dh	1.99V
12h	1.08V	29h	1.31V	40h	1.54V	57h	1.77V	6Eh	2V
13h	1.09V	2Ah	1.32V	41h	1.55V	58h	1.78V		
14h	1.1V	2Bh	1.33V	42h	1.56V	59h	1.79V		
15h	1.11V	2Ch	1.34V	43h	1.57V	5Ah	1.8V		
16h	1.12V	2Dh	1.35V	44h	1.58V	5Bh	1.81V		

Buck 3 Output Voltage Adjustment
Address – 0x02h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	B3_VSET0						
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

The output voltage is equal to B3_VSET × 0.01 + 0.5V

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
00h	0.50V	14h	0.70V	28h	0.90V	3Ch	1.10V
01h	0.51V	15h	0.71V	29h	0.91V	3Dh	1.11V
02h	0.52V	16h	0.72V	2Ah	0.92V	3Eh	1.12V
03h	0.53V	17h	0.73V	2Bh	0.93V	3Fh	1.13V
04h	0.54V	18h	0.74V	2Ch	0.94V	40h	1.14V
05h	0.55V	19h	0.75V	2Dh	0.95V	41h	1.15V
06h	0.56V	1Ah	0.76V	2Eh	0.96V	42h	1.16V
07h	0.57V	1Bh	0.77V	2Fh	0.97V	43h	1.17V
08h	0.58V	1Ch	0.78V	30h	0.98V	44h	1.18V
09h	0.59V	1Dh	0.79V	31h	0.99V	45h	1.19V
0Ah	0.60V	1Eh	0.80V	32h	1.00V	46h	1.20V
0Bh	0.61V	1Fh	0.81V	33h	1.01V		
0Ch	0.62V	20h	0.82V	34h	1.02V		
0Dh	0.63V	21h	0.83V	35h	1.03V		
0Eh	0.64V	22h	0.84V	36h	1.04V		
0Fh	0.65V	23h	0.85V	37h	1.05V		
10h	0.66V	24h	0.86V	38h	1.06V		
11h	0.67V	25h	0.87V	39h	1.07V		
12h	0.68V	26h	0.88V	3Ah	1.08V		
13h	0.69V	27h	0.89V	3Bh	1.09V		

Buck 3 Output Voltage Adjustment

Address – 0x03h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	B3_VSET1						
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

The output voltage is equal to B3_VSET × 0.01 + 0.5V

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
00h	0.50V	15h	0.71V	2Ah	0.92V	3Fh	1.13V
01h	0.51V	16h	0.72V	2Bh	0.93V	40h	1.14V
02h	0.52V	17h	0.73V	2Ch	0.94V	41h	1.15V
03h	0.53V	18h	0.74V	2Dh	0.95V	42h	1.16V
04h	0.54V	19h	0.75V	2Eh	0.96V	43h	1.17V
05h	0.55V	1Ah	0.76V	2Fh	0.97V	44h	1.18V
06h	0.56V	1Bh	0.77V	30h	0.98V	45h	1.19V
07h	0.57V	1Ch	0.78V	31h	0.99V	46h	1.20V
08h	0.58V	1Dh	0.79V	32h	1.00V		
09h	0.59V	1Eh	0.80V	33h	1.01V		
0Ah	0.60V	1Fh	0.81V	34h	1.02V		
0Bh	0.61V	20h	0.82V	35h	1.03V		
0Ch	0.62V	21h	0.83V	36h	1.04V		
0Dh	0.63V	22h	0.84V	37h	1.05V		
0Eh	0.64V	23h	0.85V	38h	1.06V		
0Fh	0.65V	24h	0.86V	39h	1.07V		
10h	0.66V	25h	0.87V	3Ah	1.08V		
11h	0.67V	26h	0.88V	3Bh	1.09V		
12h	0.68V	27h	0.89V	3Ch	1.10V		
13h	0.69V	28h	0.90V	3Dh	1.11V		
14h	0.70V	29h	0.91V	3Eh	1.12V		

Buck 4 Output Voltage Adjustment
Address – 0x04h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	DDR_SEL	B4_Mode	B4_VSET				
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set DDR SEL [6]

Code	DDR_SEL
00h	DDR4
01h	LPDDR4

Set Buck 4 Operating Mode B4_Mode [5]

Code	Buck 4 mode
00h	Buck 4 operating in buck mode
01h	Buck 4 operating in LDO mode

Set Buck 4 Output Voltage VSET [4:0]
The output voltage is equal to B4_VSET × 0.05 + 0.9V

Code	Voltage	Code	Voltage	Code	Voltage
00h	0.90V	08h	1.30V	10h	1.70V
01h	0.95V	09h	1.35V	11h	1.75V
02h	1.00V	0Ah	1.40V	12h	1.80V
03h	1.05V	0Bh	1.45V	13h	1.85V
04h	1.10V	0Ch	1.50V	14h	1.90V
05h	1.15V	0Dh	1.55V	15h	1.95V
06h	1.20V	0Eh	1.60V	16h	2.00V
07h	1.25V	0Fh	1.65V	-	-

LDO 1 Output Voltage Adjustment
Address – 0x05h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	LDO1_Mode	LDO1_VSET					
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO 1 Mode [6]

Code	LDO 1 mode
00h	LDO 1 operating in LDO mode
01h	LDO 1 operating on PLSW mode

Set LDO Output Voltage VSET [5:0]
The output voltage is equal to LDO1_VSET × 0.05 + 1.0V

Code	Voltage	Code	Voltage	Code	Voltage
00h	1.00V	10h	1.80V	20h	2.60V
01h	1.05V	11h	1.85V	21h	2.65V
02h	1.10V	12h	1.90V	22h	2.70V
03h	1.15V	13h	1.95V	-	-
04h	1.20V	14h	2.00V	-	-
05h	1.25V	15h	2.05V	-	-
06h	1.30V	16h	2.10V	-	-
07h	1.35V	17h	2.15V	-	-
08h	1.40V	18h	2.20V	-	-
09h	1.45V	19h	2.25V	-	-
0Ah	1.50V	1Ah	2.30V	-	-
0Bh	1.55V	1Bh	2.35V	-	-
0Ch	1.60V	1Ch	2.40V	-	-
0Dh	1.65V	1Dh	2.45V	-	-
0Eh	1.70V	1Eh	2.50V	-	-
0Fh	1.75V	1Fh	2.55V	-	-

LDO 2 Output Voltage Adjustment
Address – 0x06h

DATA BIT	D7	D7	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	RFU	LDO2_VSET					
READ/WRITE	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO Output Voltage VSET [5:0]
The output voltage is equal to LDO2_VSET × 0.05 + 1.0V

Code	Voltage	Code	Voltage	Code	Voltage
00h	1.00V	10h	1.80V	20h	2.60V
01h	1.05V	11h	1.85V	21h	2.65V
02h	1.10V	12h	1.90V	22h	2.70V
03h	1.15V	13h	1.95V	-	-
04h	1.20V	14h	2.00V	-	-
05h	1.25V	15h	2.05V	-	-
06h	1.30V	16h	2.10V	-	-
07h	1.35V	17h	2.15V	-	-
08h	1.40V	18h	2.20V	-	-
09h	1.45V	19h	2.25V	-	-
0Ah	1.50V	1Ah	2.30V	-	-
0Bh	1.55V	1Bh	2.35V	-	-
0Ch	1.60V	1Ch	2.40V	-	-
0Dh	1.65V	1Dh	2.45V	-	-
0Eh	1.70V	1Eh	2.50V	-	-
0Fh	1.75V	1Fh	2.55V	-	-

Rail ON/OFF Adjustment
Address – 0x07h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	RFU	LDO2_CH_EN	LDO1_CH_EN	Buck4_CH_EN	Buck3_CH_EN	Buck2_CH_EN	Buck1_CH_EN
READ/WRITE	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO 2 Enable/Disable [5]

Code	LDO 2 ON/OFF
00h	LDO 2 disable
01h	LDO 2 enable

Set LDO 1 Enable/Disable [4]

Code	LDO 1 ON/OFF
00h	LDO 1 disable
01h	LDO 1 enable

Set Buck 4 Enable/Disable [3]

Code	Buck 4 ON/OFF
00h	Buck 4 disable
01h	Buck 4 enable

Set Buck 3 Enable/Disable [2]

Code	Buck 3 ON/OFF
00h	Buck 3 disable
01h	Buck 3 enable

Set Buck 2 Enable/Disable [1]

Code	Buck 2 ON/OFF
00h	Buck 2 disable
01h	Buck 2 enable

Set Buck 1 Enable/Disable [0]

Code	Buck 1 ON/OFF
00h	Buck 1 disable
01h	Buck 1 enable

Rail ON/OFF Adjustment in SLEEP Mode and Buck 3 VID Adjustment
Address – 0x08h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	B3_VID @SLEEP_ EN	EXT_EN_ SLEEP_EN	LDO2_ SLEEP_EN	LDO1_ SLEEP_EN	Buck4_ SLEEP_EN	Buck3_ SLEEP_EN	Buck2_ SLEEP_EN	Buck1_ SLEEP_EN
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck 3 VID ON/OFF in Sleep Mode [7]

Code	Buck 3 VID ON/OFF in Sleep mode
00h	Buck 3 disable VID function; Buck 3 output keeps VSET0 when the device enters sleep mode
01h	Buck 3 enable VID function; Buck 3 output changes to VSET1 when the device enters Sleep mode

Set EXT_EN ON/OFF in Sleep Mode [6]

Code	EXT_EN ON/OFF in Sleep mode
00h	EXT_EN stays on when the device enters Sleep mode
01h	EXT_EN turns off when the device enters Sleep mode

Set LDO 2 ON/OFF in Sleep Mode [5]

Code	LDO 2 ON/OFF in Sleep mode
00h	LDO 2 stays on when the device enters Sleep mode
01h	LDO 2 turns off when the device enters Sleep mode

Set LDO 1 ON/OFF in Sleep Mode [4]

Code	LDO 1 ON/OFF in Sleep mode
00h	LDO 1 stays on when the device enters Sleep mode
01h	LDO 1 turns off when the device enters Sleep mode

Set Buck 4 ON/OFF in Sleep Mode [3]

Code	Buck 4 ON/OFF in Sleep mode
00h	Buck 4 stays on when the device enters Sleep mode
01h	Buck 4 turns off when the device enters Sleep mode

Set Buck 3 ON/OFF in Sleep Mode [2]

Code	Buck 3 ON/OFF in Sleep mode
00h	Buck 3 stays on when the device enters Sleep mode
01h	Buck 3 turns off when the device enters Sleep mode

Set Buck 2 ON/OFF in Sleep Mode [1]

Code	Buck 2 ON/OFF in Sleep mode
00h	Buck 2 stays on when the device enters Sleep mode
01h	Buck 2 turns off when the device enters Sleep mode

Set Buck 1 ON/OFF in Sleep Mode [0]

Code	Buck 1 ON/OFF in Sleep mode
00h	Buck 1 stays on when the device enters Sleep mode
01h	Buck 1 turns off when the device enters Sleep mode

Rail ON/OFF Adjustment in DPSLP Mode
Address – 0x09h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	EXT_EN_ DPSLP_EN	LDO2_ DPSLP_EN	LDO1_ DPSLP_EN	Buck4_ DPSLP_EN	Buck3_ DPSLP_EN	Buck2_ DPSLP_EN	Buck1_ DPSLP_EN
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set EXT_EN ON/OFF in Deep Sleep Mode [6]

Code	EXT_EN ON/OFF in Deep Sleep mode
00h	EXT_EN stays on when the device enters Deep Sleep mode
01h	EXT_EN turns off when the device enters Deep Sleep mode

Set LDO 2 ON/OFF in Deep Sleep Mode [5]

Code	LDO 2 ON/OFF in Deep Sleep mode
00h	LDO 2 stays on when the device enters Deep Sleep mode
01h	LDO 2 turns off when the device enters Deep Sleep mode

Set LDO 1 ON/OFF in Deep Sleep Mode [4]

Code	LDO 1 ON/OFF in Deep Sleep Mode
00h	LDO 1 stays on when the device enters Deep Sleep mode
01h	LDO 1 turns off when the device enters Deep Sleep mode

Set Buck 4 ON/OFF in Deep Sleep Mode [3]

Code	Buck 4 ON/OFF in Deep Sleep mode
00h	Buck 4 stays on when the device enters Deep Sleep mode
01h	Buck 4 turns off when the device enters Deep Sleep mode

Set Buck 3 ON/OFF in Deep Sleep Mode [2]

Code	Buck 3 ON/OFF in Deep Sleep mode
00h	Buck 3 stays on when the device enters Deep Sleep mode
01h	Buck 3 turns off when the device enters Deep Sleep mode

Set Buck 2 ON/OFF in Deep Sleep Mode [1]

Code	Buck 2 ON/OFF in Deep Sleep mode
00h	Buck 2 stays on when the device enters Deep Sleep mode
01h	Buck 2 turns off when the device enters Deep Sleep mode

Set Buck 1 ON/OFF in Deep Sleep Mode [0]

Code	Buck 1 ON/OFF in Sleep mode
00h	Buck 1 stays on when the device enters Deep Sleep mode
01h	Buck 1 turns off when the device enters Deep Sleep mode

PWM ON/OFF
Address – 0x0Ah

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	RFU	RFU	RFU	B4_PWM_EN	B3_PWM_EN	B2_PWM_EN	B1_PWM_EN
READ/WRITE	R	R	R	R	R/W	R/W	R/W	R/W

Description

Set Buck 4 LPM/FCCM [3]

Code	Buck 4 LPM/FCCM selection
00h	Buck 4 enters LPM at light load
01h	Buck 4 forced into PWM at light load

Set Buck 3 PM/FCCM [2]

Code	Buck 3 LPM/FCCM selection
00h	Buck 3 enters LPM at light load
01h	Buck 3 forced into PWM at light load

Set Buck 2 PM/FCCM [1]

Code	Buck 2 LPM/FCCM selection
00h	Buck 2 enters LPM at light load
01h	Buck 2 forced into PWM at light load

Set Buck 1 LPM/FCCM [0]

Code	Buck 1 LPM/FCCM selection
00h	Buck 1 enters LPM at light load
01h	Buck 1 forced into PWM at light load

Rail SST Adjustment
Address – 0x0Bh

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	RFU	LDO2_SST	LDO1_SST	B4_SST	B3_SST	B2_SST	B1_SST
READ/WRITE	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO 2 Soft-Start Time [5]

Code	LDO 2 soft-start time
00h	200μs
01h	360μs

Set LDO 1 Soft-Start Time [4]

Code	LDO 1 soft-start time
00h	200μs
01h	360μs

Set Buck 4 Soft-Start Time [3]

Code	Buck 4 soft-start time
00h	250μs
01	500μs

Set Buck 3 Soft-Start Time [2]

Code	Buck 3 soft-start time
00h	250μs
01h	500μs

Set Buck 2 Soft-Start Time [1]

Code	Buck 2 soft-start time
00h	250μs
01h	500μs

Set Buck 1 Soft-Start Time [0]

Code	Buck 1 soft-start time
00h	250μs
01h	500μs

Rail Power off Delay Time Adjustment
Address – 0x0Ch

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Buck1_Power Off_ DLY		Buck2_Power Off_ DLY		Buck3_Power Off_ DLY		Buck4_Power Off_ DLY	
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck 1 Power-Off Delay Time [7:6]

Code	Buck 1 power-off delay time
00h	0ms
01h	0.25ms
02h	0.5ms
03h	1.0ms

Set Buck 2 Power-Off Delay Time [5:4]

Code	Buck 2 power-off delay time
00h	0ms
01h	0.25ms
02h	0.5ms
03h	1.0ms

Set Buck 3 Power-Off Delay Time [3:2]

Code	Buck 3 power-off delay time
00h	0ms
01h	0.25ms
02h	0.5ms
03h	1.0ms

Set Buck 4 Power-Off Delay Time [1:0]

Code	Buck 4 power-off delay time
00h	0ms
01h	0.25ms
02h	0.5ms
03h	1.0ms

Rail Power off Delay Time Adjustment
Address – 0x0Dh

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	LDO1_Power Off_ DLY		LDO2_Power Off_ DLY		EXT_EN_Power Off_ DLY		nRESET_Power Off_DLY	
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO 1 Power-Off Delay Time [7:6]

Code	LDO 1 power-off delay time
00h	0ms
01h	0.25ms
02h	0.5ms
03h	1.0ms

Set LDO 2 Power-Off Delay Time [5:4]

Code	LDO 2 power-off delay time
00h	0ms
01h	0.25ms
02h	0.5ms
03h	1.0ms

Set EXT_EN Power-Off Delay Time [3:2]

Code	EXT_EN Power-off delay time
00h	0ms
01h	0.25ms
02h	0.5ms
03h	1.0ms

Set nRESET Power-Off Delay Time [1:0]

Code	nRESET power-off delay time
00h	0ms
01h	0.25ms
02h	0.5ms
03h	1.0ms

Rail Wakeup Delay Time Adjustment
Address – 0x0Eh

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Buck1_Wake Up_ DLY		Buck2_Wake Up_ DLY		Buck3_Wake Up_ DLY		Buck4_Wake Up_ DLY	
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck 1 Wakeup Delay Time [7:6]

Code	Buck 1 wakeup delay time
00h	0ms
01h	0.5ms
02h	1.0ms
03h	1.5ms

Set Buck 2 Wakeup Delay Time [5:4]

Code	Buck 2 wakeup delay time
00h	0ms
01h	0.5ms
02h	1.0ms
03h	1.5ms

Set Buck 3 Wakeup Delay Time [3:2]

Code	Buck 3 wakeup delay time
00h	0ms
01h	0.5ms
02h	1.0ms
03h	1.5ms

Set Buck 4 Wakeup Delay Time [1:0]

Code	Buck 4 wakeup delay time
00h	0ms
01h	0.5ms
02h	1.0ms
03h	1.5ms

Rail Wake up Delay Time Adjustment
Address – 0x0Fh

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RFU	RFU	LDO1_Wake Up_ DLY		LDO2_Wake Up_ DLY		EXT_EN_Wake Up_DLY	
READ/WRITE	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO 1 Wakeup Delay Time [5:4]

Code	LDO 1 wakeup delay time
00h	0ms
01h	0.5ms
02h	1.0ms
03h	1.5ms

Set LDO 2 Wakeup Delay Time [3:2]

Code	LDO 2 wakeup delay time
00h	0ms
01h	0.5ms
02h	1.0ms
03h	1.5ms

Set EXT_EN Wakeup Delay Time [1:0]

Code	EXT_EN wakeup delay time
00h	0ms
01h	0.5ms
02h	1.0ms
03h	1.5ms

Protection On/Off, and SLEEP/DPSLP Adjustment
Address – 0x10h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	DIS_OVUV	DIS_OTP	DIS_VINOVP	RFU	RFU	RFU	SLEEP_EN	DPSLP_EN
READ/WRITE	R/W	R/W	R/W	R	R	R	R/W	R/W

Description

Set OVUV Fault [7]

Code	OVUV Fault
00h	Enable hiccup mode or OVUVFLT state in ACTIVE Mode
01h	Disable hiccup mode or OVUVFLT state in AC-TIVE Mode

Set OTP [6]

Code	OTP
00h	Enable
01h	Disable

Set VINOVP [5]

Code	VIN_OVP
00h	Enable
01h	Disable

Set Sleep Mode EN [1]

Code	Sleep EN
00h	Sleep mode disable
01h	Sleep mode enable

Set Deep Sleep Mode EN [0]

Code	Deep Sleep EN
00h	Deep sleep mode disable
01h	Deep sleep mode enable

Power on Delay Time Adjustment
Address – 0x11h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	B1_Power ON_ DLY				B2_Power ON_ DLY			
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck 1 Power-On Delay Time [7:4]

Code	Buck 1 power-on delay time	Code	Buck 1 power-on delay time
00h	0ms	08h	4.0ms
01h	0.5ms	09h	4.5ms
02h	1.0ms	0Ah	5.0ms
03h	1.5ms	0Bh	5.5ms
04h	2.0ms	0Ch	6.0ms
05h	2.5ms	0Dh	6.5ms
06h	3.0ms	0Eh	7.0ms
07h	3.5ms	0Fh	7.5ms

Set Buck 2 Power-On Delay Time [3:0]

Code	Buck 2 power-on delay time	Code	Buck 2 power-on delay time
00h	0ms	08h	4.0ms
01h	0.5ms	09h	4.5ms
02h	1.0ms	0Ah	5.0ms
03h	1.5ms	0Bh	5.5ms
04h	2.0ms	0Ch	6.0ms
05h	2.5ms	0Dh	6.5ms
06h	3.0ms	0Eh	7.0ms
07h	3.5ms	0Fh	7.5ms

Power on Delay Time Adjustment

Address – 0x12h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	B3_Power ON_ DLY				B4_Power ON_ DLY			
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set Buck 3 Power-On Delay Time [7:4]

Code	Buck 3 power-on delay time	Code	Buck 3 power-on delay time
00h	0ms	08h	4.0ms
01h	0.5ms	09h	4.5ms
02h	1.0ms	0Ah	5.0ms
03h	1.5ms	0Bh	5.5ms
04h	2.0ms	0Ch	6.0ms
05h	2.5ms	0Dh	6.5ms
06h	3.0ms	0Eh	7.0ms
07h	3.5ms	0Fh	7.5ms

Set Buck 4 Power-On Delay Time [3:0]

Code	Buck 4 power-on delay time	Code	Buck 4 power-on delay time
00h	0ms	08h	4.0ms
01h	0.5ms	09h	4.5ms
02h	1.0ms	0Ah	5.0ms
03h	1.5ms	0Bh	5.5ms
04h	2.0ms	0Ch	6.0ms
05h	2.5ms	0Dh	6.5ms
06h	3.0ms	0Eh	7.0ms
07h	3.5ms	0Fh	7.5ms

Power on Delay Time Adjustment
Address – 0x13h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	LDO1_Power ON_ DLY				LDO2_Power ON_ DLY			
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set LDO 1 Power-On Delay Time [7:4]

Code	LDO 1 power-on delay time	Code	LDO 1 power-on delay time
00h	0ms	08h	4.0ms
01h	0.5ms	09h	4.5ms
02h	1.0ms	0Ah	5.0ms
03h	1.5ms	0Bh	5.5ms
04h	2.0ms	0Ch	6.0ms
05h	2.5ms	0Dh	6.5ms
06h	3.0ms	0Eh	7.0ms
07h	3.5ms	0Fh	7.5ms

Set LDO 2 Power-On Delay Time [3:0]

Code	LDO 2 power-on delay time	Code	LDO 2 power-on delay time
00h	0ms	08h	4.0ms
01h	0.5ms	09h	4.5ms
02h	1.0ms	0Ah	5.0ms
03h	1.5ms	0Bh	5.5ms
04h	2.0ms	0Ch	6.0ms
05h	2.5ms	0Dh	6.5ms
06h	3.0ms	0Eh	7.0ms
07h	3.5ms	0Fh	7.5ms

Power on Delay Time Adjustment
Address – 0x14h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	nRESET_ Input Trigger	nRESET_Power ON_ DLY			EXT_EN_Power ON_ DLY			
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Description

Set nRESET Input Trigger [7]

Code	nRESET input trigger
00h	Buck2_PG
01h	SYS_OK

Set nRESET Power-On Delay Time [6:4]

Code	nRESET power-on delay time
00h	0.5ms
01h	1ms
02h	2ms
03h	4ms
04h	8ms
05h	16ms

Set EXT_EN Power-On Delay Time [3:0]

Code	EXT_EN power-on delay time	Code	EXT_EN power-on delay time
00h	0ms	08h	4.0ms
01h	0.5ms	09h	4.5ms
02h	1.0ms	0Ah	5.0ms
03h	1.5ms	0Bh	5.5ms
04h	2.0ms	0Ch	6.0ms
05h	2.5ms	0Dh	6.5ms
06h	3.0ms	0Eh	7.0ms
07h	3.5ms	0Fh	7.5ms

GPIO5 and GPIO7 Adjustment
Address – 0x15h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	GPIO5 Function		GPIO7 Function		RFU	GPIO6 Lock	GPIO5 Open Drain	GPIO7 Open Drain
READ/WRITE	R/W	R/W	R/W	R/W	R	R	R/W	R/W

Description

Set GPIO5 Function [7:6]

Code	GPIO5 function
00h	DPSLP input
01h	I²C-controlled Output
02h	nIRQ(SYSWARN) Output

Set GPIO7 Function [5:4]

Code	GPIO7 function
00h	EXT_EN Output
01h	I²C-controlled Output
02h	PWRDIS input

Set GPIO6 Lock Function [2]

Code	GPIO6 lock function
00h	GPIO6 status not locked and LDO 2 mode can be changed when GPIO6 status changes after power-on (not recommended due to trigger protection).
01h	GPIO6 status locked and LDO mode will not change with GPIO6 status after power-on.

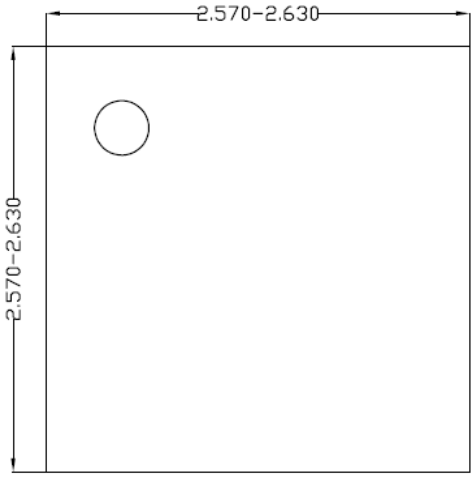
Set GPIO5 Open-Drain ON/OFF [1]

Code	GPIO5 open-drain ON/OFF
00h	Open-drain turn-off
01h	Open-drain turn-on

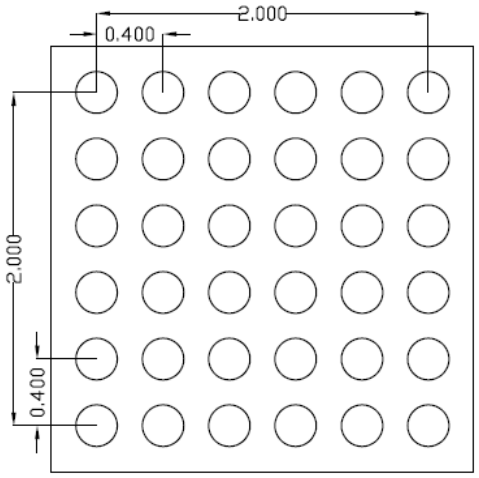
Set GPIO7 Open-Drain ON/OFF [0]

Code	GPIO7 open-drain ON/OFF
00h	Open-drain turn-off
01h	Open-drain turn-on

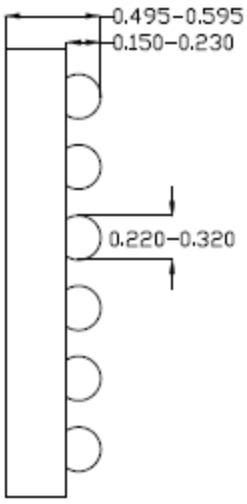
CSP2.6×2.6-36 Package Outline Drawing



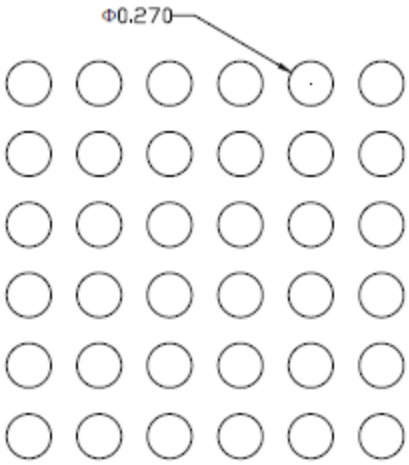
Top View



Bottom View



Side View

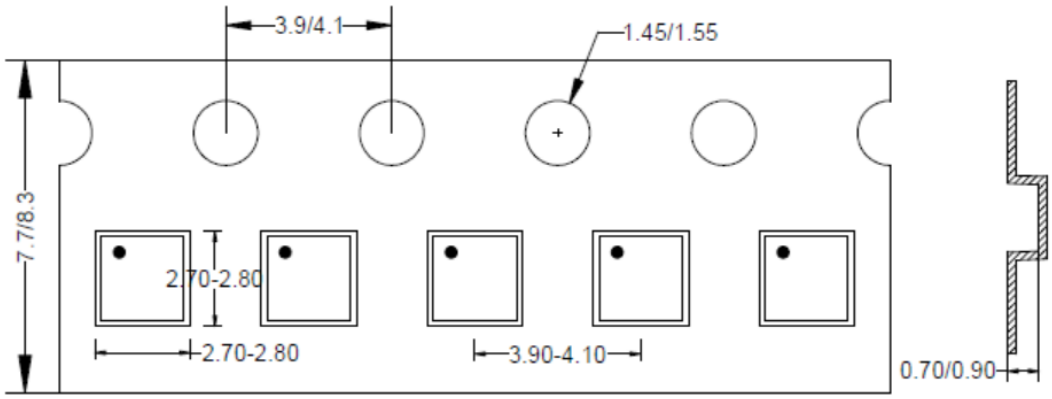


Recommended PCB Layout
(Reference only)

Notes: *All dimensions are in millimeters and exclude mold flash and metal burr.*

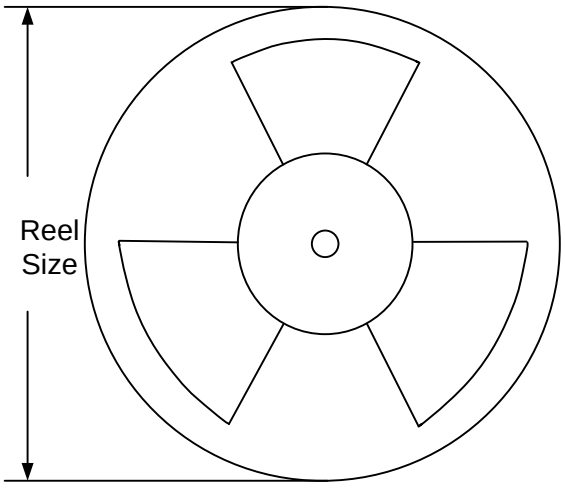
Tape and Reel Information

CSP2.6×2.6-36 Tape Dimensions and Pin 1 Orientation



Direction of feed ⟶

Reel Dimensions



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
CSP2.6×2.6-36	8	4	7"	400	400	3000

All dimensions are nominal.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
Apr.16, 2026	Revision 1.0	Initial release.	-

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