SSL2101

Dimmable GreenChip driver for LED lighting

Rev. 4.1 — 31 March 2016 Product data sheet

1. General description

The SSL2101 is a Switched Mode Power Supply (SMPS) driver IC that operates in combination with a phase cut dimmer directly from the rectified mains. It is designed to drive LED devices. The device includes a high-voltage power switch, a circuit to allow start-up directly from the rectified mains voltage and a high-voltage circuitry to supply the phase cut dimmer.

For dimmer applications, an integrated dedicated circuitry optimizes the dimming curve.

- SSL2101: fully integrated LED driver for lamps up to 10 W
- SSL2102: fully integrated LED driver for lamps up to 25 W
- SSL2103: gives the application designer flexibility to:
  - Use an external power switch to allow the IC to provide any power
  - Use external bleeder transistors to provide extended dimmer interoperability

2. Features and benefits

- Easy migration to existing lighting control infrastructure
- Supports most available dimming solutions
- Optimized efficiency with valley switching managed by a built-in circuitry
- Demagnetization detection
- OverTemperature Protection (OTP)
- Short-Winding Protection (SWP) and OverCurrent Protection (OCP)
- Internal V_{CC} generation allowing start-up from the rectified mains voltage
- Natural dimming curve by logarithmic correction, down to 1 %
- Limited external components required because of the high integration level
- Thermal enhanced SO16 wide body package
- Suitable for flyback and buck applications

3. Applications

- SSL applications below 15 W
- Retro-fit lamps (for example, GU10, E27)
- LED modules such as LED spots, down-lights
- LED strings suitable for retail displays, etc.

4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{DSon}	drain-source on-state resistance	power switch; I_{SOURCE} = –0.50 A				
		T_j = 25 °C	4.5	6.5	7.5	Ω
		I_{source} = –0.20 A				
		T_j = 125 °C	-	9.5	10	Ω
V_{CC}	supply voltage		8.5	-	40	V
f_{osc}	oscillator frequency		10	100	200	kHz
I_{DRAIN}	current on pin DRAIN	V_{DRAIN} > 60 V; no auxiliary supply	-	-	2.2	mA
		V_{DRAIN} > 60 V; with auxiliary supply	-	30	125	μA
V_{DRAIN}	voltage on pin DRAIN		40	-	600	V
δ_{min}	minimum duty factor		-	0	-	%
δ_{max}	maximum duty cycle	f = 100 kHz	-	75	-	%
T_{amb}	ambient temperature		–40	-	+100	°C

5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
SSL2101T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

6. Block diagram

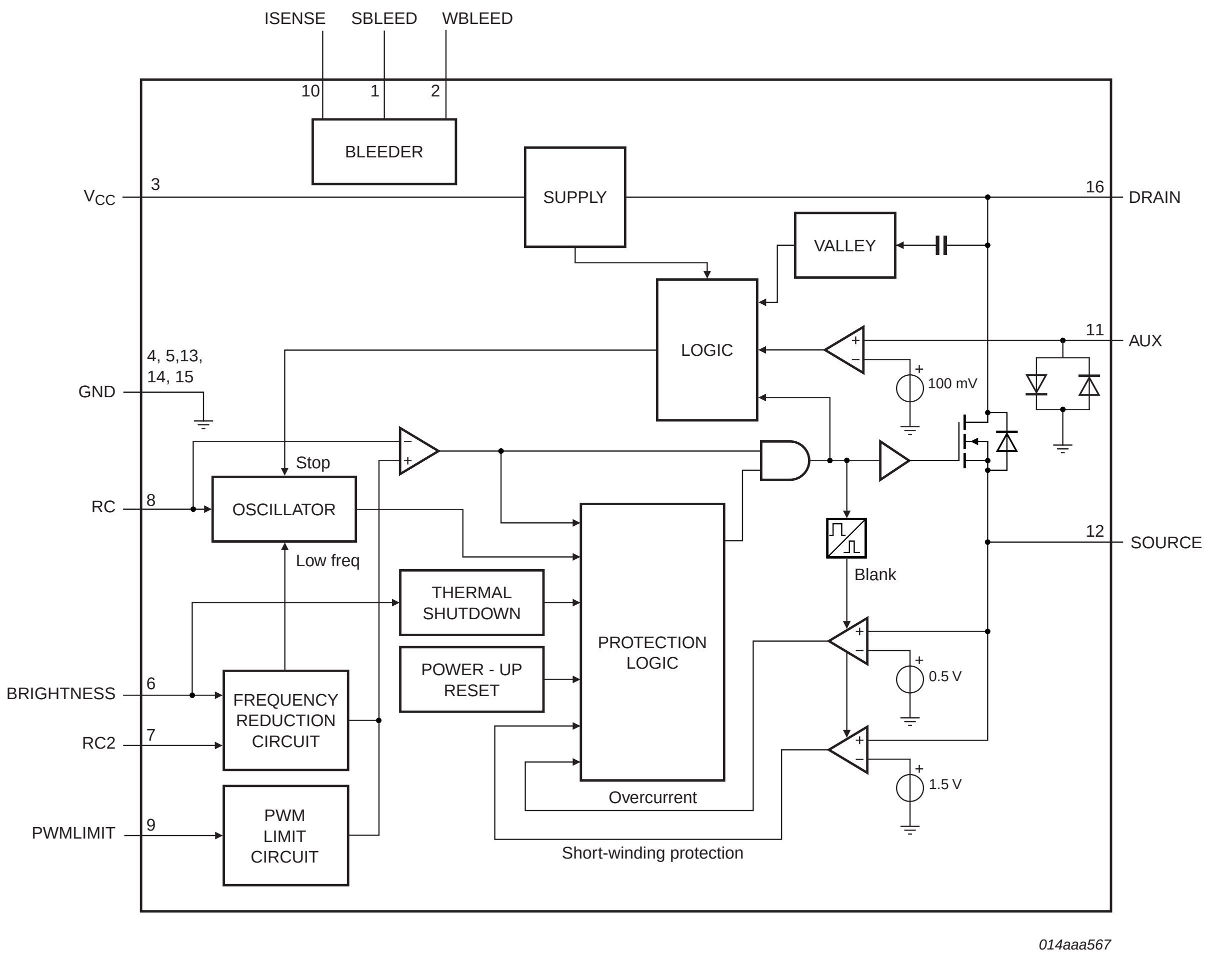


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

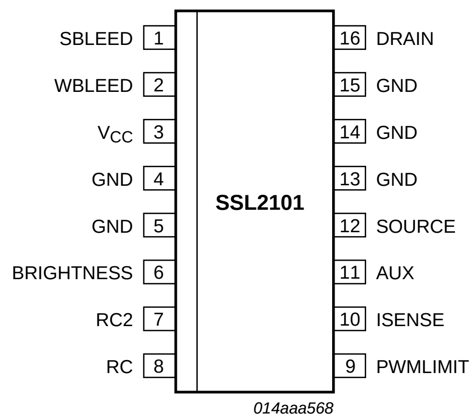


Fig 2. Pin configuration SO16

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
SBLEED	1	drain of internal strong bleeder switch
WBLEED	2	drain of internal weak bleeder switch
V_{CC}	3	supply voltage
GND	4	ground
GND	5	ground
BRIGHTNESS	6	brightness input
RC2	7	setting for frequency reduction
RC	8	frequency setting
PWMLIMIT	9	PWM limit input
ISENSE	10	current sense input for WBLEED
AUX	11	Input for voltage from auxiliary winding for timing (demagnetization)
SOURCE	12	source of internal power switch
GND	13	ground
GND	14	ground
GND	15	ground
DRAIN	16	drain of internal power switch; input for start-up current and valley sensing

8. Functional description

The SSL2101 is an LED driver IC that operates directly from the rectified mains.

The SSL2101 uses on-time mode control and frequency control to control the LED brightness. The BRIGHTNESS and PWMLIMIT input of the IC can be used to control the LED light output in combination with an external dimmer. The PWMLIMIT input can also be used for Thermal Lumen Management (TLM) and for precision LED current control.

8.1 Start-up and UnderVoltage LockOut (UVLO)

Initially, the IC is self-supplying from the rectified mains voltage. The IC starts switching as soon as the voltage on pin V_{CC} passes the $V_{CC(startup)}$ level. The supply can be taken over by the auxiliary winding of the transformer as soon as V_{CC} is high enough and the supply from the line is stopped for high efficiency operation. Alternatively the IC can be supplied via a bleeder resistor connected to a high voltage. Note however the maximum V_{CC} voltage rating of the IC.

If for some reason the auxiliary supply is not sufficient, the high-voltage supply can also supply the IC. As soon as the voltage on pin V_{CC} drops below the $V_{CC(UVLO)}$ level, the IC stops switching and will restart from the rectified mains voltage, if the internal current delivered is sufficient.

8.2 Oscillator

An internal oscillator inside the IC provides the timing for the switching converter logic.

The frequency of the oscillator is set by the external resistors and the capacitor on pin RC and pin RC2. The external capacitor is charged rapidly to the $V_{RC(max)}$ level and, starting from a new primary stroke, it discharges to the $V_{RC(min)}$ level. Because the discharge is exponential, the relative sensitivity of the duty factor to the regulation voltage at low duty factor is almost equal to the sensitivity at high duty factors. This results in a more constant gain over the duty factor range compared to Phase Width Modulated (PWM) systems with a linear sawtooth oscillator. Stable operation at low duty factors is easily realized. The frequency of the converter when $V_{BRIGHTNESS}$ is high can be estimated using Equation 1:

$$RC = \frac{1}{3.5} \cdot \left(\frac{1}{f_{osc}} - t_{charge} \right) \quad (1)$$

R equals the parallel resistance of both oscillator resistors. C is the capacitor connected at the RC pin (pin 8).

The BRIGHTNESS input controls the frequency reduction mode. Figure 3 shows that the oscillator switches over from an RC curve with R1 in parallel with R2 to R1 only. A low BRIGHTNESS voltage will reduce the switching frequency.

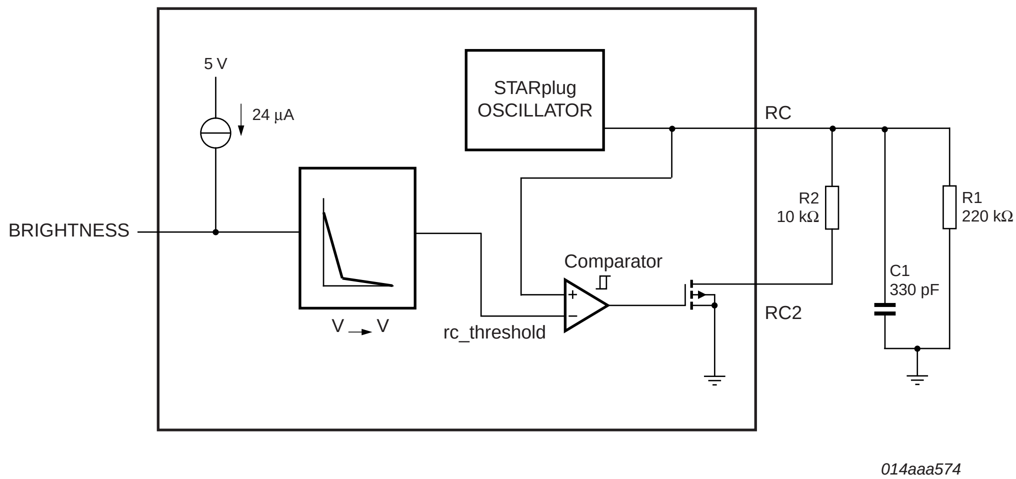


Fig 3. Brightness control block

A typical RC waveform is given in Figure 4. The RC switch-over threshold is controlled by the BRIGHTNESS pin.

To ensure that the capacitor can be charged within the charge time, the value of the oscillator capacitor should be limited to 1 nF. Due to leakage current, the value of the resistor connected between the RC pin and the ground should be limited to a maximum of 220 kΩ.

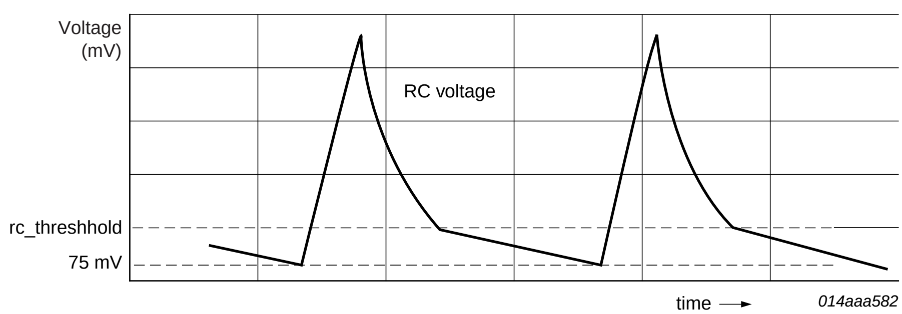


Fig 4. Brightness timing waveform

8.3 Duty factor control

The duty factor is controlled by an internally regulated voltage and the oscillator signal on pin RC. The internal regulation voltage is set by the voltage on the PWMLIMIT pin.

A low PWMLIMIT voltage will results in a low on-time for the internal power switch. The minimum duty factor of the switched mode power supply can be set to 0 %. The maximum duty factor is set to 75 %.

8.4 Bleeder for dimming applications

The SSL2101 IC contains some circuitry intended for mains dimmer compatibility. This circuit contains two current sinks that are called bleeders. A strong bleeder is used for zero-cross reset of the dimmer and triac latching. A weak bleeder is added to maintain the hold current through the dimmer.

The strong bleeder switch is switched on when the maximum voltage on pin WBLEED and SBLEED is below the $V_{th(SBLEED)}$ level (52 V typically). The weak bleeder switch is switched on as soon as the voltage on pin ISENSE exceeds the $V_{th(high)(ISENSE)}$ level (−100 mV typically). The weak bleeder switch is switched off when the ISENSE voltage drops below the $V_{th(low)(ISENSE)}$ level (−250 mV typically). The weak bleeder switch is also switched off when the strong bleeder switch is switched on. See Figure 5.

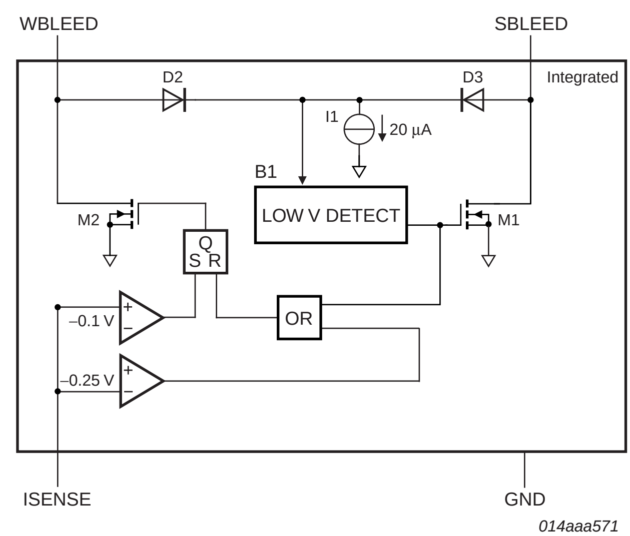


Fig 5. Bleeder circuit

8.5 Valley switching

A new cycle is started when the primary switch is switched on (see Figure 6). After a time determined by the oscillator voltage, RC and the internal regulation level, the switch is turned off and the secondary stroke starts. The internal regulation level is determined by the voltage on pin PWMLIMIT.

After the secondary stroke, the drain voltage shows an oscillation with a frequency of approximately:

$$\frac{1}{2 \times \pi \times \sqrt{(L_p \times C_p)}} \qquad (2)$$

where:

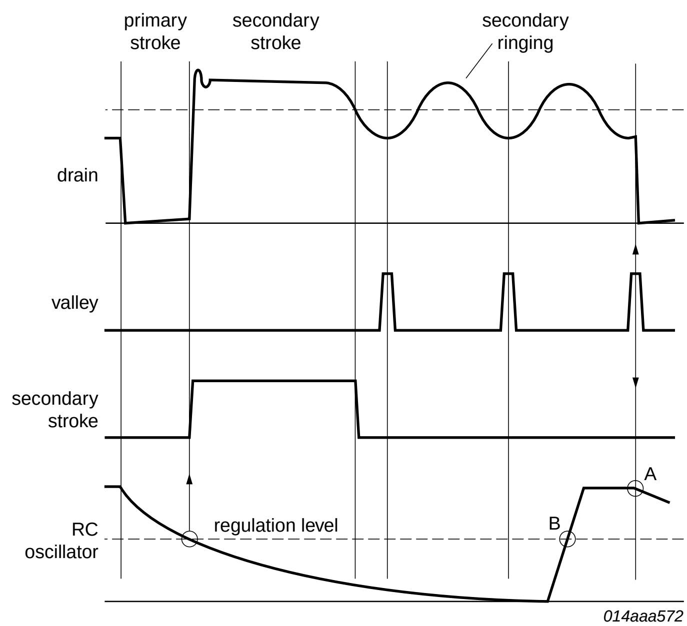
L_p = primary self inductance

C_p = parasitic capacitance on drain node

As soon as the oscillator voltage is high again and the secondary stroke has ended, the circuit waits for a low drain voltage before starting a new primary stroke.

Figure 6 shows the drain voltage together with the valley signal, the signal indicating the secondary stroke and the RC voltage.

The primary stroke starts some time before the actual valley at low ringing frequencies, and some time after the actual valley at high ringing frequencies.



A: Start of new cycle with valley switching.

B: Start of new cycle in a classical PWM system.

Fig 6. Signals for valley switching, flyback configuration

Figure 7 shows a typical curve for a reflected output voltage N at an output voltage of 80 V. This voltage is the output voltage transferred to the primary side of the transformer with the factor N (determined by the turns ratio of the transformer). It shows that the system switches exactly at minimum drain voltage for ringing frequencies of 480 kHz, thus reducing the switch-on losses to a minimum. At 200 kHz, the next primary stroke is started at 33° before the valley. The switch-on losses are still reduced significantly.

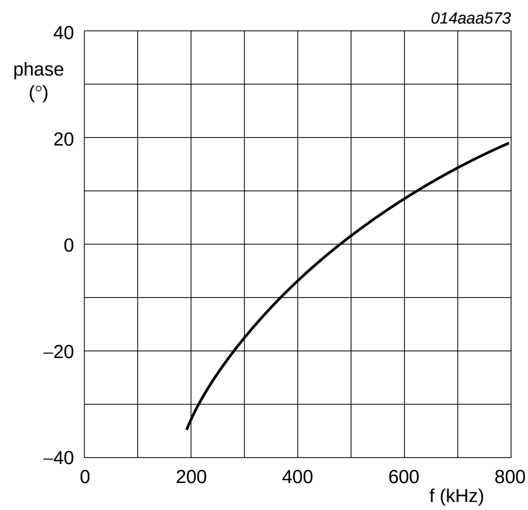


Fig 7. Typical phase of drain ringing at switch-on (at N × V_o = 80 V)

8.6 Demagnetization

The system operates in discontinuous conduction mode if the AUX pin is connected. As long as the secondary stroke has not ended, the oscillator will not start a new primary stroke. During the first $t_{sup(xfmr\_ring)}$ seconds, demagnetization recognition is suppressed. This suppression may be necessary in applications where the transformer has a large leakage inductance and at low output voltages.

8.7 Overcurrent protection

The cycle-by-cycle peak drain current limit circuit uses the external source resistor R_{SENSE} to measure the current. The circuit is activated after the leading edge blanking time t_{leb}. The protection circuit limits the source voltage over the R_{SENSE}[1] resistor to $V_{th(ocp)SOURCE}$, and thus limits the primary peak current.

8.8 Short-winding protection

The short-winding protection circuit is also activated after the leading edge blanking time. If the source voltage exceeds the short-winding protection threshold voltage $V_{th(swp)SOURCE}$, the IC stops switching. Only a power-on reset will restart normal operation. The short-winding protection also protects in case of a secondary diode short circuit.

8.9 Overtemperature protection

Accurate temperature protection is provided in the device. When the junction temperature exceeds the thermal shut-down temperature, the IC stops switching. During thermal protection, the IC current is lowered to the start-up current. The IC continues normal operation as soon as the overtemperature situation has disappeared.

1. R_{SENSE} is the resistor between the SOURCE pin and GND

9. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to ground; positive currents flow into the device; pins V_{CC} and RC cannot be current driven. Pins ISENSE and AUX cannot be voltage driven.

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{CC}	supply voltage	continuous	–0.4	+40	V
V_{RC}	voltage on pin RC		–0.4	+3	V
V_{RC2}	voltage on pin RC2		–0.4	+3	V
$V_{BRIGHTNESS}$	voltage on pin BRIGHTNESS		–0.4	+5	V
$V_{PWMLIMIT}$	voltage on pin PWMLIMIT		–0.4	+5	V
V_{SOURCE}	voltage on pin SOURCE		–0.4	+5	V
V_{DRAIN}	voltage on pin DRAIN	DMOS power transistor; T_{amb} = 25 °C	–0.4	+600	V
V_{SBLEED}	voltage on pin SBLEED	off-state; T_j = 125 °C	–0.4	+600	V
		on-state; V_{VCC} > 8.5 V; T_j < 125 °C	–0.4	+16	V
V_{WBLEED}	voltage on pin WBLEED	off-state; T_j < 125 °C	–0.4	+600	V
		on-state; V_{VCC} > 8.5 V; T_j < 125 °C	–0.4	+12	V
Currents					
I_{ISENSE}	current on pin ISENSE		–20	+5	mA
I_{AUX}	current on pin AUX		–10	+5	mA
I_{SOURCE}	current on pin SOURCE		–2	+2	A
I_{DRAIN}	current on pin DRAIN		–2	+2	A
General					
P_{tot}	total power dissipation	T_{amb} = 70 °C	-	1	W
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+100	°C
T_j	junction temperature		–40	+150	°C

Table 4: Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to ground; positive currents flow into the device; pins V_{CC} and RC cannot be current driven. Pins ISENSE and AUX cannot be voltage driven.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	human body model;	[1]			
		Pins 16, 1, 2		−1000	+1000	V
		All other pins		−2000	+2000	V
		machine model	[2]	−200	+200	V
		charged device model	[3]	−500	+500	V

[1] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] Machine model: equivalent to discharging a 200 pF capacitor through a 0.75 μH coil and a 10 Ω series resistor.

[3] Charged device model: equivalent to charging the IC up to 1 kV and the subsequent discharging of each pin down to 0 V over a 1 Ω resistor.

10. Thermal characteristics

The heat sink in the application with the SSL2101 is made with the copper on the Printed-Circuit Board (PCB). The SSL2101 uses thermal leads (pins 4, 5, 13, 14 and 15) for heat transfer from die to PCB.
Enhanced thermal lead connection may drastically reduce thermal resistance.
The following equation shows the relationship between the maximum allowable power dissipation P and the thermal resistance from junction to ambient.

$$R_{th(j-a)} = (T_{j(max)} - T_{amb})/P$$

Where:

$R_{th(j-a)}$ = thermal resistance from junction to ambient

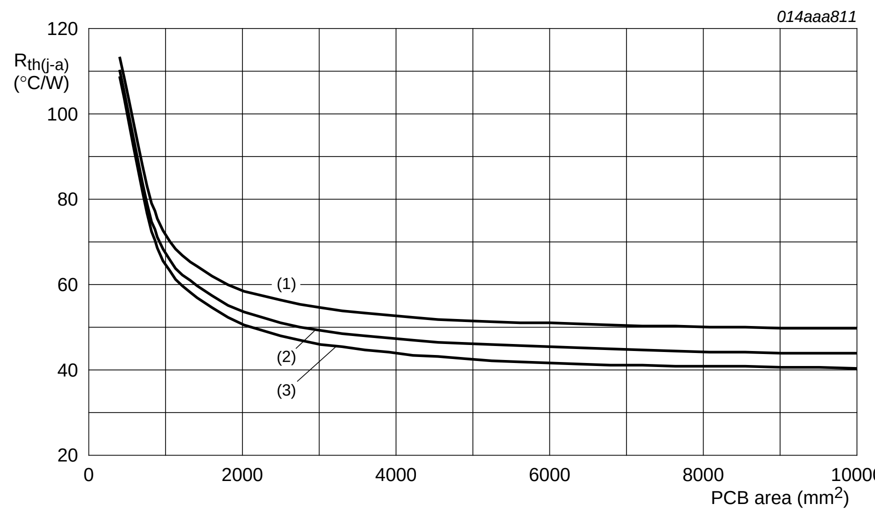
$T_{j(max)}$ = maximum junction temperature

T_{amb} = ambient temperature

P = power dissipation

The thermal resistance as a function of the PCB area (Board: 0.8 mm thickness, 2 layers, Bottom Cu coverage 90 %, Cu thickness 70 μm

(390 W/mK), Core material conductivity: 0.5 W/mK, 10 vias dia 0.3 mm) is shown in Figure 8



(1) Top Cu coverage 20 %

(2) Top Cu coverage 50 %

(3) Top Cu coverage 100 %

Fig 8. SSL2101 core material conductivity

Table 5: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1]	90	KW

[1] Measured on a JEDEC test board (standard EIA/JESD 51-3) in free air with natural convection.

11. Characteristics

Table 6: Characteristics

T_{amb} = 25 °C; no overtemperature; all voltages are measured with respect to ground; currents are positive when flowing into the IC and PWMLIMIT and BRIGHTNESS pins are disconnected unless otherwise specified. Typical frequency 100 kHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
I_{CC}	supply current	normal operation; V_{DRAIN} = 60 V; V_{CC} = 20 V	-	1.7	2	mA
$I_{CC(ch)}$	charge supply current	V_{DRAIN} > 60 V; V_{CC} = 0 V	-6	–4.5	-	mA
V_{CC}	supply voltage		8.5	-	40	V
$V_{CC(startup)}$	start-up supply voltage		9.75	10.25	10.75	V
$V_{CC(UVLO)}$	undervoltage lockout supply voltage	L	7.9	8.2	8.5	V

Table 6: Characteristics *…continued*

T_{amb} = 25 °C; no overtemperature; all voltages are measured with respect to ground; currents are positive when flowing into the IC and PWMLIMIT and BRIGHTNESS pins are disconnected unless otherwise specified. Typical frequency 100 kHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DRAIN}	current on pin DRAIN	V_{DRAIN} > 60 V; no auxiliary supply	-	-	2.2	mA
		V_{DRAIN} > 60 V; with auxiliary supply	-	30	125	μA
V_{DRAIN}	voltage on pin DRAIN		40	-	600	V
Pulse width modulator						
δ_{min}	minimum duty factor		-	0	-	%
δ_{max}	maximum duty cycle	f = 100 kHz	-	75	-	%
SOPS						
$V_{det(demag)}$	demagnetization detection voltage		50	100	150	mV
$t_{sup(xfmr\_ring)}$	transformer ringing suppression time	at start of secondary stroke	1.0	1.5	2.0	μs
RC oscillator						
$V_{RC(min)}$	minimum voltage on pin RC		60	75	90	mV
$V_{RC(max)}$	maximum voltage on pin RC		2.4	2.5	2.6	V
$t_{ch(RC)}$	charge time on pin RC		-	1	-	μs
$V_{BRIGHTNESS}$	voltage on pin BRIGHTNESS	2.5 V RC2 trip level	-	0.5	-	V
		180 mV RC2 trip level	-	1.25	-	V
		75 mV RC2 trip level	-	2.3	-	V
f_{osc}	oscillator frequency		10	100	200	kHz
$I_{BRIGHTNESS}$	current on pin BRIGHTNESS	$V_{BRIGHTNESS}$ = 0 V	−20	−24	−28	μA
Bleeder						
$V_{th(SBLEED)}$	threshold voltage on pin SBLEED		46	52	56	V
$V_{th(low)ISENSE}$	low threshold voltage on pin ISENSE		-	−250	-	mV
$V_{th(high)ISENSE}$	high threshold voltage on pin ISENSE		-	−100	-	mV
$R_{DSon(SBLEED)}$	drain-source on-state resistance on pin SBLEED	I_{SBLEED} = 25 mA				
		T_j = 25 °C	140	170	200	Ω
		T_j = 125 °C	220	270	320	Ω

Table 6: Characteristics *…continued*

T_{amb} = 25 °C; no overtemperature; all voltages are measured with respect to ground; currents are positive when flowing into the IC and PWMLIMIT and BRIGHTNESS pins are disconnected unless otherwise specified. Typical frequency 100 kHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{DSon(WBLEED)}$	drain-source on-state resistance on pin WBLEED	I_{WBLEED} = 10 mA					
		T_j = 25 °C		250	310	350	Ω
		T_j = 125 °C		400	500	600	Ω
Duty factor regulator: pin PWMLIMIT							
$I_{PWMLIMIT}$	current on pin PWMLIMIT			−25	-	−18	µA
$V_{PWMLIMIT}$	voltage on pin PWMLIMIT	maximum duty cycle = 3 V		-	3	-	V
		minimum duty factor threshold		-	0.45	-	V
Valley switching							
$(\Delta V/\Delta t)_{vrec}$	valley recognition voltage change with time	minimum absolute value	[1]	-	100	-	V/µs
f_{ring}	ringing frequency	$N \times V_O$ = 100 V		200	550	800	kHz
$t_{d(vrec-swon)}$	valley recognition to switch-on delay time			-	150	-	ns
Current and short circuit winding protection							
$V_{th(ocp)SOURCE}$	overcurrent protection threshold voltage on pin SOURCE	dV/dt = 0.1 V/µs		0.47	0.50	0.53	V
$V_{th(swp)SOURCE}$	short-winding protection threshold voltage on pin SOURCE	dV/dt = 0.1 V/µs		-	1.5	-	V
$t_{d(ocp-swoff)}$	delay time from overcurrent protection to switch-off	dV/dt = 0.5 V/µs		-	160	185	ns
t_{leb}	leading edge blanking time			250	350	450	ns
FET output stage							
$I_{L(DRAIN)}$	leakage current on pin DRAIN	V_{DRAIN} = 600 V		-	-	125	µA
$V_{BR(DRAIN)}$	breakdown voltage on pin DRAIN	T_{amb} = 25 °C		600	-	-	V
R_{DSon}	drain-source on-state resistance	power switch; I_{SOURCE} = −0.50 A					
		T_j = 25 °C		4.50	6.5	7.5	Ω
		I_{SOURCE} = −0.20 A					
		T_j = 125 °C		-	9.5	10	Ω

Table 6: Characteristics *…continued*

T_{amb} = 25 °C; no overtemperature; all voltages are measured with respect to ground; currents are positive when flowing into the IC and PWMLIMIT and BRIGHTNESS pins are disconnected unless otherwise specified. Typical frequency 100 kHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{f(DRAIN)}$	fall time on pin DRAIN	input voltage: 300 V; no external capacitor at drain	-	75	-	ns
Temperature protection						
T_{otp}	overtemperature protection trip	junction temperature	150	160	170	°C
$T_{otp(hys)}$	overtemperature protection trip hysteresis	junction temperature	-	2	-	°C

[1] Voltage change in time for valley recognition.

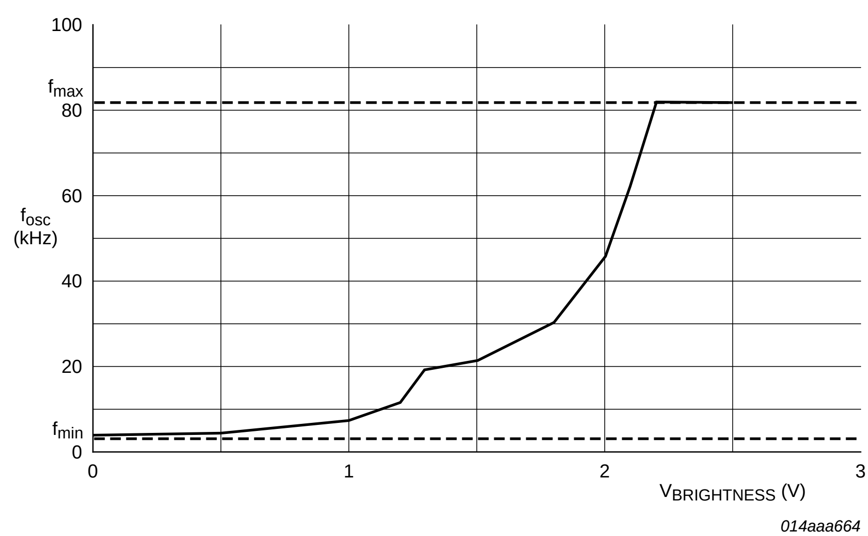
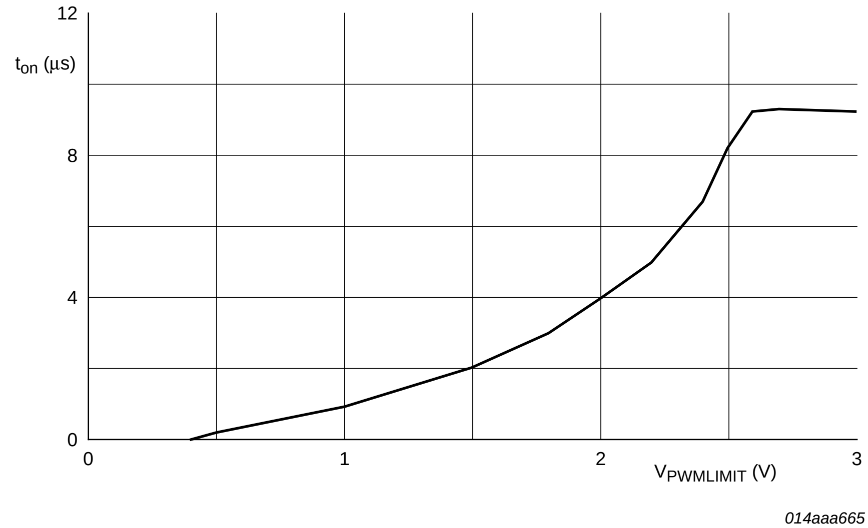
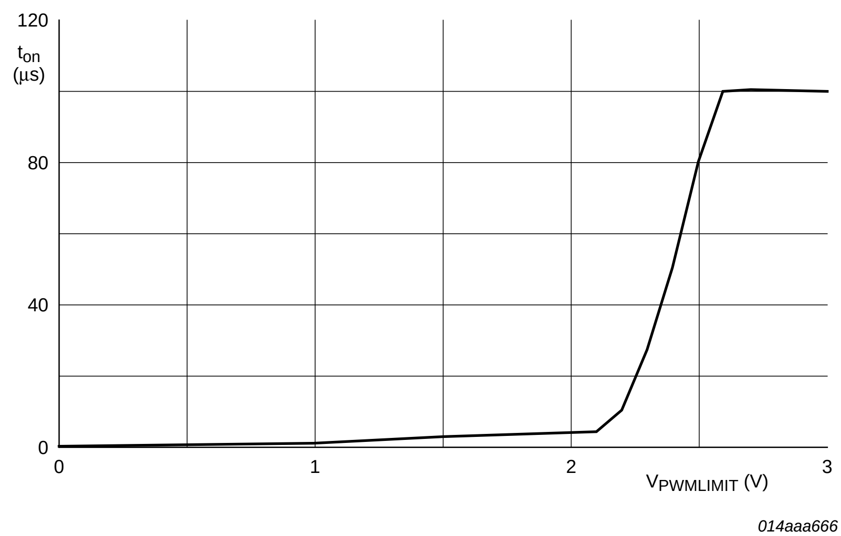


Fig 9. Typical frequency as a function of voltage on pin BRIGHTNESS



$V_{BRIGHTNESS}$ = 3 V

Fig 10. Turn-on time as a function of voltage on pin PWMLIMIT



$V_{BRIGHTNESS}$ = 1 V

Fig 11. Turn-on time as a function of voltage on pin PWMLIMIT

12. Application information

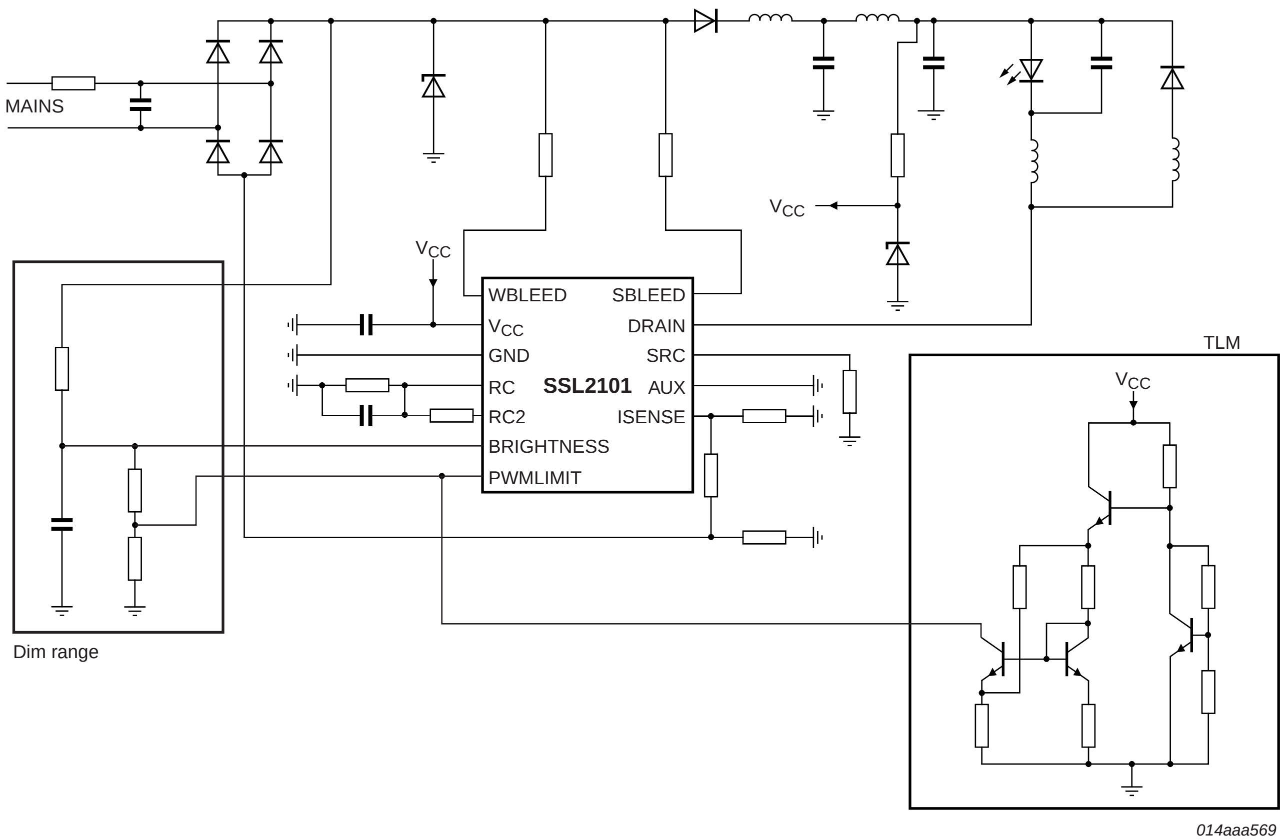


Fig 12. Buck configuration for SSL2101

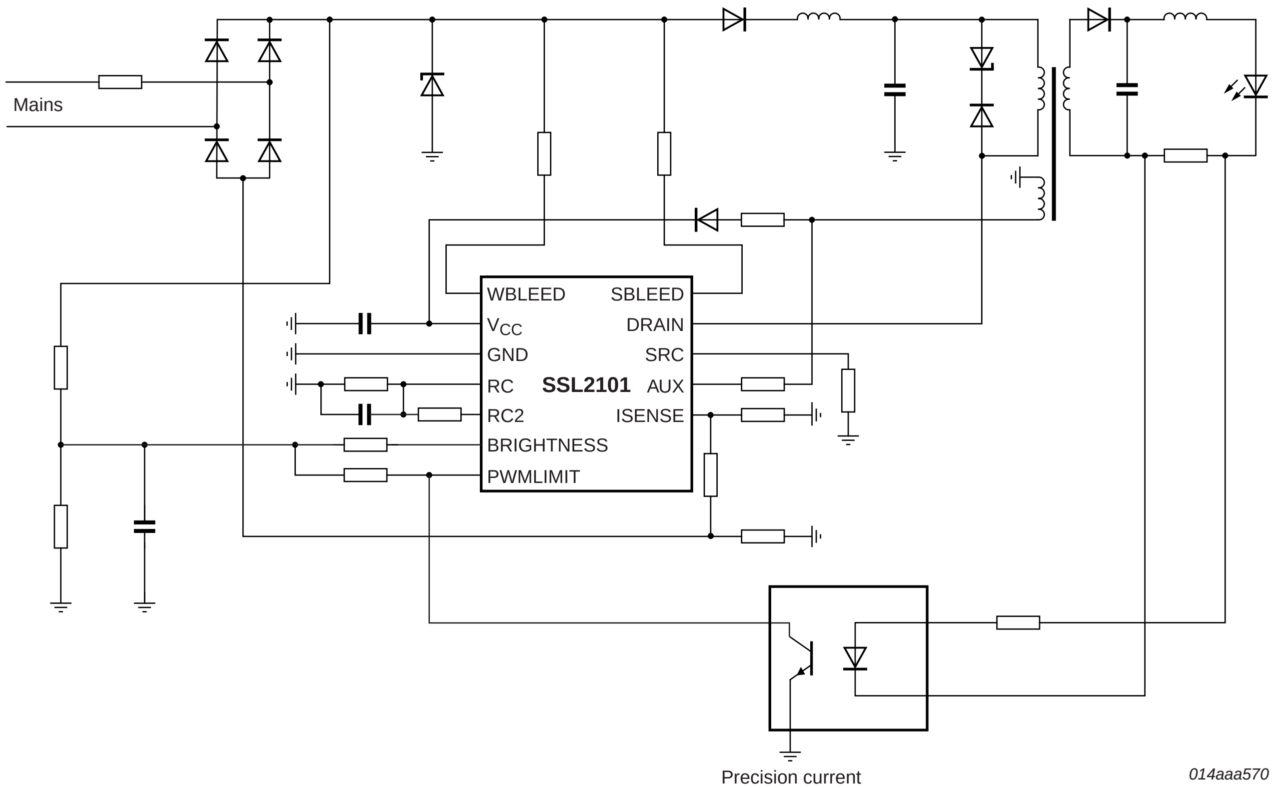
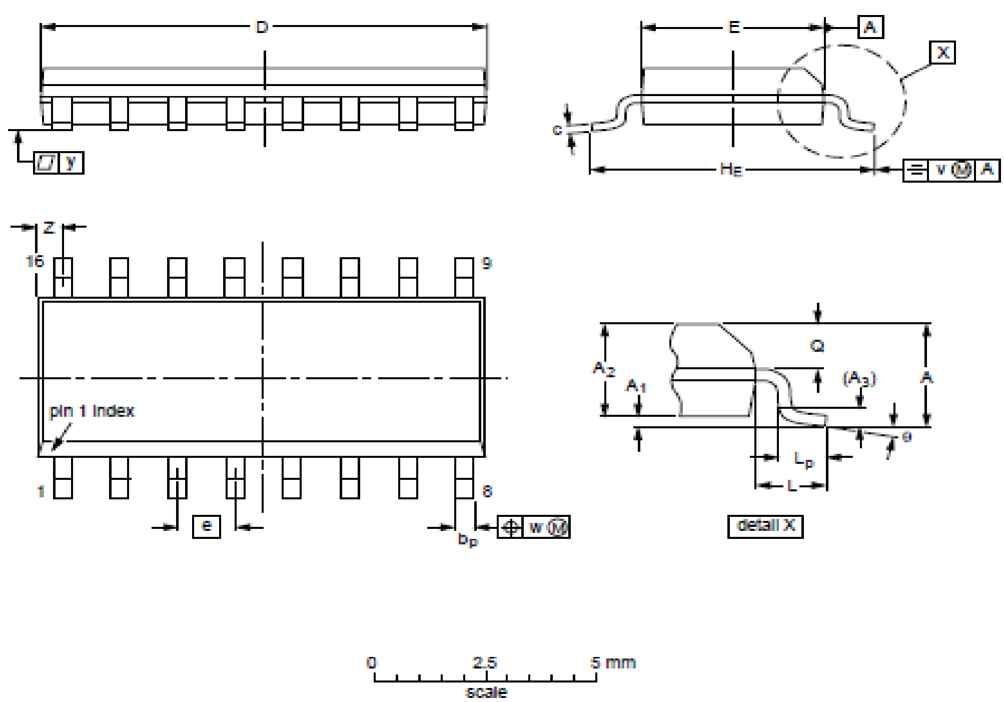


Fig 13. Flyback configuration for SSL2101

Further application information can be found in the SSL2101 application notes.

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D[(1)]	E[(1)]	e	H_E	L	L_p	Q	v	w	y	Z[(1)]	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 14. Package outline SOT109-1 (SO16)