SSL5236TE

Mains dimmable buck-boost LED driver IC 20 Ohm/700 V

Rev. 1 — 13 March 2015 Product data sheet

1. General description

The SSL5236TE is a highly integrated, high-precision buck-boost controller with an internal MOSFET. It is intended to drive low-cost compact dimmable LED lamps up to 7 W. The SSL5236TE is designed to achieve high power factor, phase-dimmable applications.

The SSL5236TE operates in Boundary Conduction Mode (BCM) with constant on-time control. It regulates a constant output current over line and load variations. The wide switching frequency range makes it possible to choose an inductor, which enables the optimization of inductor size, efficiency and EMI.

The SSL5236TE can start up and operate in switching mode directly from line using an external resistor without auxiliary supply. To provide a low-cost driver design, an off-the-shelf inductor can be used, which provides flexibility in application design.

2. Features and benefits

- Integrated MOSFET (20 Ω/700 V)
- Supports most available dimming solutions
- Deep dimming level
- Flicker-free dimming
- Low component count ensuring a compact solution and small, single layer Printed-Circuit Board (PCB) footprint
- Excellent line regulation and load regulation and good LED output current accuracy
- Efficient BCM operation with:
  - Minimal recovery losses in freewheel diode
  - Zero Current Switching (ZCS) and Valley switching for turn-on of switch
  - Minimum inductance value and size required
  - High efficiency (up to 88 %)
  - Ultra low IC current during operation (< 165 μA)
- Auto-recovery protections:
  - UnderVoltage LockOut (UVLO)
  - Cycle-by-cycle OverCurrent Protection (OCP)
  - Internal OverTemperature Protection (OTP)
  - Output OverVoltage Protection (OVP)
  - Output Short Protection (OSP)
- Extended IC lifetime

3. Applications

- The SSL5236TE is intended for low-cost, non-isolated dimmable lighting applications that work from single mains voltage.

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	operating range [1]	9.9	-	16	V
R_{DSon}	on-state resistance	$I_{I(DRAIN)}$ = 100 mA				
		T_j = 25 °C	-	20.2	-	Ω
		T_j = 125 °C	-	30.8	-	Ω
$I_{I(DRAIN)}$	input current on pin DRAIN	duty cycle < 35 %	–0.45	-	+0.45	A
$V_{I(DRAIN)}$	input voltage on pin DRAIN		–0.4	-	+700	V

[1] An internal clamp sets the supply voltage. The current into the VCC pin must not exceed the maximum I_{VCC} value (see Table 4).

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
SSL5236TE	HSO8	plastic thermal enhanced small outline package; 8 leads; body width 3.9 mm; exposed die pad	SOT786-1

6. Block diagram

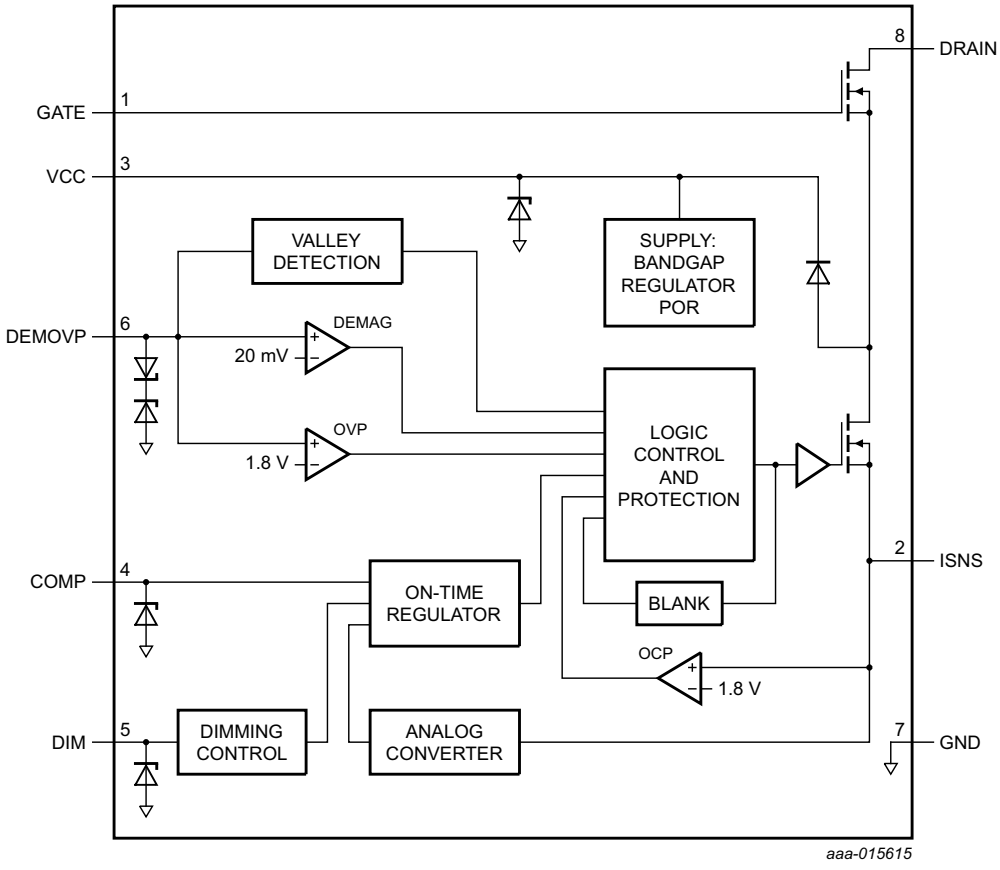


Fig 1. SSL5236TE block diagram

7. Pinning information

7.1 Pinning

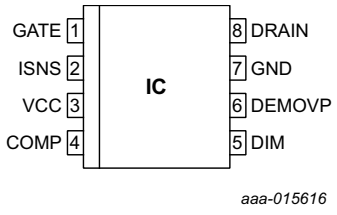


Fig 2. SSL5236TE pin configuration (HSO8 package)

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
GATE	1	gate of internal switch
ISNS	2	ground current sense input
VCC	3	supply voltage
COMP	4	loop compensation to provide stable response
DIM	5	dimming control input
DEMOVP	6	input from LED output for demagnetization timing, valley detection, and OVP
GND	7	ground
DRAIN	8	drain of high-side internal MOSFET

8. Functional description

8.1 Converter operation

The SSL5236TE is a high-side switching on-time controlled BCM buck-boost converter. Figure 3 shows the basic application diagram. To save IC supply current, an integrated source-switch topology is used.

The converter operates at the boundary between Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). Figure 5 shows the waveforms.

When the internal switch is switched on at t0, the inductor current I_L proportionally to V_{in} builds up from zero during the source-switch on-time (t0 to t1). Energy is stored in inductor L2. When the internal source-switch switches off at t1, I_L flows through the freewheeling diode D2 and the output capacitor C5. The inductor current drops proportionally to V_{out} (t2 to t3). When I_L reaches zero at t3, a new switching cycle is started after a short delay (t3 to t00) from valley detection.

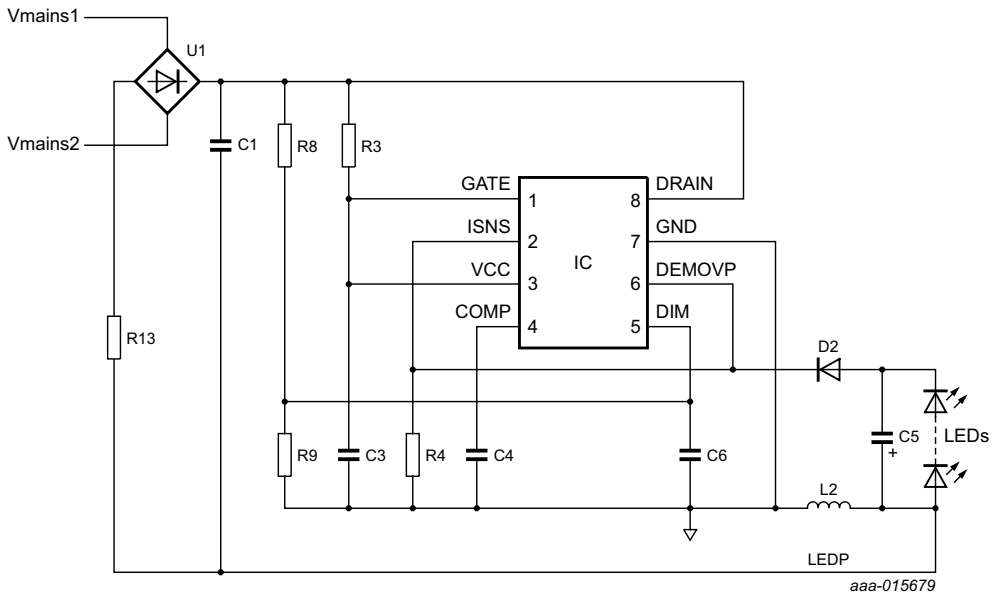


Fig 3. SSL5236TE basic application diagram

8.2 On-time control

When measuring the inductor current I_L using sense resistor R4, the on-time is regulated so that the average ISNS voltage ($V_{intregd(AV)ISNS}$) is regulated to 300 mV during the off-time of the main switch. The average output current I_{out} can be calculated with Equation 1:

$$I_{out} = \frac{V_{intregd(AV)ISNS}}{R4} \quad (1)$$

8.3 Dimming control

When measuring the phase-cut mains voltage using the DIM pin, the DIM voltage modulates the internal reference voltage. The dimmed output current $I_{O(dim)}$ can be calculated with Equation 2:

$$I_{O(dim)} = \frac{V_{dim(itg)AV(ISNS)}}{R4} \quad (2)$$

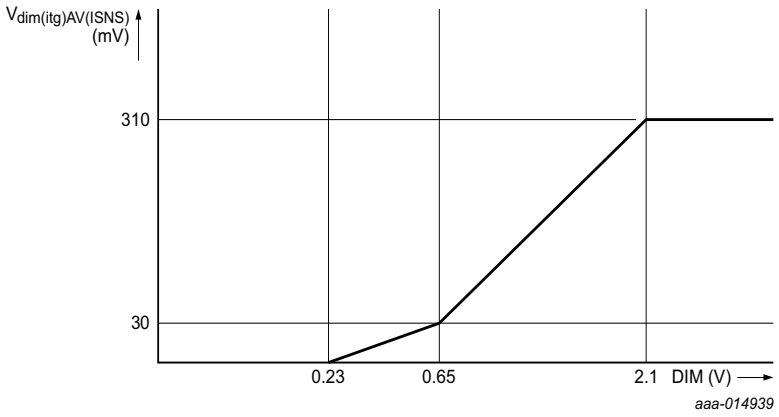


Fig 4. Dimming control transfer function

8.4 Valley detection

When I_L has decreased to zero at t3, the LEDP voltage starts to oscillate around the IC ground, with amplitude V_{out} and frequency (f_{ring}). A special circuit called valley detection is integrated in the SSL5236TE. It senses when the LEDP voltage reaches its lowest level (valley) at the DEMOVP pin. The internal source-switch is switched on again when the valley is detected. As a result, the switch-on switching losses are reduced.

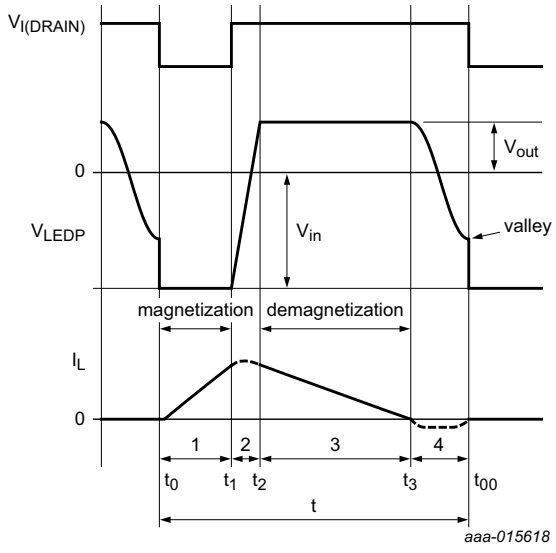


Fig 5. Buck-boost waveforms and valley detection

8.5 Start-up

The supply current for the IC is supplied by resistor R3. Just before V_{CC} reaches the start-up voltage level ($V_{startup}$), the IC draws an additional start-up current ($I_{CC(startup)}$). So the supply current in operation is lower than the supply current during start-up conditions. It prevents lamp flicker when the mains voltage increases or decreases slowly.

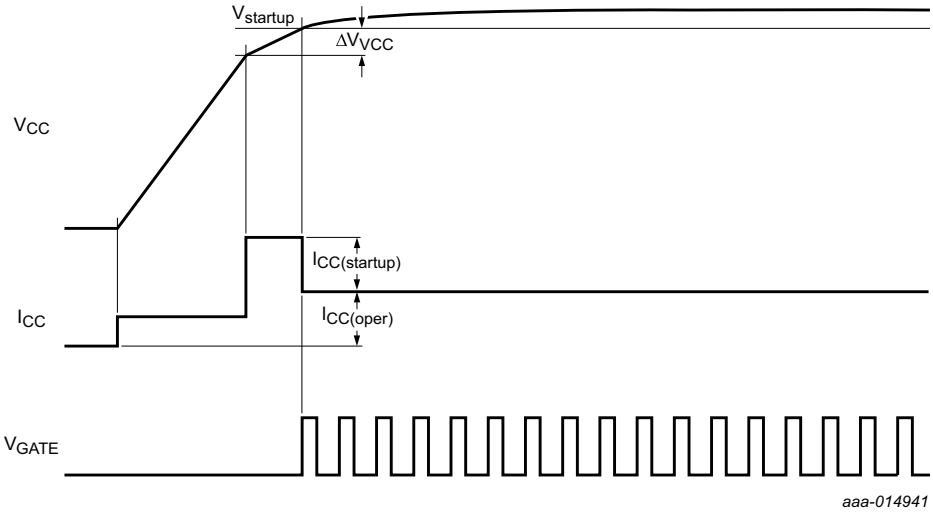


Fig 6. Start-up current waveform

8.6 Leading-Edge Blanking (LEB)

To prevent false detection of overcurrent, a blanking time following switch-on is implemented. When the internal switch turns on, a short current spike can occur because of the capacitive discharge of voltage over the drain and the source. It is disregarded during the LEB time (t_{leb}).

8.7 Magnetization switching

When the mains voltage is very low, during dimming or around the zero crossings of the mains, the system hardly delivers any energy to the LED. To improve the efficiency, maximum off-time ($t_{off(max)}$) switching limits the switching frequency to < 25 kHz. A peak voltage on the ISNS pin below the $V_{I(min)ISNS}$ voltage indicates a low mains voltage.

8.8 Protections

The IC incorporates the following protections:

- UnderVoltage LockOut (UVLO)
- Cycle-by-cycle OverCurrent Protection (OCP)
- Internal OverTemperature Protection (OTP)
- Cycle-by-cycle maximum on-time protection
- Output OverVoltage Protection (OVP)
- Output Short Protection (OSP)

8.8.1 UnderVoltage LockOut (UVLO)

When the voltage on the VCC pin drops to below $V_{th(UVLO)}$, the IC stops switching. An attempt is made to restart IC when the $V_{CC} > V_{startup}$.

8.8.2 Cycle-by-cycle OverCurrent Protection (OCP)

The SSL5236TE contains a built-in peak current detector. It triggers when the voltage at the ISNS pin reaches the peak level $V_{I(max)ISNS}$. A resistor connected to the ISNS pin senses the current through the inductor I_L. The maximum current in inductor $I_{L(max)}$ can be calculated with Equation 3:

$$I_{L(max)} = \frac{V_{I(max)ISNS}}{R4 + R_{bond} \times \delta_{swon}} \quad (3)$$

Where:

- R_{bond} is the ISNS bond wire resistance
- δ_{swon} is the switch-on duty cycle

The sense circuit is activated after the LEB time (t_{leb}). It automatically provides protection for maximum LED current during operation. A propagation delay exists between overcurrent detection and the actual source-switch switch-off. Due to this delay, the actual peak current is slightly higher than the OCP level set by the resistor in series with the ISNS pin.

8.8.3 OverTemperature Protection (OTP)

When the internal OTP function is triggered at IC junction temperature $T_{pl(IC)}$, the converter stops switching. The IC resumes switching when the IC temperature drops to below $T_{pl(IC)rst}$.

8.8.4 Cycle-by-cycle maximum on-time protection

Measuring the inductor current I_L using sense resistor R_{sense} regulates the on-time. The on-time is limited to a fixed value ($t_{on(max)}$). It protects the system and the IC when the ISNS pin is shorted or the system works at very low mains.

8.8.5 Output OverVoltage Protection (OVP)

Measuring the voltage at the DEMOVP pin during the secondary stroke gives an accurate output OVP. The resistive divider connected between the LEDP node and the DEMOVP pin sets the maximum LED voltage.

An internal counter prevents false OVP detection because of noise on the DEMOVP pin. After three continuous cycles with a DEMOVP pin voltage exceeding the OVP level, OVP is triggered.

OVP triggers a restart sequence: A discharge current ($I_{CC(dch)}$) is enabled and discharges V_{CC} to below $V_{rst(latch)}$. When $V_{rst(latch)}$ is reached, the system restarts.

8.8.6 Output Short Protection (OSP)

The converter operates in Discontinuous Conduction Mode (DCM). A new cycle is only started after the previous cycle has ended. Measuring the voltage on the DEMOVP pin detects the end of the cycle. When the DEMOVP pin voltage drops to below the demagnetization level ($V_{det(demag)}$) and a valley is detected, a new cycle starts. The converter regulates the adjusted output current and the on-time is reduced to a safe value by this feedback. The reduced on-time in combination with a very long demagnetization period prevents the converter from any damage or excessive dissipation.

To prevent false demagnetization detection, a blanking time ($t_{sup(xfmr\_ring)}$) is implemented at the start of the secondary stroke.

8.9 Supply management

The IC starts up when the voltage at the VCC pin exceeds $V_{startup}$. The IC locks out (stops switching) when the voltage at the VCC pin drops to below $V_{th(UVLO)}$. The hysteresis between the start and stop levels allows the VCC capacitor to supply the IC during zero-crossings of the mains.

The SSL5236TE incorporates an internal VCC clamping circuit. The clamp limits the voltage on the VCC supply pin to the maximum value $V_{clamp(VCC)}$. If the maximum current of the external resistor minus the current consumption of the IC is lower than the limiting value of I_{VCC} in Table 4, no external Zener diode is required.

9. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{CC}	supply voltage	current limited [1][2]	−0.4	18	V
V_{GATE}	gate voltage	current limited [1][2]	−0.4	18	V
$V_{I(DRAIN)}$	input voltage on pin DRAIN	current limited [1][2]	−0.4	+700	V
$V_{I(ISNS)}$	input voltage on pin ISNS		−0.4	+5	V
$V_{IO(COMP)}$	input/output voltage on pin COMP		−0.4	+5.3	V
$V_{I(DEMOVP)}$	input voltage on pin DEMOVP		−6	+6	V
$V_{I(DIM)}$	input voltage on pin DIM		−0.4	+5	V
Currents					
$I_{I(VCC)}$	input current on pin VCC		-	+8.8	mA
$I_{I(DRAIN)}$	input current on pin DRAIN	RMS current; maximum average current = 80 mA; duty cycle < 35 %	-	150	mA
		duty cycle < 35 %	−0.45	+0.45	A
$I_{I(ISNS)}$	input current on pin ISNS	duty cycle < 35 %	−0.45	+0.45	A
General					
P_{tot}	total power dissipation	T_{amb} < 75 °C	-	0.8	W
T_{stg}	storage temperature		−55	+150	°C
T_j	junction temperature		−40	+160	°C
ESD					
V_{ESD}	electrostatic discharge voltage	class 1			
		human body model [3]	−2000	+2000	V
		charged device model [4]	−500	+500	V

[1] The current into the VCC pin must not exceed the maximum I_{VCC} value.

[2] An internal clamp sets the supply voltage and current limits.

[3] Equivalent to discharge a 100 pF capacitor through a 1.5 kΩ series resistor.

[4] Charged device model: equivalent to charging the IC up to 1 kV and the subsequent discharging of each pin down to 0 V over a 1 Ω resistor.

10. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; HSO8 package; PCB: 2 cm × 3 cm; 35 μm copper (Cu)/layer; copper for IC: 6.6 cm	117	K/W
		in free air; HSO8 package; PCB: JEDEC 2s2p	49	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package	top package temperature measured at the warmest point on top of the case; HSO8 package	4	K/W

11. Characteristics

Table 6. Characteristics

T_{amb} = 25 °C; V_{CC} = 15 V; all voltages are measured with respect to ground pin (pin 7); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply (pin VCC)						
$V_{startup}$	start-up voltage		14.45	14.9	15.35	V
$V_{th(UVLO)}$	undervoltage lockout threshold voltage		9.6	9.9	10.2	V
ΔV_{VCC}	voltage difference on pin VCC		0.17	0.30	0.43	V
$V_{clamp(VCC)}$	clamp voltage on pin VCC	$I_{I(VCC)}$ = 2.6 mA [1]	15.2	15.8	16.4	V
$V_{rst(latch)}$	latched reset voltage		5.8	6.2	6.6	V
$I_{CC(oper)}$	operating supply current	switching at 100 kHz	125	145	165	μA
$I_{CC(startup)}$	start-up supply current		120	145	170	μA
$I_{CC(dch)}$	discharge supply current	$V_{CC} = V_{rst(latch)}$	3.7	-	-	mA
Loop compensation (pin COMP)						
$V_{ton(zero)}$	zero on-time voltage		1.9	2.0	2.1	V
$V_{ton(max)}$	maximum on-time voltage		3.8	4.0	4.2	V
$V_{clamp(COMP)}$	clamp voltage on pin COMP		4.3	4.7	5.1	V
$t_{on(max)}$	maximum on-time	$V_{IO(COMP)}$ = 4 V	12.3	15.5	18.7	μs
$I_{O(COMP)}$	output current on pin COMP	$V_{I(ISNS)}$ = 0 V; $V_{I(DIM)}$ > 2 V	2.4	3.0	3.6	μA
$I_{dch(COMP)}$	Discharge current on pin COMP	$V_{I(DIM)}$ = 0 V	350	550	750	nA
Valley detection and overvoltage detection (pin DEMOVP)						
$I_{prot(DEMOVP)}$	protection current on pin DEMOVP	open current; $V_{I(DEMOVP)}$ = 0 V	−250	−180	−50	nA
$V_{th(ovp)}$	overvoltage protection threshold voltage		1.74	1.81	1.88	V
$N_{cy(ovp)}$	number of overvoltage protection cycles		-	3	-	-

Table 6. Characteristics *...continued*

T_{amb} = 25 °C; V_{CC} = 15 V; all voltages are measured with respect to ground pin (pin 7); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$(dV/dt)_{vrec}$	valley recognition voltage change with time	[2]	-	−3.8	-	V/µs
$V_{det(demag)}$	demagnetization detection voltage		4	18	32	mV
$t_{sup(xfmr\_ring)}$	transformer ringing suppression time		1.2	1.5	1.8	µs
Current sensing (pin ISNS)						
$V_{I(min)ISNS}$	minimum input voltage on pin ISNS		30	50	70	mV
$V_{I(max)ISNS}$	maximum input voltage on pin ISNS		1.7	1.8	1.9	V
$t_{on(min)}$	minimum on-time	[3]	310	410	510	ns
t_d	delay time	[3]	-	100	-	ns
$g_{m(ISNS)}$	ISNS transconductance	$V_{I(ISNS)}$ to $I_{O(COMP)}$	8.4	9.7	11	µA/V
$V_{intregd(max)ISNS}$	maximum internal regulated voltage on pin ISNS	$V_{I(DIM)}$ > 2 V	0.298	0.31	0.324	V
Dimming control (pin DIM)						
$V_{intregd(AV)}/V_{dim}$	average internal regulated voltage ratio to dimming voltage	0.65 V < V_{DIM} < 2 V	190	200	210	mV/V
		0.25 V < V_{DIM} < 0.6 V	58	70	92	mV/V
$V_{clamp(DIM)}$	clamp voltage on pin DIM	$I_{I(DIM)}$ = 200 µA	3.8	4.0	4.2	V
Driver (pin DRAIN)						
R_{DSon}	on-state resistance	$I_{I(DRAIN)}$ = 100 mA				
		T_j = 25 °C	-	20.2	23	Ω
		T_j = 125 °C	-	30.8	35[4]	Ω
$t_{off(max)}$	maximum off-time		30	40	50	µs
$I_{leak(DRAIN)}$	leak current on pin DRAIN	$V_{I(DRAIN)}$ = 700 V	-	-	10	µA
Temperature protection						
$T_{pl(IC)}$	IC protection level temperature		140	150	165	°C
$T_{pl(IC)rst}$	reset IC protection level temperature		106	118	130	°C

[1] The start-up voltage and the clamp voltage are correlated.

[2] Guaranteed by design.

[3] $t_{leb} = t_{on(min)} - t_d$; $t_{on(min)}$ is only effective when OCP is triggered.

[4] The value is based on extrapolated data.

12. Application information

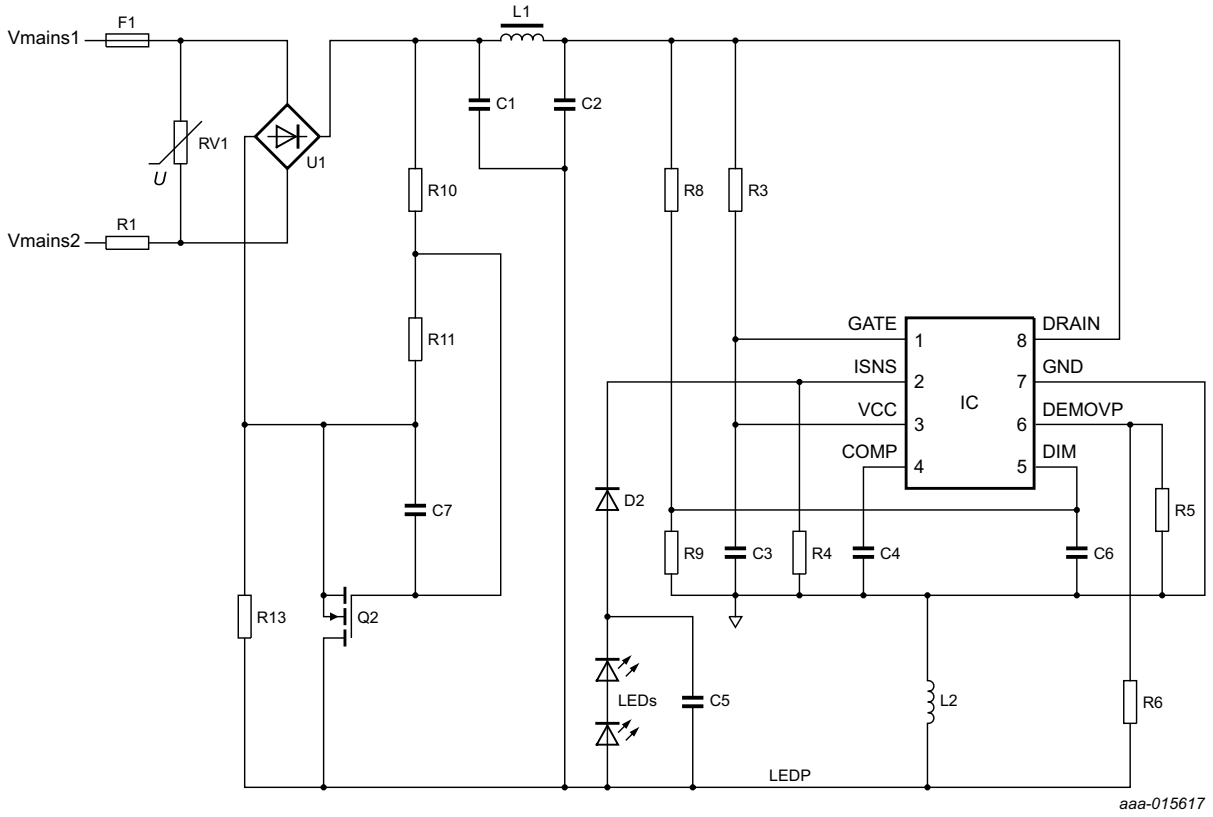
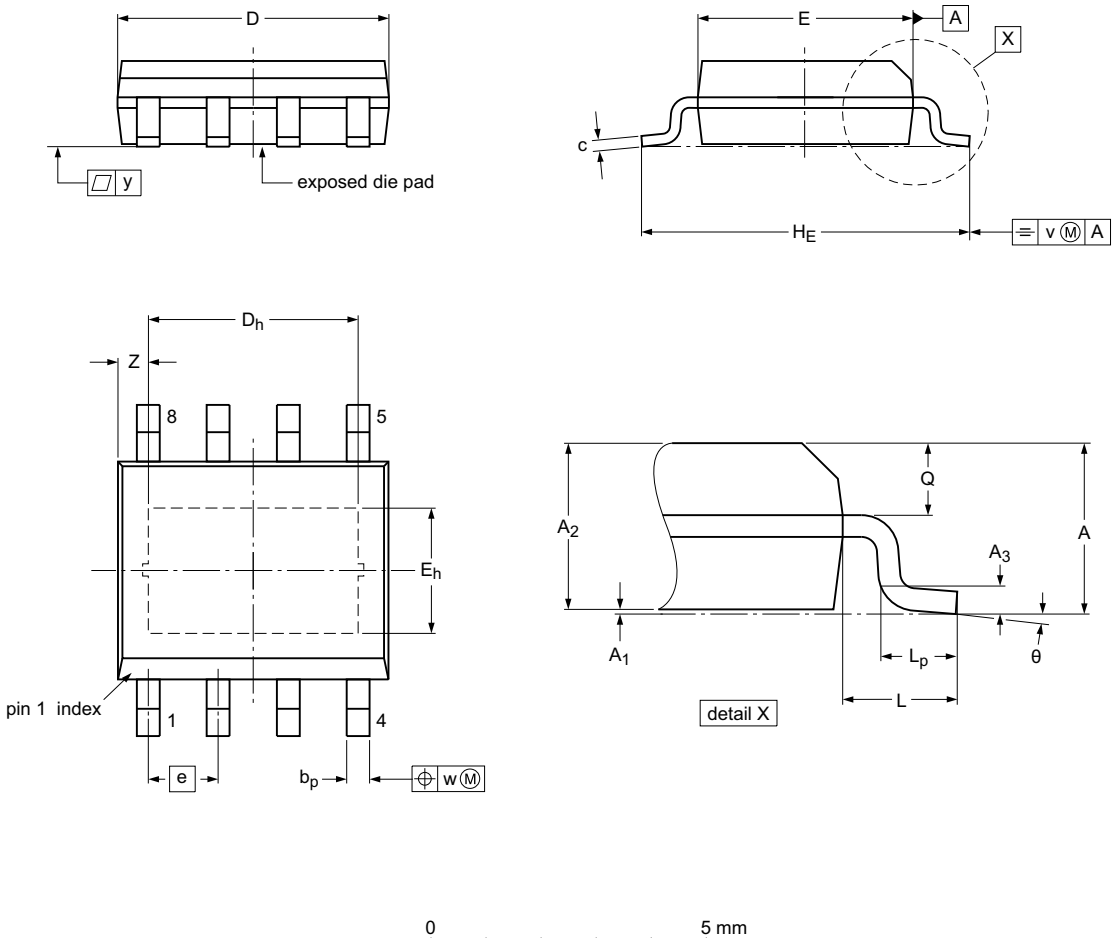


Fig 7. SSL5236TE typical application diagram

13. Package outline

HSO8: plastic thermal enhanced small outline package;
8 leads; body width 3.9 mm; exposed die pad **SOT786-3**



Dimensions (mm are the original dimensions)

Unit	A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_E	L	L_p	Q	v	w	y	Z	θ
max	1.68	0.10	1.58		0.49	0.25	5.00	3.91	4.00	2.39		6.20		0.89	0.75				0.7	8°
mm nom	1.55	0.05	1.50	0.25	0.41	0.20	4.90	3.81	3.90	2.29	1.27	5.99	1.05	0.64	0.65	0.25	0.25	0.1	0.5	5°
min	1.43	0.00	1.43		0.35	0.19	4.80	2.95	3.80	2.19		5.84		0.41	0.55				0.3	0°

Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot786-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT786-3						~~13-06-05~~ 15-02-12

Fig 8. Package outline SOT786-3 (HSO8)