Application Note: SY20111A/B/C/D/E/F

High Efficiency 3MHz, 1A Synchronous Step Down Regulator

General Description

SY20111A/B/C/D/E/F are high efficiency 3MHz synchronous step down DC/DC regulator ICs capable of delivering up to 1A output current. It can operate over a wide input voltage range from 2.5V to 5.5V and integrate main switch and synchronous switch with very low $R_{DS\,(ON)}$ to minimize the conduction loss.

Ordering Information

SY20111 □(□,□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package Type	Note
SY20111ADQC	DFN1.5×1.5-6	Fixed 1.2V_{OUT}
SY20111BDQC	DFN1.5×1.5-6	Fixed 1.5V_{OUT}
SY20111CDQC	DFN1.5×1.5-6	Fixed 1.8V_{OUT}
SY20111DDQC	DFN1.5×1.5-6	Fixed 2.5V_{OUT}
SY20111EDQC	DFN1.5×1.5-6	Fixed 3.3V_{OUT}
SY20111FDQC	DFN1.5×1.5-6	Fixed 1.0V_{OUT}

Features

- Low $R_{DS(ON)}$ for internal switches (top/bottom) 230mΩ/150mΩ
- 2.5~5.5V input voltage range
- Fixed output voltage:
  - SY20111A: Fixed 1.2V_{OUT}
  - SY20111B: Fixed 1.5V_{OUT}
  - SY20111C: Fixed 1.8V_{OUT}
  - SY20111D: Fixed 2.5V_{OUT}
  - SY20111E: Fixed 3.3V_{OUT}
  - SY20111F: Fixed 1.0V_{OUT}
- High switching frequency 3MHz minimizes the external components
- Internal soft-start limits the inrush current
- 100% dropout operation
- RoHS Compliant and Halogen Free
- Output auto discharge function
- Compact package: DFN1.5x1.5-6

Applications

- Portable Navigation Device
- Set Top Box
- USB Dongle
- Media Player
- Smart phone

Typical Applications

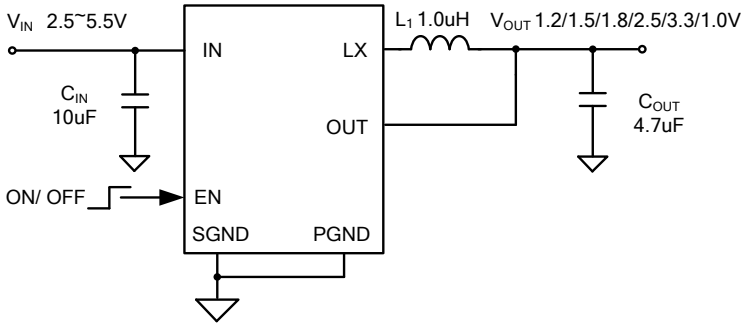

Figure1. Schematic Diagram

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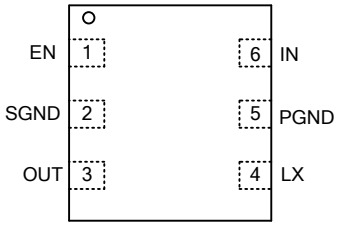
Pinout (Top View)



(DFN1.5x1.5-6)

Top Mark: QY*xyz* *for SY20111A* (device code: **QY**, ***x=year code, y=week code, z= lot number code)***
QB*xyz* *for SY20111B* (device code: **QB**, ***x=year code, y=week code, z= lot number code)***
QC*xyz* *for SY20111C* (device code: **QC**, ***x=year code, y=week code, z= lot number code)***
QD*xyz* *for SY20111D* (device code: **QD**, ***x=year code, y=week code, z= lot number code)***
RL*xyz* *for SY20111E* (device code: **RL**, ***x=year code, y=week code, z= lot number code)***
RM*xyz* *for SY20111F* (device code: **RM**, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin Number	Pin Description
EN	1	Enable control. Pull high to turn on. Do not float.
PGND	5	Power ground pin.
SGND	2	Signal ground pin.
LX	4	Inductor pin. Connect this pin to the switching node of inductor.
IN	6	Input pin. Decouple this pin to GND pin with at least 10uF ceramic cap.
OUT	3	Output Pin. Connect this pin to the output.

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- 6.0V
Enable, FB Voltage---------- V_{IN} + 0.6V
Power Dissipation, P_D @ T_A = 25°C,
DFN1.5×1.5-6 ---------- 0.8W
Package Thermal Resistance (Note 2)
θ_{JA} ----------145°C/W
θ_{JC} ----------81°C/W
Junction Temperature Range ----------125°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 2.5V to 5.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

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Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 2.5V, L = 1.0uH, C_{OUT} = 4.7uF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.5		5.5	V
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF} · 105%		40		μA
Shutdown Current	I_{SHDN}	EN=0		0.1	1	μA
Output Voltage	V_{OUT}	SY20111A	1.176	1.2	1.224	V
		SY20111B	1.47	1.5	1.53	V
		SY20111C	1.764	1.8	1.836	V
		SY20111D	2.45	2.5	2.55	V
		SY20111E	3.234	3.3	3.366	V
		SY20111F	0.98	1.0	1.02	V
PFET RON	$R_{DS(ON),P}$			230		mΩ
NFET RON	$R_{DS(ON),N}$			150		mΩ
PFET Current Limit	I_{LIM}		1.3			A
EN rising threshold	V_{ENH}		1.5			V
EN falling threshold	V_{ENL}				0.4	V
Input UVLO threshold	V_{UVLO}				2.5	V
UVLO hysteresis	V_{HYS}			0.1		V
Oscillator Frequency	F_{OSC}			3		MHz
Min ON Time				65		ns
Max Duty Cycle			100			%
Soft Start Time	T_{SS}			1		ms
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C
Output discharge resistor	R_{DSC}			120		Ω

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Exposed Paddle of DFN package is the case position for θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

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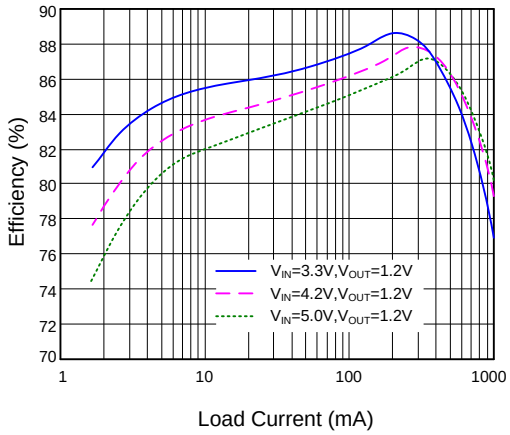
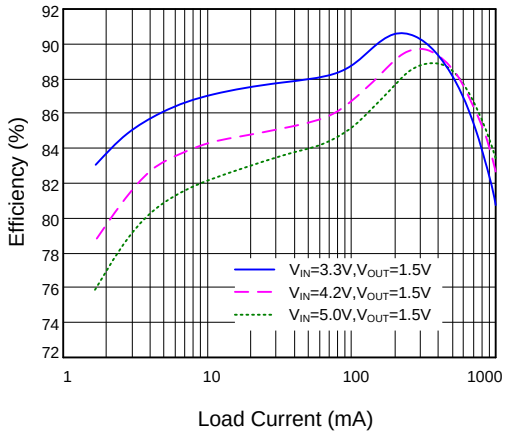
Typical Performance Characteristics

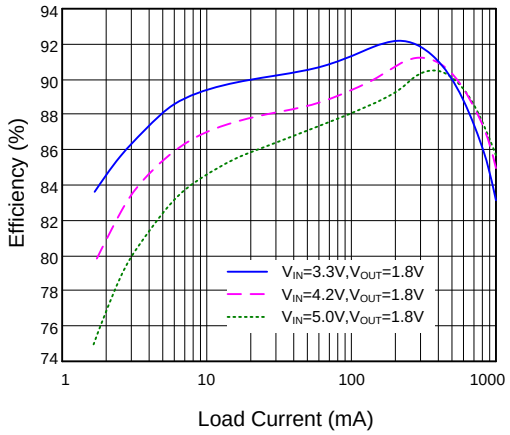
Efficiency vs. Load Current (SY20111A)



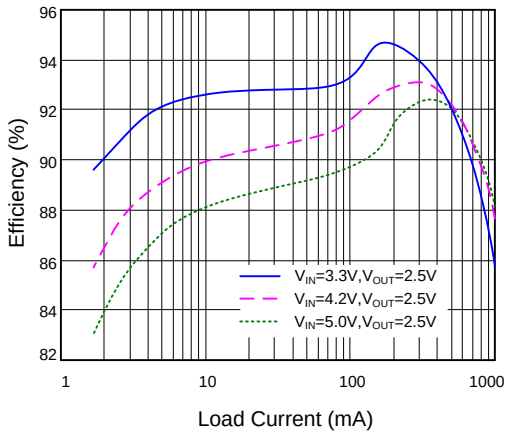
Efficiency vs. Load Current (SY20111B)



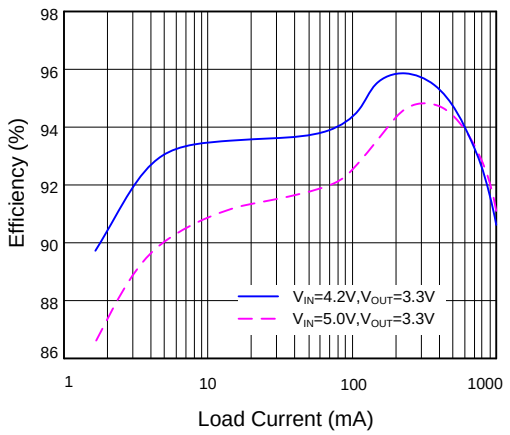
Efficiency vs. Load Current (SY20111C)



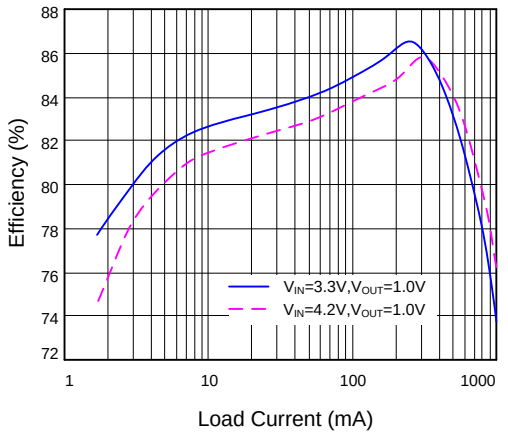
Efficiency vs. Load Current (SY20111D)



Efficiency vs. Load Current (SY20111E)



Efficiency vs. Load Current (SY20111F)



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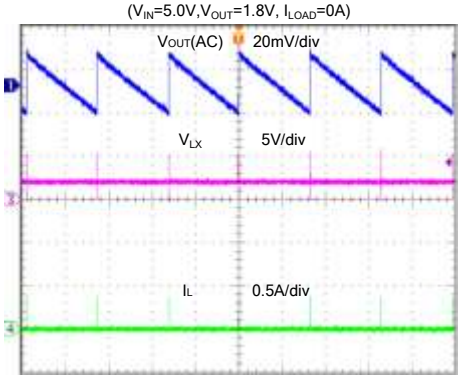
Output Ripple

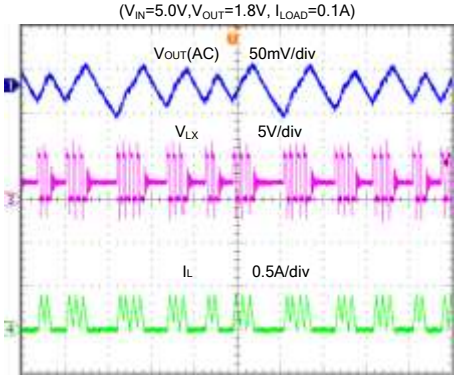
(V_{IN}=5.0V,V_{OUT}=1.8V, I_{LOAD}=0A)



Time (40μs/div)

Output Ripple

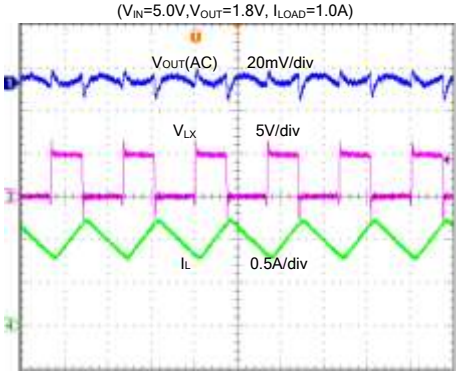
(V_{IN}=5.0V,V_{OUT}=1.8V, I_{LOAD}=0.1A)



Time (2μs/div)

Output Ripple

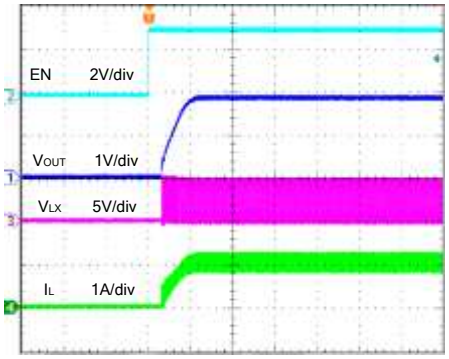
(V_{IN}=5.0V,V_{OUT}=1.8V, I_{LOAD}=1.0A)



Time (200ns/div)

Startup

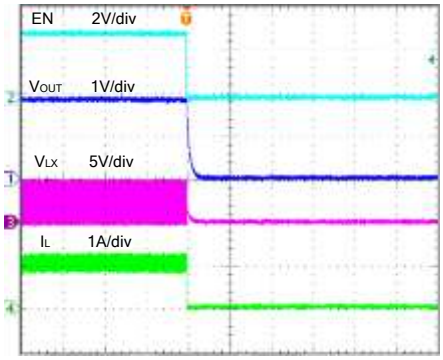
(V_{IN}=5.0V, V_{OUT}=1.8V, I_{LOAD}=1A)



Time (1ms/div)

Shutdown

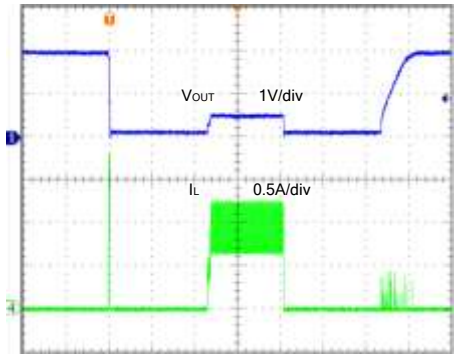
(V_{IN}=5.0V, V_{OUT}=1.8V, I_{LOAD}=1A)



Time (100μs/div)

Short Circuit Protection

(V_{IN}=5.0V, V_{OUT}=1.8V, 0A to Short)



Time (1ms/div)

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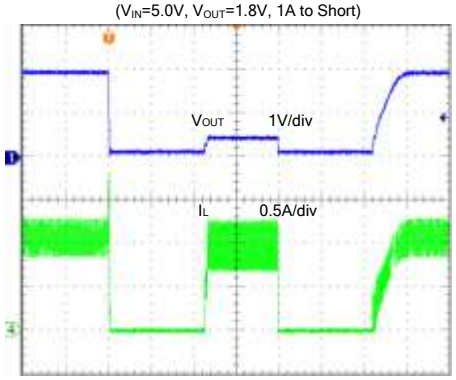
Short Circuit Protection

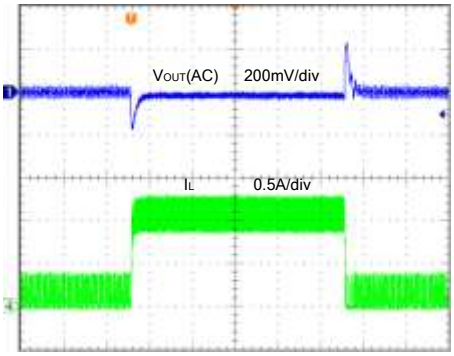
(V_{IN}=5.0V, V_{OUT}=1.8V, 1A to Short)



Time (1ms/div)

Load Transient

(V_{IN}=5.0V, V_{OUT}=1.8V, I_{LOAD}=0.1-1.0A)



Time (40μs/div)

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Operation

SY20111A/B/C/D/E/F are high efficiency 3MHz synchronous step down DC/DC regulator ICs capable of delivering up to 1A output current. It can operate over a wide input voltage range from 2.5V to 5.5V and integrate main switch and synchronous switch with very low $R_{DS\,(ON)}$ to minimize the conduction loss.

Applications Information

Because of the high integration in the SY20111A/B/C/D/E/F ICs, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT} and output inductor L need to be selected for the targeted applications specifications.

Input capacitor C_{IN}:

A typical X7R or better grade ceramic capacitor and greater than 4.7uF capacitance is recommended. To minimize the potential noise problem, place this ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins.

Output capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X7R or better grade ceramic capacitor with 6V rating and greater than 4.7uF capacitance.

Output inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX\,\times\,40\%}}$$

where Fsw is the switching frequency and Iout,max is the maximum load current.

The SY20111A/B/C/D/E/F regulator ICs are quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,\,MIN} > I_{OUT,\,MAX} + \frac{V_{OUT}(1\text{-}V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mohm to achieve a good overall efficiency.

Layout Design:

The layout design of SY20111A/B/C/D/E/F regulators are relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN} and L.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

4) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

Load Transient Considerations:

The SY20111A/B/C/D/E/F regulator ICs integrate the compensation components to achieve good stability and fast transient responses..

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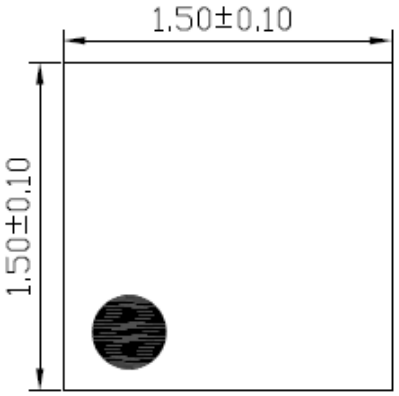
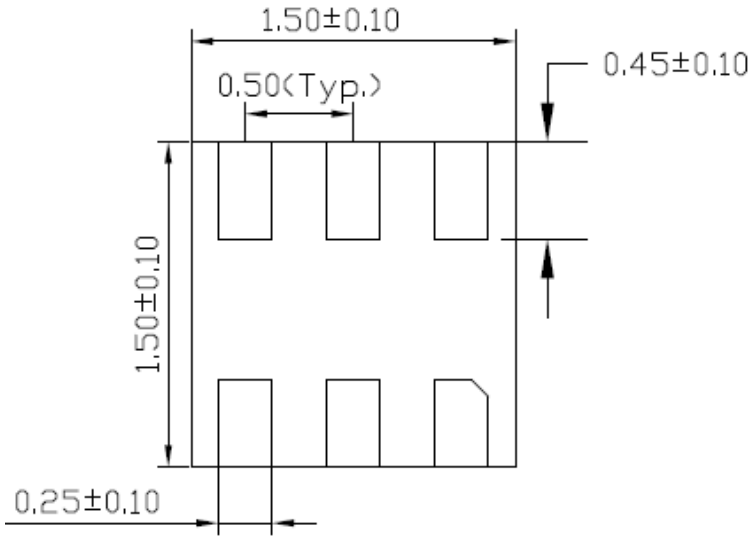
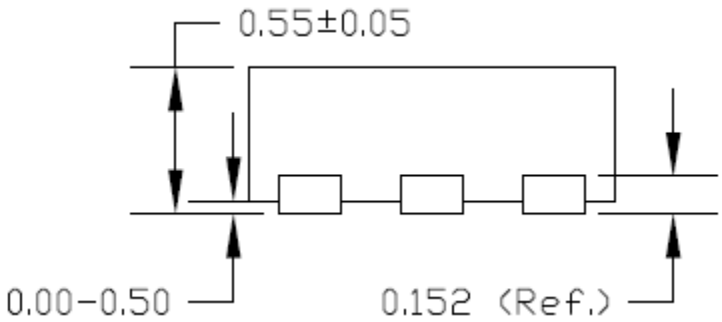
DFN1.5x1.5-6L Package Outline



Top View



Bottom View



Side View

Notes: **All dimension in MM and exclude mold flash & metal burr.**

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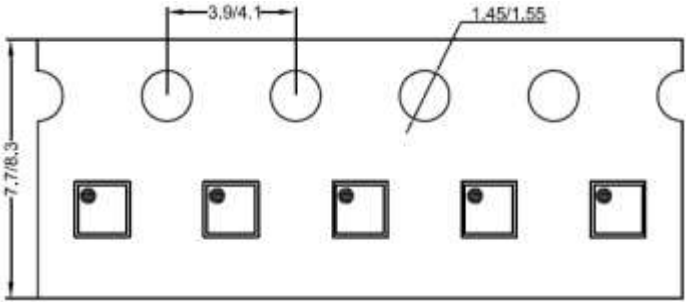
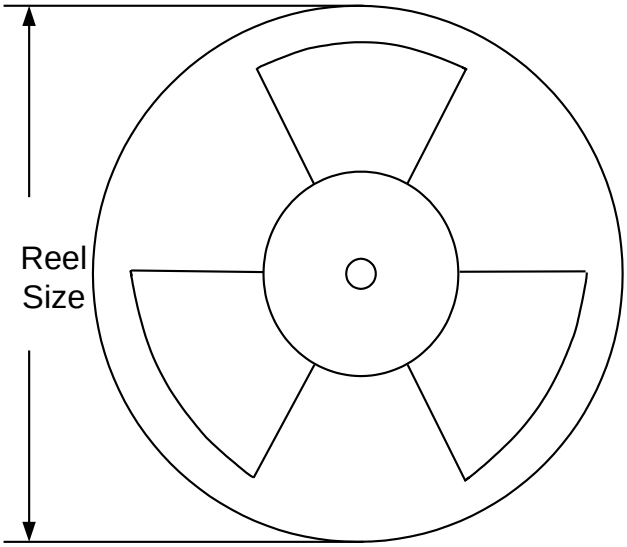
Taping & Reel Specification

1. DFN 1.5x1.5-6 taping orientation



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN1.5x1.5	8	4	7"	400	160	3000

3. Others: NA

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