SY20341

High Efficiency 2MHz, Dual 1.0A&1.5A Synchronous Step Down Regulator

General Description

The SY20341 is a dual-output, high efficiency 2MHz synchronous step down DC/DC regulator, capable of delivering up to 1.0A and 1.5A for channel 1 and channel 2. The SY20341 operates over a wide input voltage range from 2.5V to 5.5V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

Ordering Information

SY20341□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY20341SAC	DFN2x1.5-8	--

Features

- Input Range: 2.5V to 5.5V Input Voltage
- 2MHz Switching Frequency
- 180° out of Phase Operation
- Output Current: 1.0A for Channel 1
  1.5A for Channel 2
- Low Quiescent Current: <45uA for both channels
- Low $R_{DS(ON)}$ for Internal Switches (PFET/NFET): 125mΩ/100mΩ
- Internal soft-start
- 100% Dropout Operation
- RoHS Compliant and Halogen Free
- Compact Package: DFN2x1.5-8

Applications

- SSD
- Cell Phones
- Digital Cameras
- PDAs
- Portable Media Players

Typical Applications

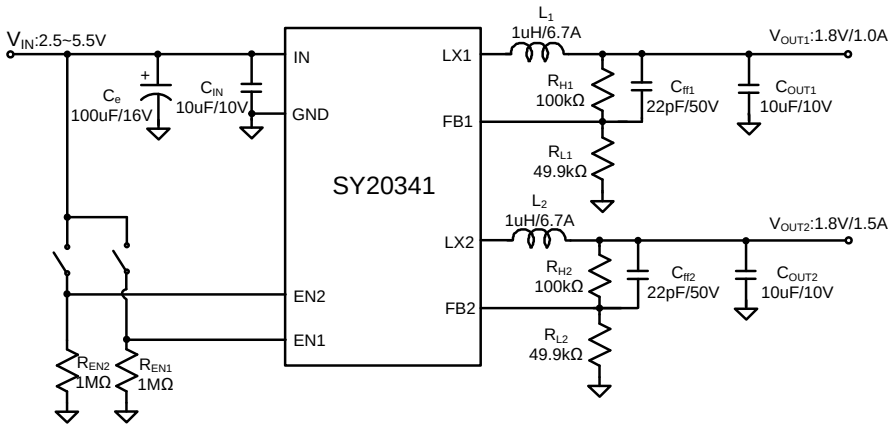

Figure1. Schematic Diagram

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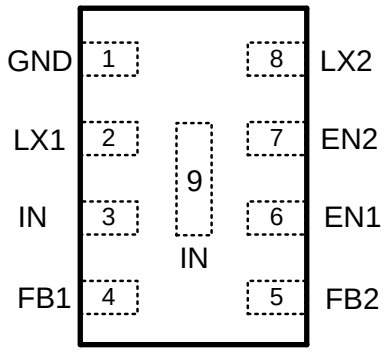
Pinout (top view)



(DFN2x1.5-8)

Top Mark: **In*xyz* for SY20341SAC(**device code: In, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
FB1	4	Feedback pin for output1. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output1 voltage: V_{OUT1}=0.6V*(1+R_{H1}/R_{L1})
IN	3	Power input pin. Decouple this pin to ground pin at least 10uF ceramic cap
LX1	2	Inductor pin for output1. Connect this pin to the switching node of inductor.
GND	1	Ground pins.
LX2	8	Inductor pin for output2. Connect this pin to the switching node of inductor.
EN2	7	Enable pin for output2. Do not leave it floating.
EN1	6	Enable pin for output1. Do not leave it floating.
FB2	5	Feedback pin for output2. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output2 voltage: V_{OUT2}=0.6V*(1+R_{H2}/R_{L2})
IN	9	Power input pin. Connect this pin to IN pin, don't leave it floating.

Absolute Maximum Ratings (Note 1)

All Pins ---------- 6V
Power Dissipation, P_D @ T_A = 25°C, DFN2x1.5-8 ---------- 1.2W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 80°C/W
θ_{JC} ---------- 15°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 2.5V to 5.5V
Enable, FB Voltage ---------- V_{IN}+0.3V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

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Electrical Characteristics

(V_{IN}= 5V, V_{OUT1}=V_{OUT2}=2.5V, L_1=L_2=1.0μH, C_{OUT1}=C_{OUT2}=10μF, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.5		5.5	V
Shutdown Current	I_{SHDN}	EN1=EN2=0		0.1	1	μA
Quiescent Current	I_Q	EN1=1 or EN2=1, I_{OUT1}= I_{OUT1}=0, no switching		35		μA
		EN1=1 and EN2=1, I_{OUT1}= I_{OUT2}=0, no switching		45		μA
Input UVLO Threshold	V_{UVLO}				2.5	V
UVLO Hysteresis	V_{HYS1}			0.2		V
Oscillator Frequency	f_{OSC}	I_{OUT1} = 0.1A, I_{OUT2} = 0.1A		2.0		MHz
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C
Feedback Reference Voltage	V_{REF1}, V_{REF2}		0.588	0.600	0.612	V
PFET R_{ON}	$R_{DS(ON),P1}$ $R_{DS(ON),P2}$			125		mΩ
NFET R_{ON}	$R_{DS(ON),N1}$ $R_{DS(ON),N2}$			100		mΩ
CH1 PFET Current Limit	I_{LIM1}		1.5			A
CH2 PFET Current Limit	I_{LIM2}		2.0			A
EN Rising Threshold	V_{ENH1}, V_{ENH2}		1.2			V
EN Falling Threshold	V_{ENL1}, V_{ENL2}				0.4	V
Internal Soft Start Time	t_{SS1}, t_{SS2}			1		ms

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θJA is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

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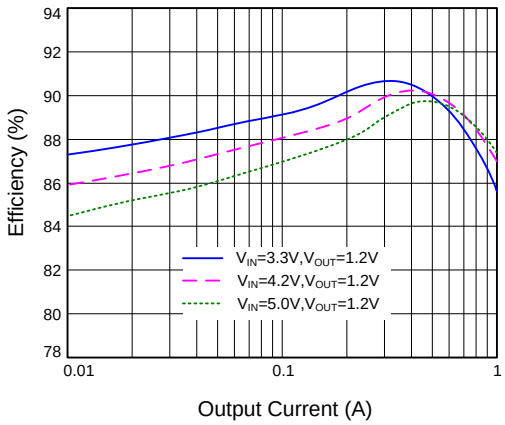
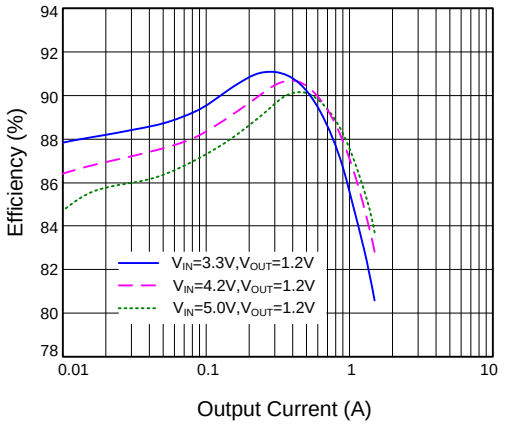
Typical Performance Characteristics

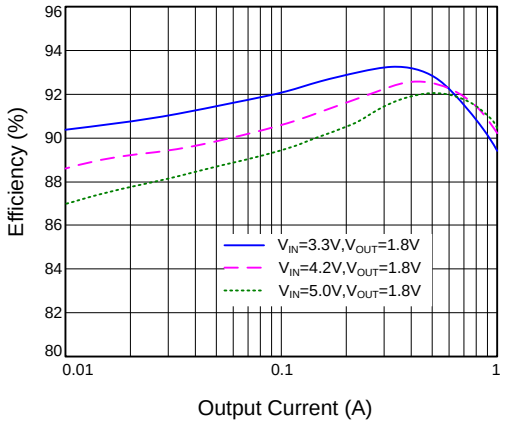
Efficiency vs. Output Current (CH1)



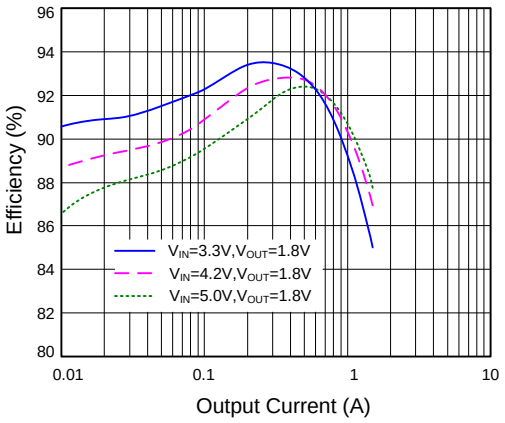
Efficiency vs. Output Current (CH2)



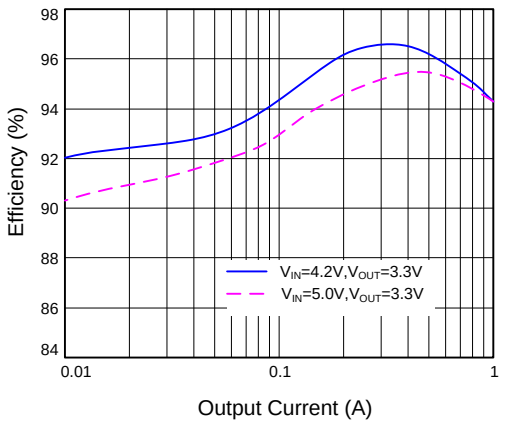
Efficiency vs. Output Current (CH1)



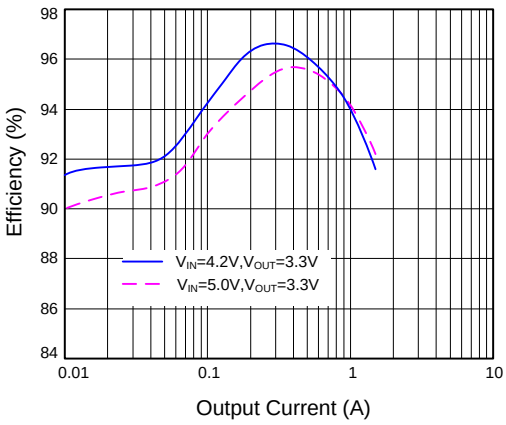
Efficiency vs. Output Current (CH2)



Efficiency vs. Output Current (CH1)



Efficiency vs. Output Current (CH2)



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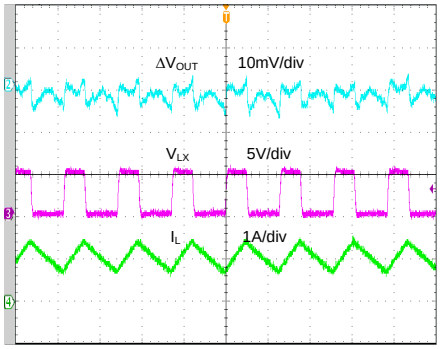
Output Ripple

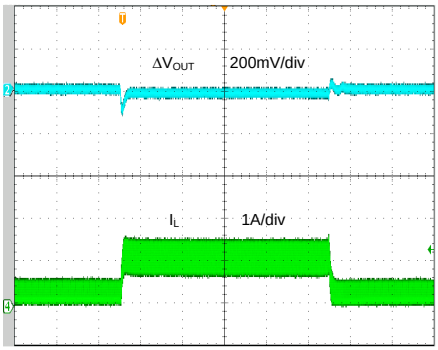
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=1.0A, CH1)



Time (400ns/div)

Load Transient

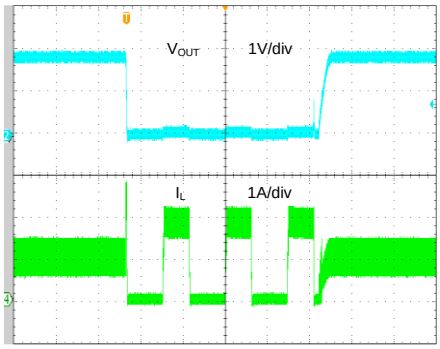
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0.1~1A, CH1)



Time (100μs/div)

Short Circuit Protection

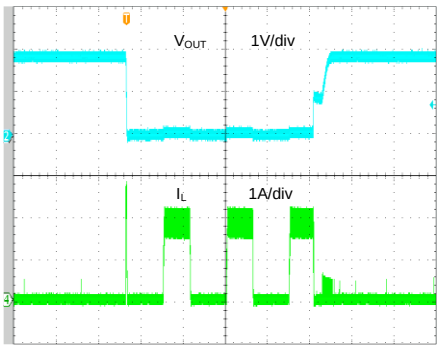
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=1.0A ~ short, CH1)



Time (2ms/div)

Short Circuit Protection

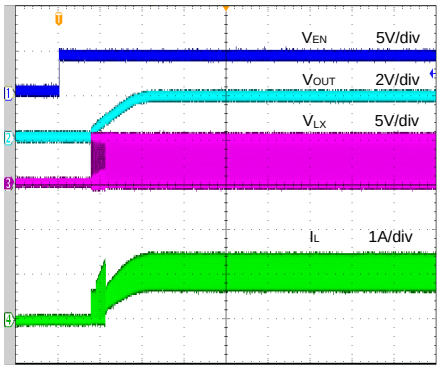
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0A ~ short, CH1)



Time (2ms/div)

Startup from Enable

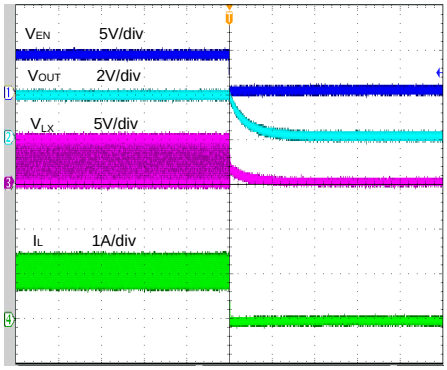
(V_{IN}=5.0V, V_{OUT}=1.8A, I_{OUT}=1.0A, CH1)



Time (400μs/div)

Shutdown from Enable

(V_{IN}=5.0V, V_{OUT}=1.8A, I_{OUT}=1.0A, CH1)



Time (40μs/div)

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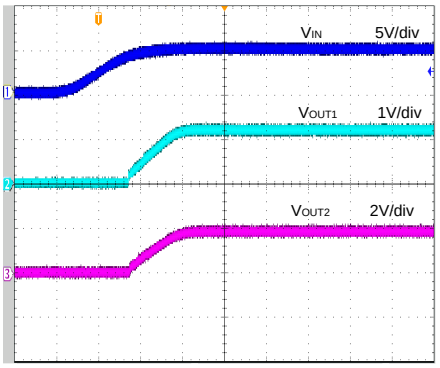
Startup from V_{IN}

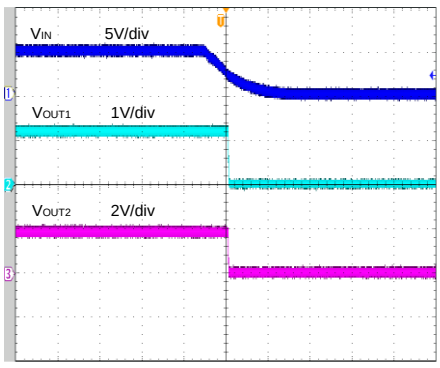
(V_{IN}=5.0V, V_{OUT1}=1.2V, V_{OUT2}=1.8V, I_{OUT1}=1.0A, I_{OUT2}=1.5A)



Time (400μs/div)

Shutdown from V_{IN}

(V_{IN}=5.0V, V_{OUT1}=1.2V, V_{OUT2}=1.8V, I_{OUT1}=1.0A, I_{OUT2}=1.5A)



Time (10ms/div)

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Operation

The SY20341 is a dual-output, high efficiency 2MHz synchronous step down DC/DC regulator, capable of delivering up to 1.0A and 1.5A for channel 1 and channel 2. The SY20341 operates over a wide input voltage range from 2.5V to 5.5V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

Applications Information

Because of the high integration in the SY20341, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L and feedback resistors (R_H and R_L) need to be selected for the targeted applications specifications.

Feedback Resistor Dividers R_H and R_L:

Choose R_H and R_L to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_H and R_L. A value of between 100k and 1M is highly recommended for both resistors. If R_H=120k is chosen, then R_L can be calculated to be:

$$R_L = \frac{0.6V \times R_H}{(V_{OUT}\text{-}0.6V)}$$

Input Capacitor C_{IN}:

This ripple current through input capacitor is calculated as:

$$I_{CIN_RMS} = I_{OUT} \times \sqrt{D(1\text{-}D)}$$

This formula has a maximum at V_{IN}=2V_{OUT} condition, where I_{CIN_RMS}=I_{OUT}/2. This simple worst-case condition is commonly used for DC/DC design.

With the maximum load current at 2.0A. A typical X5R or better grade ceramic capacitor with 10V rating and greater than 10µF capacitance can handle this ripple current well. To minimize the potential noise problem, ceramic capacitor should be placed really close to the V_{IN} and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and V_{IN}/GND pins.

Output Capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X7R or a better grade ceramic capacitor with 6V rating and greater than 10uF capacitance.

Output Inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where F_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY20341 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1\text{-}V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mohm to achieve a good overall efficiency.

Load Transient Considerations:

The SY20341 integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a 22pF ceramic cap in parallel with R_H may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.

Layout Design:

The layout design of SY20341 is relatively simple. For the best efficiency and to minimize noise problems, we should place the following components close to the IC: C_{IN}, L, R_H and R_L.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable. Reasonable vias are suggested to be placed

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underneath the ground pad to enhance the soldering quality and thermal performance.

2) Input cap must be close to Pins IN and GND. The loop area formed by input cap，IN, GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem. For the smallest loop area of C_{IN}, IN and GND, LX pin copper can pour area on internal or bottom layer.

4) The components R_H and R_L, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

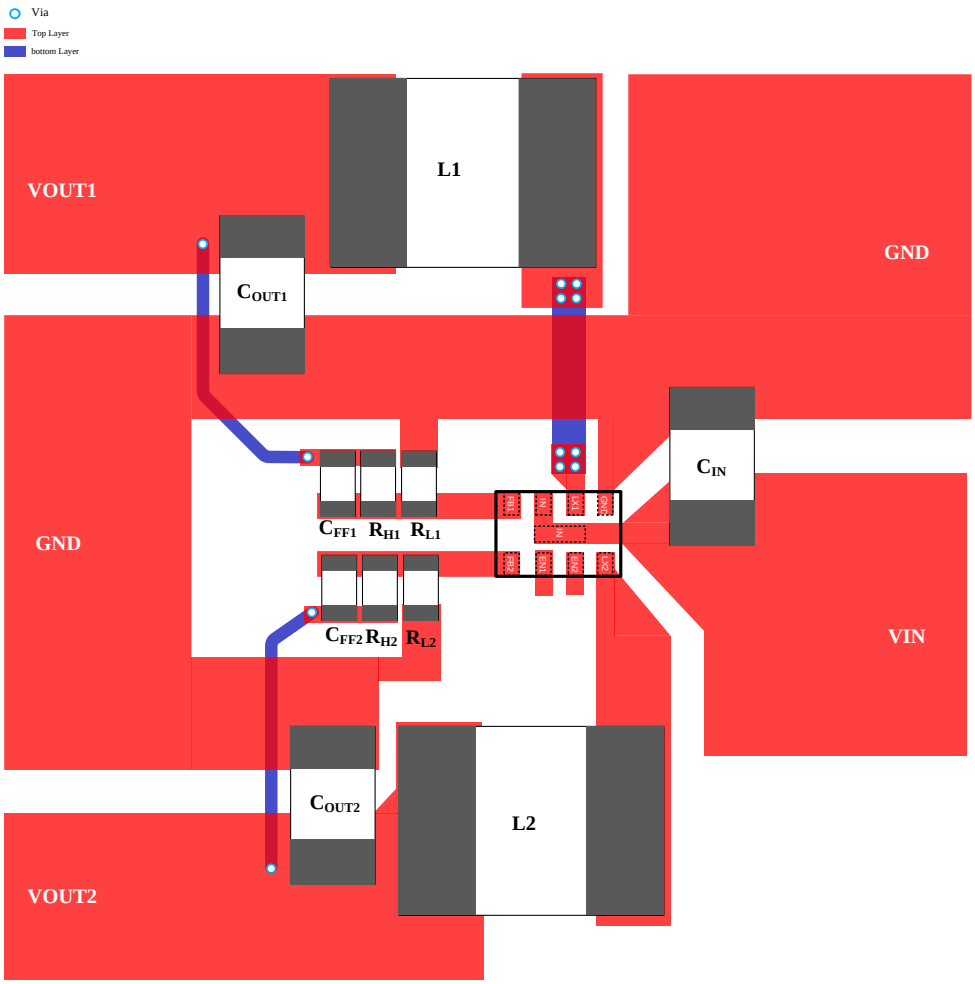

Figure2. PCB Layout Suggestion

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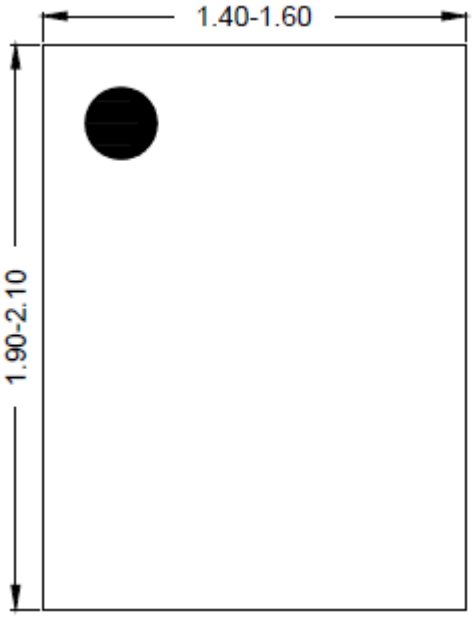
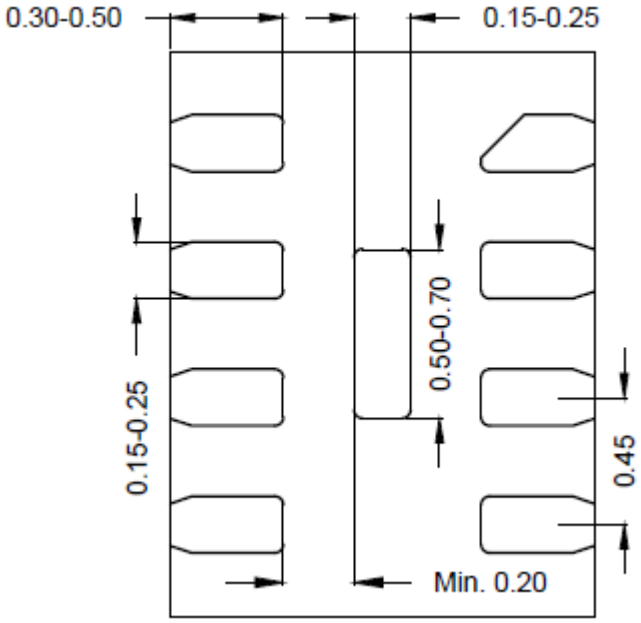
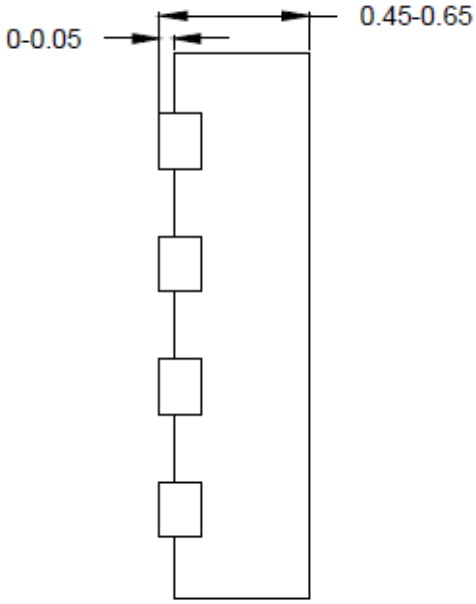
DFN2x1.5-8 Package Outline Drawing



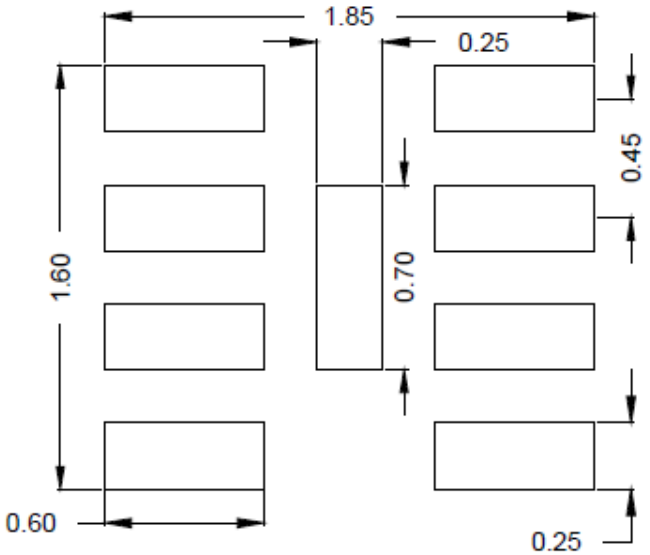
Top view



Bottom view



Side view



Recommended PCB layout
(Reference only)

Notes: **All dimension in MM and exclude mold flash & metal burr**

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