SY22778Y
Single Stage Buck PFC Regulator For LED Lighting

General Description

The SY22778Y is a single stage Buck PFC controller targeting at LED lighting applications. It integrates a 600V MOSFET to decrease physical volume. It adopts the proprietary control architecture to achieve an accurate regulation of LED current, unity power factor, and quasi-resonant valley turn-on high efficiency operation. It adopts special design to achieve quick start up and reliable protection for safety requirement.

It integrates open/short LED protection and eliminates the need for opto-coupler, thus minimizing the component count and board size.

Ordering Information

SY22778□(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY22778YAGC	DIP8	----

Features

- Integrated 600V MOSFET
- Valley Turn-on of the MOSFET to Achieve Low Switching Losses
- Power Factor >0.90 with Single-stage conversion
- Low start up current: 15μA typical
- Quick start up <500ms
- Reliable short LED and Open LED protection
- Power factor >0.90 with single-stage conversion
- RoHS Compliant and Halogen Free
- Compact package: DIP8

Applications

- LED lighting

Recommended operating output power		
Products	176~264Vac	90~132Vac
SY22778Y	32W @ V_{OUT}=100V	20W @ V_{OUT}=50V

Typical Applications

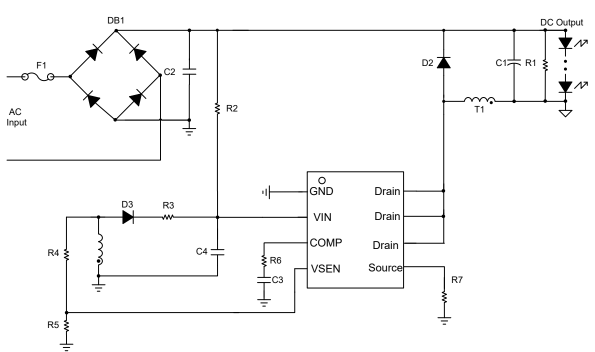


Figure 1. Schematic Diagram

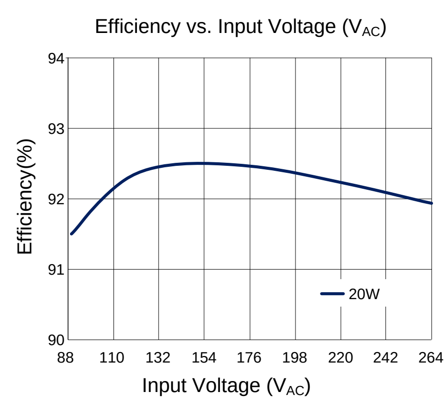
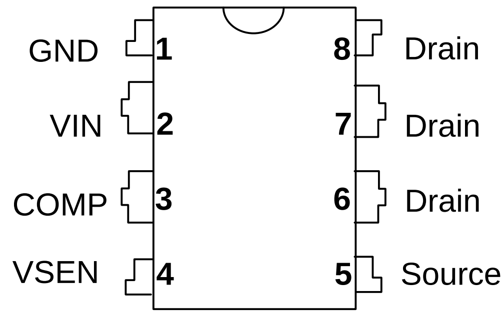


Figure 2. Efficiency vs Input Voltage

Pinout (top view)



(DIP8)

Top Mark: BBS xyz (device code: **BBS**, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
GND	1	Ground pin
VIN	2	Power supply pin. This pin also provides output over voltage protection along with VSEN pin.
COMP	3	Loop compensation pin. Connect a RC network across this pin and ground to stabilize the control loop.
VSEN	4	Inductor current zero-crossing detection pin. This pin receives the auxiliary winding voltage by a resister divider and detects the inductor current zero crossing point. This pin also provides over voltage protection and line regulation modification function simultaneously. If the voltage on this pin is above V_{VSEN_OVP}, the IC would enter over voltage protection mode. Good line regulation can be achieved by adjusting the upper resistor of the divider.
Source	5	Current sense pin. Connect this pin to the source of the switch. Connect the sense resistor across the source of the switch and the GND pin. (current sense resister R_S: $I_O = \frac{1}{2} \times \frac{V_{REF}}{R_S}$) .Also this pin used to detect transformer and secondary is short or not.
Drain	6/7/8	Drain of the internal power MOSFET.

Block Diagram

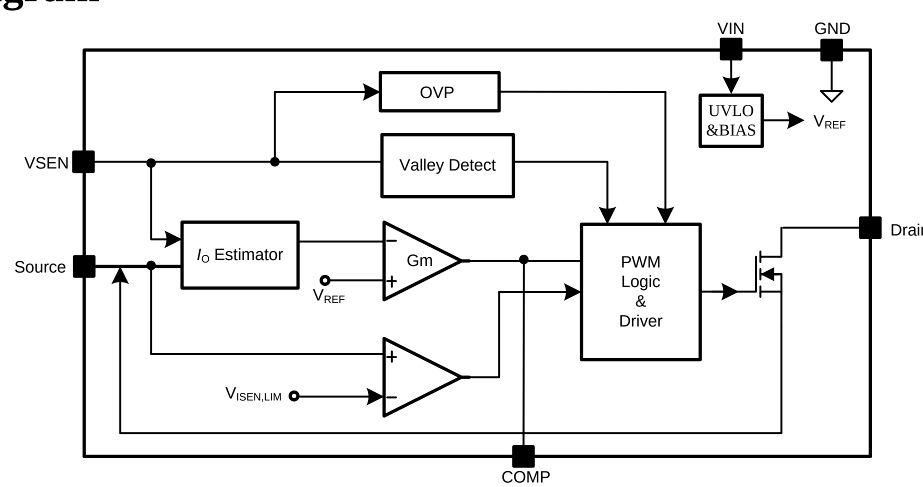


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

VIN -- -0.3V~25V
Supply Current I_{VIN} -- 15mA
VSEN-- -0.3V ~V_{IN}+0.3
Source, COMP --- -0.3~3.6V
Power Dissipation, @ T_A = 25°C DIP8---0.6W
Package Thermal Resistance (Note 2)
DIP8, θ_{JA} ---68°C/W
DIP8, θ_{JC} ---55°C/W
Junction Temperature Range --- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) --- 260°C
Storage Temperature Range -- -65°C to 150°C

Recommended Operating Conditions (Note 3)

VIN --- 9.5V~21V

Electrical Characteristics

(V_{IN} = 12V (Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VIN turn-on threshold	V_{VIN_ON}		19	20	21	V
VIN turn-off threshold	V_{VIN_OFF}		7.5	8.5	9.5	V
VIN OVP voltage	V_{VIN_OVP}			$V_{IN,ON}$+1.6V		V
Start up Current	I_{ST}	$V_{VIN}<V_{VIN\_OFF}$	10	15	21	μA
Shunt current in OVP mode	I_{VIN_OVP}	V_{VIN}=12V after $V_{VIN}>V_{VIN\_OVP}$	3.5	4.7	5.9	mA
Error Amplifier Section						
Internal reference voltage	V_{REF}		0.294	0.300	0.306	V
Current Sense Section						
Current limit voltage	V_{ISEN_LIMIT}		0.65	0.73	0.81	V
ON State Resistance	R_{DSON}	T_C=25°C		2.2		Ω
Continuous Drain Current	I_D	T_C=25°C		0.9		A
VSEN pin Section						
VSEN pin OVP voltage threshold	V_{VSEN_OVP}		1.43	1.5	1.57	V
PWM Section						
Max ON Time	T_{ON_MAX}	ISEN=0V		26		μs
Max OFF Time	T_{OFF_MAX}			150		μs
Blanking time for ON time	T_{ON_BLK}			350		ns
Blanking time for OFF time	T_{OFF_BLK}			1.8		μs
Maximum switching frequency	f_{MAX}			120		kHz
Thermal Section						
Thermal Shutdown Temperature	T_{SD}			150		ºC

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: Increase VIN pin voltage gradually higher than $V_{VIN,ON}$ voltage then turn down to 12V.

Operation

SY22778Y is a constant current Buck PFC regulator targeting at LED lighting applications.

It integrates a MOSFET with 600V breakdown voltage to decrease physical volume.

High power factor is achieved by constant on-time operation mode, with which the control scheme and the circuit structure are both simple.

Start up process is optimized inside SY22778Y, and quick start up (less than 500ms) is achieved without any additional circuit

In order to reduce the switching losses and improve EMI performance, Quasi-Resonant switching mode is applied, which means to turn on the power MOSFET at voltage valley; the start up current of SY22778Y is rather small (15μA typically) to reduce the standby power loss further; the maximum switching frequency is clamped to 120kHz to reduce switching losses and improve EMI performance when the converter is operated at light load condition.

SY22778Y provides reliable protections such as Short Circuit Protection (SCP), Open LED Protection (OLP), Over Temperature Protection (OTP), transformer shorted protection and power diode shorted protection, etc.
.
SY22778Y is available with DIP8

Applications Information

Start up

After AC supply or DC BUS is powered on, the capacitor C_{VIN} across VIN and GND pin is charged up by BUS voltage through a start up resistor R_{ST}. Once V_{VIN} rises up to V_{VIN_ON}, the internal blocks start to work and PWM output is enabled.

The output voltage is feedback by VSEN pin, which is taken as V_{FBV}. If V_{FBV} is lower than certain threshold V_{VSEN_ST}, the typical value of V_{VSEN_ST} is 0.75V, which means the output voltage is not built up, V_{COMP} is pulled up to high clamped; if V_{FBV} is higher than V_{VSEN_ST}, V_{COMP} is under charge of the internal gain modulator.

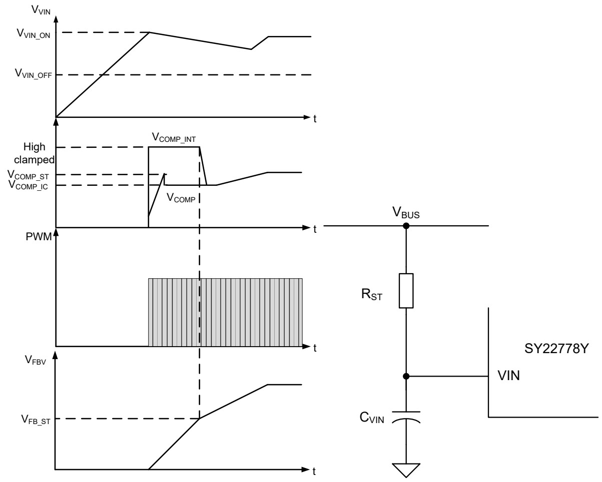


Fig4. Start up

This operation is aimed to build up enough output voltage for auxiliary winding bias supply as quickly as possible. It is enabled only one time just when V_{VIN} is over V_{VIN_ON}.

V_{COMP} is pre-charged by internal current source to V_{COMP_ST}, the typical value of V_{COMP_ST} is 1.0V and hold V_{COMP_IC} at this level until fast start up process is finished.

The start up resistor R_{ST} and C_{VIN} are designed by rules below:

(a) Preset start-up resistor R_{ST}, make sure that the current through R_{ST} is larger than I_{ST} and smaller than I_{VIN_OVP}

$$\frac{V_{BUS}}{I_{VIN\_OVP}} < R_{ST} < \frac{V_{BUS}}{I_{ST}}$$

Where V_{BUS} is the BUS line voltage.

(b) Select C_{VIN} to obtain an ideal start up time t_{ST}, and ensure the output voltage is built up at one time.

$$C_{VIN} = \frac{\left(\frac{V_{BUS}}{R_{ST}} - I_{ST}\right) \times t_{ST}}{V_{VIN\_ON}}$$

(d) If the C_{VIN} is not big enough to build up the output voltage at one time. Increase C_{VIN} and decrease R_{ST}, go back to step (a) and redo such design flow until the ideal start up procedure is obtained.

Shut down

After AC supply or DC BUS is powered off, the energy stored in the BUS capacitor will be discharged. When the auxiliary winding of Buck transformer can not supply enough energy to VIN pin, V_{VIN} will drop down. Once V_{VIN} is below $V_{VIN\text{-}OFF}$, the IC will stop working and V_{COMP} will be discharged to zero.

Constant-current control

The switching waveforms are shown in Fig.5. The output current I_{OUT} can be represented by,

$$I_{OUT} = \frac{I_{PK}}{2} \times \frac{t_{EFF}}{t_S}$$

Where I_{PK} is the peak current of the inductor; t_{EFF} is the effective time of inductor current rising and falling; t_S is the switching period.

I_{PK} and t_{EFF} can be detected by Source and VSEN pin, which is shown in Fig.6. These signals are processed and applied to the negative input of the gain modulator. In static state, the positive and negative inputs are equal.

$$V_{REF} = I_{PK} \times R_S \times \frac{t_{EFF}}{t_S}$$

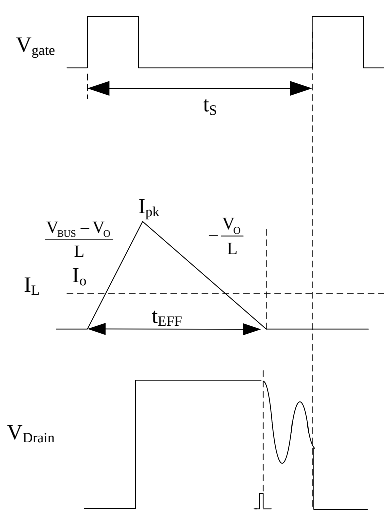


Fig.5 switching waveforms

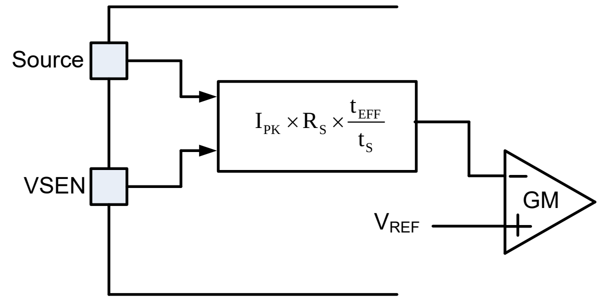


Fig.6 Output current detection diagram

Finally, the output current I_{OUT} can be represented by

$$I_{OUT} = \frac{V_{REF}}{R_S \times 2}$$

Where V_{REF} is the internal reference voltage; R_S is the current sense resistor.

V_{REF} is internal constant parameters; I_{OUT} can be programmed by R_S.

$$R_S = \frac{V_{REF}}{I_{OUT} \times 2}$$

Quasi-Resonant Operation

QR mode operation provides low turn-on switching losses for Buck converter.

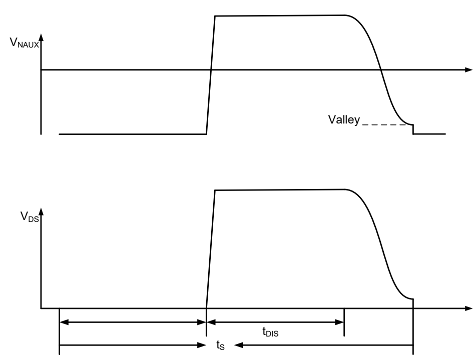


Fig.7 QR mode operation

The voltage across drain and source of the MOSFET is reflected by the auxiliary winding of the Buck transformer. VSEN pin detects the voltage across the auxiliary winding by a resistor divider. When the voltage across drain and source of the MOSFET is at voltage valley, the MOSFET would be turned on.

Over Voltage Protection (OVP) & Open LED Protection (OLP)

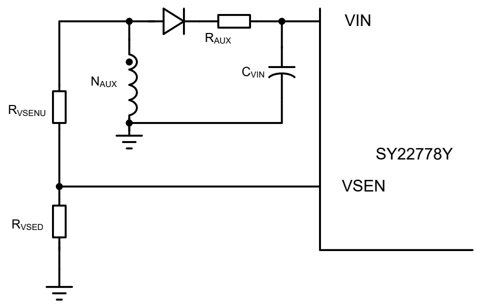


Fig8. OVP&OLP

The output voltage is reflected by the auxiliary winding voltage of the Buck transformer, and both VSEN pin and VIN pin provide over voltage protection function. When the load is null or large transient happens, the output voltage will exceed the rated value. When V_{VIN} exceeds V_{VIN_OVP} or V_{VSEN} exceeds V_{VSEN_OVP}, the over voltage protection is triggered and the IC will discharge V_{VIN} by an internal current source I_{VIN_OVP}. Once V_{VIN} is below V_{VIN_OFF}, the IC will shut down and be charged again by BUS voltage through start up resistor. If the over voltage condition still exists, the system will operate in hiccup mode.

Thus, the turns of the auxiliary winding N_{AUX} and the resistor divider is related with the OVP function.

$$\frac{V_{SEN\_OVP}}{V_{OVP}} = \frac{N_{AUX}}{N} \times \frac{R_{VSEND}}{R_{VSENU} + R_{VSEND}}$$

$$\frac{V_{VIN\_OVP}}{V_{OVP}} \geq \frac{N_{AUX}}{N}$$

Where V_{OVP} is the output over voltage specification; R_{VSENU} and R_{VSEND} compose the resistor divider. The turns ratio of N to N_{AUX} and the ratio of R_{VSENU} to R_{VSEND} could be induced from equation above.

Short Circuit Protection (SCP)

When the output is shorted to ground, the output voltage is clamped to zero. The voltage of the auxiliary winding is proportional to the output winding, so valley signal cannot be detected by VSEN. Without valley detection, MOSFET cannot be turned ON until maximum off time t_{OFF_MAX} is matched. If MOSFET is turned ON by t_{OFF_MAX} 64 times continuously, IC will be shut down and enter into hiccup mode.

If the output voltage is not low enough to disable valley detection in short condition, V_{VIN} will drop down without auxiliary winding supply. Once V_{VIN} is below V_{VIN_OFF}, the IC will shut down and be charged again by the BUS voltage through the start up resistor. If the short circuit condition still exists, the system will operate in hiccup mode.

Line regulation modification

The IC provides line regulation modification function to improve line regulation performance.

Due to the sample delay of Source pin and other internal delay, the output current increases with increasing input BUS line voltage. A small compensation voltage $\Delta V_{ISEN\text{-}C}$ is added to Source pin during ON time to improve such performance. This ΔV_{ISEN_C} is adjusted by the upper resistor of the divider connected to VSEN pin.

$$\Delta V_{ISEN\_C} = (V_{BUS} - V_{OUT}) \times \frac{N_{AUX}}{N} \times \frac{1}{R_{VSEN,U}} \times K_2 \times R_{K2}$$

Where R_{VSENU} is the upper resistor of the divider; k_2 is an internal constant as the modification coefficient, the typical value of k_2 is 0.1; R_{k2} is an internal feed-forward resistor, the typical value of R_{k2} is 170Ω.

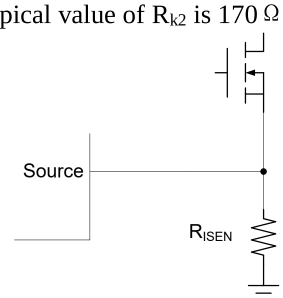


Fig9. Feed-forward resistor

Power design reference

A few applications are shown as below

Products	Input range	Output current	Application	Temperature rise
SY22778Y	176Vac~264Vac	0.40A	19W/T8	45℃
	176Vac~264Vac	0.30A	17W/T8	40℃
	176Vac~264Vac	0.30A	15W/T8	35℃
	90Vac~132Vac	0.30A	17W/T8	45℃
	90Vac~132Vac	0.30A	16W/T8	40℃
	90Vac~132Vac	0.30A	15W/T8	35℃

The test is operated in natural cooling condition at 25 ℃ ambient temperature.

Power Device Design

MOSFET and Diode

When the operation condition is with maximum input voltage and full load, the voltage stress of MOSFET and output power diode is maximized;

$$V_{MOS\_DS\_MAX} = \sqrt{2}V_{AC\_MAX}$$
$$V_{D\_R\_MAX} = \sqrt{2}V_{AC\_MAX}$$

Where V_{AC_MAX} is maximum input AC RMS voltage.
When the operation condition is with minimum input voltage and full load, the current stress of MOSFET and power diode is maximized.

Inductor (L)

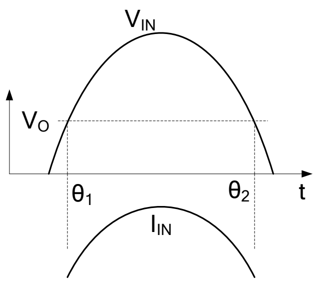


Fig.10 input waveforms

The power is transferred from AC input to output only when the input voltage is larger than output voltage in Buck converter. The input voltage and inductor current waveforms are shown in Fig.10, where θ_1 and θ_2 are the time that input voltage is equal to output voltage.

In Quasi-Resonant mode, each switching period cycle tS consists of three parts: current rising time t_1, current falling time t_2 and quasi-resonant time t_3 shown in Fig.11.

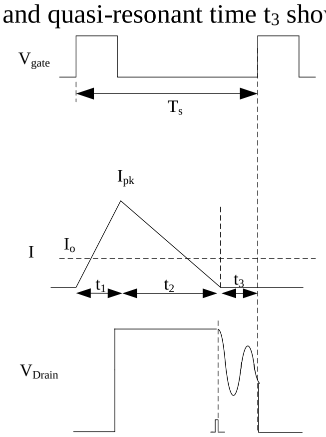


Fig.11 switching waveforms

The system operates in the constant on time mode to achieve high power factor. The ON time increases with the input AC RMS voltage decreasing and the load increasing. When the operation condition is with minimum input AC RMS voltage and full load, the ON time is maximized. On the other hand, when the input voltage is at the peak value, the OFF time is maximized. Thus, the minimum switching frequency $f_{S\text{-}MIN}$ happens at the peak value of input voltage with minimum input AC RMS voltage and maximum load condition; meanwhile, the maximum peak current through MOSFET and the transformer happens.

Once the minimum frequency $f_{S\text{-}MIN}$ is set, the inductance of the transformer could be calculated. The design flow is shown as below:

(a) Preset minimum frequency $f_{S\text{-}MIN}$

(b) Compute relative t_S, t_1

$$t_S = \frac{1}{f_{S\_MIN}}$$

$$t_1 = \frac{t_S \times (V_{OUT} + V_{DF})}{(\sqrt{2}V_{AC\_MIN} + V_{DF})}$$

$$t_2 = t_S - t_1$$

Where V_{DF} is the forward voltage of the diode

(c) Design inductance L

$$\theta_1 = \arcsin\left(\frac{V_{OUT}}{\sqrt{2}V_{AC\_MIN}}\right) \times \frac{1}{\pi} \times \frac{1}{2 \times f_{AC}}$$

$$\theta_2 = \frac{1}{2 \times f_{AC}} - \theta_1$$

$$L = \frac{\eta \times f_{AC} \times V_{OUT} \times t_1}{P_{OUT}} \times$$
$$[\sqrt{2}V_{AC\_MIN} \times \frac{\cos(2\pi f_{AC} \times \theta_1) - \cos(2\pi f_{AC} \times \theta_2)}{2\pi f_{AC}} - V_{OUT}(\theta_2 - \theta_1)]$$

Where η is the efficiency; P_{OUT} is rated full load power;

(d) Compute inductor maximum peak current $I_{L\text{-}PK\text{-}MAX}$.

$$I_{L\_PK\_MAX} = \frac{(\sqrt{2}V_{AC\_MIN} - V_{OUT}) \times t_1}{L}$$

Where $I_{L\text{-}PK\text{-}MAX}$ is maximum inductor peak current ;

(e) Compute RMS current of the inductor

$I_{L\_RMS\_MAX}$ is Inductor RMS current of whole AC period

$$I_{L\_RMS\_MAX}=\frac{t_1}{\sqrt{3}\times L}\sqrt{V_{AC\_MIN}{}^2+V_{OUT}{}^2-\frac{4\sqrt{2}V_{AC\_MIN}\times V_{OUT}}{\pi}}$$

(f) compute RMS current of the MOSFET

$$I_{L\_RMS\_MAX}=\sqrt{\frac{t_1}{3t_S}}\times\frac{t_1}{L}\sqrt{V_{AC\_MIN}{}^2+V_{OUT}{}^2-\frac{4\sqrt{2}V_{AC\_MIN}\times V_{OUT}}{\pi}}$$

Inductor design (N, N_{AUX})

the parameters below are necessary:

Necessary parameters	
Inductance	L
inductor maximum current	$I_{L\_PK\_MAX}$
inductor maximum RMS current	$I_{L-RMS-MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e.

(b) Preset the maximum magnetic flux ΔB

ΔB=0.22~0.26T

(c) Compute primary turn N

$$N=\frac{L_M\times I_{L\_PK\_MAX}}{\Delta B\times A_e}$$

(d) Compute auxiliary turn N_{AUX}

$$N_{AUX}=N\times\frac{V_{VIN}}{V_{OUT}}$$

Where V_{VIN} is the working voltage of VIN pin.

(e) Select an appropriate wire diameter with $I_{L-RMS-MAX}$, select appropriate wire to make sure the current density ranges from 4A/mm^2 to 10A/mm^2.

(f) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

Output capacitor C_{OUT}

Preset the output current ripple ΔI_{OUT}, C_{OUT} is induced by

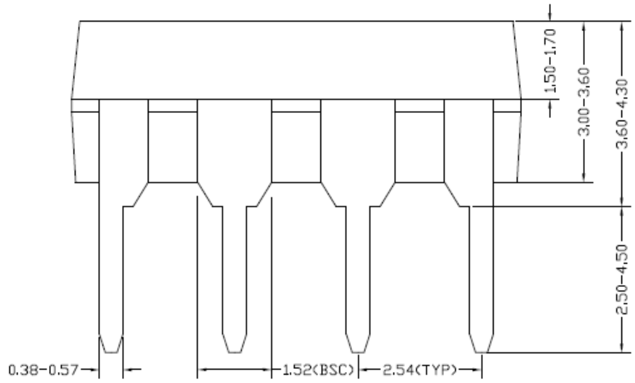
$$C_{OUT}=\frac{\sqrt{(\frac{2I_{OUT}}{\Delta I_{OUT}})^2-1}}{4\pi f_{AC}R_{LED}}$$

Where I_{OUT} is the rated output current; ΔI_{OUT} is the demanded current ripple; f_{AC} is the input AC supply frequency; R_{LED} is the equivalent series resistor of the LED load.

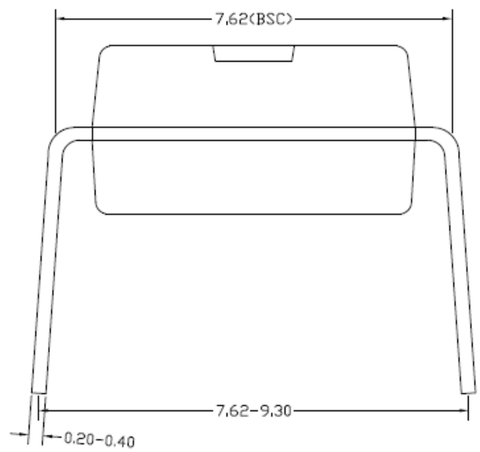
Single fault design

If VSEN pin is shorted to GND pin or floating, valley detection is failed, which is similar to SLP, the system will operate in hiccup mode.

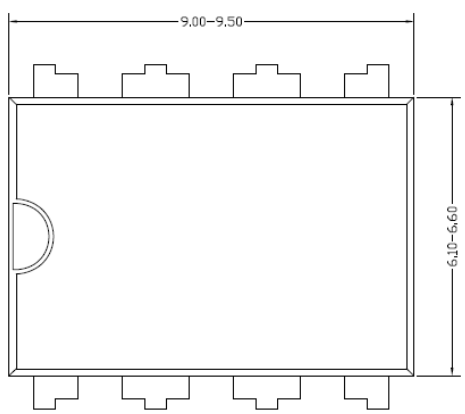
DIP8 Package Outline



Side view A



Side view B



Top view

Notes: All dimension in MM and exclude mold flash & metal burr

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