

## High Efficiency, 3.5A, Multi-Cell Li-Ion Battery Charger

### General Description

The SY20764B is a 4-14V input, 3.5A multi-cell Li-ion battery step-down charger. The charge current up to 3.5A can be programmed by using the external resistor for different portable applications. It also has a programmable charge timeout and adaptive input power limit for safety battery charge operation. It consists of 16V rating reverse blocking FET and power switching FETs with extremely low on resistance to achieve high charge efficiency and simple peripheral circuit design.

The SY20764B is available in QFN3×3 package to minimize the PCB layout size for wide portable application.

### Ordering Information

SY20764 □(□)□□  
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 Temperature Code  
 Package Code  
 Optional Spec Code

Ordering Number	Package type	Note
SY20764BQDC	QFN3×3-16	

### Features

- Integrated Synchronous Buck and Reverse Blocking FET with 16V Rating
- Adaptive Input Power Limit for 4-14V Wide Input Voltage
- Maximum 3.5A Programmable Charge Current
- 4.25V and 4.4V Constant Voltage Selectable
- +/-0.5% Cell Voltage Accuracy
- Support Single-cell or Two-cell Battery Pack
- External Shutdown Function
- Input Voltage UVLO and OVP
- Thermal Fold-back Protection
- Over Temperature Protection
- Battery Short Protection
- Programmable Charge Timeout
- Charge Status Indication
- Low Profile QFN3×3 Package for Portable Applications

### Applications

- Power Bank
- Cellular Telephones, PDA, MP3 Players, MP4 Players
- PSP Game Players, NDS Game Players

### Typical Applications

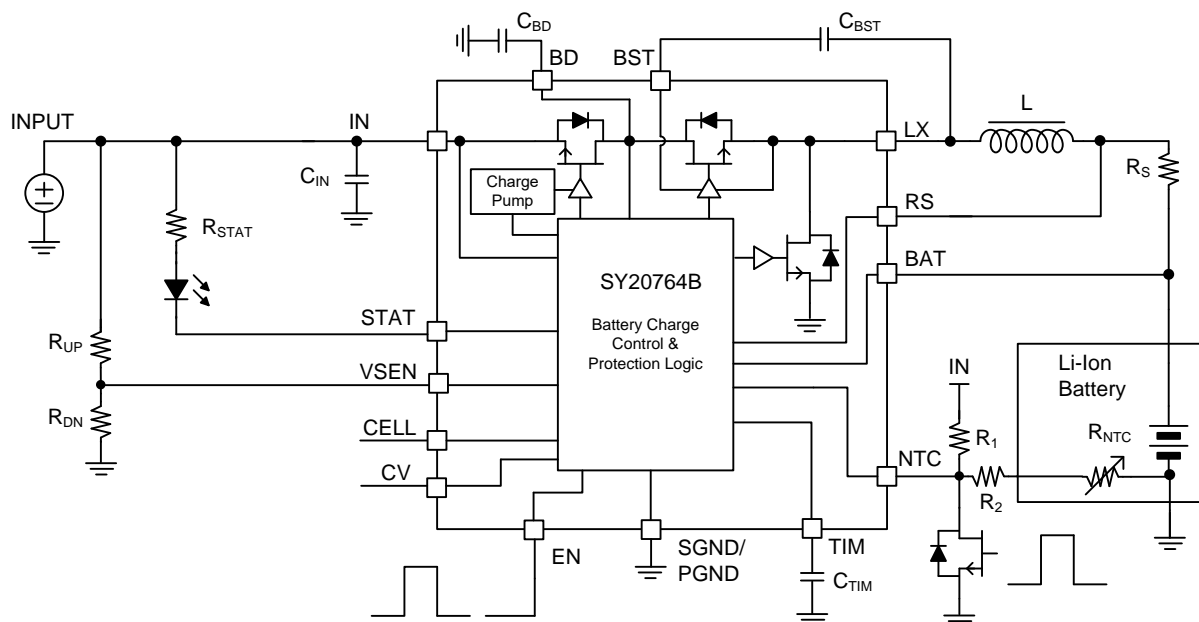
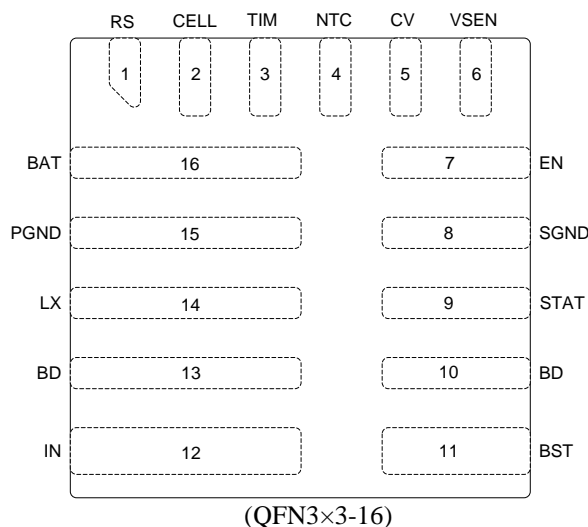


Figure1. Schematic Diagram

## Pinout (top view)



Top Mark: **CQRxyz**, (Device code: CQR, *x=year code*, *y=week code*, *z=lot number code*)

Pin Name	Pin Number	Description
RS	1	Charge current sense resistor positive pin. The sensed voltage drop between RS and BAT is used for charge current regulation and charge termination detection.
CELL	2	Battery voltage selection pin. Floating for two cells battery and grounding for single cell battery. CELL pin can't be pulled high to any bias voltage higher than 3.3V.
TIM	3	Charge time-out programming pin. Connect this pin with a capacitor to ground to program the time-out protection threshold. Internal current source charge the capacitor for TC mode and fast charge (CC&CV) mode's charge time limit. TC charge time limit is about 1/9 of fast charge time.
NTC	4	Battery thermal sense pin. The voltage on the NTC pin is sensed for battery thermal protection. UTP threshold is typical 76% $V_{IN}$ and OTP threshold is typical 45% $V_{IN}$ . NTC pin also can be used for the adaptive input power limit reference refresh. The adaptive input power limit threshold will be refreshed when NTC is pulled low for more than 100ms. SY20764B sets the charge current to the trickle value, then IC refreshes the adaptive input power limit threshold according the input voltage. For higher than 6V input, IC clamps the input voltage at $V_{IN}-0.65V$ by regulating the duty cycle of Buck converter. For lower than 6V input, the clamped input voltage is set by VSEN pin.
CV	5	Battery CV voltage selection pin.
VSEN	6	Input voltage sense pin for adaptive input power limit. If the voltage drops to internal 1.21V reference voltage, the $V_{IN}$ will be clamped to setting value and input current will be limited.
EN	7	Enable control pin. High logic for enable on and low logic for enable off.
SGND	8	Signal ground pin.
STAT	9	Charge status indication pin. Open drain pin. Pull high to IN thru a LED to indicate the charge in process. When the charge is done, LED is off.
BD	10, 13	Connect to the drain of internal blocking FET. Bypass at least 10uF ceramic capacitor to GND.
BST	11	Boot-strap pin. Supply main FET's gate driver. Decouple this pin to LX with 0.1uF ceramic cap.

IN	12	DC power input pin. Connect a MLCC from this pin to ground to decouple high harmonic noise. This pin has OVP and UVLO function to make the charger operate within safe input voltage area.
LX	14	Switch node pin. Connect to external inductor.
PGND	15	Power ground pin.
BAT	16	Battery voltage sense pin.

## Absolute Maximum Ratings (Note 1)

IN, RS, BAT, LX, NTC, STAT, BD, EN, CV, VSEN ----- -0.3V to 18V  
 TIM, CELL----- -0.3V to 4V  
 BST-LX ----- -0.3V to 4V  
 RS-BAT ----- -0.3V to 0.3V  
 LX Pin Current Continuous ----- 5A  
 Power Dissipation,  $P_D$  @  $T_A = 25^\circ\text{C}$ , QFN3×3----- 2.1W  
 Package Thermal Resistance (Note 2)  
 $\theta_{JA}$  ----- 48  $^\circ\text{C/W}$   
 $\theta_{JC}$  ----- 4  $^\circ\text{C/W}$   
 Junction Temperature Range -----  $-40^\circ\text{C}$  to  $125^\circ\text{C}$   
 Lead Temperature (Soldering, 10 sec.) -----  $260^\circ\text{C}$   
 Storage Temperature Range -----  $-65^\circ\text{C}$  to  $150^\circ\text{C}$

## Recommended Operating Conditions (Note 3)

IN ----- 4V to 14V  
 RS, BAT, LX, NTC, STAT, BD, EN, CV, VSEN-----0V to16V  
 TIM, CELL----- 0V to 3.3V  
 BST-LX ----- 0V to 3.3V  
 RS-BAT ----- -0.25V to 0.25V  
 LX Pin Current Continuous ----- 3.5A  
 Ambient Temperature Range -----  $-40^\circ\text{C}$  to  $85^\circ\text{C}$

## Electrical Characteristics

T<sub>A</sub>=25°C, V<sub>IN</sub>=5V, GND=0V, C<sub>IN</sub>=10μF, L=2.2μH, R<sub>S</sub>=7.1mΩ, C<sub>TIM</sub>=330nF, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Bias Supply (V <sub>IN</sub> )						
Supply Voltage Operation Range	V <sub>IN</sub>		4		14	V
Input Voltage Lockout Threshold	V <sub>UVLO</sub>	V <sub>IN</sub> rising and measured from IN to ground			4	V
Input Voltage Lockout Hysteresis	ΔV <sub>UVLO</sub>	Measured from IN to ground		0.2		V
Input Over Voltage Protection	V <sub>IN_OVP</sub>	V <sub>IN</sub> rising and measured from IN to ground	13.5			V
Input Over Voltage Protection Hysteresis	ΔV <sub>OVP</sub>	Measured from IN to ground		0.5		V
Quiescent Current						
Battery Discharge Current	I <sub>BAT</sub>	V <sub>IN</sub> absent or EN=Low		5	10	μA
Input Quiescent Current	I <sub>IN</sub>	Disable charge		0.8	1.1	mA
Oscillator and PWM						
Switching Frequency	f <sub>SW</sub>			500		kHz
Power MOSFET						
R <sub>DS(ON)</sub> of Main N-FET	R <sub>NFET_M</sub>			25		mΩ
R <sub>DS(ON)</sub> of Rectified N-FET	R <sub>NFET_R</sub>			45		mΩ
R <sub>DS(ON)</sub> of Blocking N-FET	R <sub>NFET_B</sub>			35		mΩ
Voltage Regulation						
Battery Charge Voltage	V <sub>BAT_REG</sub>	1-cell battery, V <sub>CV</sub> <0.4V	4.227	4.248	4.269	V
		1-cell battery, V <sub>CV</sub> >1.5V	4.378	4.4	4.422	
		2-cell battery, V <sub>CV</sub> <0.4V	8.455	8.497	8.539	
		2-cell battery, V <sub>CV</sub> >1.5V	8.756	8.8	8.844	
Recharge Threshold Refer to V <sub>BAT_REG</sub>	ΔV <sub>RCH</sub>	1-cell battery	50	100	150	mV
		2-cell battery	100	200	300	
Trickle Charge Rising Edge Threshold	V <sub>TRK</sub>	1-cell battery	2.73	2.83	2.93	V
		2-cell battery	5.46	5.66	5.86	
Adaptive Input Current REF Modify						
NTC Voltage Threshold for Adaptive Input Current Reference Refresh	V <sub>NTC</sub>	NTC falling edge	0.4			V
NTC Low Time to Enable the Adaptive Input Current Refresh	t <sub>DET</sub>	Low pulse width		100		ms
Charge Current						
Charge Current Accuracy for Constant Current Mode	I <sub>CC</sub>	I <sub>CC</sub> =25mV/R <sub>S</sub>	-10%		10%	
Charge Current Accuracy for Trickle Current Mode	I <sub>TC</sub>	I <sub>TC</sub> =2.5mV/R <sub>S</sub>	-50%		50%	
Termination Current	I <sub>TERM</sub>	I <sub>TERM</sub> =2.5mV/R <sub>S</sub>	-50%		50%	
Output Voltage OVP						
Output Voltage OVP Threshold	V <sub>O_OVP</sub>		105%	110%	115%	V <sub>BAT_REG</sub>
Adaptive Input Power Limit Reference						
Reference for Adaptive Input Power Limit	V <sub>SEN</sub>		1.18	1.21	1.24	V
The Adaptive Input Power Limit Reference is V <sub>IN</sub> -Δ V <sub>AICL</sub>	ΔV <sub>AICL</sub>	NTC pull low than 100ms and V <sub>IN</sub> is higher than 6V		650		mV

Timer						
Trickle Current Charge Timeout	t <sub>TC</sub>		0.34	0.5	0.67	hour
Constant Current Charge Timeout	t <sub>CC</sub>		3.1	4.5	6.2	hour
Charge Mode Change Delay Time	t <sub>MC</sub>			30		ms
Termination Delay Time	t <sub>TERM</sub>			30		ms
Recharge Time Delay	t <sub>RCHG</sub>			30		ms
Short Circuit Protection						
Output Short Protection Threshold, Falling Edge	V <sub>SHORT</sub>		1.70	2.00	2.30	V
Auto Shut Down						
Auto Shutdown Voltage Threshold	V <sub>ASD</sub>	V <sub>IN</sub> fall, Measured from IN to BAT	40	110	180	mV
Auto Shutdown Voltage Threshold Hysteresis	ΔV <sub>ASD</sub>	Measured from IN to BAT		65		
Logical Control						
High Level Logic for Enable Control	V <sub>ENH</sub>		1.5			V
Low Level Logic for Enable Control	V <sub>ENL</sub>				0.4	
High Level Logic for CV	V <sub>CVH</sub>		1.5			V
Low Level Logic for CV	V <sub>CVL</sub>				0.4	
Battery Thermal Protection NTC						
Under Temperature Protection	V <sub>NTC_UTP</sub>		75%	76%	77%	V <sub>IN</sub>
Under Temperature Protection Hysteresis	V <sub>NTC_UTP_HYS</sub>	Falling edge		5%		
Over Temperature Protection	V <sub>NTC_OTP</sub>		44%	45%	46%	
Over Temperature Protection Hysteresis	V <sub>NTC_OTP_HYS</sub>	Rising edge		1.5%		
Thermal Fold-back and Thermal Shutdown						
Thermal Fold-back Threshold	T <sub>Fold</sub>	Rising edge		120		°C
Thermal Fold-back Hysteresis	T <sub>FoldHYS</sub>			20		°C
Thermal Fold-back Ratio	I <sub>Fold</sub>			0.25		I <sub>CC</sub>
Thermal Shutdown Temperature	T <sub>SD</sub>	Rising edge		160		°C
Thermal Shutdown Temperature Hysteresis	T <sub>SDHYS</sub>			30		°C

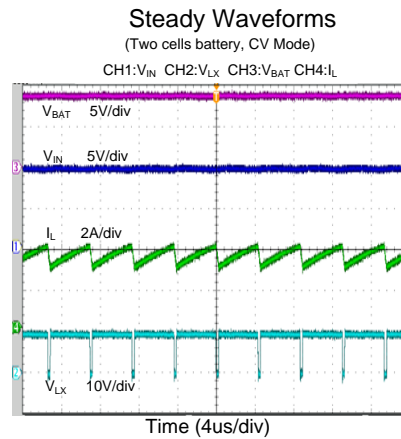
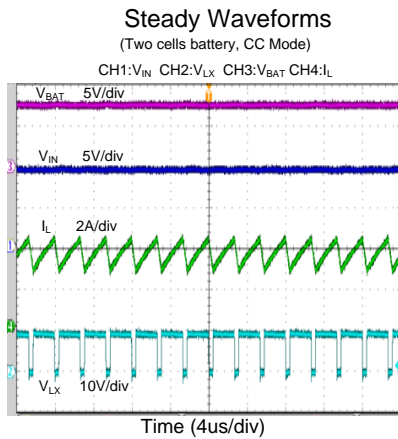
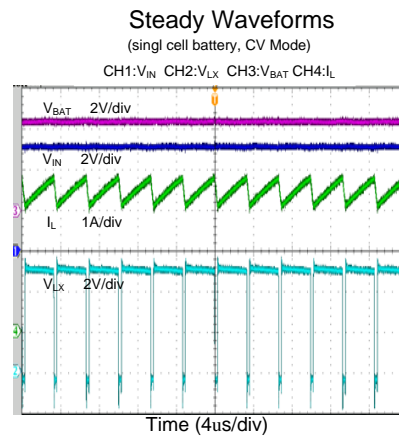
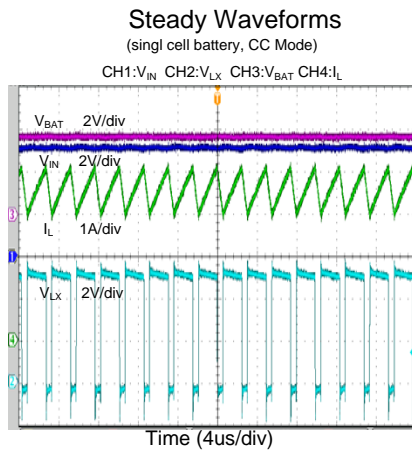
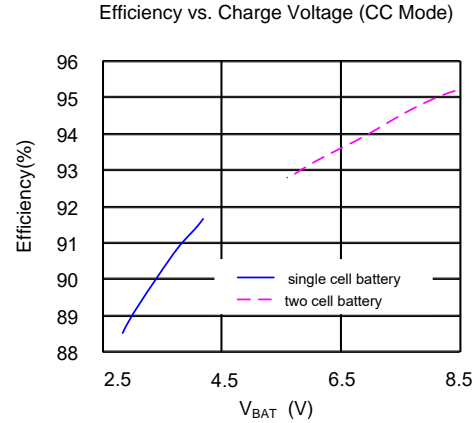
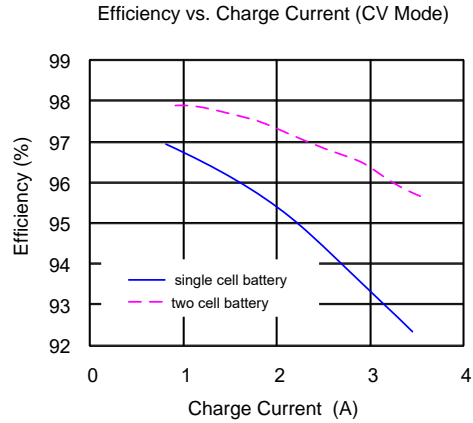
**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:** θ<sub>JA</sub> is measured in the natural convection at T<sub>A</sub> = 25°C on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

**Note 3:** The device is not guaranteed to function outside its operating conditions

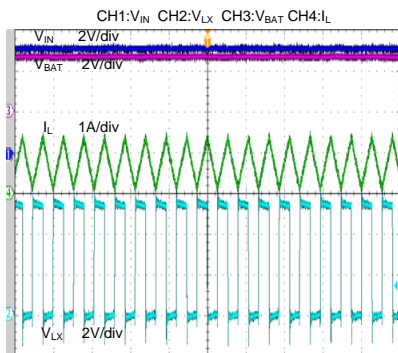
## Typical Performance Characteristics

( $T_A=25^{\circ}\text{C}$ ,  $V_{IN}=5\text{V}$ ,  $V_{BAT}=3.6\text{V}$  for single-cell battery application.  $V_{IN}=9\text{V}$ ,  $V_{BAT}=7.6\text{V}$  for two-cell battery application.  $R_S=7.1\text{m}\Omega$ ,  $C_{TIM}=330\text{nF}$ , unless otherwise specified. )



## Steady Waveforms

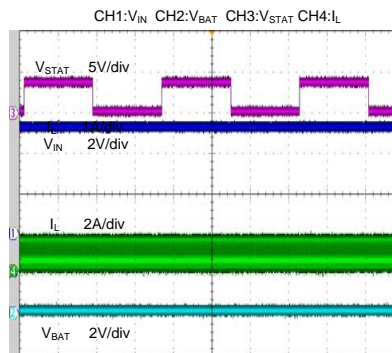
(TC Mode)



Time (4us/div)

## Steady Waveforms

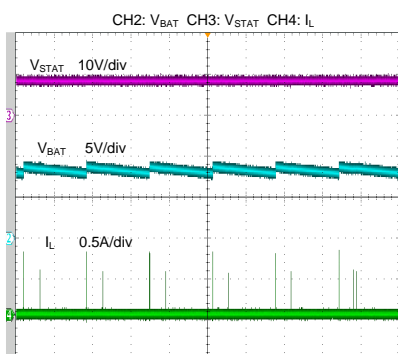
(Short Mode)



Time (200ms/div)

## Steady Waveform When No Battery

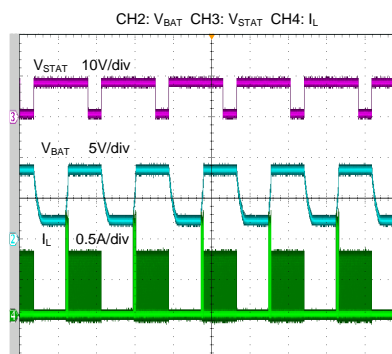
(NTC=50% V<sub>IN</sub>, No battery)



Time (100ms/div)

## Steady Waveform

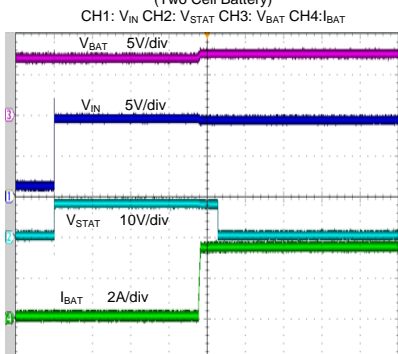
(NTC=50% V<sub>IN</sub>, 100mA load to BAT, V<sub>BAT</sub>=3V)



Time (100ms/div)

## Power On

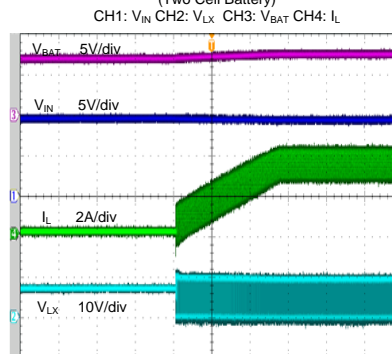
(Two Cell Battery)



Time (200ms/div)

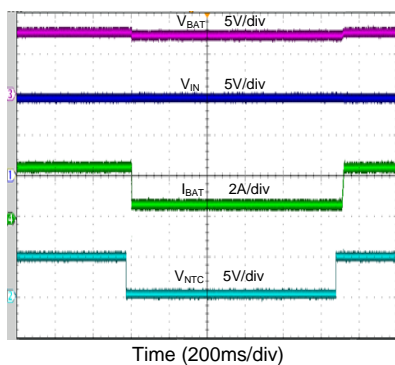
## Soft Start

(Two Cell Battery)

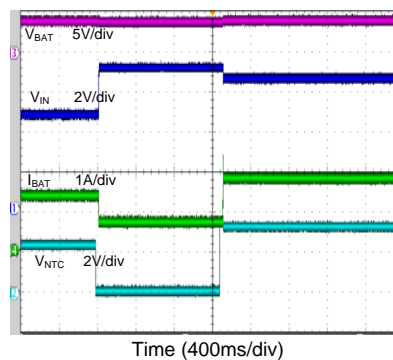


Time (4ms/div)

Low Pulse on NTC Pin  
 ( $V_{IN}=9V$   $V_{BAT}=7.6V$ )  
 CH1:  $V_{IN}$  CH2:  $V_{NTC}$  CH3:  $V_{BAT}$  CH4:  $I_{BAT}$



Adaptive Input Power Limit Reference Refresh  
 (Input Adapter changes to 7V/1A  $V_{BAT}=3.6V$ )  
 CH1:  $V_{IN}$  CH2:  $V_{NTC}$  CH3:  $V_{BAT}$  CH4:  $I_{BAT}$





## General Function Description

The SY20764B is a 4V-14V input, 3.5A step-down Multi-cell Li-Ion battery charger, which integrates reverse blocking FET, 500 kHz synchronous buck and full protection functions. The charge current up to 3.5A can be programmed by using the external resistor for different portable applications. It also has a programmable charge timeout and adaptive input power limit for safety battery charge operation. It consists of 16V rating FETs with extremely low ON resistance to achieve high charge efficiency and simple peripheral circuit design.

### Charging Status Indication Description

STAT is an open drain pin and a pull up resistor is needed for charging status indication. Connect a LED from IN to STAT pin, LED ON means Charge-in-Process, LED OFF means Charge Done, LED Flashing with 1.3Hz means Fault Mode.

1. Charge-in-Process – Pull and keep STAT pin to Low;
2. Charge Done – Pull and keep STAT pin to High;
3. Fault Mode – Output high and low voltage alternatively with 1.3Hz frequency. The faults include input OVP, BAT OVP, BAT short, BAT UTP, BAT OTP, time-out and thermal shutdown.

## Switching Mode Buck Charger Basic Operation Description

### Switching Mode Control Strategy

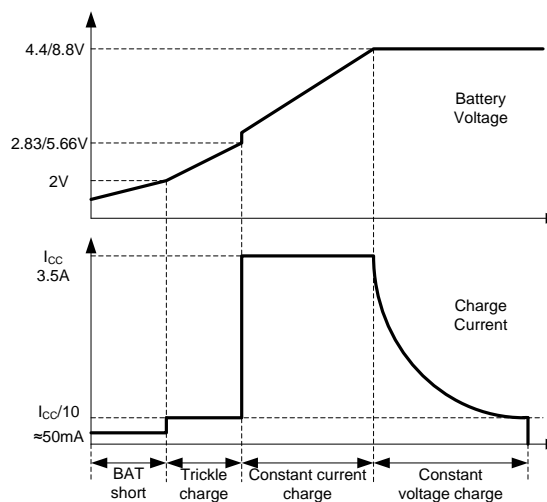
The SY20764B utilizes quasi-fixed frequency control to simplify the internal close-loop compensation design. The quasi-fixed frequency settled at 500kHz is easy for the size minimization of peripheral circuit design. During the light load operation, the OFF time of the main switch is going to be stretched to achieve frequency fold back.

### Operation Principle

The SY20764B will work as a synchronous Buck mode battery charger when the adapter is present. It utilizes 500kHz switching frequency to minimize the PCB design.

The charger will operate in battery short mode, trickle charge mode, constant current charge mode and constant voltage charge mode according to the battery voltage. The charge current in every mode is showed in following charge curve. In constant voltage mode, if charge current is lower than

termination current, the charger will stop charging until battery voltage drops to recharge voltage.



### Basic Adaptive Input Power Limit Principle

The SY20764B can limit the input power adaptively and adjust this threshold according to the input voltage. It will automatically decrease charge current when IN voltage drops to adaptive input power limit reference  $V_{REF}$ .

For typical 5V adapter,  $V_{REF}$  is set by VSEN pin, that is calculated as:

$$V_{REF} = 1.21 \times \frac{R_{UP} + R_{DN}}{R_{DN}}$$

If IN voltage is higher than 6V,  $V_{REF}$  is calculated as:

$$V_{REF} = V_{IN} - \Delta V_{AICL}$$

Where  $\Delta V_{AICL}$  is 0.65V typically.

$V_{IN}$  is the input voltage when adapter insert.  $V_{REF}$  can be modified after a more than 100ms low pulse on NTC pin if the adapter is always present.

When NTC is pulled low, the charge current will be set to the trickle value; battery thermal protection and adaptive input power limit function will be disabled.

### Full Charger Protections Description

In charge mode, the SY20764B has full protection to protect the IC and the battery.

**Input Over Voltage Protection** –The SY20764B has IN over voltage protection. It will turn off switching charger when input OVP occurs. IC will auto recover normal operation when fault removes.

**BAT Over Voltage Protection**—The SY20764B will stop charging when BAT OVP occurs. IC will auto recover normal operation when fault removes.

**Timeout Protection**— The charger can detect a bad battery. It will stop charge and latch off when the charger works over safety time which is set by  $C_{TIM}$ . Only recycling the input can release this fault.

**Battery Thermal Protection**— When NTC voltage is lower than OTP threshold or higher than UTP threshold, the converter will stop switching. IC will auto recovery when fault removes.

**Thermal Shutdown Protection**— The IC will stop operation when the junction temperature is higher than 160°C. It will auto recover normal when fault removes.

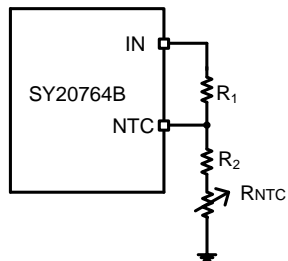
## Applications Information

Because of the high integration of the SY20764B, the application circuit based on this regulator IC is rather simple. Only input capacitor  $C_{BD}$ , output capacitor  $C_{OUT}$ , inductor  $L$ , NTC resistors  $R_1$ ,  $R_2$ , charging current sense resistor  $R_s$  and timer capacitor  $C_{TIM}$  need to be selected for the targeted applications specifications.

### NTC Resistor

The SY20764B monitors battery temperature by measuring the input voltage and NTC voltage. The controller triggers the UTP or OTP when the ratio  $K$  ( $K = V_{NTC}/V_{IN}$ ) reaches the threshold of UTP ( $K_{UT}$ ) or OTP ( $K_{OT}$ ). The temperature sensing network is showed as below.

Choose  $R_1$  and  $R_2$  to program the proper UTP and OTP points.



The calculation steps are:

1. Define  $K_{UT}$ ,  $K_{UT} = 75 \sim 77\%$
2. Define  $K_{OT}$ ,  $K_{OT} = 44 \sim 46\%$
3. Assume the resistance of the battery NTC thermistor is  $R_{UT}$  at UTP threshold and  $R_{OT}$  at OTP threshold.

4. Calculate  $R_2$ ,

$$R_2 = \frac{K_{OT}(1-K_{UT})R_{UT}-K_{UT}(1-K_{OT})R_{OT}}{K_{UT}-K_{OT}}$$

5. Calculate  $R_1$

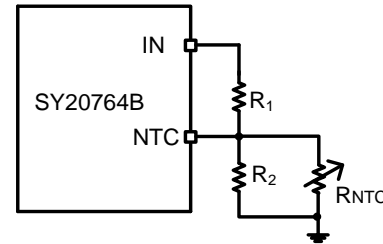
$$R_1 = (1/K_{OT}-1)(R_2+R_{OT})$$

If choose the typical values  $K_{UT} = 76\%$  and  $K_{OT} = 45\%$ , then

$$R_2 = 0.348R_{UT} - 1.348R_{OT}$$

$$R_1 = 1.222(R_2 + R_{OT})$$

The SY20764B accepts flexible NTC divider circuits. For below method,  $R_1$  and  $R_2$  can be calculated by below equations.



$$R_2 = \frac{R_{OT} \times R_{UT}(K_{UT}-K_{OT})}{K_{OT} \times K_{UT}(R_{OT}-R_{UT}) + R_{UT} \times K_{OT} - R_{OT} \times K_{UT}}$$

$$R_1 = \frac{R_2 \times R_{UT}(1-K_{UT})}{K_{UT} \times (R_2 + R_{UT})}$$

If choose the typical values  $K_{UT} = 76\%$  and  $K_{OT} = 45\%$ , then

$$R_2 = \frac{0.31R_{UT} \times R_{OT}}{0.108 \times R_{UT} - 0.418 \times R_{OT}}$$

$$R_1 = \frac{0.316R_2 \times R_{UT}}{R_{UT} + R_2}$$

### Charging Current Sense Resistor $R_s$

The charging current sense resistor  $R_s$  is calculated as below:

$$R_s = \frac{25mV}{I_{CC}}, \quad \text{Unit: } m\Omega$$

Where the  $I_{CC}$  is the battery constant charging current, unit: A.

### Timer Capacitor $C_{TIM}$

The charger also provides a programmable charging timer. The charging time is programmed by the capacitor connected between the TIM pin and GND. The capacitance is given by the formula:

$$C_{TIM} = 2 \times 10^{-11} S \times t_{CC} \quad \text{Unit: F}$$

$t_{CC}$  is the permitted fast charging time, unit: s.

## Input Capacitor C<sub>BD</sub>

The ripple current through input capacitor is greater than

$$I_{C_{BD\_MIN}} = I_{CC} \sqrt{D(1-D)}$$

To minimize the potential noise problem, place a typical X7R or a better grade ceramic capacitor really close to the BD and GND pins. Care should be taken to minimize the loop area formed by C<sub>BD</sub>, and BD/GND pins.

## Output Capacitor C<sub>OUT</sub>

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X7R or better grade ceramic capacitor with 10μF capacitance.

## Output Inductor L

There are several considerations in choosing this inductor.

- 1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average charge current. The inductance is calculated as:

$$L = \frac{V_{OUT} \times (1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where F<sub>SW</sub> is the switching frequency and I<sub>OUT,MAX</sub> is the maximum load current.

The SY20764B is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

- 2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT} \times (1 - V_{OUT}/V_{IN,MAX})}{2 \times F_{SW} \times L}$$

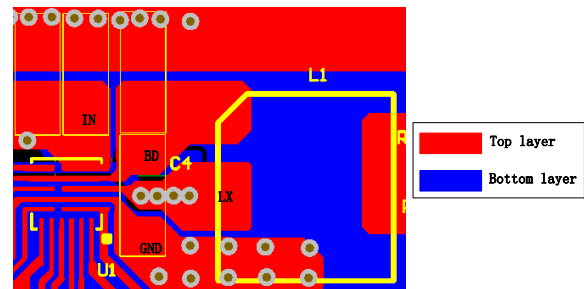
- 3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR < 20mΩ to achieve a good overall efficiency.

The SY20764B is a high integrated charger and the internal compensation circuits also limit the inductor choice. Out of the range from 0.68μH to 3.3μH is not suggested. The 2.2μH inductor can almost cover the normal applications.

## Layout Design

The layout design of the SY20764B regulator is relatively simple. For the best efficiency and minimum noise problems, the following components should be placed close to the IC: C<sub>BD</sub>, L.

- 1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.
- 2) C<sub>BD</sub> must be close to pins BD and GND. The loop area formed by C<sub>BD</sub> and GND must be minimized. Following picture is the recommended layout design of C<sub>BD</sub>.



- 4) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.
- 5) The capacitor C<sub>TIM</sub> and the trace connecting to the TIM pin must not be adjacent to the LX net on the PCB layout to avoid the noise problem.
- 6) The current sense resistor should be adjacent to the junction of the inductor and output capacitor. The routes from the sense leads on the sense resistor to the IC pins should be close to each other to minimize loop area. Please don't route the sense leads through a high current path. Following picture is the recommended layout design.

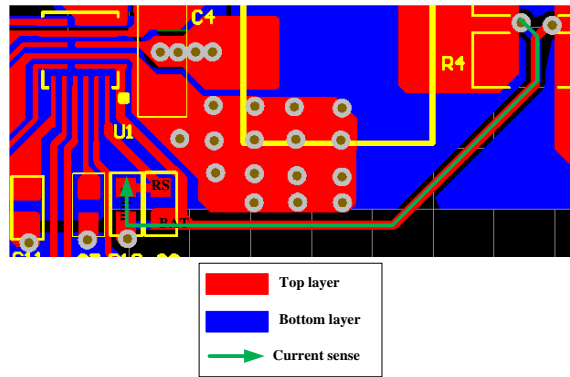
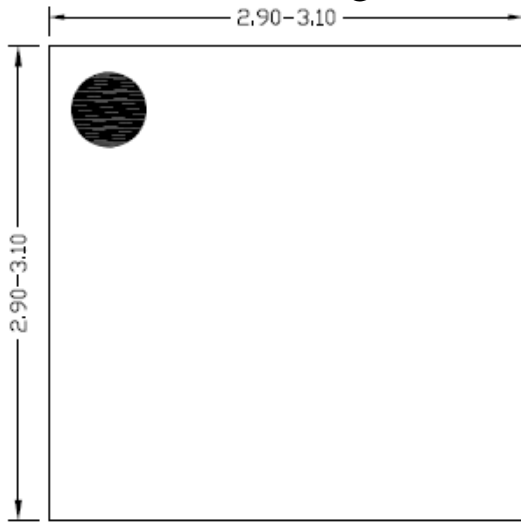
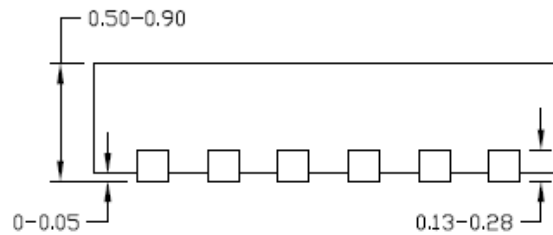


Figure2. PCB Layout Suggestion

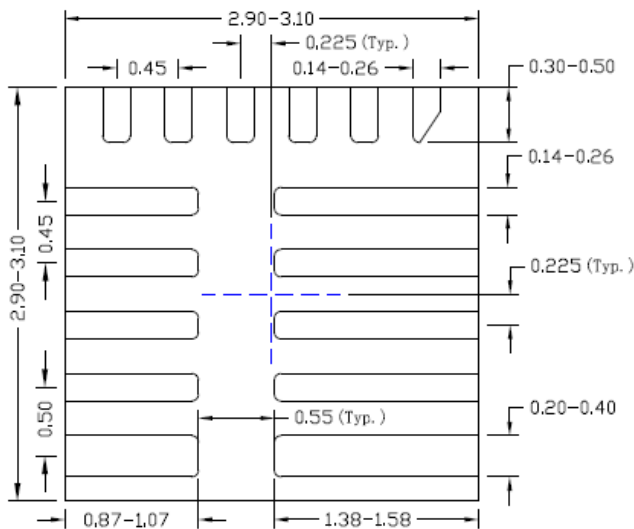
## QFN3×3-16 Package Outline Drawing



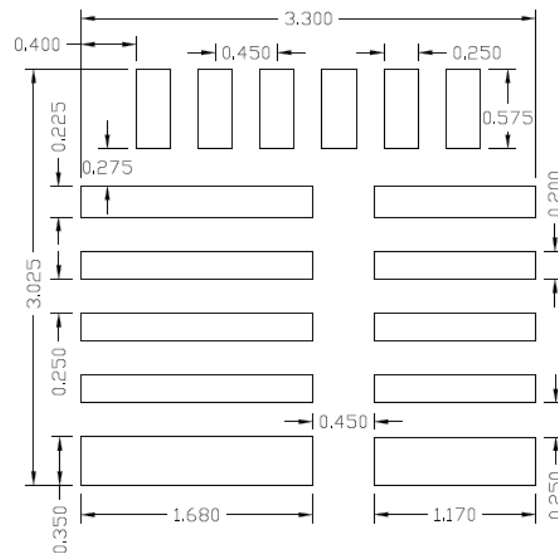
**Top View**



**Side View**



**Bottom View**



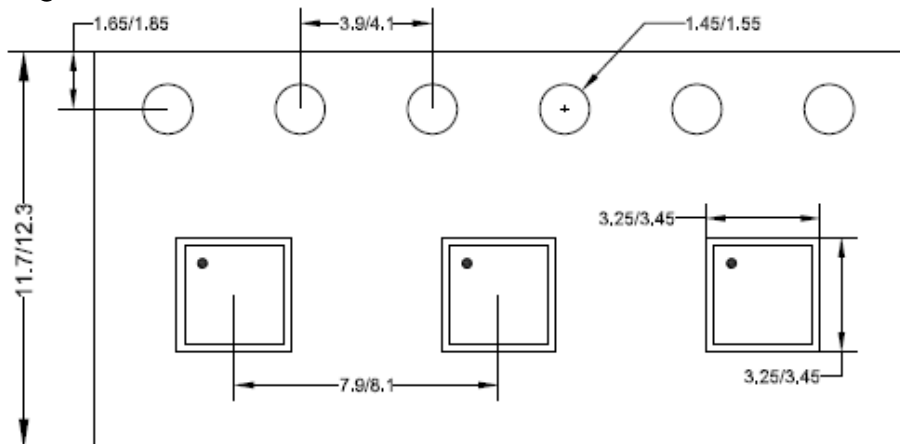
**Recommended PCB layout  
(Reference only)**

**Notes:** All dimension in millimeter and exclude mold flash & metal burr.

## Taping & Reel Specification

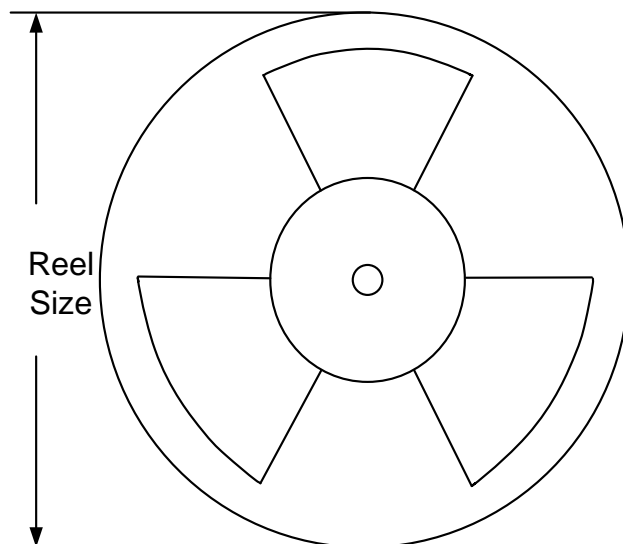
### 1. Taping orientation

QFN3×3



Feeding direction →

### 2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×3	12	8	13"	400	400	5000

### 3. Others: NA



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