SY24106L

High Performance, High Fidelity Digital Audio-Power Amplifier

General Description

The SY24106L is a digital audio power amplifier for driving bridge-tied stereo speakers at up to 2×20W maximum output power. One serial data input allows processing of up to two discrete audio channels and seamless integration to most digital audio processors. The SY24106L is an I^2S slave device receiving all clocks from external sources.

The SY24106L has the essential audio signal processing functions like dynamic range control, loudness control and parametric equalization.

Ordering Information

SY24106 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY24106LQEC	QFN5×5-32	

Applications

- LCD TV, LED TV or Monitor
- Digital Speaker, Bluetooth Speaker
- Sound Bar

Features

- 2×10W into 8Ω Loads from a 13.2V Supply
- 2×15W into 8Ω Loads from a 16V Supply
- 2.0 BTL Mode or PBTL Mode Support
- 4.5V to 16.5V PVDD Range
- 32kHz to 96kHz Sample Rate Support (LJ/RJ/I^2S)
- I^2C Address Selection Pin
- Independent Channel Volume Controls with 48dB to Mute
- SDATA Generator (I^2S Output)
- Two DC Blocking Filters
- 14 PEQs or 10 PEQs + 4 SPEQs Each Channel for Speaker Protection and Speaker Compensation
- 3 Bands Dynamic Range Control Plus a Post Dynamic Range Control
- Loudness Control
- Power Level Meter
- 3-wire I^2S Digital Audio Interface without MCLK
- Thermal, Over Current, Short Circuit Protection and EQ/DRC Coefficients Checksum
- Support Automatic Audio Sample Rate Detection
- SY24106LQEC Surface Mount, QFN 32Pin, 5mm×5mm

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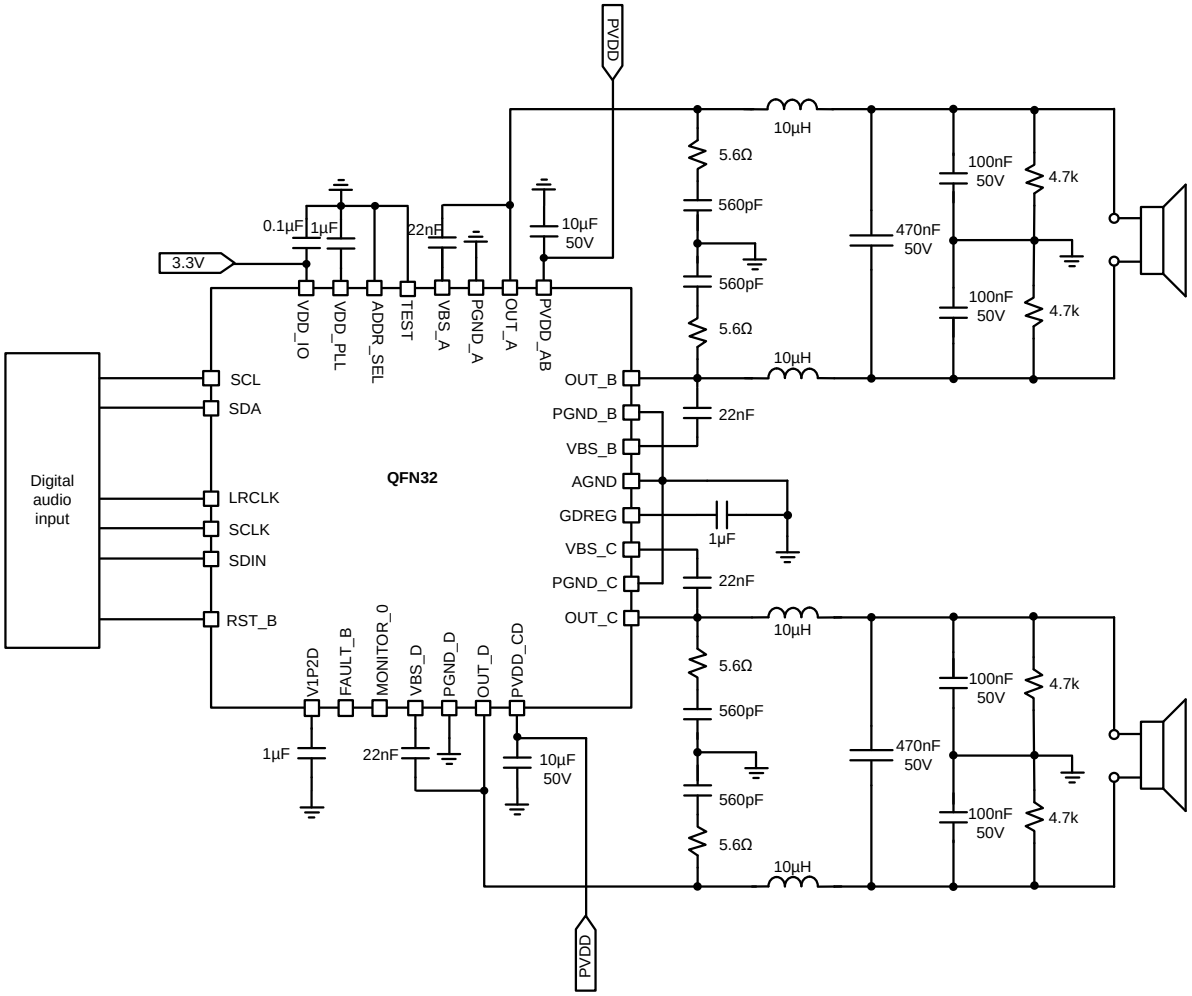
Typical Application

BTL



(a) Stereo Class-D Amplifier with BTL Output

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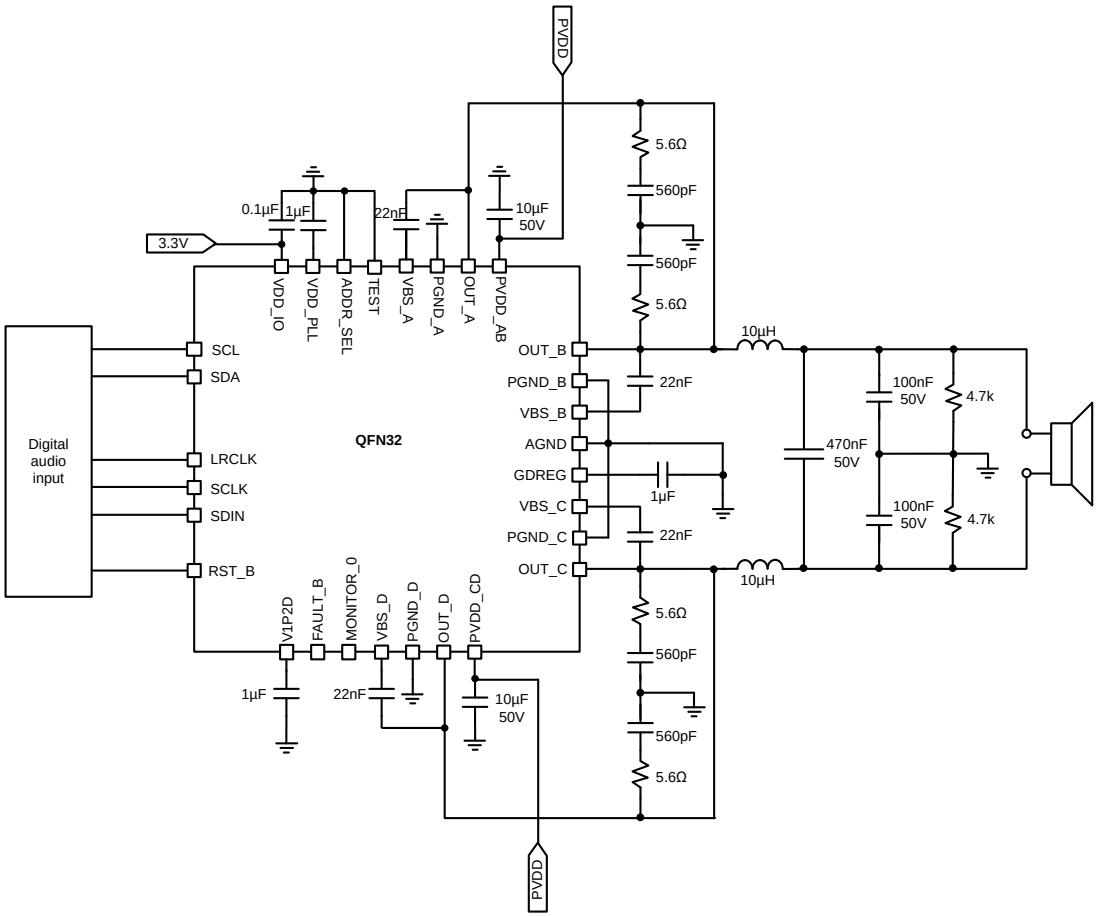
PBTL



(b) Mono Class-D Amplifier with PBTL Output

Figure1. Typical Application Circuit

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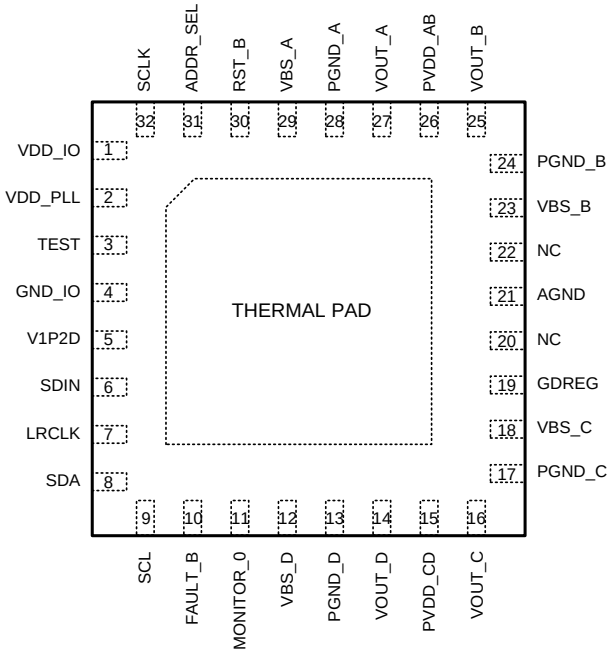
Pinout (top view)



(QFN5×5-32)

Top mark: **BRC** ***xyz*** (Device code: **BRC**, ***x=year code, y=week code, z= lot number code***)

Name	No.	Type(1)	Termination(2)	Description
VOUT_A	27	O		Half-bridge A output.
VOUT_B	25	O		Half-bridge B output.
VOUT_C	16	O		Half-bridge C output.
VOUT_D	14	O		Half-bridge D output.
PVDD_AB	26	P		Power supply for half-bridge A and B.
PVDD_CD	15	P		Power supply for half-bridge C and D.
VBS_A	29	P		High side supply offset voltage for half-bridge A.
VBS_B	23	P		High side supply offset voltage for half-bridge B.
VBS_C	18	P		High side supply offset voltage for half-bridge C.
VBS_D	12	P		High side supply offset voltage for half-bridge D.
GDREG	19	P		Gate driver internal regulator output. This pin must not be used for driving the external devices.
GND_IO	4	P		Analog 3.3V power supply ground.
NC	20, 22			Not connected.
VDD_IO	1	P		Power supply for digital interface I/O, 3.3V.
ADDR_SEL	31	DI	Pull down	I^2C address selection pin.
V1P2D	5	P		Internal regulated 1.2V digital power supply for digital core. This pin must not be used for powering the external devices.
VDD_PLL	2	P		Internal regulated 1.2V digital power supply for PLL. This pin must not be used for powering the external devices.
FAULT_B	10	DI	Pull up	This pin low means turning off the PWM signal path.
LRCLK	7	DI	Pull down	Serial audio data left or right clock input.
SCLK	32	DI	Pull down	Serial audio data bit clock input.

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SDIN	6	DI	Pull down	Serial audio data input.
SDA	8	DIO	Pull up	I^2C serial control data input or output.
SCL	9	DI	Pull up	I^2C serial clock input.
MONITOR_0	11	DO		Monitoring the signal out from the processor block / I^2S output.
RST_B	30	DI	Pull-up	Logic low to this pin to reset the system. When reset pulls low, DAP will restore to its default conditions, and place the PWM in the hard mute state.
TEST	3	DI	Pull down	Test pin.
AGND	21	P		Power stage analog ground.
PGND_A	28	P		Power ground for half-bridge A.
PGND_B	24	P		Power ground for half-bridge B.
PGND_C	17	P		Power ground for half-bridge C.
PGND_D	13	P		Power ground for half-bridge D.

Note: (1) Type: A =analog; D =digital; P =power/ground/decoupling; I =input; O =output; IO=inout
(2) All pull-ups and pull-downs are weak.

Function Block

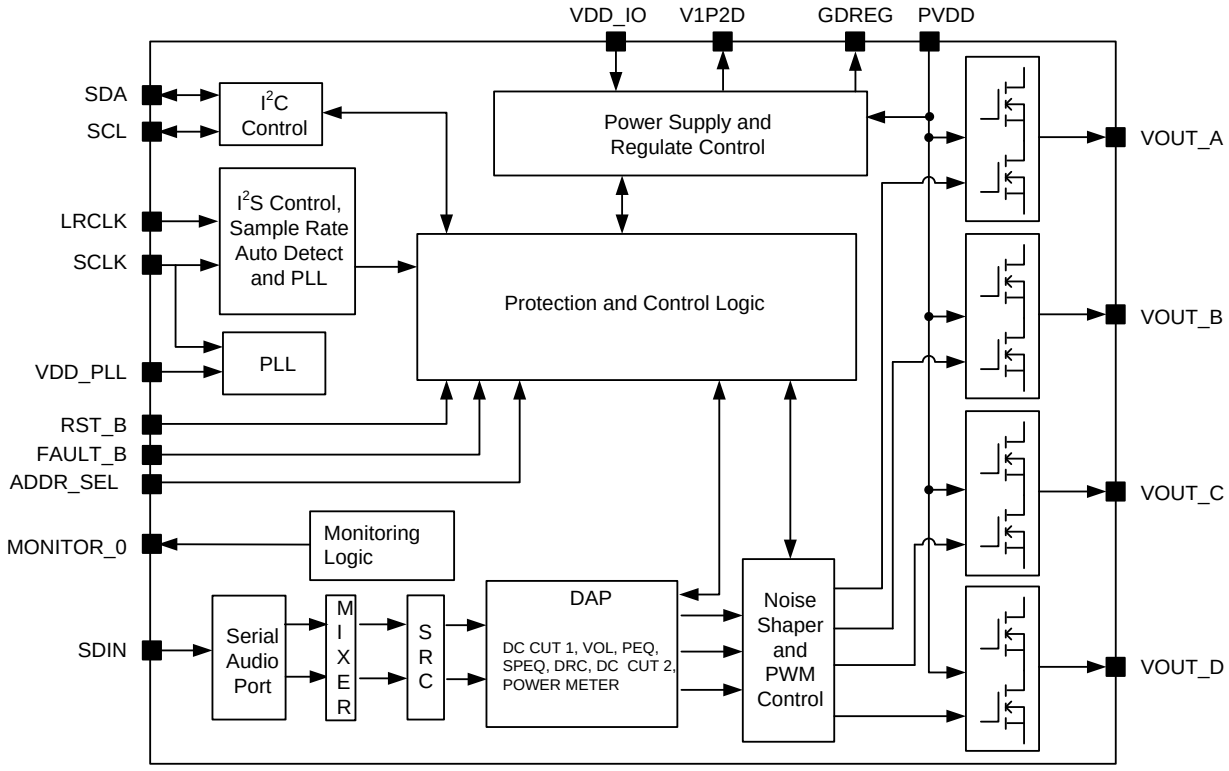

Figure2. Function Block

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Absolute Maximum Ratings (Note 1)

VDD_IO, Power Supply for Digital Interface I/O ---------- -0.3V to 3.6V
PVDD, Half-bridge Supply Voltage (Note 2) ---------- -0.3V to 18V
Digital Input ---------- -0.5V to (VDD_IO+0.5)V
VOUT_x ---------- 18V
GDREG ---------- -0.5V to 4V
VBS_x to VOUT_x ---------- -0.5V to 4V
Junction Temperature Range ---------- 0°C to 150°C
Storage Temperature Range ---------- -40°C to 125°C

Recommended Operating Conditions

VDD_IO, Power Supply for Digital Interface I/O ---------- 3.3V
PVDD, Half-bridge Supply Voltage ---------- 4.5V to 16.5V
V_{IH}, High-level Input Voltage ---------- ≥2V
V_{IL}, Low-level Input Voltage ---------- ≤0.8V
$R_{L(BTL)}$, Load Impedance(BTL) ---------- 8Ω
$R_{L(PBTL)}$, Load Impedance(PBTL) ---------- 4Ω
Operating Ambient Temperature Range ---------- 0°C to 85°C
Operating Junction Temperature Range ---------- 0°C to 125°C

PWM Operation at Recommended Operating Conditions

Parameter	Test Conditions	Value	Unit
Output Sample Rate	44.1kHz data rate	352.8	kHz
	32/48/96kHz data rate	384	

PLL Input Parameters and External Filter Components

Parameter	Test Conditions	Min	Typ	Max	Unit
F_{SCLK} SCLK Frequency		1.024		6.144	MHz
SCLK Duty Cycle		40	50	60	%
$t_{r(sclk)}$ SCLK Rise Time				5	ns
$t_{f(sclk)}$ SCLK Fall Time				5	ns

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Electrical Characteristics

DC Characteristics

(T_A=25°C, PVDD_x=12V, VDD_IO=3.3V, R_L=8Ω, BTL Ternary Mode, f_S=48 kHz)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PVDD	Half-bridge Supply Voltage		4.5		16.5	V
VDD_IO	Power Supply for Digital Interface I/O		2.7		3.6	V
GDREG	Gate Drive Supply		3.2		3.4	V
V_{IH}	High Level Input Voltage	TEST, SDIN, LRCLK,SDA, SCL, FAULT_B, RST_B, ADDR_SEL, SCLK	2			V
V_{IL}	Low Level Input Voltage	TEST, SDIN, LRCLK,SDA, SCL, FAULT_B, RST_B, ADDR_SEL, SCLK			0.8	V
I_{IL}	Low Level Input Current	TEST, SDIN, LRCLK, SDA, SCL, FAULT_B, RST_B, ADDR_SEL, SCLK			75	μA
I_{IH}	High Level Input Current	TEST, SDIN, LRCLK, SDA, SCL, FAULT_B, RST_B, ADDR_SEL, SCLK			75	μA
I_{DD}	3.3V Supply Current	No Input No Load		9.3		mA
		Reset(RST_B = low, FAULT_B = high)		0.7		
I_{PVDD}	No Load, Half-bridge Supply Current (Without Snubber)	Normal		26.5		mA
		Reset(RST_B = low, FAULT_B = high)		1		
Power MOSFET						
$R_{DS(on)}$	High Side Drain-to-source Resistance	T_j=25°C, includes metallization resistance		150		mΩ
	Low Side Drain-to-source Resistance			150		mΩ
I/O Protection						
V_{UVP}	PVDD Falling		3	3.6		V
	PVDD Rising			4.0	4.45	
OVTP(Note 3)	Over Temperature Protection			150		°C
$OVTP_{HYST}$ (Note 3)	Over Temperature Protection Hysteresis			30		°C
I_{OVC}	Over Current Protection			5		A

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AC Characteristics (Note 3)

(T_A=25°C, BTL ternary mode, f_S=48 kHz, C_{VBS}=22nF, audio frequency=1 kHz, AES17 filter, snubber=5.6Ω+560pF, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_o	Output Power	BTL Mode, PVDD=8V, R_L=8Ω, 1%THD+N		3.3		W
		BTL Mode, PVDD=8V, R_L=8Ω, 10%THD+N		4.1		
		BTL Mode, PVDD=12V, R_L=8Ω, 1%THD+N		7.5		
		BTL Mode, PVDD=12V, R_L=8Ω, 10%THD+N		9.2		
		BTL Mode, PVDD=16V, R_L=8Ω, 1%THD+N		13.1		
		BTL Mode, PVDD=16V, R_L=8Ω, 10%THD+N		16.2		
		PBTL Mode, PVDD=12V, R_L=4Ω, 1%THD+N		14.9		
		PBTL Mode, PVDD=12V, R_L=4Ω, 10%THD+N		18.4		
THD+N	Total Harmonic Distortion	PVDD=8V, R_L=8Ω, P_O=1W		0.042		%
		PVDD=12V, R_L=8Ω, P_O=1W		0.048		
		PVDD=16V, R_L=8Ω, P_O=1W		0.036		
V_n	Output Integrated Noise(rms)	PVDD=8V, R_L=8Ω, A-weighted		40.3		μV
		PVDD=12V, R_L=8Ω, A-weighted		73.0		
		PVDD=16V, R_L=8Ω, A-weighted		96.3		
	Crosstalk	PVDD=16V, R_L=8Ω, Po=1 W, f = 1kHz ,		87.9		dB
SNR	Signal to Noise Ratio	PVDD=8V, A weighted, f = 1kHz, maximum power at THD+N <1%		102.2		dB
		PVDD=12V, A weighted, f = 1kHz, maximum power at THD+N <1%		100.4		
		PVDD=16V, A weighted, f = 1kHz, maximum power at THD+N <1%		100.6		

Note 1: Stresses beyond the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2: DC voltage rating could be derated a little according to the possible switching spike on switching node if the snubber is not appropriate enough.

Note 3: Typical value tested on the demonstration board is guaranteed by design.

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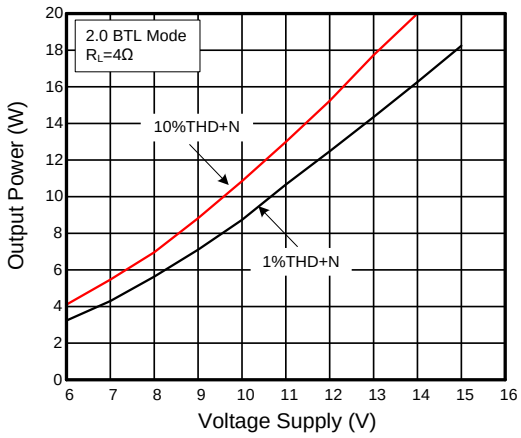
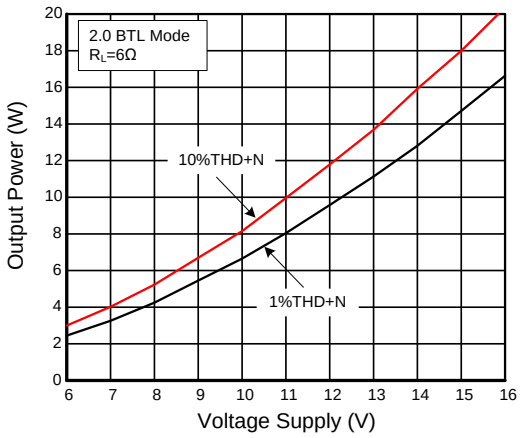
Typical Performance Characteristics

(All measurements with snubber =5.6Ω+560pF.)

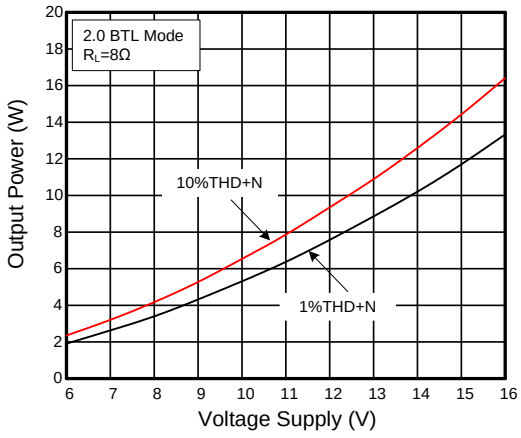
Maximum Output Power vs. Supply Voltage



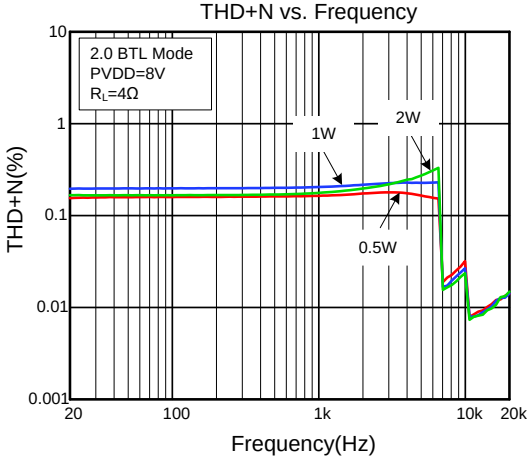
Maximum Output Power vs. Supply Voltage



Maximum Output Power vs. Supply Voltage



THD+N vs. Frequency



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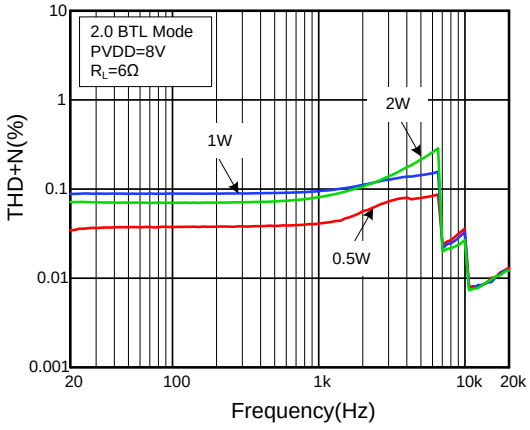

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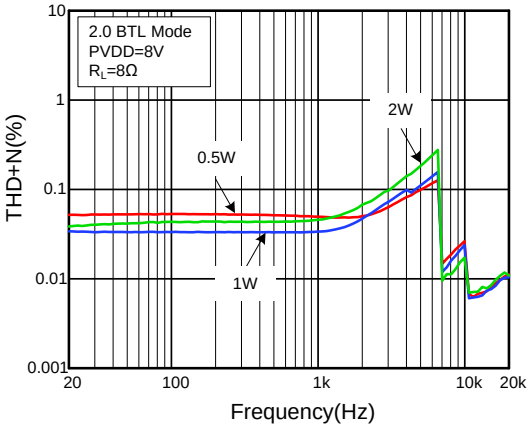

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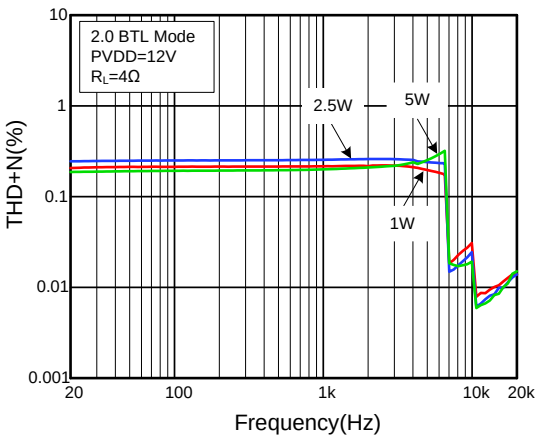
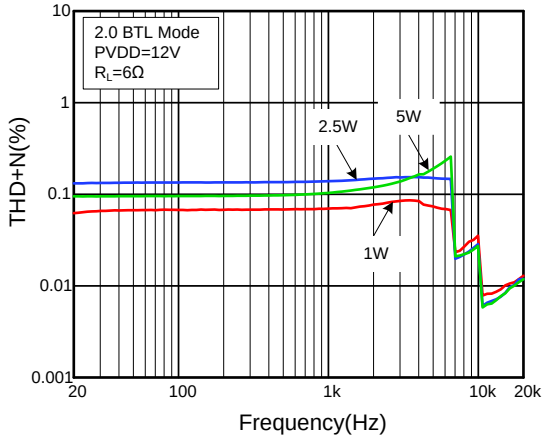
THD+N vs. Frequency



THD+N vs. Frequency



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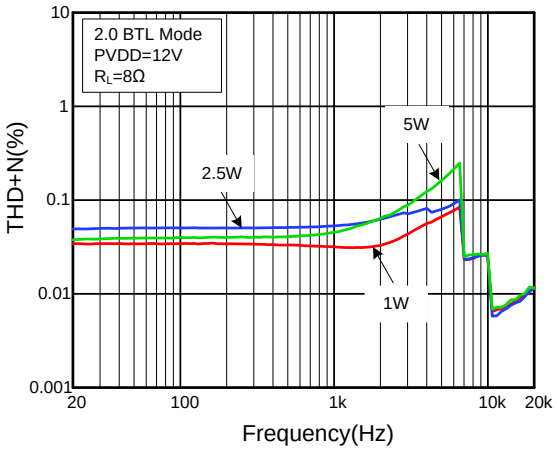

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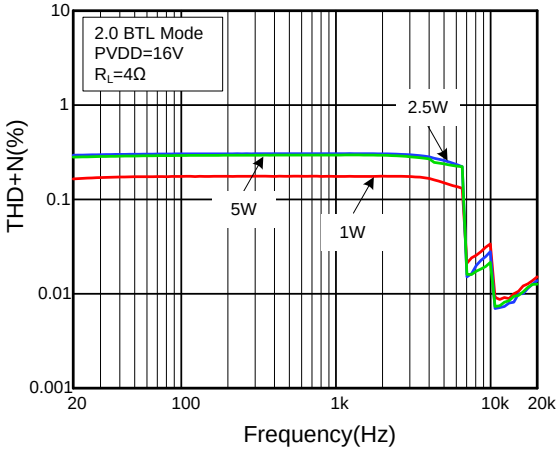

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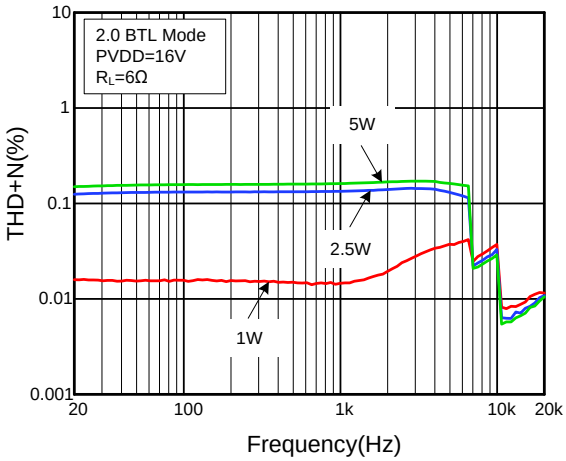

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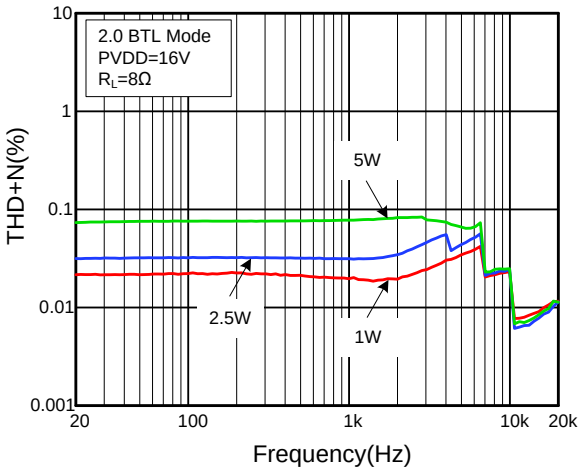

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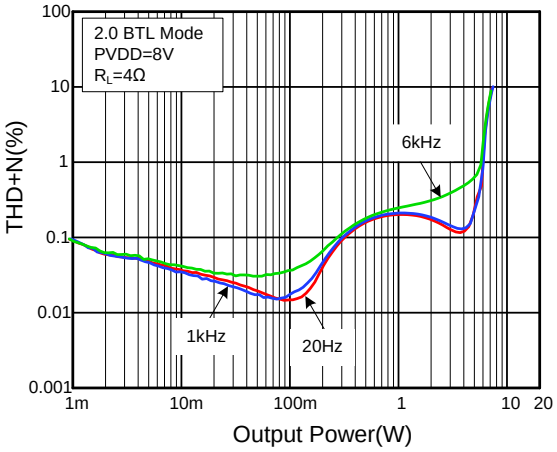
THD+N vs. Output Power



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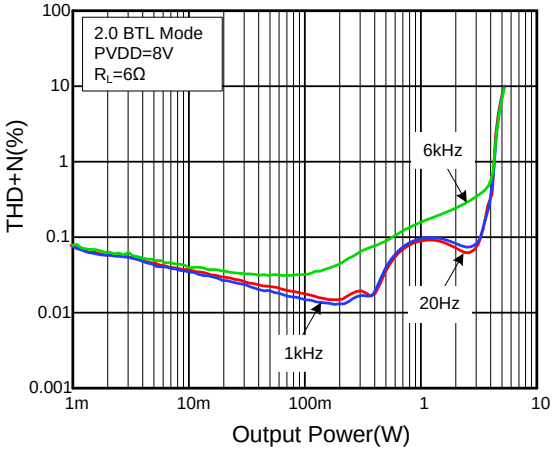

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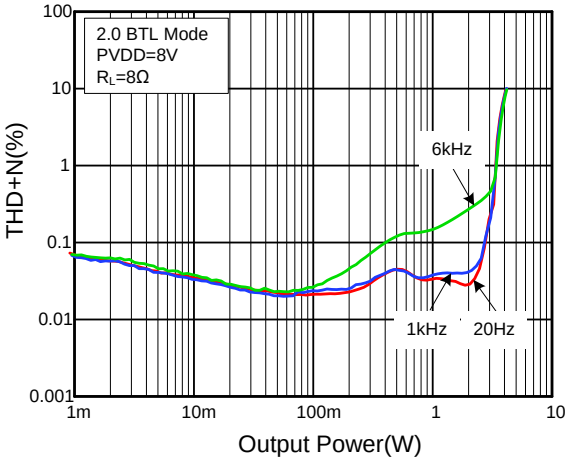

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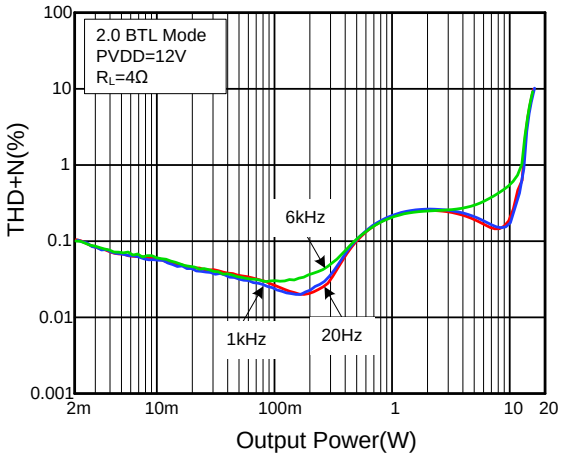

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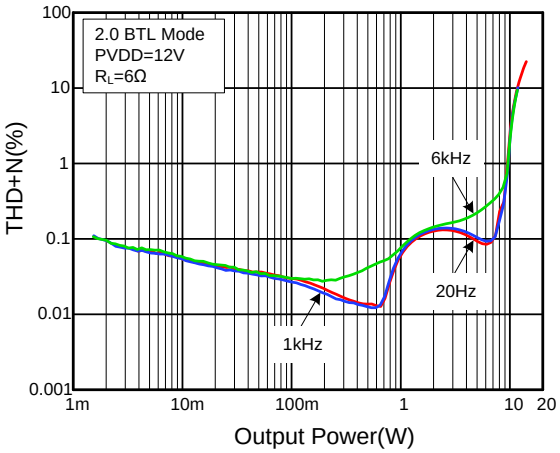

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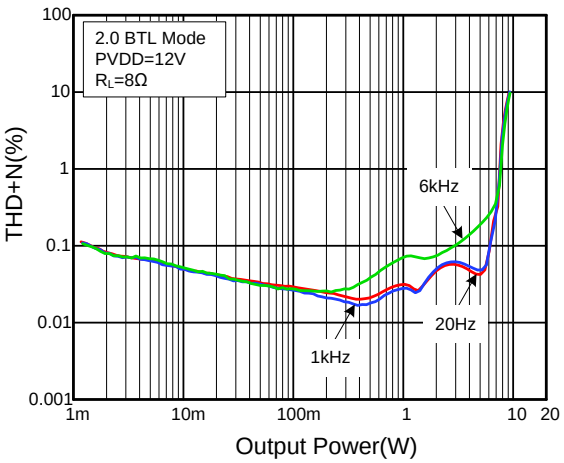

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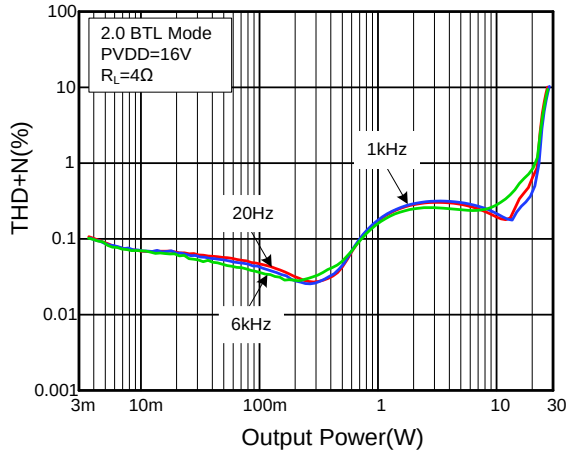
THD+N vs. Output Power



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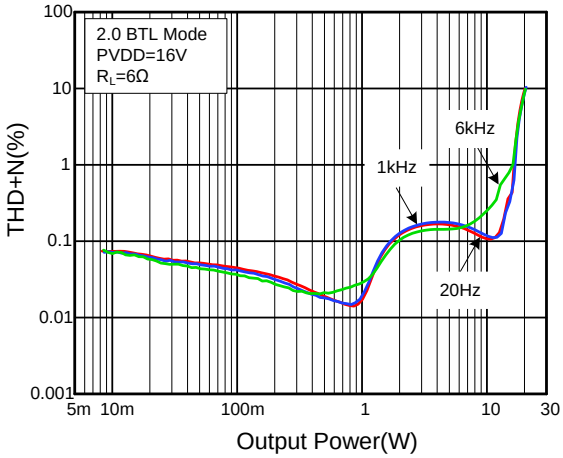

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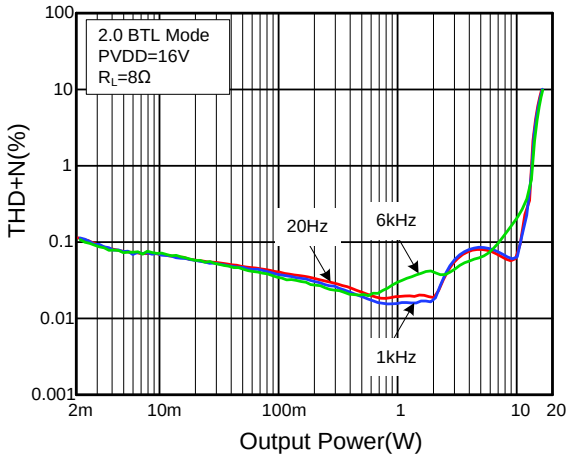
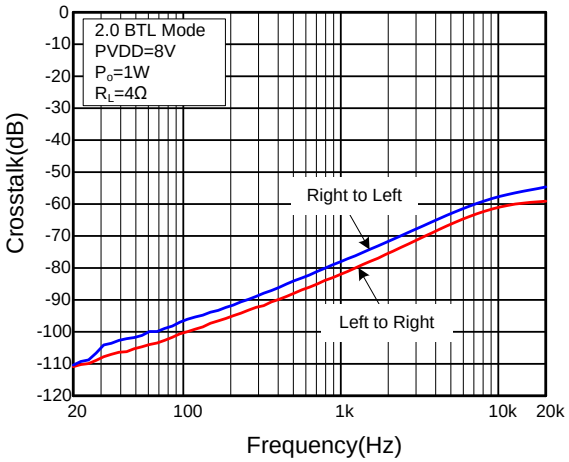


Crosstalk vs. Frequency



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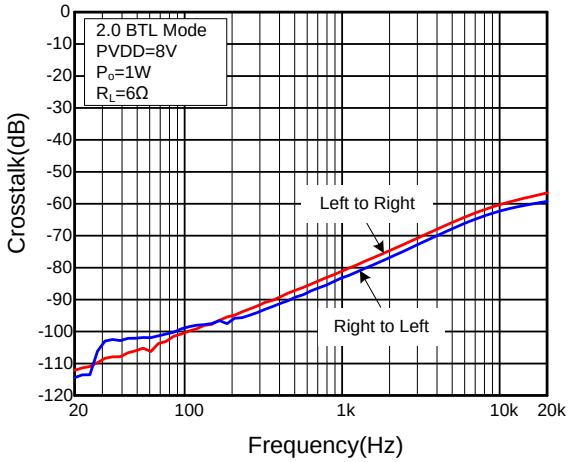

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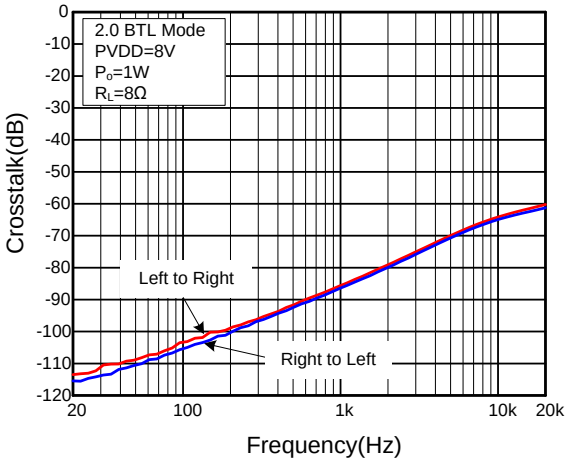

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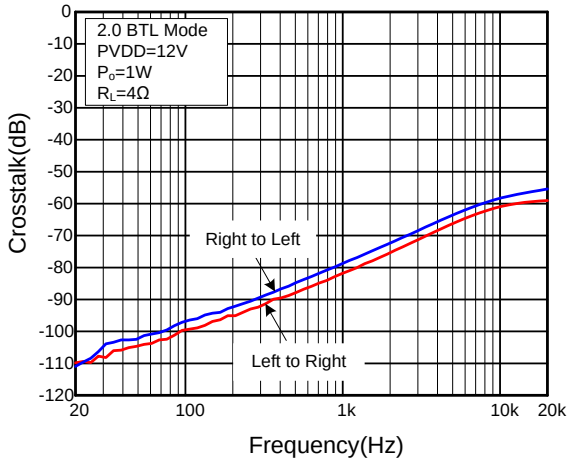
Crosstalk vs. Frequency



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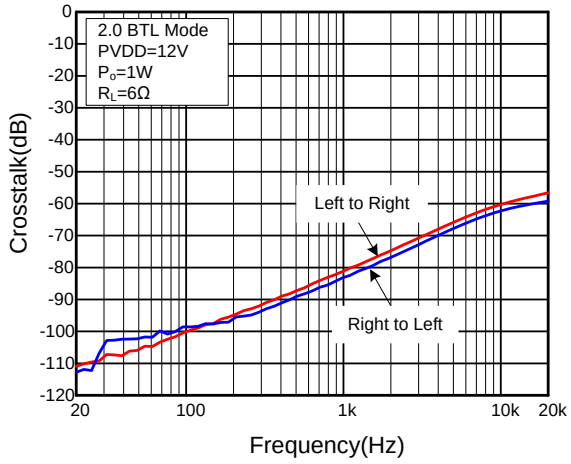

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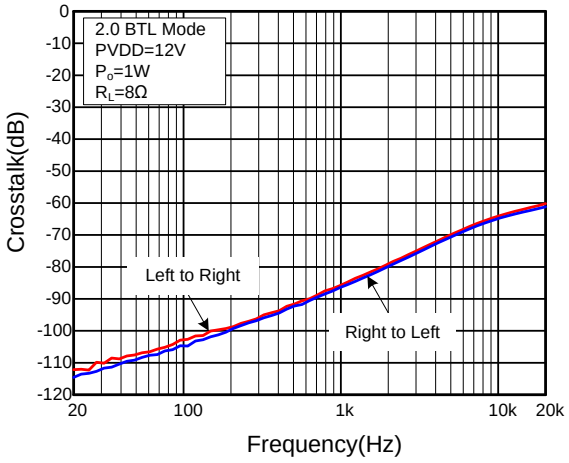
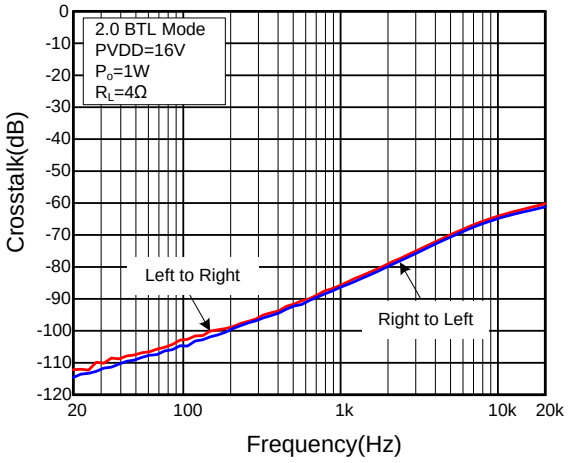
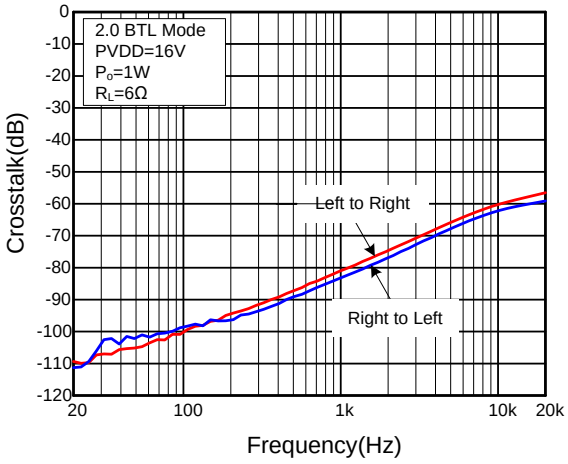


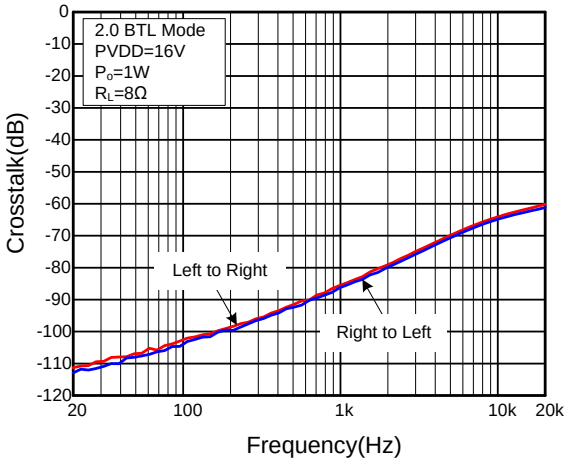
Crosstalk vs. Frequency



Crosstalk vs. Frequency



Crosstalk vs. Frequency



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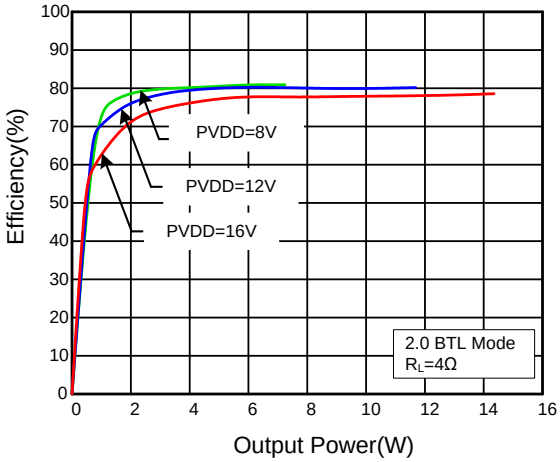
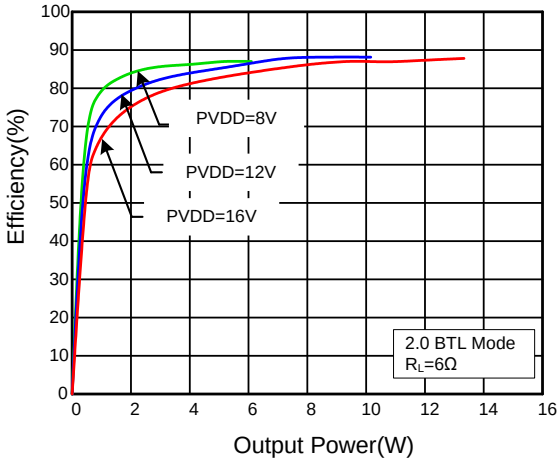
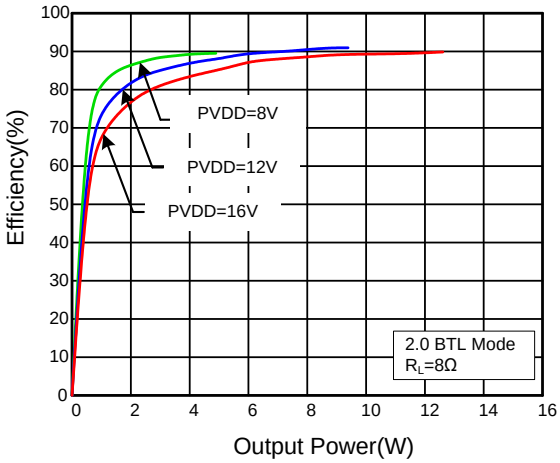
Efficiency vs. Power



Efficiency vs. Power



Efficiency vs. Power



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I²C Serial Control Port Operation

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCL}	SCL Frequency	No wait states		400	kHz
t_r	SCL and SDA Rise Time			300	ns
t_f	SCL and SDA Fall Time			300	ns
t_{WH}	SCL High Duration Time		0.6		µs
t_{WL}	SCL Low Duration Time		1.3		µs
t_{S1}	SDA to SCL Setup Time		100		ns
t_{h1}	SCL to SDA Hold Time		0		ns
t_{buf}	Free Time Between Stop and Start Condition		1.3		µs
t_{S2}	SCL to Start Condition		0.6		µs
t_{h2}	Start Condition to SCL Hold Time		0.6		µs
t_{S3}	SCL to Stop Condition		0.6		µs
C_{Load}	Load Capacitor for Each BUS Line			400	pF

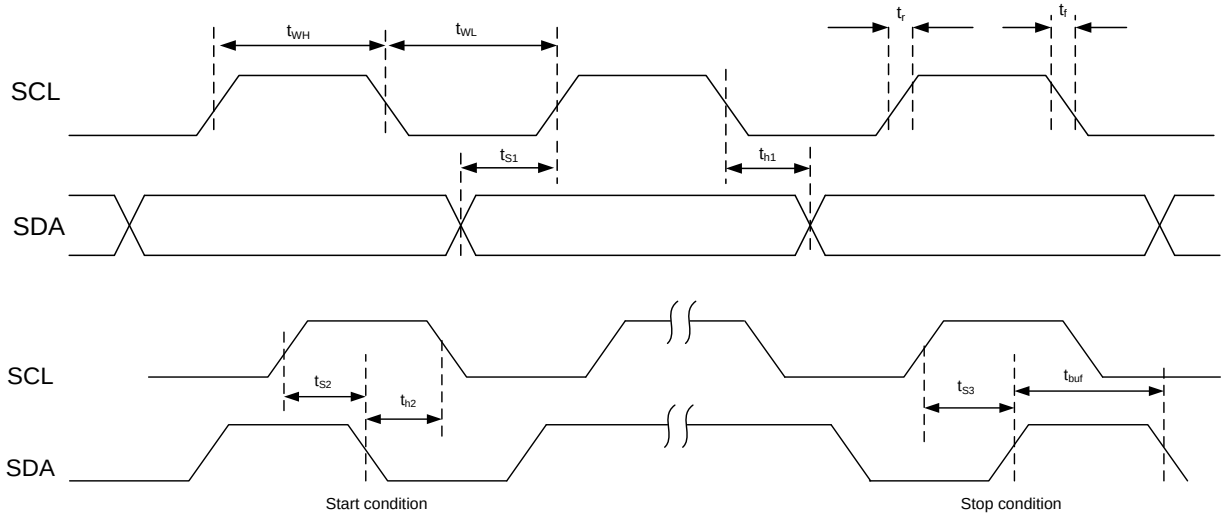

Figure3. I²C Timing Diagram

Reset Timing (RST_B)

Symbol	Parameter	Min	Typ	Max	Unit
t_{WRST}	Reset Active Pulse Duration	100			µs
t_{delay_I2C}	Enable the I²C Duration Time			0.1	ms

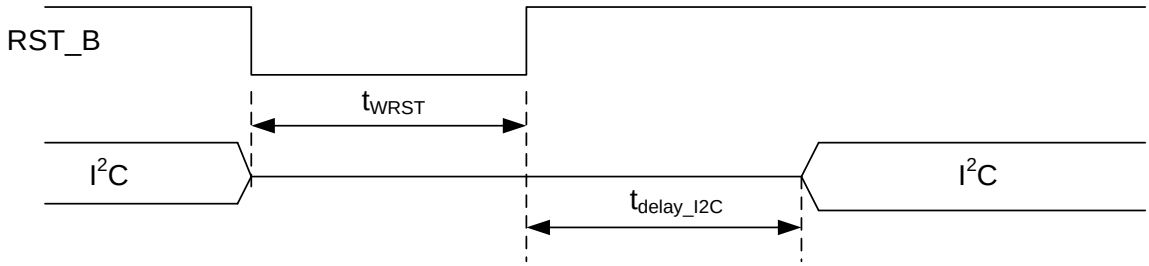

Figure4. Reset Timing Diagram

NOTES: RST_B is held low for at least 100 µs after VDD_IO reaches 3V on power up.

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Serial Audio Ports Slave Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCLK}	SCLK Frequency	C_{load}=30pF	1.024		6.144	MHz
t_{S4}	LRCLK to SCLK Rising Edge Setup Time		10			ns
t_{h3}	LRCLK From SCLK Rising Edge Hold Time		10			ns
t_{S5}	SDIN to SCLK Rising Edge Setup Time		10			ns
t_{h4}	SDIN from SCLK Rising Edge Hold Time		10			ns
	LRCLK Frequency		32	48	96	kHz
	SCLK Duty Cycle		40	50	60	%
	LRCLK Duty Cycle		40	50	60	%
t_{edge}	LRCLK Edge with Respect to the Falling Edge of SCLK		-1/4		1/4	SCLK period
t_{rs}	Rise Time for SCLK/LRCLK				8	ns
t_{fs}	Fall Time for SCLK/LRCLK				8	ns

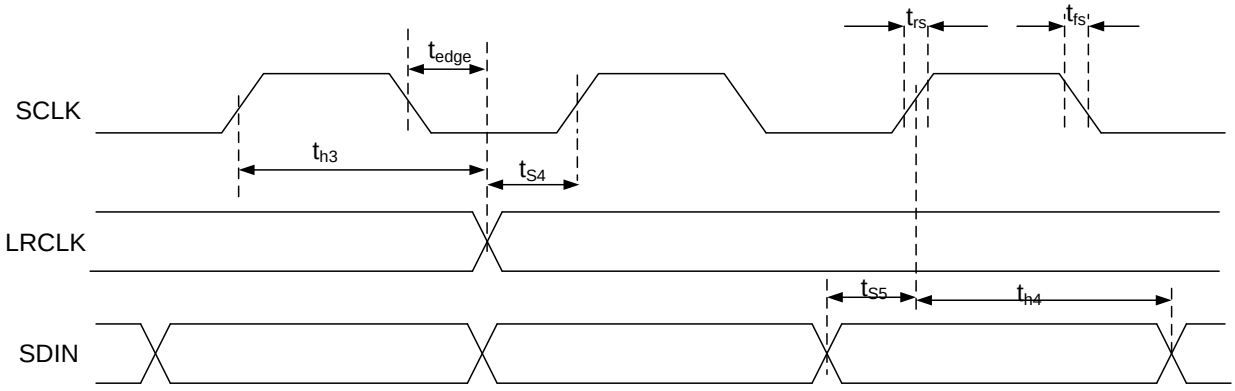

Figure5. I²S Timing Diagram

Detailed Description and Theory of Operation

Under Voltage Protection and Power on Reset

When power on, the Power on reset circuit will reset the overload circuit and ensures that all circuits will be fully operational when PVDD and AVDD supply voltage reaches 4.0V and 2.7V respectively. A voltage drops below the UVP threshold on AVDD or PVDD results in all half bridge outputs being set in the high impedance state, and the FAULT being set to low.

Clock, Auto Detection and PLL

This device is a slave only device. The digital audio processor supports all the sample rates and SCLK rates that are defined in the clock control register.

The DAP only supports a 1fs LRCLK. The clock section uses SCLK or the internal oscillator clock (when SCLK is unstable, out of range, or absent) to produce the internal clock running at 512 times of the PWM switching frequency.

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The device has the robust clock error handing that uses the built-in trimmed oscillator clock to quickly detect changes or errors. Once the system detects a clock change or error, it will mute the audio and then force PLL to limp using the internal oscillator as a reference clock. Once the clock is stable, the system will revert to normal operation. During this operation, the default volume will be restored in a single step (also called hard unmute). The ramp process can be programmed to ramp back slowly (also called soft unmute) as defined in volume register (0x06).

Serial Data Interface

Serial data is input on SDIN. The PWM outputs are derived from SDIN. The DAP accepts serial data in 16, 20, 18, or 24 bit left justified, right justified, and I²S serial data formats.

PWM Section

The device PWM section accepts 24bit PCM data from DAP and output two BTL PWM audio output channels. The PWM section has an adjustable maximum modulation limit of 96.1% to 98.2%.

Serial Interface Control and Timing

The I²S mode is set by writing to register 0x15.

I²S Timing

I²S uses LRCLK for determining whether the transmitted data is for the left channel or the right channel.LRCLK is low for the left channel and high for the right channel. A clock running at 64fs/48fs/32fs is used for clocking in data. There is a delay of one bit clock from the time the LRCLK changes state to the first bit of data on the data lines. The data is written MSB first and is valid on the rising edge of clock. The DAP masks unused trailing data bit positions.

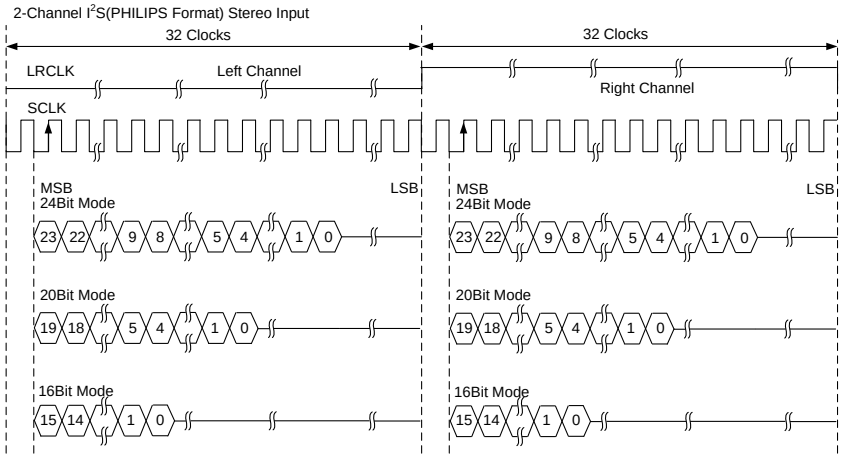

Figure6. I²S 64fs Format

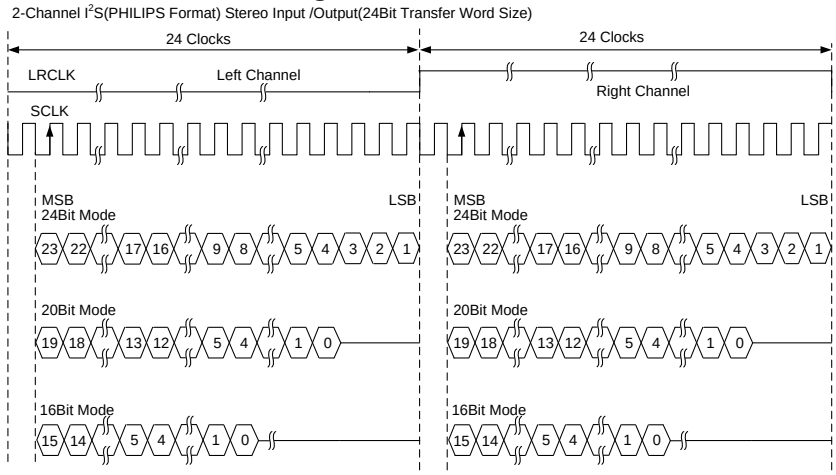

Figure7. I²S 48fs Format

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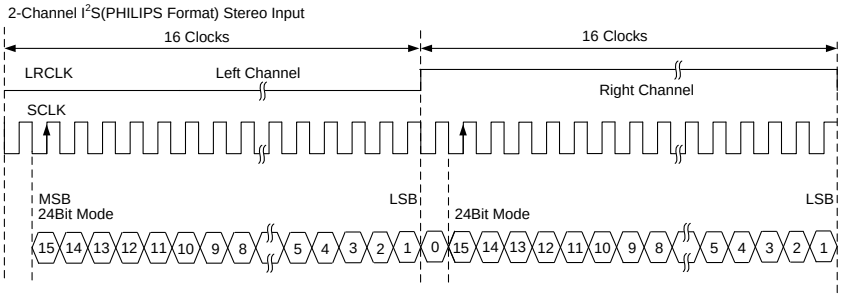

Figure8. I²S 32fs Format

Left Justified

Left Justified (LJ) timing uses LRCLK for determining whether the transmitted data is for the left channel or the right channel. LRCLK is high for the left channel and low for the right channel. A clock running at 64fs/48fs/32fs is used for clocking in data. The first bit of data on the data lines at the same time LRCLK toggles. The data is written MSB first and is valid on the rising edge of clock. The DAP masks unused trailing data bit positions.

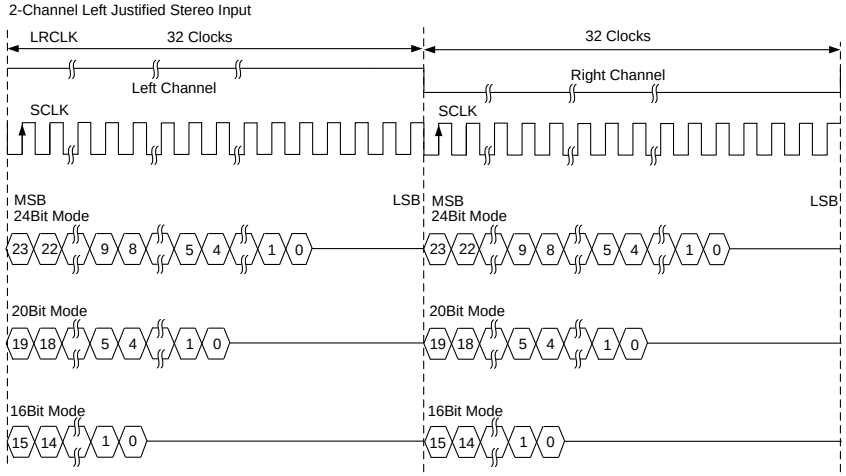

Figure9. Left Justified 64fs Format

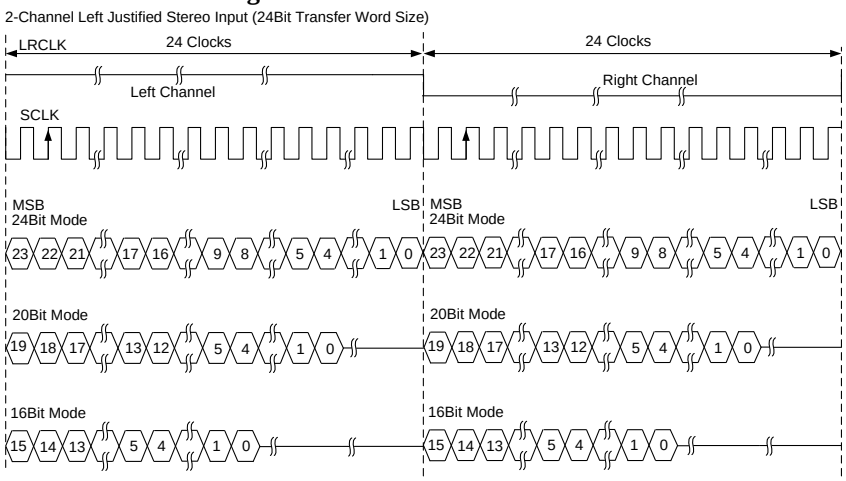

Figure10. Left Justified 48fs Format

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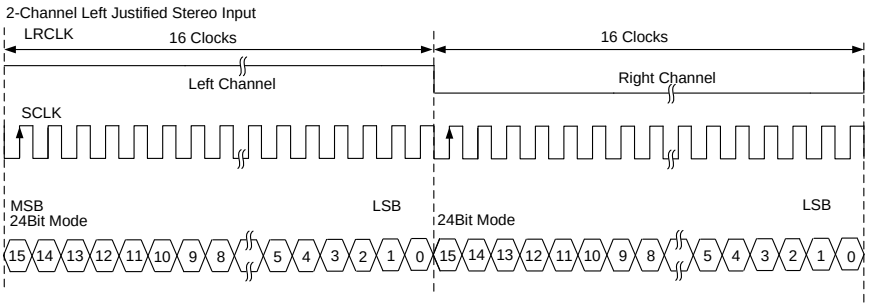

Figure11. Left Justified 32fs Format

Right Justified

Left Justified (LJ) timing uses LRCLK for determining whether the transmitted data is for the left channel or the right channel. LRCLK is high for the left channel and low for the right channel. A clock running at 64fs/48fs/32fs is used for clocking in data. The first bit of data on the data 8bit clock periods after LRCLK toggles. The data is written MSB first and is valid on the rising edge of clock. The DAP masks unused trailing data bit positions.

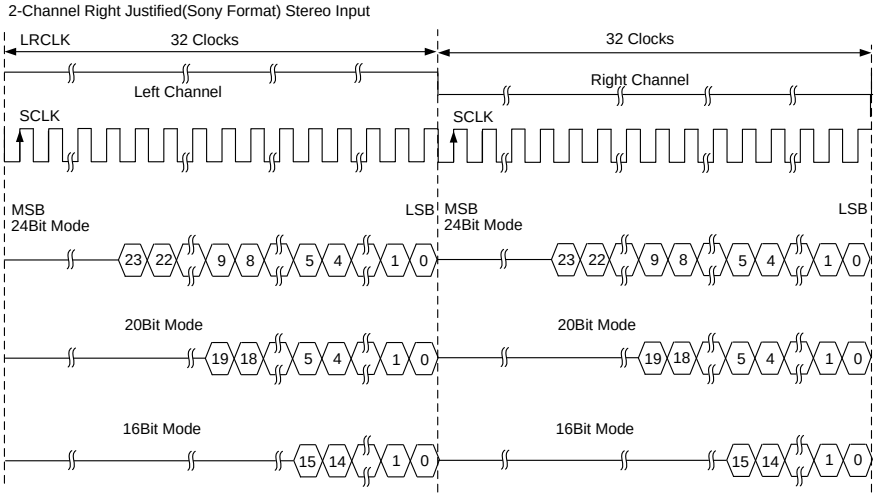

Figure12. Right Justified 64fs Format

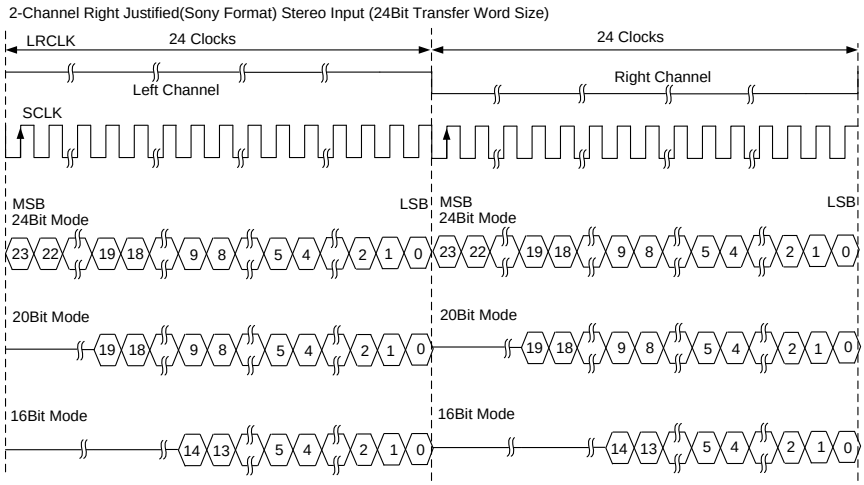

Figure13. Right Justified 48fs Format

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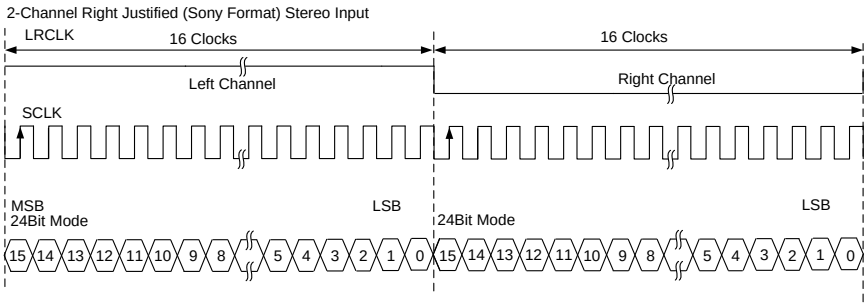

Figure14. Right Justified 32fs Format

I²C Serial Control Interface

The device DAP has a bidirectional I²C interface that compatible with the I²C BUS protocol and supports both 100kHz and 400kHz data transfer rates for single and multiple byte writing and reading operations. The device does not support a multi-master BUS or wait state insertion. The I²C control is used to program the registers of the device and to read device status. The device performs all I²C operations without I²C wait cycles.

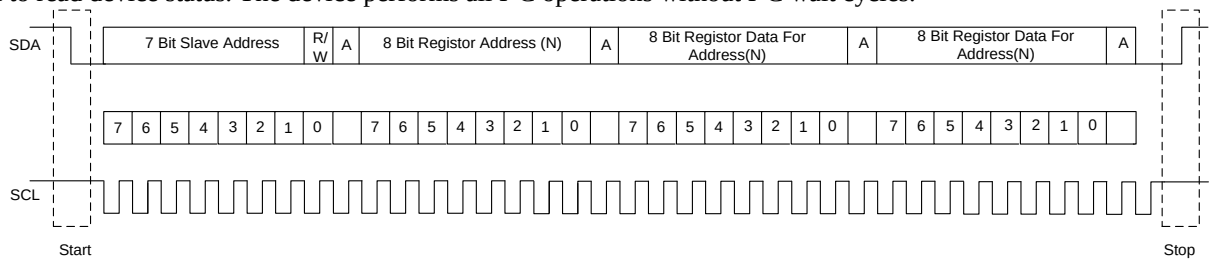

Figure15. Typical I²C Sequence

The ADDR_SEL pin defines the I²C device address. A 15kΩ resistor pull down on this pin gives this device address of 0x54 and a 15kΩ resistor pull up gives this device address 0x56.

I²C Device Address Change Procedure

Write to device address change enable register, 0xF8 with value of 0xF9 A5 A5A5.
Write to device register 0xF9 with a value of 0x0000 00XX, where XX is the new address.
Any writing after that should use the new device address XX.

Single and Multiple Byte Transfers

The I²C serial control interface supports both single byte and multiple bytes reading/writing operations for sub addresses 0x00 to 0x1F.

During multiple byte read operations, the DAP responds with data, a byte at a time, starting at the sub address assigned, as long as the master device continues to response with acknowledges. If a particular sub address does not contain 8*N bits, the unused bits are read as logic 0.

During multiple byte write operations, the DAP compares the number of bytes transmitted to the number of bytes that are required for each specific sub address. For example, if a write command is received for a biquad sub address, the DAP expects to receive five 32bit words. If fewer than five 32bit data words have been received when a stop command (or another start command) is received, the data received is discarded.

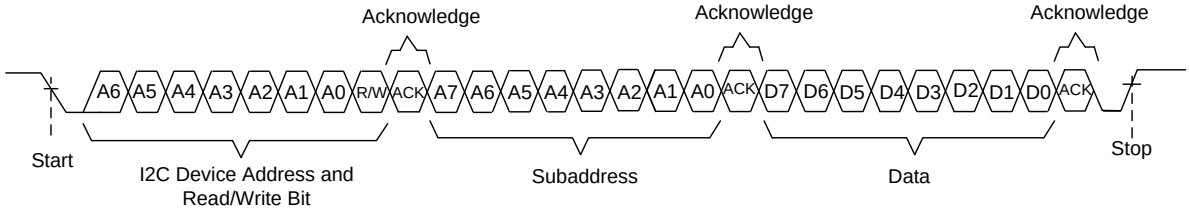

Figure16. Single Byte Write Transfer

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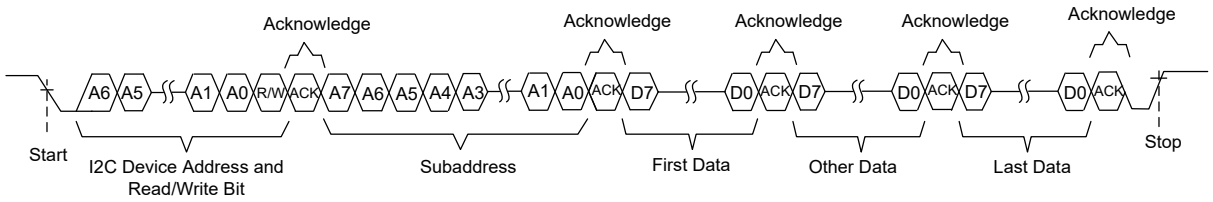

Figure17. Multiple Byte Write Transfer

Single Byte Write Transfer

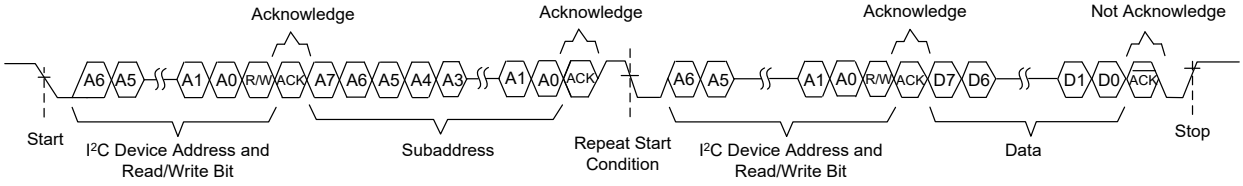

Figure18. Single Byte Read Transfer

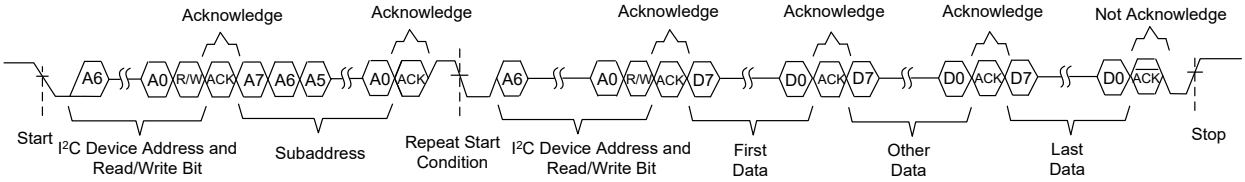

Figure19. Multiple Byte Read Transfer

SDATA Generator

The SDATA generator of SY24106L sends out I^2S out signal. In order for SDATA out process to stably function, the falling of SCLK should either synchronize or occur ahead of falling or rising of LRCLK. The monitor 0 pin can be configured as SDATA out signal in register 0x18.

Output Mode and MUX Selection

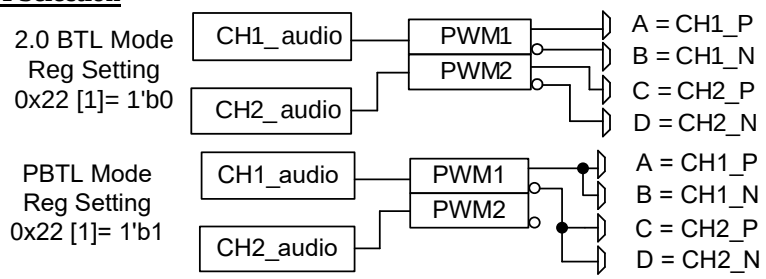

Figure20. Output Mode and MUX Selection

Single Filter PBTL Mode Support

The device supports parallel BTL mode with VOUT_A / VOUT_B (and VOUT_C / VOUT_D) connected before the LC filter. The bit 1 of register 0x22 should be set 1'b1 to configure the PBTL mode. If an over current or short condition is detected in either half bridge, all of bridges will be turned off. In BTL mode, The bit 1 of register 0x22 should be set to 1'b0.

Mixer

The input channels can be mixed into each output channels with designated gains and polarity in the register 0x5F. Step size of mixer gain is variable according to the gain level as shown below.

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Volume Range (dB)	Step (dB)
≤ -32	-∞
-6 ~ -32	1
+5.5 ~ -5.5	0.5
+18 ~ +6	1

Table1. Mixing Gain and Variable Step

4 mixing gain coefficients M11, M12, M21 and M22 are defined as shown in the equation below. Each Mxx stores volume value in dB scale, and the number values versus gain in dB are shown in table 3. By default, each input channel connected to each output channel directly; M11 and M22 are set as 0 dB in plus polarity, M12 and M21 are set as -∞ dB.

[Output Channels] = [Mixer Matrix] × [Input Channels]

$$\begin{bmatrix} CH1OUT \\ CH2OUT \end{bmatrix} = \begin{bmatrix} M11 & M12 \\ M21 & M22 \end{bmatrix} \bullet \begin{bmatrix} CH1IN \\ CH2IN \end{bmatrix}$$

Table2. Serial Mixer Matrix

Refer to table 3 to set mixer gain in register Address 0x5F in the Appendix.

Mixer Gain			
Index	dB	Index	dB
3F	18	1F	-4
3E	17	1E	-4.5
3D	16	1D	-5
3C	15	1C	-5.5
3B	14	1B	-6
3A	13	1A	-7
39	12	19	-8
38	11	18	-9
37	10	17	-10
36	9	16	-11
35	8	15	-12
34	7	14	-13
33	6	13	-14
32	5.5	12	-15
31	5	11	-16
30	4.5	10	-17
2F	4	0F	-18
2E	3.5	0E	-19
2D	3	0D	-20
2C	2.5	0C	-21
2B	2	0B	-22
2A	1.5	0A	-23
29	1	09	-24
28	0.5	08	-25
27	0	07	-26
26	-0.5	06	-27
25	-1	05	-28
24	-1.5	04	-29
23	-2	03	-30
22	-2.5	02	-31
21	-3	01	-32
20	-3.5	00	mute

Table3. Mixer Gain

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Pre-Processing

29 Bits 6.23 Number Format

All gain coefficients are 29bit coefficients using a 6.23 number format. 6.23 number format means that there are 6 bits to the left of the decimal point and 23 bits to the right of the decimal point.

Figure21. 6.23 Number Format

If the most significant sign bit is logic 0, then the number is a positive number, the weighting shown yields the correct number.

If the most significant sign bit is logic 1, then the number is a negative number. Every bit must be inverted, then add 1 to the result, and then the weighting shown in Figure 22.

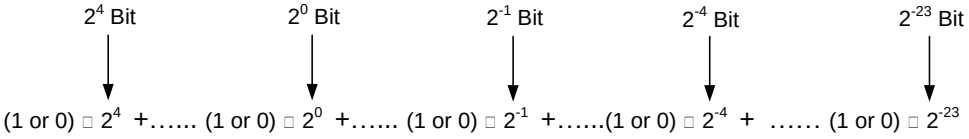

Figure22. Conversion weighting Factors—6.23 Format to Floating Point

Gain coefficients, entered via I^2C bus, must be entered as 32bits binary numbers. Bit[31:29] are zero padding.

Biquad Structure

Each biquad has a 2nd IIR filter structure and has three coefficients on the direct path (b_0, b_1, b_2) and 2 coefficients on feedback path (a_1, a_2) as shown in the diagram.

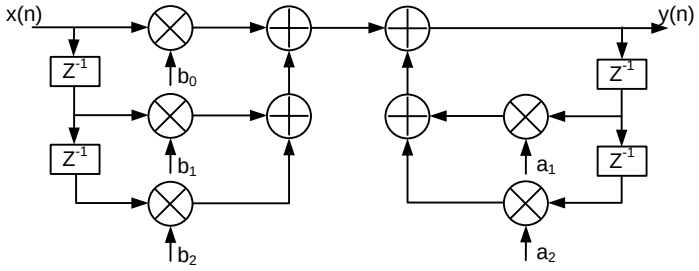

Figure23. Biquad Filter Structure

There are fourteen biquad filters linked serially in one channel. The biquad filters can be configured differently for each filter. The coefficients of BQn(n is from 0 to 13) are shared for both channel 1 and channel 2. BQn of channel 1 and channel 2 can be separately enabled or disabled. For example, BQ1 of channel 1 is enabled while BQ1 of channel 2 is disabled. As shown in Figure 24, first three filters can be configured as loudness control with loudness gain, and last four filters can be configured as SPEQ with SPEQ control.

The first BQ BQ0 must be enabled if enable loudness or prescale functionality by modifying the prescaler gain or

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loudness gain.

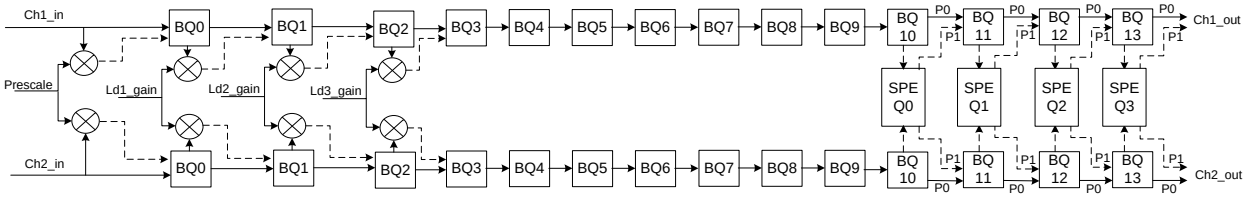

Figure24. Biquad Filter Chain

Filter coefficients are 29bit binary numbers and can be downloaded through I²C interface. Write actual coefficient values to 20 register addresses in the range from 0x30 to 0x4D to download biquad filter coefficients to SY24106L. Refer to table 4. The amount of bytes for each register address is variable. For example, 20 bytes are for a BQ filter while 4 bytes are for the Pre-scaler.

The enable/disable operation of these Bi-Quad filters can be made by configuring the bits in register addresses of 0x25~0x2B. When BQn(n from 10 to 13) is configured as SPEQ or SPEQ Limit in register 0x2B, the BQn of both channels are functional as SPEQ or SPEQ Limit together, which can't be separately enabled or disabled for each channel. When BQn is configured as EQn, the EQn can be separately enabled or disabled for each channel.

I²C address	0x30	0x31	0x32	0x33	0x34
Byte count	20	20	20	20	20
Description	BQ0 of CH1/2	BQ1 of CH1/2	BQ2 of CH1/2	BQ3 of CH1/2	BQ4 of CH1/2
I²C Address	0x35	0x36	0x37	0x38	0x39
Byte count	20	4	20	20	20
Description	BQ5 of CH1/2	Pre-scale of CH1/2	BQ6 of CH1/2	BQ7 of CH1/2	BQ8 of CH1/2
I²C address	0x3A	0x3B	0x3C	0x3D	0x3E
Byte count	20	20	20	20	20
Description	BQ9 of CH1/2	BQ10 of CH1/2	BQ11 of CH1/2	BQ12 of CH1/2	BQ13 of CH1/2
I²C address	0x43	0x44	0x45	0x46	0x4D
Byte count	12	12	12	12	12
Description	Coefficients of SPEQ0	Coefficients of SPEQ1	Coefficients of SPEQ2	Coefficients of SPEQ3	Loudness Gain

Table4. Address of Coefficients for Biquad Filter Chain

Loudness Control

The frequency characteristics can be compensated in low volume level to fit the acoustic characteristics of human ears with loudness control. The three coefficient of loudness can be downloaded through writing the 12 bytes of the register 0x4D. Four bytes are for one BQ loudness gain. The loudness gain values are shared for both channel 1 and channel 2. The first BQ BQ0 must be enabled before enable loudness by setting bit 0 of register 0x03.

Register Address 0x4D	byte count 12	bits[95:64]	3'b000, ld3_gain[28:0]
		bits[63:32]	3'b000, ld2_gain[28:0]
		bits[31:0]	3'b000, ld1_gain[28:0]

Table5. Loudness Gain

Super Parametric Equalizer

The frequency characteristics based on input signal level can be compensated to fit the acoustic characteristics of human ears with SPEQ function.

There are a biquad filter' coefficients and three additional coefficients for SPEQ. The three additional coefficients are related to gain and threshold. The biquad filter coefficient can be downloaded through writing 0x3B~0x3E. The three additional coefficients can be downloaded through writing the 12 bytes of the register 0x43~0x46. There are four bytes for one coefficient. The SPEQ coefficients are shared for both channel 1 and channel 2.

It can be configured as SPEQ Limit function as well. The frequency characteristics at some frequency point can't be limited to no more than the threshold with SPEQ Limit function. The way to download the coefficient is the same as SPEQ.

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Volume & Dynamic Range Control

Volume Control

The volume register 0x07, 0x08, and 0x09 correspond to master volume, channel 1 volume, and channel 2 volume.
Master Volume Control
Master volume – 0x07 (default is mute, 0x00)

Step	Range
0.5 dB	0 ~ -126 dB

Table6. Master Volume Steps

Channel Volume Control
Channel-1 volume – 0x08 (default is 0 dB, 0x9F)
Channel-2 volume – 0x09 (default is 0 dB, 0x9F)

Step	Range
0.5 dB	+48 ~ -79 dB

Table7. Channel Volume Steps

Volume Fine Control and Offset

Fine control for volume is +0.125dB step up to maximum +7.875dB boost. Step size is 0.125dB. It has high accurate step size and provides an offset gain for the channel volume and master volume.

Step	Range
0.125 dB	0 ~ +7.875 dB

Table8. Volume Fine Control Steps

Mute and Soft Volume Change

The chip enters mute state by setting soft mute flag of register Address 0x06. The bit 3 of register 0x06 is master mute flag for both left channel and right channel. The bit 0 of register 0x06 is individually mute flag for left channel while the bit 1 of register 0x06 is individually mute flag for right channel. With soft mute, the volume gradually increases or decreases when mute is turned off or on respectively.

Dynamic Range Control

The SY24106L features three multiband DRCs, as well as a full-band DRC, named post DRC. The multiband DRC is used as a three-band crossover, having an independent custom configuration for low, high, and mid frequency bands. Each band DRC has two dedicated BQs for frequency band crossover.
The DRC scheme has three DRC blocks. There is one ganged DRC for the high-band left/right channels, one DRC for the mid-band left/right channels, and one ganged DRC for the low-band left/right channels.
SY24106L has advanced algorithm taking input signal level, volume and threshold for dynamic gain of DRC, which provides powerful and balanced excellent sound experience.
There are two dedicated BQs for each band, and the amplitude of each DRC output can be adjusted by corresponding gain control. The outputs of three bands DRC are merged and followed by post DRC which produces the output data with the fully controlled dynamic range. For detailed setting of the DRC registers, please refer to the system register addresses in Table 9.

I^2C address	0x47	0x48	0x49	0x4A	0x4B	0x4C
Byte count	20	20	20	20	20	20
Description	BQ1 of LDRC	BQ2 of LDRC	BQ1 of MDRC	BQ2 of MDRC	BQ1 of HDRC	BQ2 of HDRC

Table9. Coefficient Register Map for Dynamic Range Control

The DRC input/output diagram is shown in figure 25.

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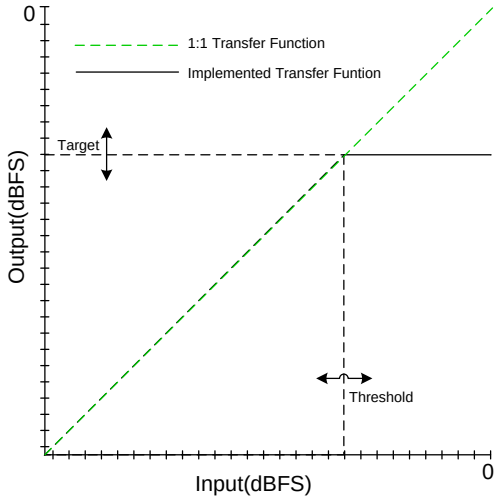

Figure25.Dynamic Range Control

Power Meter

The power meter measures internal signal's energy, which can be used to study the power profile. It can be configured by sending value of energy through register address 0x57 and parts of 0x58. Read the 10bit value in dB through register address 0x58 while read the 23bit linear value through register address 0x59.

DC Protection

The system from outputting DC signal can cause a speaker unit burnt. The chip employs three sub functions to prevent DC output, which are dynamically calculating and monitoring the memory checksum, detecting PWM DC, and cutting DC component via two hard-wired filters. The hard-wired DC cut filter removes the DC component. The other two functionalities only report the error status, and external controller may reset the chip by writing register 0x0F to assert a soft reset.

Memory Checksum

While initializing the system, the checksum data of coefficients are downloaded from the external MCU from the address 0x5A to 0x5B. This memory checksum block compares the checksum data of current memory block and the checksum data at the initial time. If there is a discrepancy between two values due to some memory fault, the error flag bit 7 or/and bit 6 of address 0x07 is set to high. The external MCU can monitor these error flags and reset the chip by setting the DC soft reset to high at address 0x0F. This DC soft reset will initialize the whole chip, and initialization process of the memory should be done thereafter

PWM DC Detection

A PWM DC detector is employed. When there is a DC component in the output, it sets PWM DC error flag of address 0x02 to high. The external controller may monitor this error flag and reset the chip by writing register 0x0F to assert a soft reset. The threshold of PWM DC detection at address 0x19 can be set to decide the level of DC monitoring for both Ternary and BD mode.

Hard-wired DC Cut

Two hard-wired DC cut filters are employed, which can prevent the system from outputting the signal of less than 1Hz frequency.

Recommended Command Sequences

Initialization Sequence

1) Hold all digital inputs low and ramp up AVDD/DVDD to at least 3.3V.
2) Initialize digital inputs and PVDD supply as follows:
   - Drive RST_B = 0, and other digital inputs to their desired state while ensuring that all are never more than 2.5V above AVDD/DVDD. Wait at least 100µs, drive RST_B= 1, and wait at least another 13.5ms.
   - Increase VDD_IO to 3.3V, after 100µs ramp up PVDD to at least 4.5V, then wait 10µs.

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3) Configure the DAP via I²C
4) Configure remaining registers
5) Exit shutdown (sequence defined below).

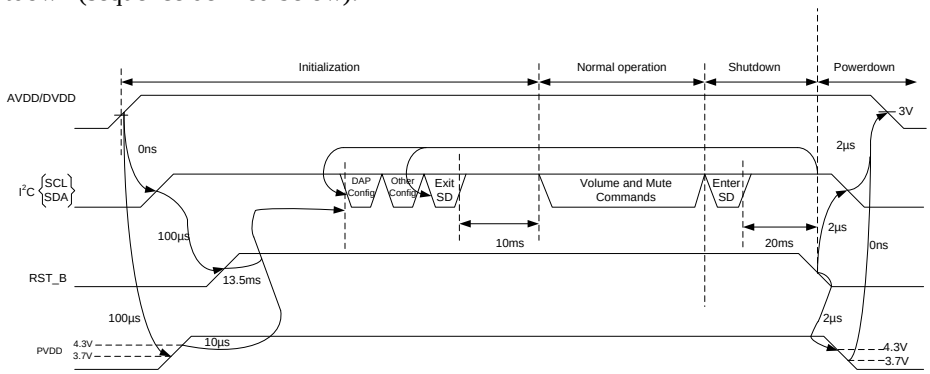

Figure26. Recommended Command Sequence

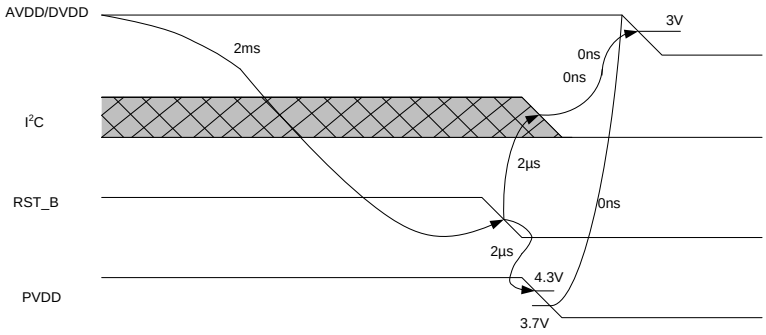

Figure27. Power Loss Sequence

Normal Operation

1) Write 0x00 or 0x01 to register 0x22.
2) Write to master/channel volume registers.
3) Write to soft mute registers.
4) Enter and exit shutdown (sequence defined below).

Shutdown Sequence

Enter:

1) Write 1'b1 to bit4 of register 0x22 to standby. Wait at least 10 ms
2) Write 1'b1 to bit5 of register 0x22 to shutdown.
3) Wait at least 20 ms
4) If desired, reconfigure by returning to step 4 of initialization sequence.

Exit:

1) Write1'b0 to bit5 of register 0x22.
2) Wait at least 10 ms.
3) Proceed with normal operation.

Appendix

Configuration Register Summary

Sub-address	Register Name	Bytes	Contents	Initialization Value
			A u indicates unused bits.	
0x00	Clock Control Register	1	brt_sel, u[6:5], fs_cnfg_manual_en, fs_rate_cnfg[1:0], fs_ rate_det[1:0]	0x1A

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0x01	Device ID Register	1	DEV_ID_REG[7:0]	0x25/0x35
0x02	Error Status Register	1	pbq_check_error, drc_check_error, sclk_err, lrclk_err, pwm_dc_error, short_fault, oc_fault, otuv_fault	0x00
0x03	System Control Register 1	1	u[7:5],soft_reset_en, fade_en, u[2:1], i2c_access_coef_ram_en	0x19
0x04	System Control Register 2	1	u[7:5], eq_en, dc_blocking_en, mixer_en, pm_en, loudness_en	0x1E
0x05	System Control Register 3	1	delay_line_lgth[4:0], u[2:1], a_sel_mode_reg	0x78
0x06	Soft Mute Register	1	u[7:5], hard_soft_umute, mvol_mute, u[2], dvol_mute_r, dvol_mute_l	0x10
0x07	Master Volume	1	mvol[7:0]	0x00(mute)
0x08	Channel 1 volume	1	dvol_l[7:0]	0x9F(0 dB)
0x09	Channel 2 volume	1	dvol_r[7:0]	0x9F(0 dB)
0x0A	Postscaler	1	postscaler[7:0]	0x7F
0x0B	mvol_fine_tune	1	u[7:6], vol_fine_tune[5:0]	0x00
0x0C~0x0E	N/A	1	Reserved	0x00
0x0F	DC Soft Reset Register	1	u[7:1], dc_soft_reset	0x00
0x10	Modulation Limit Register	1	u[7:4], pwm_mod_limit[3:0]	0x07
0x11	PWM OUTA Delay	1	pwm_phaseoffset1[7:0]	0x00
0x12	PWM OUTB Delay	1	pwm_phaseoffset2[7:0]	0x00
0x13	PWM OUTC Delay	1	pwm_phaseoffset3[7:0]	0x00
0x14	PWM OUTD Delay	1	pwm_phaseoffset4[7:0]	0x00
0x15	I^2S Control	1	u[7], i2s_sclk_inv, i2s_lr_polarity, i2s_enable, i2s_fmt[1:0], i2s_vbits[1:0]	0x10
0x16	DSP Control Register1	1	u[7:3], ch1_en, ch2_en, u[0]	0x06
0x17	Monitor Config1	1	u[7:5], sda_out_loc, monitor0_cfg[3:0]	0x00
0x18	Monitor Config2	1	Monitor0_cfg[3:0]	0x00
0x19	PWM DC Threshold	1	u[7:4], threshold_sel[3:0]	0x05
0x1A	N/A	1	Reserved	0x00
0x1B	Short Control Reg	1	u[7], fault_clr_interval[2:0], second_phase_en,retry_interval[2:0]	0x35
0x1C~1E	N/A	1	Reserved	0x00
0x1F	Checksum Control Register	1	u[7:3], pwm_dc_det_en, pbq_checksum_en, mdrc_checksum_en	0x00
0x20	Input MUX Register	1	i2s_din_sel[1:0], u[5:0]	0x00
0x21	N/A	1	Reserved	0x00
0x22	PWM Control Register	1	u[7:6], all_shutdown, enter_all_standby, u[3:2], pbtl_en, ternary_mode_en	0x31
0x23	Fault Select Register	1	u[7], cnt_x_cfg[2:0], u[3:0]	0x10
0x24	N/A	1	Reserved	0x00
0x25	CH1_EQ_CTRL1	1	u[7:6], ch1_eq_ctrl1[5:0]	0x00
0x26	CH1_EQ_CTRL2	1	ch1_eq_ctrl2[7:0]	0x00
0x27	CH2_EQ_CTRL1	1	u[7:6], ch2_eq_ctrl1[5:0]	0x00
0x28	CH2_EQ_CTRL2	1	ch2_eq_ctrl2[7:0]	0x00
0x29	SPEQ_CTRL_1	1	bq9_ctrl[1:0], bq8_ctrl[1:0], bq7_ctrl[1:0], bq6_ctrl[1:0]	0x00
0x2A	SPEQ_CTRL_2	1	bq13_ctrl[1:0], bq12_ctrl[1:0], bq11_ctrl[1:0], bq10_ctrl[1:0]	0x00

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0x2B	SPEQ_CTRL_3	1	u[7:1], speq_det_method[0]	0x00
0x2C~2F	N/A	1	Reserved	0x00
0x30	bq0	20	u[2:0], bq0_b0[28:0]	0x0080 0000
			u[2:0], bq0_b1[28:0]	0x0000 0000
			u[2:0], bq0_b2[28:0]	0x0000 0000
			u[2:0], bq0_a1[28:0]	0x0000 0000
			u[2:0], bq0_a2[28:0]	0x0000 0000
0x31	bq1	20	u[2:0] ,bq1_b0[28:0]	0x0080 0000
			u[2:0] ,bq1_b1[28:0]	0x0000 0000
			u[2:0], bq1_b2[28:0]	0x0000 0000
			u[2:0], bq1_a1[28:0]	0x0000 0000
			u[2:0], bq1_a2[28:0]	0x0000 0000
0x32	bq2	20	u[2:0], bq2_b0[28:0]	0x0080 0000
			u[2:0], bq2_b1[28:0]	0x0000 0000
			u[2:0], bq2_b2[28:0]	0x0000 0000
			u[2:0], bq2_a1[28:0]	0x0000 0000
			u[2:0], bq2_a2[28:0]	0x0000 0000
0x33	bq3	20	u[2:0], bq3_b0[28:0]	0x0080 0000
			u[2:0], bq3_b1[28:0]	0x0000 0000
			u[2:0], bq3_b2[28:0]	0x0000 0000
			u[2:0], bq3_a1[28:0]	0x0000 0000
			u[2:0], bq3_a2[28:0]	0x0000 0000
0x34	bq4	20	u[2:0], bq4_b0[28:0]	0x0080 0000
			u[2:0], bq4_b1[28:0]	0x0000 0000
			u[2:0], bq4_b2[28:0]	0x0000 0000
			u[2:0], bq4_a1[28:0]	0x0000 0000
			u[2:0], bq4_a2[28:0]	0x0000 0000
0x35	bq5	20	u[2:0], bq5_b0[28:0]	0x0080 0000
			u[2:0], bq5_b1[28:0]	0x0000 0000
			u[2:0], bq5_b2[28:0]	0x0000 0000
			u[2:0], bq5_a1[28:0]	0x0000 0000
			u[2:0], bq5_a2[28:0]	0x0000 0000
0x36	eq_prescaler	4	u[2:0], eq_prescaler[28:0]	0x0800 0000
0x37	bq6	20	u[2:0], bq6_b0[28:0]	0x0080 0000
			u[2:0], bq6_b1[28:0]	0x0000 0000
			u[2:0], bq6_b2[28:0]	0x0000 0000
			u[2:0], bq6_a1[28:0]	0x0000 0000
			u[2:0], bq6_a2[28:0]	0x0000 0000
0x38	bq7	20	u[2:0], bq7_b0[28:0]	0x0080 0000
			u[2:0], bq7_b1[28:0]	0x0000 0000
			u[2:0], bq7_b2[28:0]	0x0000 0000
			u[2:0], bq7_a1[28:0]	0x0000 0000
			u[2:0], bq7_a2[28:0]	0x0000 0000

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0x39	bq8	20	u[2:0], bq8_b0[28:0]	0x0080 0000
			u[2:0], bq8_b1[28:0]	0x0000 0000
			u[2:0], bq8_b2[28:0]	0x0000 0000
			u[2:0], bq8_a1[28:0]	0x0000 0000
			u[2:0], bq8_a2[28:0]	0x0000 0000
0x3A	bq9	20	u[2:0], bq9_b0[28:0]	0x0080 0000
			u[2:0], bq9_b1[28:0]	0x0000 0000
			u[2:0], bq9_b2[28:0]	0x0000 0000
			u[2:0], bq9_a1[28:0]	0x0000 0000
			u[2:0], bq9_a2[28:0]	0x0000 0000
0x3B	bq10	20	u[2:0], bq10_b0[28:0]	0x0080 0000
			u[2:0], bq10_b1[28:0]	0x0000 0000
			u[2:0], bq10_b2[28:0]	0x0000 0000
			u[2:0], bq10_a1[28:0]	0x0000 0000
			u[2:0], bq10_a2[28:0]	0x0000 0000
0x3C	bq11	20	u[2:0], bq11_b0[28:0]	0x0080 0000
			u[2:0], bq11_b1[28:0]	0x0000 0000
			u[2:0], bq11_b2[28:0]	0x0000 0000
			u[2:0], bq11_a1[28:0]	0x0000 0000
			u[2:0], bq11_a2[28:0]	0x0000 0000
0x3D	bq12	20	u[2:0], bq12_b0[28:0]	0x0080 0000
			u[2:0], bq12_b1[28:0]	0x0000 0000
			u[2:0], bq12_b2[28:0]	0x0000 0000
			u[2:0], bq12_a1[28:0]	0x0000 0000
			u[2:0], bq12_a2[28:0]	0x0000 0000
0x3E	bq13	20	u[2:0], bq13_b0[28:0]	0x0080 0000
			u[2:0], bq13_b1[28:0]	0x0000 0000
			u[2:0], bq13_b2[28:0]	0x0000 0000
			u[2:0], bq13_a1[28:0]	0x0000 0000
			u[2:0], bq13_a2[28:0]	0x0000 0000
0x3F	Reserved	12	Reserved	0x0004_0000
			Reserved	0x0080_0000
			Reserved	0x0040_0000
0x40	Reserved	12	Reserved	0x0004_0000
			Reserved	0x0080_0000
			Reserved	0x0040_0000
0x41	Reserved	12	Reserved	0x0004_0000
			Reserved	0x0080_0000
			Reserved	0x0040_0000
0x42	Reserved	12	Reserved	0x0004_0000
			Reserved	0x0080_0000
			Reserved	0x0040_0000
0x43	speq0_coef	12	u[2:0], speq0_th[28:0]	0x0004_0000
			u[2:0], speq0_coef1[28:0](p0)	0x0080_0000
			u[2:0], speq0_coef2[28:0](p1)	0x0040_0000
0x44	speq1_coef	12	u[2:0], speq1_th[28:0]	0x0004_0000
			u[2:0], speq1_coef1[28:0]	0x0080_0000
			u[2:0], speq1_coef2[28:0]	0x0040_0000
0x45	speq2_coef	12	u[2:0], speq2_th[28:0]	0x0004_0000
			u[2:0], speq2_coef1[28:0]	0x0080_0000
			u[2:0], speq2_coef2[28:0]	0x0040_0000

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0x46	speq3_coef	12	u[2:0], speq3_th[28:0]	0x0004_0000
			u[2:0], speq3_coef1[28:0]	0x0080_0000
			u[2:0], speq3_coef2[28:0]	0x0040_0000
0x47	ldrc_bq1	20	u[2:0], ldrc_bq1_b0[28:0]	0x0080 0000
			u[2:0], ldrc_bq1_b1[28:0]	0x0000 0000
			u[2:0], ldrc_bq1_b2[28:0]	0x0000 0000
			u[2:0], ldrc_bq1_a1[28:0]	0x0000 0000
			u[2:0], ldrc_bq1_a2[28:0]	0x0000 0000
0x48	ldrc_bq2	20	u[2:0], ldrc_bq2_b0[28:0]	0x0080 0000
			u[2:0], ldrc_bq2_b1[28:0]	0x0000 0000
			u[2:0], ldrc_bq2_b2[28:0]	0x0000 0000
			u[2:0], ldrc_bq2_a1[28:0]	0x0000 0000
			u[2:0], ldrc_bq2_a2[28:0]	0x0000 0000
0x49	mdrc_bq1	20	u[2:0], mdrc_bq1_b0[28:0]	0x0080 0000
			u[2:0], mdrc_bq1_b1[28:0]	0x0000 0000
			u[2:0], mdrc_bq1_b2[28:0]	0x0000 0000
			u[2:0], mdrc_bq1_a1[28:0]	0x0000 0000
			u[2:0], mdrc_bq1_a2[28:0]	0x0000 0000
0x4A	mdrc_bq2	20	u[2:0], mdrc_bq2_b0[28:0]	0x0080 0000
			u[2:0], mdrc_bq2_b1[28:0]	0x0000 0000
			u[2:0], mdrc_bq2_b2[28:0]	0x0000 0000
			u[2:0], mdrc_bq2_a1[28:0]	0x0000 0000
			u[2:0],mdrc_bq2_a2[28:0]	0x0000 0000
0x4A	mdrc_bq2	20	u[2:0], mdrc_bq2_b0[28:0]	0x0080 0000
			u[2:0], mdrc_bq2_b1[28:0]	0x0000 0000
			u[2:0], mdrc_bq2_b2[28:0]	0x0000 0000
			u[2:0], mdrc_bq2_a1[28:0]	0x0000 0000
			u[2:0], mdrc_bq2_a2[28:0]	0x0000 0000
0x4B	hdrc_bq1	20	u[2:0], hdrc_bq1_b0[28:0]	0x0080 0000
			u[2:0], hdrc_bq1_b1[28:0]	0x0000 0000
			u[2:0], hdrc_bq1_b2[28:0]	0x0000 0000
			u[2:0], hdrc_bq1_a1[28:0]	0x0000 0000
			u[2:0], hdrc_bq1_a2[28:0]	0x0000 0000
0x4C	hdrc_bq2	20	u[2:0], hdrc_bq2_b0[28:0]	0x0080 0000
			u[2:0], hdrc_bq2_b1[28:0]	0x0000 0000
			u[2:0], hdrc_bq2_b2[28:0]	0x0000 0000
			u[2:0], hdrc_bq2_a1[28:0]	0x0000 0000
			u[2:0], hdrc_bq2_a2[28:0]	0x0000 0000
0x4D	loundness	12	u[2:0], ld1_gain[28:0]	0x0800 0000
			u[2:0], ld2_gain[28:0]	0x0800 0000
			u[2:0], ld3_gain[28:0]	0x0800 0000
0x4E	ldrc_envlp_tc_up	3	u[23], ldrc_envlp_tc_up[22:0]	0x01_FC05
0x4F	ldrc_envlp_tc_dn	3	u[23], ldrc_envlp_tc_dn[22:0]	0x7F_E900
0x50	mdrc_envlp_tc_up	3	u[23], mdrc_envlp_tc_up[22:0]	0x01_FC05
0x51	mdrc_envlp_tc_d	3	u[23], mdrc_envlp_tc_dn[22:0]	0x7F_9E9F
0x52	hdrc_envlp_tc_up	3	u[23], hdrc_envlp_tc_up[22:0]	0x01_FC05
0x53	hdrc_envlp_tc_dn	3	u[23], hdrc_envlp_tc_dn[22:0]	0x7D_5C65
0x54	PWM MUX Register	4	u[31:21], pwm_connection_test[4:0], u[15:0]	0x0000_0000
0x55	PWM Outflip Register	4	u[31], pwm_dvol_ramp_point[6:0], u[23:22], pwm_clip_mode, pwm_ad_mode_en, u[19:17], pwm_outflip_reg[12], u[15], pwm_outflip_reg[11:9], u[11], pwm_outflip_reg[8:6], u[7],	0x4000_3210

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			pwm_outflip_reg[5:3], u[3], pwm_outflip_reg[2:0]	
0x56	PWM Control Register	4	u[31:28], pwm_ns_order, pwm_ns_bf_clr, pwm_roundup, pwm_direct_fs, pwm_dither_clr, pwm_dither_en, pwm_dither_range, dither_pos[4:0], pwm_cnvt_dstep[7:0], pwm_cnvt_dvalue[7:0]	0x0000_002F
0x57	pm_coef	6	u[47], pm_coef_up[22:0], u[23], pm_coef_dn[22:0]	0x000800_7FF800
0x58	pm_crtl_rb1	3	u[23:20], pm_det_method, pm_source[1:0], pm_loc, pm_lvl_db[9:2], u[7:2], pm_lvl_db[1:0]	0x000_000
0x59	pm_crtl_rb2	3	u[23], pm_lvl_linear_rb[22:0]	0x00 0000
0x5A	pbq_checksum	4	u[31:29], pbq_checksum_key[28:0]	0x0800_0000
0x5B	mdrc_checksum	4	u[31:29], mdrc_checksum_key[28:0]	0x0000_0000
0x5C	N/A	1	Reserved	0x00
0x5D	speq_atk_rel_tc_1	12	u[95], speq3_atk_tc[22:0]	0x000800
			u[71], speq2_atk_tc[22:0]	0x000800
			u[47], speq1_atk_tc[22:0]	0x000800
			u[23], speq0_atk_tc[22:0]	0x000800
0x5E	speq_atk_rel_tc_2	12	u[95], speq3_rel_tc[22:0]	0x7ff800
			u[71], speq2_rel_tc[22:0]	0x7ff800
			u[47], speq1_rel_tc[22:0]	0x7ff800
			u[23], speq0_rel_tc[22:0]	0x7ff800
0x5F	ch12_mixer_gain	4	u[31], ch1_fch1_p, ch1_mixer_fch1_gain[5:0]	0x27
			u[23], ch1_fch2_p, ch1_mixer_fch2_gain[5:0]	0x00
			u[15], ch2_fch1_p, ch2_mixer_fch1_gain[5:0]	0x00
			u[7], ch2_fch2_p, ch2_mixer_fch2_gain[5:0]	0x27
0x60	drc_ctrl	4	u[31:25], drc_det_method, u[23:9], envlp_mode, u[7:4], ldrc_lmt_en, mdrc_lmt_en, hdrc_lmt_en, pdrc_lmt_en	0x0100_0000
0x61	LDRC_LMT_CFG1	3	u[23:22], ldrc_makeup[9:0], u[11:10], ldrc_lmt_thr[9:0]	0x3C9_30C
0x62	LDRC_LMT_CFG2	3	1'b0	0x7F_FF51
			ldrc_lmt_atk_tc[[22:0]	
0x63	LDRC_LMT_CFG3	3	1'b0	0x7F_55C6
			ldrc_lmt_rel_tc[[22:0]	
0x64	MDRC_LMT_CFG1	3	u[23:22], mdrc_makeup[9:0], u[11:10], mdrc_lmt_thr[9:0]	0x3C5_30C
0x65	MDRC_LMT_CFG2	3	1'b0	0x7F_FF51
			mdrc_lmt_atk_tc[[22:0]	
0x66	MDRC_LMT_CFG3	3	1'b0	0x7F_1D3B
0x65	MDRC_LMT_CFG2	3	1'b0	0x7F_FF51
			mdrc_lmt_atk_tc[[22:0]	
0x66	MDRC_LMT_CFG3	3	1'b0	0x7F_1D3B
			mdrc_lmt_rel_tc[[22:0]	
0x67	HDRC_LMT_CFG1	3	u[23:22], mdrc_makeup[9:0], u[11:10], mdrc_lmt_thr[9:0]	0x3C9_30C
0x68	HDRC_LMT_CFG2	3	1'b0	0x7F_FF51
			hdrc_lmt_atk_tc[[22:0]	
0x69	HDRC_LMT_CFG3	3	1'b0	0x0F_F016
			hdrc_lmt_rel_tc[[22:0]	

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0x6A	PDRC_LMT_CFG1	3	u[23:10] pdrc_lmt_thr[9:0]	0x000_30C
0x6B	PDRC_LMT_CFG2	3	1'b0 pdrc_lmt_atk_tc[[22:0]	0x7F_FF51
0x6C	PDRC_LMT_CFG3	3	1'b0 pdrc_lmt_rel_tc[[22:0]	0x7A_C6B8
0x6D	drc_envlp_tc_up	3	u[23], drc_envlp_tc_up[22:0]	0x01_FC05
0x6E	drc_envlp_tc_dn	3	u[23], drc_envlp_tc_dn[22:0]	0x7F_BBCD
0x6F	N/A	1	Reserved	0x00
0x70	BIST Control	1	u[7], bist_mode, bist_go, bist_ram1_skip, u[3], bist_ram3_skip, bist_ram4_skip, u[0]	0x00
0x71	PLL Status	4	sw_refclk_sel_en, sw_refclk_sel, pllc_pllclksel, pllc_pll_prog, pllc_refdiv_pll[7:0], u[19], pllc_fbdiv_pll[10:0], u[7], pllc_cp_pll[2:0], pllc_rz_pll[1:0], pllc_vcci_pll[1:0]	0x00_63_00_2D
0x72	PLL Control	2	u[15:13], pll_enable_sel,manual_pll_enable, u[10:9], brt_sel,u[7:1], pll_osc_force_en	0x0000
0x73	spk_seq_bypass	1	u[7:2], spk_seq_bypass[1:0],	0x00
0x74	Func_test	1	ps_test_en_b, ps_test_mod0, ps_test_mod1, i2s_loop_en, u[3], func_test[2:0]	0x80
0x75	Tm_by_reg	1	u]7:5], tm_by_reg[4:0]	0x00
0x76	PROT_SYS_CNTL	1	u[7:5],poweron_short_protect_enshort_protect_en, otuv_protect_en, oc_protect_en, avdd_uv_protect_en	0x1F
0x77	I^2C Control	1	u[7:2],i2c_dly_en,i2c_sda_timeout_en	0x03
0x78~0x79	N/A	1	Reserved	0x00
0x7A	Exit Over Current Register	1	ocdet_dis_num[7:0]	0x40
0x7B	Oscillator trim Control	1	u[7:2], osc_trim_done, factory_trim_dis	0x01
0x7C	Oscillator Trim Register1	4	u[31:13], osc_trim_data[4:0], u[7:3], osc_trim_go, d2a_osc_pwd, d2a_post_trim_pwd	0x0000_1000
0x7D	Oscillator Trim Register2	4	u[31:22], trim_program_en, trim_program_data[4:0], u[15:14], trim_efuse_data_en, trim_efuse_data[4:0], u[7], efuse_time[5:0], trim_efuse_en	0x000F_0F17
0x7E	Analog Ref_top Control	4	u[31:12], v1p8d_ctrl[1:0], d2a_ref_ib_ctrl[1:0], d2a_ref_pf[2:0], d2a_reg_avdd_ctrl[1:0], d2a_ref_pwd, d2a_reg_avdd_pwd, d2a_uv_detect_pwd	0x0000_0200
0x7F	N/A	1	Reserved	0x00
0x80	dsp_3d_coef	3	dsp_3d_coef[23:0]	0x40 0000
0x81	dsp_3d_mix	3	dsp_3d_mix[23:0]	0x40 0000
0x82	Inter_Private Register	4	u[31:8], refclk_stop_reg_en, sclk_err_en, lr_err_en, refclk_stop_err_en, u[3:1], spk_scdet_en	0x0000_00F0
0x83	DRC_FTUNE	1	pdrc_ftune[1:0],hdrc_ftune[1:0], mdrc_ftune[1:0],ldrc_ftune[1:0]	0x00
0x84	N/A	1	Reserved	0x00

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0x85	Fault Over Current Small Detect Windows Width	4	u[31:10],ocfast_trig_en, ocdet_mannual_sel,u[7:6], ocdet_wind_width[5:0]	0x0000_0001
0x86	Fault Over Current Threshold	4	u[31:15],filter_deglitch[2:0], u[11:9],ocdet_en_num[8:0]	0x0000_0001
0x87	N/A	1	Reserved	0x00
0x88	N/A	1	Reserved	0x00
0x89	N/A	1	Reserved	0x00
0x8A	N/A	1	Reserved	0x00
0x8B	FUNC_CTRL	1	u[7:2], 3d_en, u[0]	0x00
0x8C~0x F7	N/A		Reserved	
0xF8	Device Address Enable Register	4	Write F9 A5 A5 A5 in this register to enable write to device address update (0xF9)	0x0000 0000
0xF9	Device Address Update Register	4	u[31:8] , New Dev Id[7:1] , ZERO[0] (New Dev Id (7:1) defines the new device address)	0x0000 0036
0xFB~0xFF		4	Reserved	0x0000 0000

Configuration Registers

Clock Control Register

Register Address	Bit	Type	Label	Default		Description
0x00	7	RW	brt_sel	1'b0	8'h1A	1'b0: 48kHz (in case of pll_ref_clk = osc_clk) 1'b1: 44.1kHz (in case of pll_ref_clk = osc_clk)
	6:5	R	N/A	2'b00		Reserved
	4	RW	fs_cnfg_manual_en	1'b1		1'b0: Auto detect I^2S sample rate 1'b1: Configured I^2S sample rate by MCU
	3:2	RW	fs_ rate_cnfg[1:0]	2'b10		2'b00: 32kHz 2'b01: 96kHz 2'b10: 44.1kHz/48kHz 2'b11: Reserved If fs_cnfg_manual_en is set to 1, the two bits are valid to configure the I^2S sample rate.
	1:0	R	fs_ rate_det[1:0]	2'b10		Sample rate detected: 2'b00: 32kHz 2'b01: 96kHz 2'b10: 44.1kHz/48kHz 2'b11: Reserved

Device ID Register

Register Address	Bit	Type	Label	Default		Description
0x01	7:0	R	N/A	0x25/0x35	0x25/0x35	Identification code 0x25: Not support headphone 0x35: Support headphone

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Each error bit will be sticked once the error occurs, which can be cleared by writing 1'b0 to it.

Error Status Register						
Register Address	Bit	Type	Label	Default		Description
0x02	7	RW	pbq_check_error	1'b0	8'h00	1'b0: Normal 1'b1:BQ checksum error
	6	RW	drc_check_error	1'b0		1'b0: Normal 1'b1:DRC checksum error
	5	RW	sclk_err	1'b0		1'b0: Normal 1'b1:SCLK error
	4	RW	lrclk_err	1'b0		1'b0: Normal 1'b1:LRCLK error
	3	RW	pwm_dc_error	1'b0		1'b0: Normal 1'b1:PWM DC detected
	2	RW	short_fault	1'b0		1'b0: Normal 1'b1:Short is detected
	1	RW	oc_fault	1'b0		1'b0: Normal 1'b1: Over current is detected
	0	RW	otuv_fault	1'b0		1'b0: Normal 1'b1: Over temperature or under voltage is detected

System Control Register 1						
Register Address	Bit	Type	Label	Default		Description
0x03	7:5	R	N/A	3'b000	0x19	Reserved
	4	RW	dc_soft_reset_en	1'b1		1'b0:DC soft reset disabled 1'b1:DC soft reset enabled
	3	RW	dsp_fade_en_reg	1'b1		1'b0:Fade disabled, volume changes immediately 1'b1:Fade enabled, volume changes fades between old/new value
	2:1	R	N/A	2'b00		Reserved
	0	RW	i2c_access_coef_ram_en	1'b1		1'b0: DAP access to register 0x30~4D(RAM) 1'b1: I^2C bus access to register 0x30~4D(RAM)

System Control Register 2						
Register Address	Bit	Type	Label	Default		Description
0x04	7:5	R	N/A	3'b000	0x1E	Reserved
	4	RW	eq_enable	1'b1		Eq, speq, enable or not: 1'b0: Disable 1'b1:Enable
	3	RW	dc_blocking_en	1'b1		Enable dc blocking: 1'b0: Disable 1'b1: Enable
	2	RW	mixer_en	1'b1		Enable mixer: 1'b0: Disable 1'b1: Enable
	1	RW	pm_en	1'b1		Enable power meter: 1'b0: Disable 1'b1: Enable
	0	RW	loudness_en	1'b0		Enable loudness: 1'b0: Disable 1'b1: Enable

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System Control Register 3						
Register Address	Bit	Type	Label	Default		Description
0x05	7:3	RW	delay_line_lgth [4:0]	5'h0f	0x78	Length of DRC delay line. 0~20 samples.
	2:1	R	N/A	2'b00		Reserved
	0	RW	a_sel_mode_reg	1'b0		1'b0: When reset release, the I²C device address will be fixed by ADDR_SEL. 1'b1:When ADDR_SEL configured as input, the I²C device address could be changed according to ADDR_SEL in any moment.

Soft Mute Register						
Register Address	Bit	Type	Label	Default		Description
0x06	7:5	R	N/A	3'b000	0x10	Reserved
	4	RW	hard_soft_umute	1'b1		1'b0:Soft unmute on recovery from clock error 1'b1:Hard unmute on recovery from clock error
	3	RW	dsp_mvol_mute_reg	1'b0		1'b0:Master unmute 1'b1:Master mute
	2	R	N/A	1'b0		Reserved
	1	RW	dsp_dvol_mute_r_reg	1'b0		1'b0:Soft unmute channel 2 1'b1:Soft mute channel 2
	0	RW	dsp_dvol_mute_l_reg	1'b0		1'b0:Soft unmute channel 1 1'b1:Soft mute channel 1

Master Volume						
Register Address	Bit	Type	Label	Default		Description
0x07	7:0	RW	mas_vol[7:0]	8'h00	0x00	8'h00~8'h02: soft mute 8'h03: -126dB 8'hff: 0dB Step: 0.5dB

Channel 1 Volume						
Register Address	Bit	Type	Label	Default		Description
0x08	7:0	RW	dsp_dvol_l[7:0]	8'h9F	8'h9F	8'h00: Mute 'h01: -79dB 88'h9F: 0dB 8'hFF: 48dB Sep: 0.5dB

Channel 2 Volume						
Register Address	Bit	Type	Label	Default		Description
0x09	7:0	RW	dsp_dvol_r[7:0]	8'h9F	8'h9F	8'h00: Mute 8'h01: -79dB 8'h9F: 0dB 8'hFF: 48dB step: 0.5dB

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Postsacler(0x0A)						
Register Address	Bit	Type	Label	Default		Description
0x0A	7:0	RW	postscaler[7:0]	8'h7F	8'h7F	00~FF, Post scale. Linear gain, 7F is 1(0dB). FF is 2(6dB)

VOL_FTUNE(0x0B)						
Register Address	Bit	Type	Label	Default		Description
0x0B	7:6	R	N/A	2'b00	0x00	Reserved
	5:0	RW	vol_fine_tune[5:0]	6'h00		Volume offset and fine tune. 6'h00~6'h3F: 0db ~ +7.875dB. Bits , step is 0.125dB

Reserved(0x0C~0x0E)						
Register Address	Bit	Type	Label	Default		Description
0x0C ~0E	7:0	R	N/A	8'h00	8'h00	Reserved

Soft Reset Register						
Register Address	Bit	Type	Label	Default		Description
0x0F	7:1	R	N/A	7'h00	0x00	Reserved
	0	RW	dc_soft_reset	1'b0		Write this bit 1, will reset the whole chip. The bit will be automatically cleared to 1'b0 after DC soft reset is asserted.

Modulation Limit Register						
Register Address	Bit	Type	Label	Default		Description
0x10	7:4	R	N/A	4'h0	8'h07	Reserved
	3:0	RW	pwm_mod_limt [3:0]	4'h7		4'h0: Max 511; Min 1; 4'h1: Max 509; Min 3; 4'h2: Max 508; Min 4; 4'h3: Max 507; Min 5; 4'h4: Max 506; Min 6; 4'h5: Max 505; Min 7; 4'h6: Max 504; Min 8; 4'h7: Max 503; Min 9; 4'h8: Max 502; Min 10; 4'h9: Max 501; Min 11; 4'ha: Max 500; Min 12; 4'hb: Max 499; Min 13; 4'hc: Max 498; Min 14; 4'hd: Max 496; Min 16; 4'he: Max 494; Min 18; 4'hf: Max 492; Min 20;

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PWM A Channel Delay						
Register Address	Bit	Type	Label	Default		Description
0x11	7:0	RW	pwm_phaseoffset1 [7:0]	8'h00	8'h00	Add an offset delay to PWM_CH1P , -128(lead 128 cycles) ~127(lag 127 cycles), 80H(-128)->FF(-1)->00(0)->7F(127) Step: 5.1ns 48kHz base rate, 5.536ns 44.1kHz base rate

PWM B Channel Delay						
Register Address	Bit	Type	Label	Default		Description
0x12	7:0	RW	pwm_phaseoffset2 [7:0]	8'h00	8'h00	Add an offset delay to PWM_CH1N ,-128(lead 128 cycles) ~127(lag 127 cycles), 80H(-128)->FF(-1)->00(0)->7F(127) Step: 5.1ns 48kHz base rate, 5.536ns 44.1kHz base rate

PWM C Channel Delay						
Register Address	Bit	Type	Label	Default		Description
0x13	7:0	RW	pwm_phaseoffset3 [7:0]	8'h00	8'h00	Add an offset delay to PWM_CH2P , -128(lead 128 steps) ~127(lag 127 steps), 80H(-128)->FF(-1)->00(0)->7F(127) Step: 5.1ns 48kHz base rate, 5.536ns 44.1kHz base rate

PWM D Channel Delay						
Register Address	Bit	Type	Label	Default		Description
0x14	7:0	RW	pwm_phaseoffset4 [7:0]	8'h00	8'h00	Add an offset delay to PWM_CH2N , -128(lead 128 cycles) ~127(lag 127 cycles), 80H(-128)->FF(-1)->00(0)->7F(127) Step: 5.1ns 48kHz base rate, 5.536ns 44.1kHz base rate

I^2S Control						
Register Address	Bit	Type	Label	Default		Description
0x15	7		N/A		8'h10	Reserved
	6	RW	i2s_sclk_inv	1'b0		1'b0:Not invert sclk 1'b1: Invert sclk
	5	RW	i2s_lr_polarity	1'b0		1'b0:Not invert lrclk 1'b1:Invert lrclk
	4	RW	i2s_en	1'b1		0:Disable 1: Enable
	3:2	RW	i2s_fmt	2'b00		2'b00: I^2S 2'b01: LJ 2'b10: RJ 2'b11: Reserved
	1:0	RW	i2s_vbits	2'b00		2'b00: 24bits 2'b01: 20bits 2'b10: 18bits 2'b11: 16bits

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DSP Control Register1						
Register Address	Bit	Type	Label	Default		Description
0x16	7:3	R	N/A	5'd0	8'h06	Reserved
	2	RW	ch1_en	1'b1		Enable channel 1: 1'b0 Disable 1'b1: Enable
	1	RW	ch2_en	1'b1		Enable channel 2: 1'b0 Disable 1'b1: Enable
	0	R	N/A	1'b0		Reserved

Monitor Pin Configured Register1						
Register Address	Bit	Type	Label	Default		Description
0x17	7:5	R	N/A	3'h0	8'h00	Reserved
	4	RW	sda_out_loc	1'b0		I^2S data out selection. 1: Select audio data prior to processing. 0: Select data behind prcossing.
	3:0	RW	N/A	4'h0		Reserved

Monitor Pin Configured Register2						
Register Address	Bit	Type	Label	Default		Description
0x18	7:4	RW	N/A	4'h0	8'h00	Reserved
	3:0	RW	Monitor0_cfg[3:0]	4'h0		4'h0: i2s_data_out 4'h1: pwm_out_a 4'h2: pwm_out_b 4'h3: pwm_out_c 4'h4: pwm_out_d 4'h5~4'hf : Reserved

PWM Direct Current Threshold						
Register Address	Bit	Type	Label	Default		Description
0x19	7:4	R	Reserved	4'h0	8'h05	Reserved
	3:0	RW	threshold_sel[3:0]	4'h5		When enable PWM DC detection, it will monitor the duty cycle of all of PWM outputs; The threshold can be set as following, step is 1%: 4'h0:1% 4'h1:2% …… 4'hf: 15%

Reserved						
Register Address	Bit	Type	Label	Default		Description
0x1A	7:5	R	N/A	3'b000	8'h00	Reserved
	4:0	RW	N/A	5'h00		Reserved

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Short Control Register						
Register Address	Bit	Type	Label	Default		Description
0x1B	7	R	N/A	1'b0	8'h35	Reserved
	6:4	RW	fault_clr_interval	3'b011		3'd0:1ms 3'd1: 1ms 3'd2: 2ms 3'd3: 4ms 3'd4: 8ms 3'd5: 16ms Others: Reserved
	3	RW	second_phase_en	1'b0		1'b0: Disable 1'b1: Enable
	2:0	RW	retry_interval	3'b101		3'd0:100ms 3'd1:200ms 3'd2:400ms 3'd3:600ms 3'd4:800ms 3'd5:1second 3'd6:2second 3'd7:4second

Reserved						
Register Address	Bit	Type	Label	Default		Description
0x1C ~0x1E	7:0	R	N/A	8'h00	8'h00	Reserved

Checksum Control Register						
Register Address	Bit	Type	Label	Default		Description
0x1F	7:3	R	N/A	5'h00	8'h00	Reserved
	2	RW	pwm_dc_det_en	1'b0		1'b0: Disable the DC detection on PWM 1'b1: Enable the DC detection
	1	RW	pbq_checksum_en	1'b0		1'b0: Disable 1'b1: Check the PBQ coefficient part of memory (from 0x30 to 0x46)
	0	RW	mdrc_checksum_en	1'b0		1'b0: Disable 1'b1: Check the DRC coefficient part of memory (from 0x47 to 0x4C)

Input MUX Register						
Register Address	Bit	Type	Label	Default		Description
0x20	7:6	RW	ch_src_sel[1:0]	2'b00	8'h00	2'b00:I^2S left channel data for ch1, right channel data for ch2 2'b01:I^2S right channel data for ch1, left channel data for ch2 2'b10:1/2 * (right + left) for ch1 and ch2 2'b11:Data = 0;
	5:0	R	N/A	6'd0		

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Reserved					
Register Address	Bit	Type	Label	Default	Description
0x21	7:4	RW	N/A	4'h0	Reserved
	3:0	R	N/A	4'h0	Reserved

PWM Control Register					
Register Address	Bit	Type	Label	Default	Description
0x22	7:6	R	N/A	2'b00	Reserved
	5	RW	enter_all _shutdown	1'b1	1'b0:Exit all-channel shutdown (normal operation) 1'b1:Enter all-channel shutdown (hard mute, HIZ)
	4	RW	enter_all_standby	1'b1	1'b0:Exit all-channel standby 1'b1:Enter all-channel standby (hard mute, HIZ, sound off)
	3:2	R	N/A	2'b00	Reserved
	1	RW	pbtl_en	1'b0	1'b0: BTL mode 1'b1: PBTL mode, A->A/B, B->C/D
	0	RW	pwm_ternary _mode_en	1'b1	1'b0: BD MODE 1'b1:Ternary MODE

Fault Short Select Register					
Register Address	Bit	Type	Label	Default	Description
0x23	7	R	N/A	1'b0	Reserved
	6:4	RW	fault_clr_times_sel[2:0]	3'b001	3'b000: Fault detected 2 times, fault_lock active 3'b001: Fault detected 5 times, fault_lock active 3'b010: Fault detected 10 times, fault_lock active 3'b011: Fault detected 15 times, fault_lock active 3'b100: Fault detected 20 times, fault_lock active 3'b101: Fault detected 25 times, fault_lock active 3'b110: Fault detected 30 times, fault_lock active 3'b111: Fault detected infinte times, fault_lock active
	3:0	R	N/A	4'h0	Reserved

Reserved(0x24)					
Register Address	Bit	Type	Label	Default	Description
0x24	7:0	R	N/A	8'h00	Reserved

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Channel1 EQ Filter Control Register 1						
Register Address	Bit	Type	Label	Default		Description
0x25	7:6	R	N/A	2'b00	8'h00	Reserved
	5	RW	ch1_eq_en[5:0]	1'b0		Ch1 EQ5, 1'b0: Bypass, 1'b1: Enable
	4	RW		1'b0		Ch1 EQ4, 1'b0: Bypass, 1'b1: Enable
	3	RW		1'b0		Ch1 EQ3, 1'b0: Bypass, 1'b1: Enable
	2	RW		1'b0		Ch1 EQ2, 1'b0: Bypass, 1'b1: Enable
	1	RW		1'b0		Ch1 EQ1, 1'b0: Bypass, 1'b1: Enable
	0	RW		1'b0		Ch1 EQ0, 1'b0: Bypass, 1'b1: Enable

Channel1 EQ Filter Control Register 2						
Register Address	Bit	Type	Label	Default		Description
0x26	7	RW	ch1_eq_en[13:6]	1'b0	8'h00	Ch1 EQ13, 1'b0: Bypass, 1'b1: Enable
	6	RW		1'b0		Ch1 EQ12, 1'b0: Bypass, 1'b1: Enable
	5	RW		1'b0		Ch1 EQ11, 1'b0: Bypass, 1'b1: Enable
	4	RW		1'b0		Ch1 EQ10, 1'b0: Bypass, 1'b1: Enable
	3	RW		1'b0		Ch1 EQ9, 1'b0: Bypass, 1'b1: Enable
	2	RW		1'b0		Ch1 EQ8, 1'b0: Bypass, 1'b1: Enable
	1	RW		1'b0		Ch1 EQ7, 1'b0: Bypass, 1'b1: Enable
	0	RW		1'b0		Ch1 EQ6, 1'b0: Bypass, 1'b1: Enable

Channel2 EQ Filter Control Register 1						
Register Address	Bit	Type	Label	Default		Description
0x27	7:6	R	N/A	2'b00	8'h00	Reserved
	5	RW	ch2_eq_en[5:0]	1'b0		Ch2 EQ5, 1'b0: Bypass, 1'b1: Enable
	4	RW		1'b0		Ch2 EQ4, 1'b0: Bypass, 1'b1: Enable
	3	RW		1'b0		Ch2 EQ3, 1'b0: Bypass, 1'b1: Enable
	2	RW		1'b0		Ch2 EQ2, 1'b0: Bypass, 1'b1: Enable
	1	RW		1'b0		Ch2 EQ1, 1'b0: Bypass, 1'b1: Enable
	0	RW		1'b0		Ch2 EQ0, 1'b0: Bypass, 1'b1: Enable

Channel2 EQ Filter Control Register 2						
Register Address	Bit	Type	Label	Default		Description
0x28	7	RW	ch2_eq_en[13:6]	1'b0	8'h00	Ch2 EQ13, 1'b0: Bypass, 1'b1: Enable
	6	RW		1'b0		Ch2 EQ12, 1'b0: Bypass, 1'b1: Enable
	5	RW		1'b0		Ch2 EQ11, 1'b0: Bypass, 1'b1: Enable
	4	RW		1'b0		Ch2 EQ10, 1'b0: Bypass, 1'b1: Enable
	3	RW		1'b0		Ch2 EQ9, 1'b0: Bypass, 1'b1: Enable
	2	RW		1'b0		Ch2 EQ8, 1'b0: Bypass, 1'b1: Enable
	1	RW		1'b0		Ch2 EQ7, 1'b0: Bypass, 1'b1: Enable
	0	RW		1'b0		Ch2 EQ6, 1'b0: Bypass, 1'b1: Enable

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SPEQ Filter Control Register1						
Register Address	Bit	Type	Label	Default		Description
0x29	7:6	RW	N/A	2'b00	8'h00	Reserved
	5:4	RW	N/A	2'b00		Reserved
	3:2	RW	N/A	2'b00		Reserved
	1:0	RW	N/A	2'b00		Reserved

SPEQ Filter Control Register2						
Register Address	Bit	Type	Label	Default		Description
0x2A	7:6	RW	bq13_ctrl[1:0]	2'b00	8'h00	2'b00: bq13 configured as EQ13 2'b01: bq13 configured as SPEQ3 2'b10: bq13 configured as SPEQ3 Limit 2'b11: reserved
	5:4	RW	bq12_ctrl[1:0]	2'b00		2'b00: bq12 configured as EQ12 2'b01: bq12 configured as SPEQ2 2'b10: bq12 configured as SPEQ2 Limit 2'b11: reserved
	3:2	RW	bq11_ctrl[1:0]	2'b00		2'b00: bq11 configured as EQ11 2'b01: bq11 configured as SPEQ1 2'b10: bq11 configured as SPEQ1 Limit 2'b11:Reserved
	1:0	RW	bq10_ctrl[1:0]	2'b00		2'b00: bq10 configured as EQ10 2'b01: bq10 configured as SPEQ0 2'b10: bq10 configured as SPEQ0 Limit 2'b11:Reserved

SPEQ Filter Control Register3						
Register Address	Bit	Type	Label	Default		Description
0x2B	7:1	R	N/A	7'd0	8'h00	Reserved
	0	RW	speq_det_method	1'b0		1'b0: Envelope 1'b1: RMS

Reserved(0x2C~2F)						
Register Address	Bit	Type	Label	Default		Description
0x2C ~0x2F	7:0	R	N/A	8'h00	8'h00	Reserved

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BQn_ADDR	Register Name
0x30	BQ0
0x31	BQ1
0x32	BQ2
0x33	BQ3
0x34	BQ4
0x35	BQ5
0x37	BQ6
0x38	BQ7
0x39	BQ8
0x3A	BQ9
0x3B	BQ10
0x3C	BQ11
0x3D	BQ12
0x3E	BQ13

BQn						
Register Address	Bit	Type	Label	Default		Description
BQn _ADDR	159 : 128	RW	bqn_a2[31:0]	0x0000 _0000		BQ coefficient, [31:29] is reserved
	127 : 96	RW	bqn_a1[31:0]	0x0000 _0000		BQ coefficient, [31:29] is reserved
	95: 64	RW	bqn_b2[31:0]	0x0000 _0000		BQ coefficient, [31:29] is reserved
	63: 32	RW	bqn_b1[31:0]	0x0000 _0000		BQ coefficient, [31:29] is reserved
	31: 0	RW	bqn_b0[31:0]	0x0080 _0000		BQ coefficient, [31:29] is reserved

Prescaler						
Register Address	Bit	Type	Label	Default		Description
0x36	31: 0	RW	prescaler[31:0]	0x0800 _0000		EQ prescaler. [31:29] is reserved. [28] is 1'b0, only positive. 0x0000_0000(-inf)~0x0800_0000(x1, 0dB)~0x0FFF_FFFF(x2, +6dB)

Reserved(0x3F~42)						
Register Address	Bit	Type	Label	Default		Description
0x3F ~0x42	7:0	R	N/A	8'h00		Reserved

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COEF_SPEQn_ADDR	Register Name
0x43	COEF_SPEQ0
0x44	COEF_SPEQ1
0x45	COEF_SPEQ2
0x46	COEF_SPEQ3

COEF_SPEQn						
Register Address	Bit	Type	Label	Default		Description
COEF_SPEQn_ADDR	95:64	RW	speqn_coef2 [31:0]	0x0040_0000		SPEQn coefficient 2, [31:29] is reserved
	63:32	RW	speqn_coef1 [31:0]	0x0080_0000		SPEQn coefficient 1, [31:29] is reserved
	31:0	RW	speqn_th[31:0]	0x0004_0000		SPEQn threshold, [31:29] is reserved

xDRCn_BQ	Register Name
0x47	LDRC0
0x48	LDRC1
0x49	MDRC0
0x4A	MDRC1
0x4B	HDRC0
0x4C	HDRC1

xDRCn						
Register Address	Bit	Type	Label	Default		Description
xDRCn_BQ	159:128	RW	xdrcn_bq0_a2 [31:0]	0x0000_0000		BQ coefficient, [31:29] is reserved
	127:96	RW	xdrcn_bq0_a1 [31:0]	0x0000_0000		BQ coefficient, [31:29] is reserved
	95:64	RW	xdrcn_bq0_b2 [31:0]	0x0000_0000		BQ coefficient, [31:29] is reserved
	63:32	RW	xdrcn_bq0_b1 [31:0]	0x000 0_0000		BQ coefficient, [31:29] is reserved
	31:0	RW	xdrcn_bq0_b0 [31:0]	0x0080_0000		BQ coefficient, [31:29] is reserved

Channel 1&2 Loudness					
Register Address	Bit	Type	Label	Default	Description
0x4D	95:64	RW	ld3_gain[31:0]	0x0800_0000	Loudness gain of BQ3, [31:29] is reserved. [28] is 1'b0, only positive. 0x0000_0000(-inf)~0x0800_0000(x1, 0dB)~0x0FFF_FFFF(x2, +6dB)
	63:32	RW	ld2_gain[31:0]	0x0800_0000	Loudness gain of BQ2, [31:29] is reserved. [28] is 1'b0, only positive. 0x0000_0000(-inf)~0x0800_0000(x1, 0dB)~0x0FFF_FFFF(x2, +6dB)
	31:0	RW	ld1_gain[31:0]	0x0800_0000	Loudness gain of BQ1, [31:29] is reserved. [28] is 1'b0, only positive. 0x0000_0000(-inf)~0x0800_0000(x1, 0dB)~0x0FFF_FFFF(x2, +6dB)

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ldrc_envlp_tc_up						
Register Address	Bit	Type	Label	Default		Description
0x4E	23	R	N/A	1'd0	24'h01 _FC05	Reserved
	22:0	RW	ldrc_envlp_tc_up [22:0]	23'h01 _FC05		The attack coefficient of DRC signal level envelop detection

ldrc_envlp_tc_dn						
Register Address	Bit	Type	Label	Default		Description
0x4F	23	R	N/A	1'd0	24'h7F _E900	Reserved
	22:0	RW	ldrc_envlp_tc_dn [22:0]	23'h7F _E900		The release coefficient of DRC signal level envelop detection

mdrc_envlp_tc_up						
Register Address	Bit	Type	Label	Default		Description
0x50	23	R	N/A	1'd0	24'h01 _FC05	Reserved
	22:0	RW	mdrc_envlp_tc_up[22:0]	23'h01 _FC05		The attack coefficient of DRC signal level envelop detection

mdrc_envlp_tc_dn						
Register Address	Bit	Type	Label	Default		Description
0x51	23	R	N/A	1'd0	24'h7F _9E9F	Reserved
	22:0	RW	mdrc_envlp_tc_dn[22:0]	23'h7F _9E9F		The release coefficient of DRC signal level envelop detection

hdrc_envlp_tc_up						
Register Address	Bit	Type	Label	Default		Description
0x52	23	R	N/A	1'd0	24'h01 _FC05	Reserved
	22:0	RW	hdrc_envlp_tc_up [22:0]	23'h01 _FC05		The attack coefficient of DRC signal level envelop detection

hdrc_envlp_tc_dn						
Register Address	Bit	Type	Label	Default		Description
0x53	23	R	N/A	1'd0	24'h7D _5C65	Reserved
	22:0	RW	hdrc_envlp_tc_dn [22:0]	23'h7D _5C65		The release coefficient of DRC signal level envelop detection

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PWM MUX Register						
Register Address	Bit	Type	Label	Default		Description
0x54	31:21	R	N/A	11'd0	32'h0	Reserved
	20	RW	pwm_connection_test[4]	1'b0		1'b0: pwm connection test disable 1'b1: pwm_connection test enable
	19	RW	pwm_connection_test[3]	1'b0		1'b0: pwm_out_D= 0 1'b1: pwm_out_D= 1
	18	RW	pwm_connection_test[2]	1'b0		1'b0: pwm_out_C= 0 1'b1: pwm_out_C= 1
	17	RW	pwm_connection_test[1]	1'b0		1'b0:pwm_out_B = 0 1'b1: pwm_out_B = 1
	16	RW	pwm_connection_test[0]	1'b0		1'b0: Pwm_out_A = 0 1'b1: Control pwm_Out_A in case of pwm_conection enable, used for testing analog connection.
	15:0	R	N/A	16'd0		Reserved

PWM Outflip Register						
Register Address	Bit	Type	Label	Default		Description
0x55	31	R	N/A	1'b0	32'h4000_3210	Reserved
	30:24	RW	pwm_dval_ramp_point[6:0]	7'h40		Start point to decrease the PWM compensation pulse
	23:22	R	N/A	2'b00		Reserved
	21	RW	pwm_clip_mode	1'b0		1'b0: Trunck to 0 1'b1: Clip to pwm_mod_limt[2:0]
	20	RW	pwm_ad_mode_en	1'b0		1'b0: Tri-Mode 1'b1: Binary Mode
	19:17	R	N/A	3'b0		Reserved
	16	RW	pwm_outflip_reg[12]	1'b0		1'b0: pwm_outflip[12] disable 1'b1: pwm outflip[12] enable
	15	R	N/A	1'b0		Reserved
	14:12	RW	pwm_outflip_reg[11:9]	3'b011		3'b000: pwm_outflip[11:9]: pwm_outD = side1_ p 3'b001: pwm_outflip[11:9]: pwm_outD = side1_n 3'b010: pwm_outflip[11:9]: pwm_outD = side2_p 3'b011: pwm_outflip[11:9]: pwm_outD = side2_n Others: Reserved
	11	R	N/A	1'b0		Reserved
	10:8	RW	pwm_outflip_reg[8:6]	3'b010		3'b000: pwm_outflip[7:6]: pwm_outC = side1_p 3'b001: pwm_outflip[7:6]: pwm_outC = side1_n 3'b010: pwm_outflip[7:6]: pwm_outC =

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						side2_p 3'b011: pwm_outflip[7:6]: pwm_outC = side2_n Others: Reserved
	7	R	N/A	1'b0		Reserved
	6:4	RW	pwm_outflip_reg [5:3]	3'b001		3'b000: pwm_outflip[5:3]: pwm_outB = side1_p 3'b001: pwm_outflip[5:3]: pwm_outB = side1_n 3'b010: pwm_outflip[5:3]: pwm_outB = side2_p 3'b011: pwm_outflip[5:3]: pwm_outB = side2_n Others: Reserved
	3	R	N/A	1'b0		Reserved
	2:0	RW	pwm_outflip_reg [2:0]	3'b000		3'b000: pwm_outflip[2:0]: pwm_outA = side1_p 3'b001: pwm_outflip[2:0]: pwm_outA = side1_n 3'b010: pwm_outflip[2:0]: pwm_outA = side2_p 3'b011: pwm_outflip[2:0]: pwm_outA = side2_n Others: Reserved

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PWM Control Register						
Register Address	Bit	Type	Label	Default		Description
0x56	31:28	R	N/A	4'h0	32'h0000_002F	Reserved
	27	RW	pwm_ns_order	1'b0		1'b0: pwm_ns_order, third order 1'b1: pwm_ns_order, fourth order
	26	RW	pwm_ns_bf_clr	1'b0		1'b0: pwm_ns_bf_clr 1'b1: pwm_ns_bf_clr, clear noise shaper sate counter
	25	RW	pwm_roundup	1'b0		1'b0: pwm_roundup, quantize to 9 or 10 bits, truncate 1'b1: pwm_roundup, quantize to 9 or 10 bits, roundup
	24	RW	pwm_direct_fs	1'b0		1'b0: pwm_direct_fs 1'b1: pwm_direct_fs, full 512 segments when full scale
	23	RW	pwm_dither_clr	1'b0		1'b0: pwm_dither_clr 1'b1: pwm_dither_clr, clear dither module generate a triangular
	22	RW	pwm_dither_en	1'b0		1'b0: pwm_dither_en, disable dither 1'b1: pwm_dither_en, enable dither
	21	RW	pwm_dither_range	1'b0		1'b0: pwm_dither_range, -3 to 3 1'b1: pwm_dither_range, -1 to 1
	20:16	RW	pwm_dither_pos[4:0]	5'd0		5'd0: Shift the dither[23:0] to right 0 bit, and complementary "0" 5'd1: Shift to right 0 bit 5'd2: Shift to right 0 bit 5'd3: Shift to right 1 bit 5'd4: Shift to right 2 bit 5'd5: Shift to right 3 bit 5'dx: pwm_dither_pos[4:0], shift the dither to where the lsb of the quantizer will be. (shift to right (x-2) bits) 5'd18: Shift to right 16 bit 5'd19: Shift to right 17 bit Others: Shift 0 bit
	15:8	RW	pwm_cnvt_dstep[5:0]	8'h00		pwm_cnvt_dstep[5:0], differential step value
	7:0	RW	pwm_cnvt_dvalue[5:0]	8'h2F		pwm_cnvt_dvalue [5:0], differential value

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PM_COEF						
Register Address	Bit	Type	Label	Default		Description
0x57	47	RW	N/A	1'b0	0x000800_7FF800	Reserved
	46:24	RW	pm_coef_up [22:0]	23'h000800		Power meter envelop detection attack coefficient
	23	RW	N/A	1'b0		Reserved
	22:0	RW	pm_coef_dn [22:0]	23'h7FF800		Power meter envelop detection release coefficient

Power Meter Control rb1						
Register Address	Bit	Type	Label	Default		Description
0x58	23:20	RW	N/A	4'h0	24'h00_0000	Reserved
	19	RW	pm_det_method	1'b0		1'b0: Envelope 1'b1: rms
	18:17	RW	pm_source[1:0]	2'b00		00: (L+R)/2, 01: Left channel, 10: Right Channel, 11:Reserved
	16	RW	pm_loc	1'b0		1'b0: After volume 1'b1:Before volume
	15:8	R	pm_lvl_db[9:2]	8'd0		8'h00 ~ 8'hFF: -127.5dB~0dB, Step is 0.5dB
	7:2	R	N/A	6'd0		Reserved
	1:0	R	pm_lvl_db[1:0]	2'd0		10'h000 ~ 10'h3FC: -127.875dB~0dB, Step is 0.125dB

Power Meter Control rb2						
Register Address	Bit	Type	Label	Default		Description
0x59	23	R	N/A	1'b0	24'h000_000	Reserved
	22:0	R	pm_lvl_linear [22:0]	23'd0		23'h000000 ~ 23'h7FFFFF: 2^(-23)~1

PBQ Checksum						
Register Address	Bit	Type	Label	Default		Description
0x5A	31:29	R	N/A	3'b000	32'h0800_0000	Reserved
	28:0	RW	pbq_checksum_key[28:0]	29'h0800_0000		The reference value of PBQ memory checksum result

MDRC Checksum						
Register Address	Bit	Type	Label	Default		Description
0x5B	31:29	R	N/A	3'b000	32'h0000_0000	Reserved
	28:0	RW	mdrc_checksum_key[28:0]	29'h0		The reference value of DRC memory checksum result

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Reserved						
Register Address	Bit	Type	Label	Default		Description
0x5C	7:0	R	N/A	8'h00	8'h00	Reserved

SPEQ_ATK_REL_TC_1						
Register Address	Bit	Type	Label	Default		Description
0x5D	95	R	N/A	1'b0	96'h 000800 _000800 _000800 _000800	Reserved
	94: 72	RW	speq_atk_tc3 [22:0]	23'h0		Attack time control
	71	R	N/A	1'b0		Reserved
	70: 48	RW	speq_atk_tc2 [22:0]	23'h0		Attack time control
	47	R	N/A	1'b0		Reserved
	46: 24	RW	speq_atk_tc1 [22:0]	23'h0		Attack time control
	23	R	N/A	1'b0		Reserved
	22:0	RW	speq_atk_tc0 [22:0]	23'h0		Attack time control

SPEQ_ATK_REL_TC_2						
Register Address	Bit	Type	Label	Default		Description
0x5E	95	R	N/A	1'b0	96'h 7FF800 _7FF800 _7FF800 _7FF800	Reserved
	94: 72	RW	speq_rel_tc3 [22:0]	23'h0		Release time control
	71	R	N/A	1'b0		Reserved
	70: 48	RW	speq_rel_tc2 [22:0]	23'h0		Release time control
	47	R	N/A	1'b0		Reserved
	46: 24	RW	speq_rel_tc1 [22:0]	23'h0		Release time control
	23	R	N/A	1'b0		Reserved
	22:0	RW	speq_rel_tc0 [22:0]	23'h0		Release time control

ch12_mixer_gain						
Register Address	Bit	Type	Label	Default		Description
0x5F	31	R	N/A	1'b0	32'h2700 _0027	Reserved
	30	RW	ch1_mixer_fch1 _polarity	1'b0		1'b0: Plus 1'b1: Minus
	29: 24	RW	ch1_mixer_fch1 _gain[5:0]	6'h27		Refer to Table 3, mixer gain table
	23	R	N/A	1'b0		Reserved
	22	RW	ch1_mixer_fch2 _polarity	1'b0		1'b0: Plus 1'b1: Minus
	21:	RW	ch1_mixer_fch2	6'h00		Refer to Table 3, mixer gain table

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	16		_gain[5:0]			
	15	R	N/A	1'b0		Reserved
	14	RW	ch2_mixer_fch1 _polarity	1'b0		1'b0: Plus 1'b1: Minus
	13:8	RW	ch2_mixer_fch1 _gain[5:0]	6'h00		Refer to Table 3, mixer gain table
	7	R	N/A	1'b0		Reserved
	6	RW	ch2_mixer_fch2 _polarity	1'b0		1'b0: Plus 1'b1: Minus
	5:0	RW	ch2_mixer_fch2_ gain[5:0]	6'h27		Refer to Table 3, mixer gain table

DRC Control						
Register Address	Bit	Type	Label	Default		Description
0x60	31: 25	R	N/A	7'd0	32'h0100 _0000	Reserved
	24	RW	drc_det_method	1'b1		1'b0: Envelope 1'b1: rms
	23: 9	R	N/A	15'd0		Reserved
	8	RW	envlp_mode	1'b0		Envelope detection method selection. 0: Classic method, 1: New method.
	7:4	R	N/A	4'd0		Reserved
	3	RW	ldrc_lmt_en	1'b0		0:Disable 1: Enable
	2	RW	mdrc_lmt_en	1'b0		0:Disable 1: Enable
	1	RW	hdrc_lmt_en	1'b0		0:Disable 1: Enable
	0	RW	pdrc_lmt_en	1'b0		0:Disable 1: Enable

xDRC_LMT_CFG1_ADDR	**xDRC__LMT_CFG**	**Default**
0x61	LDRC_LMT_CFG1	24'h3C9_30C
0x64	MDRC_LMT_CFG1	24'h3C5_30C
0x67	HDRC_LMT_CFG1	24'h3C9_30C

xdrc_lmt_cfg1						
Register Address	Bit	Type	Label	Default		Description
Xdrc _LMT _CFG1 _ADDR	23: 22	R	N/A	2'b00		Reserved
	21: 12	RW	xdrc_makeup [9:0]	see above table		Gain control of DRC band. 10'h000(-121.5dB)~10'h3FC(6dB), step is 0.125dB 10'h3FC = 6dB, 10'h3CC = 0dB
	11: 10	R	N/A	2'b00		Reserved
	9:0	RW	xdrc_lmt_thr[9:0]	10'h30C		DRC limit threshold, 10'h000(-97.5dB)~10'h3FC(30dB), step is 0.125dB 10'h30C = 0dB, 10'h3FC = 30dB

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xdrc_lmt_cfg1						
Register Address	Bit	Type	Label	Default		Description
0x6A	23:10	R	N/A	14'd0	24'h000_30C	Reserved
	9:0	RW	pdrc_lmt_thr[9:0]	10'h30C		DRC limit threshold, 10'h000(-97.5dB)~10'h3FC(30dB), step is 0.125dB 10'h30C = 0dB, 10'h3FC = 30dB

xDRC_LMT_CFG_ADDR	xDRC__LMT_CFG	Default
0x62	LDRC_LMT_CFG2	24'h7F_FF51
0x65	MDRC_LMT_CFG2	24'h7F_FF51
0x68	HDRC_LMT_CFG2	24'h7F_FF51
0x6B	PDRC_LMT_CFG2	24'h7F_FF51

xdrc_lmt_cfg2						
Register Address	Bit	Type	Label	Default		Description
xDRC_LMT_CFG2_ADDR	23	R	N/A	1'b0	See above	Reserved
	22:0	RW	xdrc_lmt_atk_tc [22:0]	23'h7F_FF51		Release Time Control

xDRC_LMT_CFG_ADDR	xDRC__LMT_CFG	Default
0x63	LDRC_LMT_CFG3	24'h7F_55C6
0x66	MDRC_LMT_CFG3	24'h7F_1D3B
0x69	HDRC_LMT_CFG3	24'h0F_F016
0x6C	PDRC_LMT_CFG3	24'h7A_C6B8

xdrc_lmt_cfg3						
Register Address	Bit	Type	Label	Default		Description
xDRC_LMT_CFG3_ADDR	23	R	N/A	1'b0	See above	Reserved
	22:0	RW	xdrc_lmt_rel_tc [22:0]	See above		Attack time control

drc_envlp_tc_up						
Register Address	Bit	Type	Label	Default		Description
0x6D	23	R	N/A	1'd0	24'h01_FC05	Reserved
	22:0	RW	drc_envlp_tc_up [22:0]	23'h01_FC05		The attack coefficient of DRC signal level envelop detection

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drc_envlp_tc_dn						
Register Address	Bit	Type	Label	Default		Description
0x6E	23	R	N/A	1'd0	24'h7F _BBCD	Reserved
	22:0	RW	drc_envlp_tc_dn [22:0]	23'h7F _BBCD		The release coefficient of DRC signal level envelop detection

Reserved						
Register Address	Bit	Type	Label	Default		Description
0x6F	7:0	R	N/A	8'h00		Reserved

BIST Control						
Register Address	Bit	Type	Label	Default		Description
0x70	7	R	N/A	1'b0	8'h00	Reserved
	6	RW	bist_mode	1'b0		1'b0: 7 bist pattern and compare read results. 1'b1:1 bist pattern and do not compare
	5	RW	bist_go_reg	1'b0		1'b0: Disable 1'b1:I^{2}C write "1" to start do bist
	4	RW	bist_ram1_skip	1'b0		Bist Skips RAM1 1'b0: Normal 1'b1: Skip
	3	R	N/A	1'b0		Reserved
	2	RW	bist_ram3_skip	1'b0		Bist skips RAM3 1'b0: Normal 1'b1: Skip
	1	RW	bist_ram4_skip	1'b0		Bist skips RAM4 1'b0: Normal 1'b1:Skip
	0	R	N/A	1'b0		Reserved

PLL Status						
Register Address	Bit	Type	Label	Default		Description
0x71	31	RW	sw_refclk_sel_en	1'b0	32'h0063 _002D	1'b0:sw_refclk_sel_disable 1'b1:sw_refclk_sel_enbale
	30	RW	sw_refclk_sel	1'b0		1'b0:sw_refclk_sel : select OSC_CLK 1'b1:sw_refclk_sel : select SCLK
	29	RW	pllc_pllclksel	1'b0		1'b0:pllc_pllclksel, pll refer_clk select OSC 1'b1:pllc_pllclksel, pll refer_clk select SCLK
	28	RW	pllc_pll_prog	1'b0		1'b0:pllc_pll_prog, they would be auto controlled. 1'b1:pllc_pll_prog, all pll reference value would use register control : 1) refdiv 2) fbdiv 3) rz_pll 4) cp_pll 5) vco_i_pll 6) d2a_ref_sel_osc
	27:20	RW	pllc_refdiv_pll [7:0]	8'h63		PLL referrence divider, 1~255

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	19	R	N/A	1'b0		Reserved
	18:8	RW	pllc_fbdiv_pll [10:0]	11'd0		PLL feedback divider, 1~1023
	7	R	N/A	1'b0		Reserved
	6:4	RW	pllc_cp_pll[2:0]	3'b010		PLL charge pump setting
	3:2	RW	pllc_rz_pll[1:0]	2'b11		PLL resistor setting
	1:0	RW	pllc_vco_i_pll [1:0]	2'b01		PLL vco setting

PLL Control Register						
Register Address	Bit	Type	Label	Default		Description
0x72	15:13	R	N/A	3'b000	16'h0000	Reserved
	12	RW	pll_enable_sel	1'b0		1'b0: Select auto control : hardware control 1'b1:pll_enable_sel, select register control : pll manual enable
	11	RW	pll_manual_en	1'b0		1'b0:PLL manual disable 1'b1:PLL manual enable
	10:9	R	N/A	2'b00		Reserved
	8	RW	brt_sel	1'b0		1'b0:48kHz (in case of pll_ref_clk = osc_clk) 1'b1:44.1kHz (in case of pll_ref_clk = osc_clk)
	7:1	R	N/A	7'd0		Reserved
	0	RW	pll_osc_force_en	1'b0		1'b0: PLL reference clock is SCLK, if no SCLK apply PLL will not start; 1'b1: When no SCLK, force PLL power up ,using OSC CLK as refercnce clock

SPK Sequence Bypass						
Register Address	Bit	Type	Label	Default		Description
0x73	7:2	R	N/A	6'd0	8'h00	Reserved
	1	RW	ch2_seq_bypass_1ms	1'b0		1'b0:Channel 2 SPK_STATE bypass disable 1'b1:Channel 2 SPK_STATE bypass (not wait 1ms)
	0	RW	ch1_seq_bypass_1ms	1'b0		1'b0:Channel 1 SPK_STATE bypass disable 1'b1:Channel 1 SPK_STATE bypass, (not wait 1ms)

Function Test Register						
Register Address	Bit	Type	Label	Default		Description
0x74	7	RW	ps_test_en_b	1'b1	8'h80	1'b0: Enter the Power Stage Test Mode 1'b1: Disalbed
	6	RW	ps_test_mod0	1'b0		Available when ps_test_en_b is low
	5	RW	ps_test_mod1	1'b0		Available when ps_test_en_b is low
	4	RW	i2s_loop_en	1'b0		I^2S rx loop back to i2s tx 1'b0: disable 1'b1: enable

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	3	R	N/A	1'b0		Reserved
	2:0	RW	func_test_cfg [2:0]	3'b000		3'b000: Normal mode 3'b010: Addr_sel = pwm_p_side1; Pwd_b = pwm_n_side1 3'b011: Addr_sel = pwm_p_side2; Pwd_b = pwm_n_side2 3'b101: Addr_sel = fault_oc; pwd_b = fault_otuv 3'b110: Addr_sel = fault_short; pwd_b = fault_clr Others: Reserved

Temp_ By_Reg Register						
Register Address	Bit	Type	Label	Default		Description
0x75	7:5	R	N/A	3'b000	8'h00	Reserved
	4	RW	Tmp_by_reg[4]	1'b0		1'b0: External data input test mode. 1'b1: register control test mode enable.
	3:0	RW	Tmp_by_reg[3:0]	4'h0		4'h0: Reset all flops test mode 4'h1: Scan test mode 4'h2:V_{OUT} test mode 4'h3: V_{IN} test mode 4'h6: Burn in test mode 4'hF: ATE test mode Others: Reserved

Protection System Control						
Register Address	Bit	Type	Label	Default		Description
0x76	7:5	R	N/A	3'b000	8'h1F	Reserved
	4	RW	poweron_short _protect_en	1'b1		1'b0:Disable 1'b1: Enable
	3	RW	short_protect_en	1'b1		1'b0: Disable 1'b1: Enable
	2	RW	otuv_protect_en	1'b1		1'b0: Disable 1'b1:Enable
	1	RW	oc_protect_en	1'b1		1'b0: Disable 1'b1: Enable
	0	RW	avdd_uv_protect _en	1'b1		1'b0: Disable 1'b1:Enable

I^2C Control Register						
Register Address	Bit	Type	Label	Default		Description
0x77	7:2	R	N/A	6'd0	8'h03	Reserved
	1	RW	i2c_dly_en	1'b1		1'b0: disable 1'b1: enable
	0	RW	i2c_sda_timeout _en	1'b1		1'b0: disable 1'b1: enable

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Reserved						
Register Address	Bit	Type	Label	Default		Description
0x78~79	7:0	R	N/A	8'h00		Reserved

Exit Over Current register						
Register Address	Bit	Type	Label	Default		Description
0x7A	7:0	RW	ocdet_dis_num [7:0]	8'h40	8'h40	8'd64: 64*4 clock cysles(384kHz) 8'dm: m*4 clock cycles(384kHz) 8'd3: 3*4 clock cycles (384kHz) 8'd2: 2*4 clock cycles (384kHz) 8'd1: 1*4 clock cycles (384kHz) 8'd0: 1*4 clock cycles (384kHz)

Oscillator Trim Control						
Register Address	Bit	Type	Label	Default		Description
0x7B	7:2	R	N/A	6'd0	8'h01	Reserved
	1	R	osc_trim_done	1'b0		1'b0:Osc trim is not done (Read Only) 1'b1:Osc_trim_done, the bit could write "0" clear 1. (read only)
	0	RW	factory_trim_dis	1'b1		1'b0:Select factory trim (Write a 0 to select factory trim; default is 1.) 1'b1:Facotry trim disable

Oscillator Trim Register1						
Register Address	Bit	Type	Label	Default		Description
0x7C	31:13	R	N/A	19'd0	32'h0000_1000	Reserved
	12:8	R	osc_trim_data [4:0]	5'h10		trim_data[4:0]
	7:3	R	N/A	5'd0		Reserved
	2	RW	osc_trim_go	1'b0		1'b0: Osc_trim_go is disabled. 1'b1: Write 1 to this bit, osc_trim will start.. Trim data would be efused to analog part.
	1	RW	d2a_osc_pwd_reg	1'b0		1'b0: d2a_osc_pwd disabled 1'b1: d2a_osc_pwd enable
	0	RW	d2a_post_trim_pwd	1'b0		1'b0: Not power down analog trim module 1'b1: Power down analog trim module

Oscillator Trim Register2						
Register Address	Bit	Type	Label	Default		Description
0x7D	31:22	R	N/A	10'd0	32'h000F_0F17	Reserved
	21	RW	trim_program_en	1'b0		1'b0: Program disable 1'b1: Program enable

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	20:16	RW	trim_program_data[4:0]	5'h0F		program_data, the data could be directed into OSC analog module part in case of program_enable.
	15:14	R	N/A	2'b00		Reserved
	13	RW	trim_efuse_data_en	1'b0		1'b0: trim_efuse_data disable 1'b1: trim_efuse_data enable
	12:8	RW	trim_efuse_data[4:0]	5'd0F		trim_efuse_data, the data could be efused to analog part in case of trim_efuse_enable.
	7	R	N/A	1'b0		Reserved
	6:1	RW	efuse_time[5:0]	6'd0B		6'd63: efuse_time:63ms 6'd62: efuse_time:63ms 6'd(m):efuse_time:(m+1)ms 6'd11:efuse_time:12ms 6'd(n): efuse_time:(n+1)ms 6'd2: efuse_time:3ms 6'd1: efuse_time:2ms 6'd0: efuse_time:1ms
	0	RW	trim_efuse_en	1'b1		1'b0: Trim effuse disable 1'b1: Trim effuse enable

Analog Ref_top Control						
Register Address	Bit	Type	Label	Default		Description
0x7E	31:12	R	N/A	20'd0	32'h0000_0200	Reserved
	11:10	RW	v1p2d_ctrl[1:0]	2'b00		V1p2d[1:0]
	9:8	RW	d2a_ref_ib_ctrl[1:0]	2'b10		d2a_ref_ib_ctrl[1:0]
	7:5	RW	d2a_ref_pf[2:0]	3'b000		d2a_ref_pf[2:0]
	4:3	RW	d2a_reg_avdd_ctrl[1:0]	2'b00		d2a_reg_avdd_ctrl[1:0]
	2	RW	d2a_ref_pwd	1'b0		da2_ref_pwd
	1	RW	d2a_reg_avdd_pwd	1'b0		d2a_reg_avdd_pwd
	0	RW	d2a_uv_detect_pwd	1'b0		d2a_uv_detect_pwd is disable

Reserved(0x7F)						
Register Address	Bit	Type	Label	Default		Description
0x7F	7:0	R	N/A	8'h00		Reserved

Dsp_3d_coef						
Register Address	Bit	Type	Label	Default		Description
0x80	23:0	RW	dsp_3d_coef[23:0]	0x400000		3D coefficient, linear gain. 2's complement, 0(-inf) ~ 0x7FFFFF(2), 0x800000(-2)~0xFFFFFF(near -0), 0x400000 =1, 0x7FFFFF = 2, 0xc00000 = -1.

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Dsp_3d_mix						
Register Address	Bit	Type	Label	Default		Description
0x81	23:0	RW	dsp_3d_mix [23:0]	0x400000		3D mix gain, linear gain. 2's complement, 0(-inf) ~ 0x7FFFFF(2), 0x800000(-2)~0xFFFFFF(near -0), 0x400000 =1, 0x7FFFFF = 2, 0xc00000 = -1.

Inter Private Register						
Register Address	Bit	Type	Label	Default		Description
0x82	31:8	R	N/A	24'd0	32'h0000_00F0	Reserved
	7	RW	refclk_stop_reg_en	1'b1		1'b0: sclk_stop disable , would not shown in 0x02 (bit[7]) 1'b1: sclk_stop enable, would show in 0x02(bit[7])
	6	RW	sclk_err_en	1'b1		1'b0: SCLK error disable 1'b1: SCLK error enable
	5	RW	lrclk_err_en	1'b1		1'b0: lr_clk_error disable 1'b1: lr_clk_error enable
	4	R	refclk_stop_err_en	1'b1		1'b0: sclk_stop will not be judged a clock error 1'b1: sclk stop will be judged a clock error
	3:1	R	N/A	3'b000		Reserved
	0	RW	spk_scdet_en	1'b0		1'b0: spk_scdet_en, enable All channel should be set Binary mode 1'b1: pwm_outA = pwm_outB = CH1_P_SIDE pwm_outC = pwm_outD = CH2_P_SIDE

Reserved						
Register Address	Bit	Type	Label	Default		Description
0x83	7:6	RW	pdrc_ftune[1:0]	2'b00	8'h00	Post DRC threshold fine tune, 0.125dB per step. 2'b00(0dB)~2'b11(0.375dB)
	5:4	RW	hdrc_ftune[1:0]	2'b00		High band DRC threshold fine tune, 0.125dB per step. 2'b00(0dB)~2'b11(0.375dB)
	3:2	RW	mdrc_ftune[1:0]	2'b00		Moddile band DRC threshold fine tune, 0.125dB per step. 2'b00(0dB)~2'b11(0.375dB)
	1:0	RW	Ldr c_ftune[1:0]	2'b00		Low band DRC threshold fine tune, 0.125dB per step. 2'b00(0dB)~2'b11(0.375dB)

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Fault Over Current Detect Gear Register						
Register Address	Bit	Type	Label	Default		Description
0x84	7:0	R	N/A	8'h00		Reserved

OC Detect Window Width						
Register Address	Bit	Type	Label	Default		Description
0x85	31:10	R	N/A	22'd0	32'h0000_0001	Reserved
	9	RW	ocfast_trig_en	1'b0		OC fast trigger
	8	RW	ocdet_mannual_sel	1'b0		ocdet_mannual_sel
	7:6	R	N/A	2'd0		Reserved
	5:0	RW	ocdet_wind_width[5:0]	6'h01		ocdet_wind_width

Fault Over Current Threshold						
Register Address	Bit	Type	Label	Default		Description
0x86	31:15	R	N/A	17'd0	32'h0000_0001	Reserved
	14:12	RW	filter_deglitch[2:0]	3'b000		Deglitch all the fault_OC signal pulse if its width is smaller than this configured cycle number
	11:9	R	N/A	3'b000		Reserved
	8:0	RW	ocdet_en_num[8:0]	9'h001		Threshold of total cycles that "fault_OC" be counted in large detect window. A counted number over the threshold will trigger an OC fault

DSP Limit Enable Threshold						
Register Address	Bit	Type	Label	Default		Description
0x87	7:0	R	N/A	8'h00		Reserved

DSP Limit Disable Threshold						
Register Address	Bit	Type	Label	Default		Description
0x88	7:0	R	N/A	8'h00		Reserved

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Register Address						
Register Address	Bit	Type	Label	Default		Description
0x89	7:4	R	N/A	8'h00	4'h0	Reserved
	3	R	pwm_ndc_err_ch1		1'b0	1'b1: Channel 1 has an n-side DC error; 1'b0: no such error;
	2	R	pwm_pdc_err_ch1		1'b0	1'b1: Channel 1 has an p-side DC error; 1'b0: no such error;
	1	R	pwm_ndc_err_ch2		1'b0	1'b1: Channel 2 has an n-side DC error; 1'b0: no such error;
	0	R	pwm_pdc_err_ch2		1'b0	1'b1: Channel 2 has an p-side DC error; 1'b0: no such error;

Register Address						
Register Address	Bit	Type	Label	Default		Description
0x8A	7:0	R	N/A	8'h00	8'h00	Reserved

DSP Control Register 3						
Register Address	Bit	Type	Label	Default		Description
0x8B	7:2	R	N/A	6'd0	8'h00	Reserved
	1	RW	3d_en	1'b0		3d enable: 1'b0:Disable 1'b1:Enable
	0	R	N/A	1'b0		Reserved

Device Address Enable Register						
Register Address	Register Name	Bit	Type	Label	Default	Description
0xF8	DEV_ADDR_ENA	31:0	RW		32'd0	Write F9 A5 A5 A5 in this register to enable updated device address (0xF9)

Device Address Update Register						
Register Address	Register Name	Bit	Type	Label	Default	Description
0xF9	DEV_ADDR_UPD	31:0	RW		32'h0000_0054	

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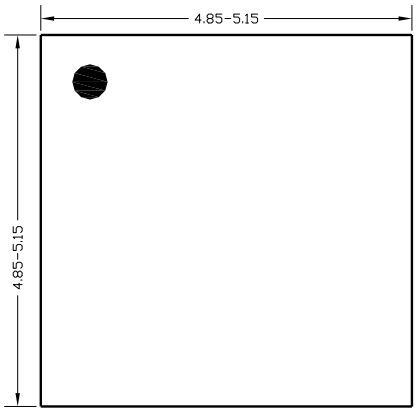
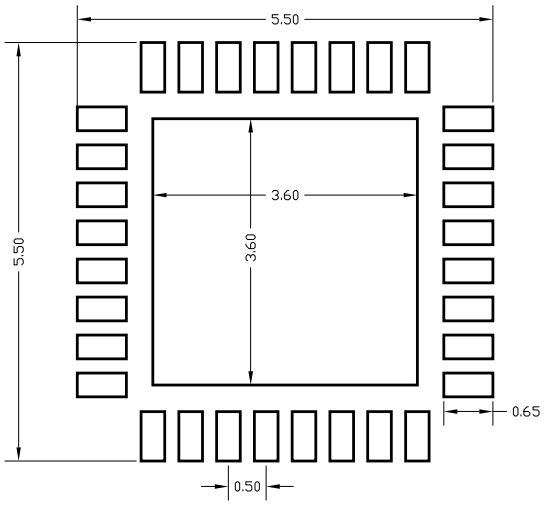
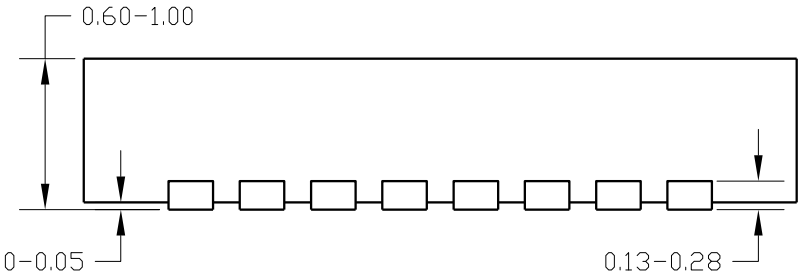
QFN5×5-32 Package Outline & PCB Layout



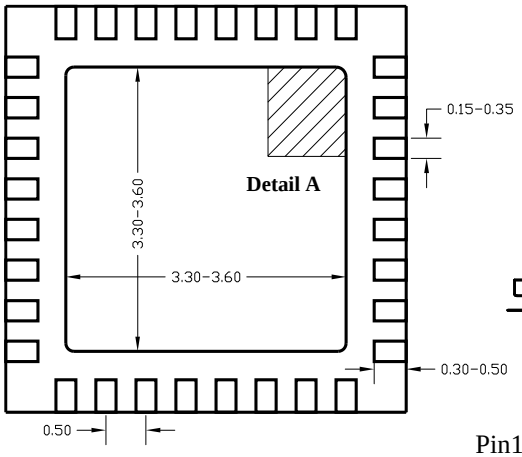
Top View

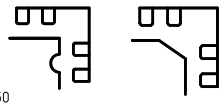


PCB Layout (Recommended)



Side View





Detail A
Pin1 identifier: two options

Bottom View

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

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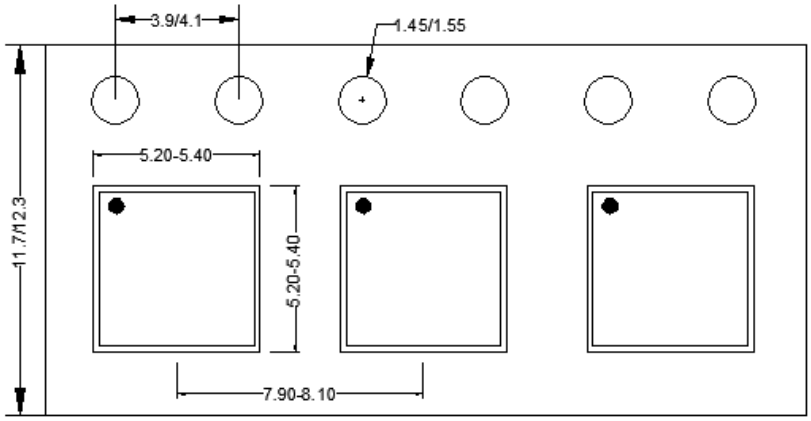
Taping & Reel Specification

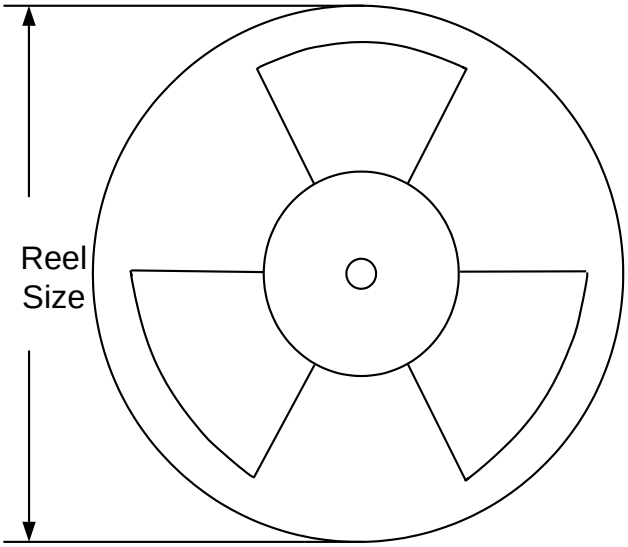
1. Taping orientation

QFN5×5



Feeding direction

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN5×5	12	8	13"	400	400	5000

3. Others: NA

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Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Sept.10, 2022	Revision 1.0	Production Release
Sept.10, 2021	Revision 0.9C	1. Update the max value of "Enable the I^2C Duration Time" from 12.0 to 0.1ms 2. Update the min value of "SCLK Frequency" from 2.048 to 1.024MHz
Mar.11, 2021	Revision 0.9B	1. Delete single filter in Feature 2. Delete the description of BD or Ternary mode support 3. Delete the Block in the description of DRC
Mar.20, 2020	Revision 0.9A	Update the Feature from "I^2C Serial Control Interface Operational without MCLK" to "3-wire I^2S Digital Audio Interface without MCLK"
Sept. 13, 2018	Revision 0.9	Initial Release

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