SY24106L

High Performance, High Fidelity Digital Audio-Power Amplifier

General Description

The SY24106L is a digital audio power amplifier for driving bridge-tied stereo speakers at up to 2×20W maximum output power. One serial data input allows processing of up to two discrete audio channels and seamless integration to most digital audio processors. The SY24106L is an I^2S slave device receiving all clocks from external sources.

The SY24106L has the essential audio signal processing functions like dynamic range control, loudness control and parametric equalization.

Ordering Information

SY24106 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY24106LQEC	QFN5×5-32	

Applications

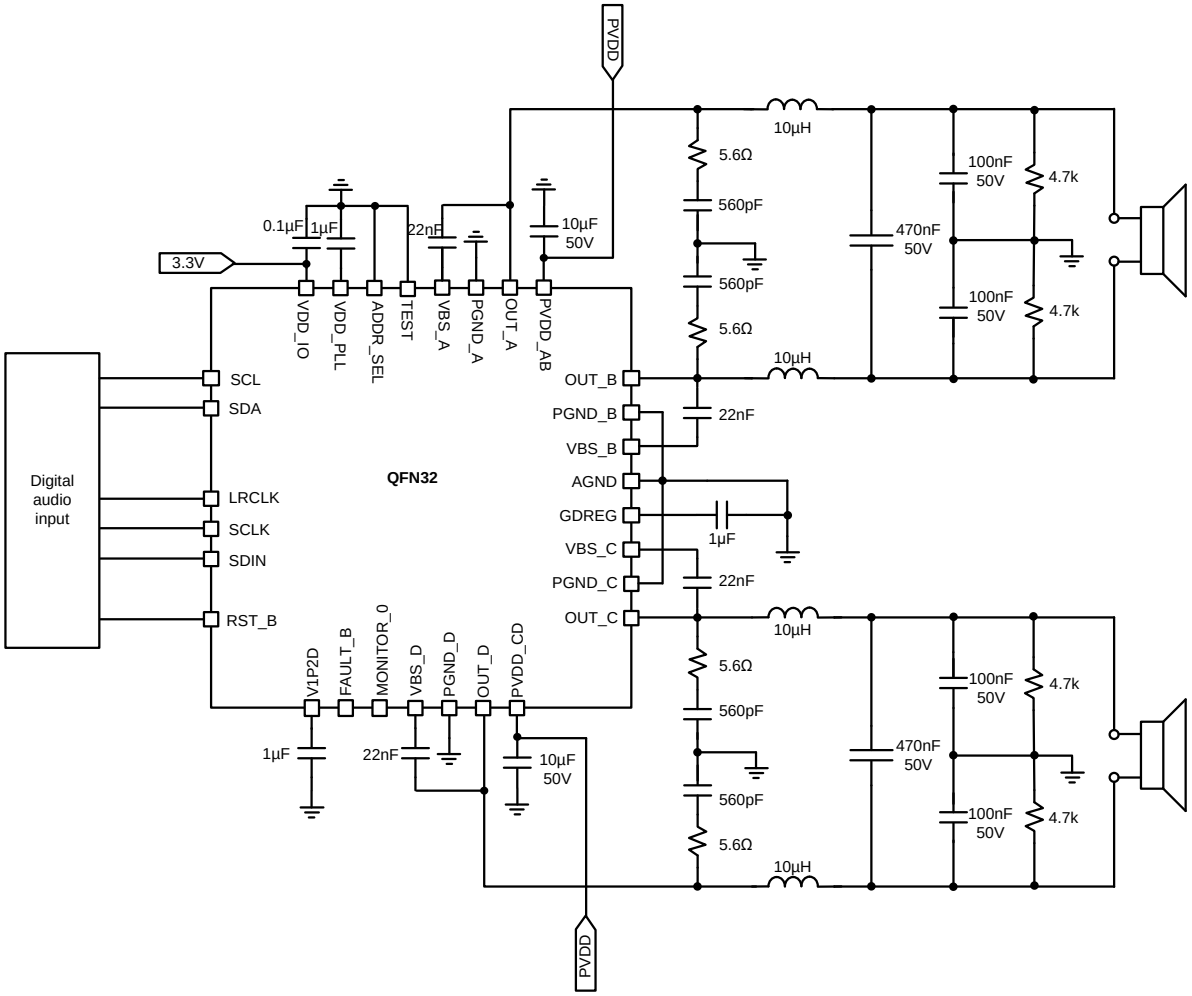
- LCD TV, LED TV or Monitor
- Digital Speaker, Bluetooth Speaker
- Sound Bar

Features

- 2×10W into 8Ω Loads from a 13.2V Supply
- 2×15W into 8Ω Loads from a 16V Supply
- 2.0 BTL Mode or PBTL Mode Support
- 4.5V to 16.5V PVDD Range
- 32kHz to 96kHz Sample Rate Support (LJ/RJ/I^2S)
- I^2C Address Selection Pin
- Independent Channel Volume Controls with 48dB to Mute
- SDATA Generator (I^2S Output)
- Two DC Blocking Filters
- 14 PEQs or 10 PEQs + 4 SPEQs Each Channel for Speaker Protection and Speaker Compensation
- 3 Bands Dynamic Range Control Plus a Post Dynamic Range Control
- Loudness Control
- Power Level Meter
- 3-wire I^2S Digital Audio Interface without MCLK
- Thermal, Over Current, Short Circuit Protection and EQ/DRC Coefficients Checksum
- Support Automatic Audio Sample Rate Detection
- SY24106LQEC Surface Mount, QFN 32Pin, 5mm×5mm

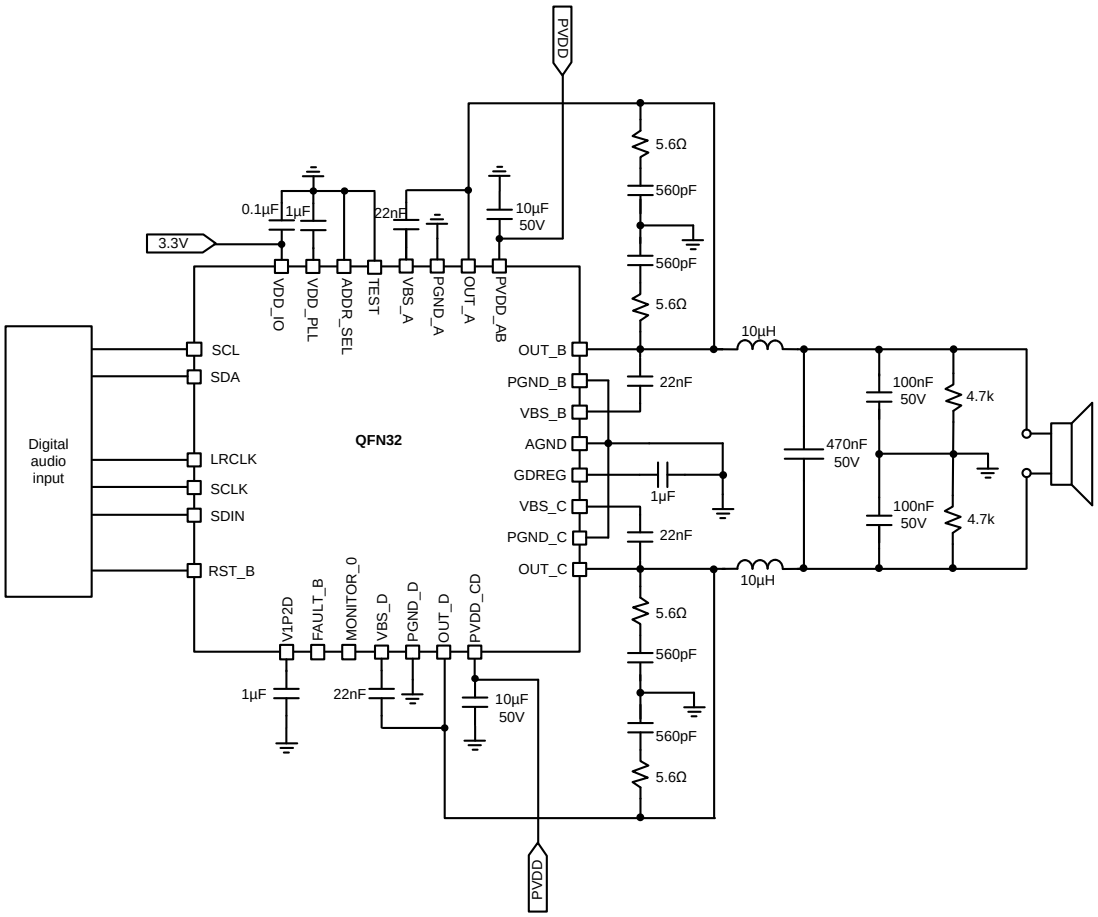
Typical Application

BTL



(a) Stereo Class-D Amplifier with BTL Output

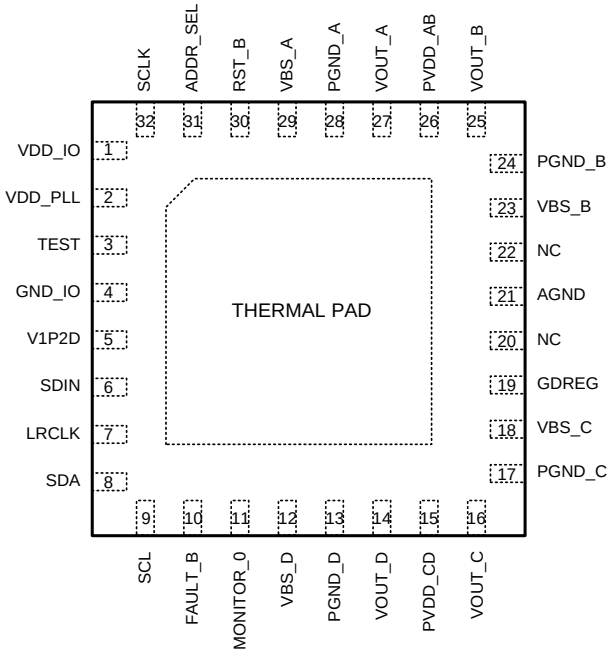
PBTL



(b) Mono Class-D Amplifier with PBTL Output

Figure1. Typical Application Circuit

Pinout (top view)



(QFN5×5-32)

Top mark: **BRC** ***xyz*** (Device code: **BRC**, ***x=year code, y=week code, z= lot number code*****)**

Name	No.	Type(1)	Termination(2)	Description
VOUT_A	27	O		Half-bridge A output.
VOUT_B	25	O		Half-bridge B output.
VOUT_C	16	O		Half-bridge C output.
VOUT_D	14	O		Half-bridge D output.
PVDD_AB	26	P		Power supply for half-bridge A and B.
PVDD_CD	15	P		Power supply for half-bridge C and D.
VBS_A	29	P		High side supply offset voltage for half-bridge A.
VBS_B	23	P		High side supply offset voltage for half-bridge B.
VBS_C	18	P		High side supply offset voltage for half-bridge C.
VBS_D	12	P		High side supply offset voltage for half-bridge D.
GDREG	19	P		Gate driver internal regulator output. This pin must not be used for driving the external devices.
GND_IO	4	P		Analog 3.3V power supply ground.
NC	20, 22			Not connected.
VDD_IO	1	P		Power supply for digital interface I/O, 3.3V.
ADDR_SEL	31	DI	Pull down	I^2C address selection pin.
V1P2D	5	P		Internal regulated 1.2V digital power supply for digital core. This pin must not be used for powering the external devices.
VDD_PLL	2	P		Internal regulated 1.2V digital power supply for PLL. This pin must not be used for powering the external devices.
FAULT_B	10	DI	Pull up	This pin low means turning off the PWM signal path.
LRCLK	7	DI	Pull down	Serial audio data left or right clock input.
SCLK	32	DI	Pull down	Serial audio data bit clock input.

SDIN	6	DI	Pull down	Serial audio data input.
SDA	8	DIO	Pull up	I^2C serial control data input or output.
SCL	9	DI	Pull up	I^2C serial clock input.
MONITOR_0	11	DO		Monitoring the signal out from the processor block / I^2S output.
RST_B	30	DI	Pull-up	Logic low to this pin to reset the system. When reset pulls low, DAP will restore to its default conditions, and place the PWM in the hard mute state.
TEST	3	DI	Pull down	Test pin.
AGND	21	P		Power stage analog ground.
PGND_A	28	P		Power ground for half-bridge A.
PGND_B	24	P		Power ground for half-bridge B.
PGND_C	17	P		Power ground for half-bridge C.
PGND_D	13	P		Power ground for half-bridge D.

Note: (1) Type: A =analog; D =digital; P =power/ground/decoupling; I =input; O =output; IO=inout
(2) All pull-ups and pull-downs are weak.

Function Block

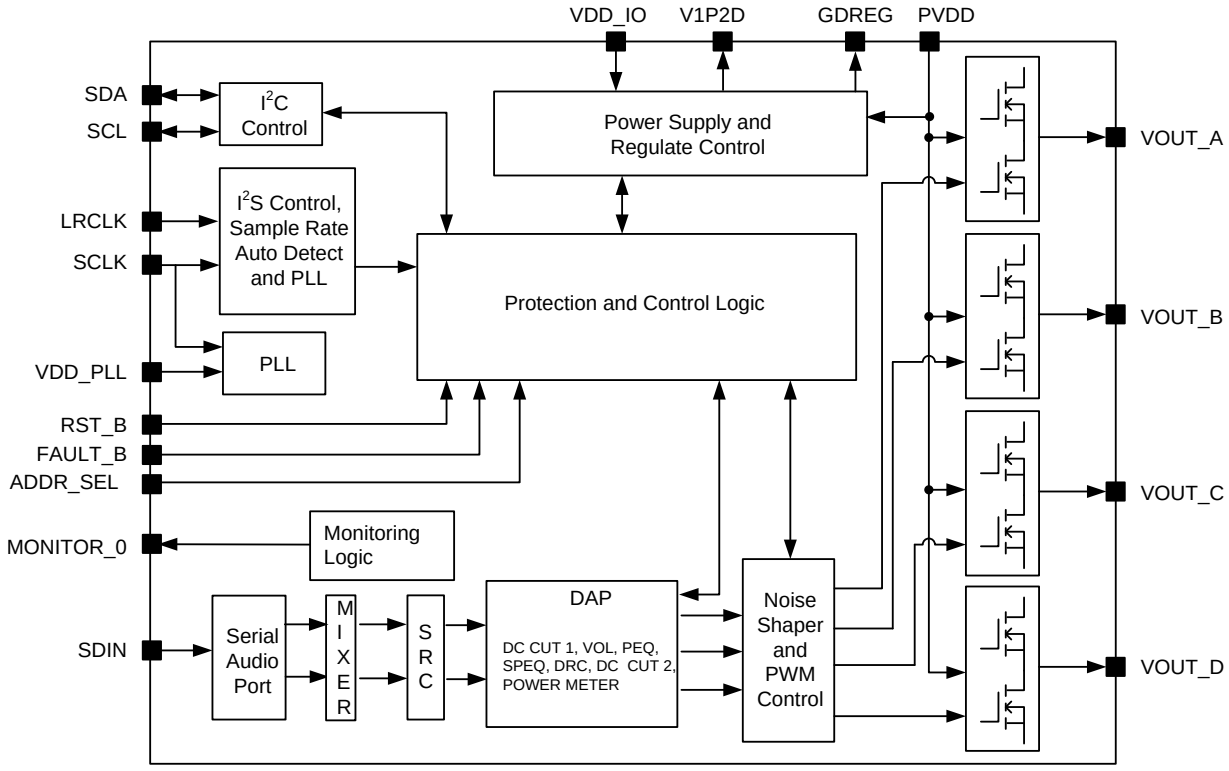


Figure2. Function Block

Absolute Maximum Ratings (Note 1)

VDD_IO, Power Supply for Digital Interface I/O ---------- -0.3V to 3.6V
PVDD, Half-bridge Supply Voltage (Note 2) ---------- -0.3V to 18V
Digital Input ---------- -0.5V to (VDD_IO+0.5)V
VOUT_x ---------- 18V
GDREG ---------- -0.5V to 4V
VBS_x to VOUT_x ---------- -0.5V to 4V
Junction Temperature Range ---------- 0°C to 150°C
Storage Temperature Range ---------- -40°C to 125°C

Recommended Operating Conditions

VDD_IO, Power Supply for Digital Interface I/O ---------- 3.3V
PVDD, Half-bridge Supply Voltage ---------- 4.5V to 16.5V
V_{IH}, High-level Input Voltage ---------- ≥2V
V_{IL}, Low-level Input Voltage ---------- ≤0.8V
$R_{L(BTL)}$, Load Impedance(BTL) ---------- 8Ω
$R_{L(PBTL)}$, Load Impedance(PBTL) ---------- 4Ω
Operating Ambient Temperature Range ---------- 0°C to 85°C
Operating Junction Temperature Range ---------- 0°C to 125°C

PWM Operation at Recommended Operating Conditions

Parameter	Test Conditions	Value	Unit
Output Sample Rate	44.1kHz data rate	352.8	kHz
	32/48/96kHz data rate	384	

PLL Input Parameters and External Filter Components

Parameter	Test Conditions	Min	Typ	Max	Unit
F_{SCLK} SCLK Frequency		1.024		6.144	MHz
SCLK Duty Cycle		40	50	60	%
$t_{r(sclk)}$ SCLK Rise Time				5	ns
$t_{f(sclk)}$ SCLK Fall Time				5	ns

Electrical Characteristics

DC Characteristics

(T_A=25°C, PVDD_x=12V, VDD_IO=3.3V, R_L=8Ω, BTL Ternary Mode, f_S=48 kHz)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PVDD	Half-bridge Supply Voltage		4.5		16.5	V
VDD_IO	Power Supply for Digital Interface I/O		2.7		3.6	V
GDREG	Gate Drive Supply		3.2		3.4	V
V_{IH}	High Level Input Voltage	TEST, SDIN, LRCLK,SDA, SCL, FAULT_B, RST_B, ADDR_SEL, SCLK	2			V
V_{IL}	Low Level Input Voltage	TEST, SDIN, LRCLK,SDA, SCL, FAULT_B, RST_B, ADDR_SEL, SCLK			0.8	V
I_{IL}	Low Level Input Current	TEST, SDIN, LRCLK, SDA, SCL, FAULT_B, RST_B, ADDR_SEL, SCLK			75	μA
I_{IH}	High Level Input Current	TEST, SDIN, LRCLK, SDA, SCL, FAULT_B, RST_B, ADDR_SEL, SCLK			75	μA
I_{DD}	3.3V Supply Current	No Input No Load		9.3		mA
		Reset(RST_B = low, FAULT_B = high)		0.7		
I_{PVDD}	No Load, Half-bridge Supply Current (Without Snubber)	Normal		26.5		mA
		Reset(RST_B = low, FAULT_B = high)		1		
Power MOSFET						
$R_{DS(on)}$	High Side Drain-to-source Resistance	T_j=25°C, includes metallization resistance		150		mΩ
	Low Side Drain-to-source Resistance			150		mΩ
I/O Protection						
V_{UVP}	PVDD Falling		3	3.6		V
	PVDD Rising			4.0	4.45	
OVTP(Note 3)	Over Temperature Protection			150		°C
$OVTP_{HYST}$ (Note 3)	Over Temperature Protection Hysteresis			30		°C
I_{OVC}	Over Current Protection			5		A

AC Characteristics (Note 3)

(T_A=25°C, BTL ternary mode, f_S=48 kHz, C_{VBS}=22nF, audio frequency=1 kHz, AES17 filter, snubber=5.6Ω+560pF, unless otherwise specified.)

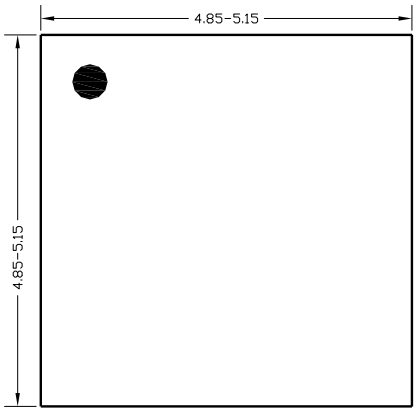
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_o	Output Power	BTL Mode, PVDD=8V, R_L=8Ω, 1%THD+N		3.3		W
		BTL Mode, PVDD=8V, R_L=8Ω, 10%THD+N		4.1		
		BTL Mode, PVDD=12V, R_L=8Ω, 1%THD+N		7.5		
		BTL Mode, PVDD=12V, R_L=8Ω, 10%THD+N		9.2		
		BTL Mode, PVDD=16V, R_L=8Ω, 1%THD+N		13.1		
		BTL Mode, PVDD=16V, R_L=8Ω, 10%THD+N		16.2		
		PBTL Mode, PVDD=12V, R_L=4Ω, 1%THD+N		14.9		
		PBTL Mode, PVDD=12V, R_L=4Ω, 10%THD+N		18.4		
THD+N	Total Harmonic Distortion	PVDD=8V, R_L=8Ω, P_O=1W		0.042		%
		PVDD=12V, R_L=8Ω, P_O=1W		0.048		
		PVDD=16V, R_L=8Ω, P_O=1W		0.036		
V_n	Output Integrated Noise(rms)	PVDD=8V, R_L=8Ω, A-weighted		40.3		μV
		PVDD=12V, R_L=8Ω, A-weighted		73.0		
		PVDD=16V, R_L=8Ω, A-weighted		96.3		
	Crosstalk	PVDD=16V, R_L=8Ω, Po=1 W, f = 1kHz ,		87.9		dB
SNR	Signal to Noise Ratio	PVDD=8V, A weighted, f = 1kHz, maximum power at THD+N <1%		102.2		dB
		PVDD=12V, A weighted, f = 1kHz, maximum power at THD+N <1%		100.4		
		PVDD=16V, A weighted, f = 1kHz, maximum power at THD+N <1%		100.6		

Note 1: Stresses beyond the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

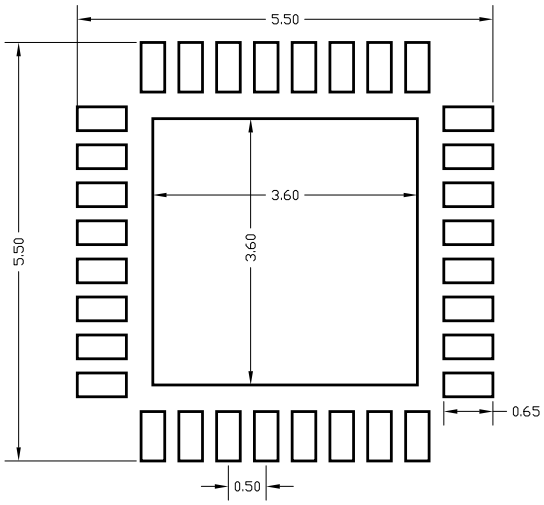
Note 2: DC voltage rating could be derated a little according to the possible switching spike on switching node if the snubber is not appropriate enough.

Note 3: Typical value tested on the demonstration board is guaranteed by design.

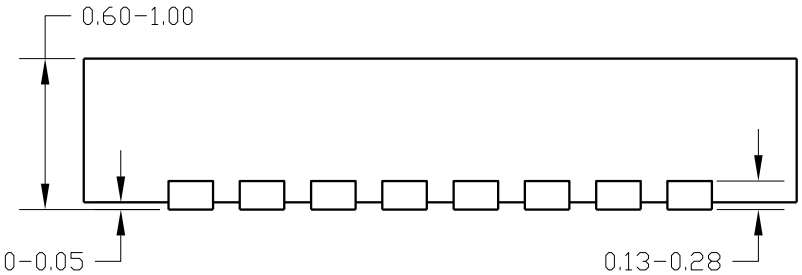
QFN5×5-32 Package Outline & PCB Layout



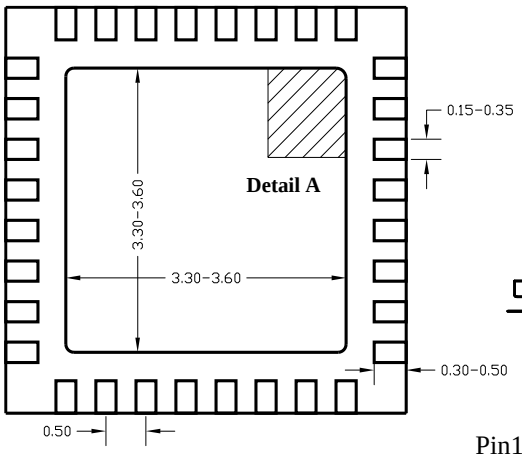
Top View

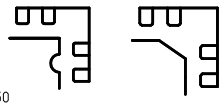


PCB Layout (Recommended)



Side View





Detail A
Pin1 identifier: two options

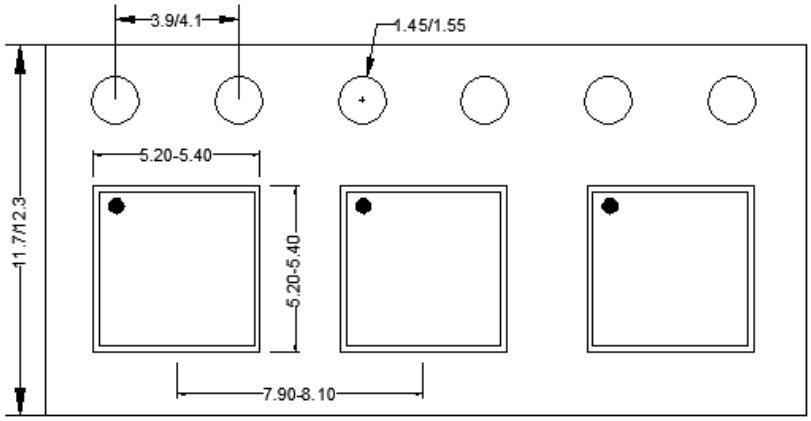
Bottom View

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

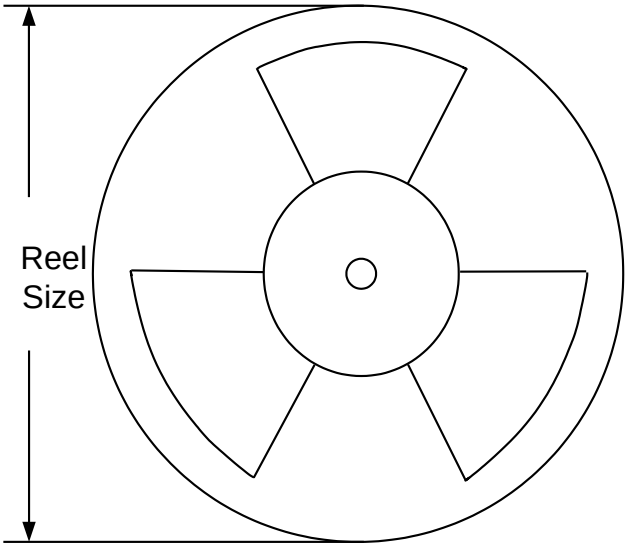
1. Taping orientation

QFN5×5



Feeding direction

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN5×5	12	8	13"	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Sept.10, 2022	Revision 1.0	Production Release
Sept.10, 2021	Revision 0.9C	1. Update the max value of "Enable the I^2C Duration Time" from 12.0 to 0.1ms 2. Update the min value of "SCLK Frequency" from 2.048 to 1.024MHz
Mar.11, 2021	Revision 0.9B	1. Delete single filter in Feature 2. Delete the description of BD or Ternary mode support 3. Delete the Block in the description of DRC
Mar.20, 2020	Revision 0.9A	Update the Feature from "I^2C Serial Control Interface Operational without MCLK" to "3-wire I^2S Digital Audio Interface without MCLK"
Sept. 13, 2018	Revision 0.9	Initial Release

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