SY21228L

High Efficiency Fast Response 8A Continuous, 16A Peak, 28V Input Synchronous Step Down Regulator

General Description

The SY21228L is a high-efficiency synchronous step-down DC/DC regulator featuring internal power and synchronous rectifier switches capable of delivering 8A of continuous output current and up to 16A peak output current over a wide input voltage ranging from 4.5V to 28V.

Silergy's proprietary Instant-PWM™ fast-response, constant-on-time (COT) PWM control method supports high input/output voltage ratios (low duty cycles), and fast transient response while maintaining a near constant operating frequency over line, load and output voltage ranges. This control method provides stable operation without complex compensation and even with low ESR ceramic capacitors.

Internal 20mΩ power and 10mΩ synchronous rectifier switches provide excellent efficiency over a range of applications, especially for low output voltages and low duty cycles. Cycle-by-cycle current limit, input under voltage lock-out, internal soft-start, output under and over voltage protection, and over temperature protection provide safe operation in all operating conditions.

The SY21228L is available in a compact QFN3×3-12 package.

Ordering Information

SY21228□(□□)□

- └ Temperature Code
- └ Package Code
- └ Optional Spec Code

Ordering Number	Package type	Note
SY21228LQQC	QFN3×3-12	--

Features

- Fast Transient Response
- Wide Input Voltage Range: 4.5-28V
- Low $R_{DS(ON)}$ for Internal Switches（Top FET/Bottom FET）:20mΩ/10mΩ
- 8A Continuous/16A Peak Output Current Capability
- Accurate Feedback Reference Voltage: 0.6V ±1%
- Pseudo-constant 500kHz Operating Frequency
- Internal 600μs Soft-start Limits Inrush Current
- PSM/FCCM Selectable Light Load Operation Mode
- Power Good Indicator
- Cycle-by-Cycle Current Limit
- Latch Off Mode Output Under Voltage and Over Voltage Protection
- Over Temperature Protection with Auto Recovery
- Compact Package: QFN3×3-12

Applications

- LCD-TV/Net-TV/3DTV
- Set Top Box
- Notebook
- High Power AP

Typical Applications

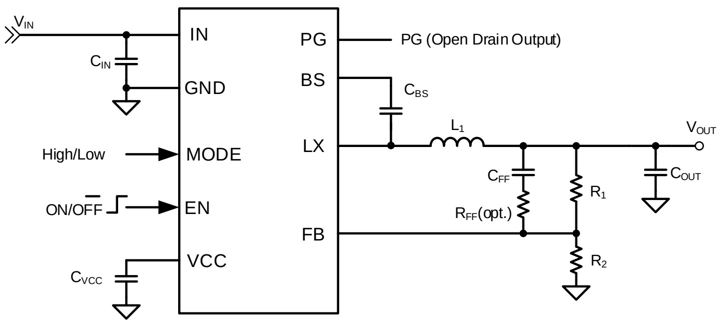


Figure1. Schematic

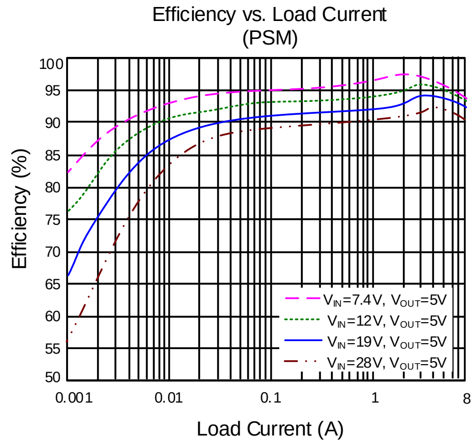
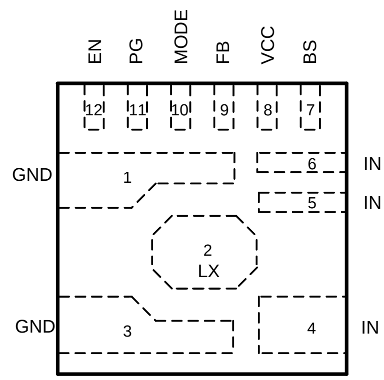


Figure2. Efficiency

Pinout (top view)



(QFN3×3-12)

Top Mark: BQH*xyz*, **(**Device code: BQH, ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin Number	Pin Description
GND	1,3	Ground pin
LX	2	Inductor pin. Connect this pin to the switching node of inductor
IN	4,5,6	Input pin. Decouple this pin to GND pin with at least 10μF ceramic cap
BS	7	Boot-Strap pin. Supply high side gate driver. Decouple this pin to LX pin with 0.1μF ceramic cap.
VCC	8	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuit. Bypass this pin to GND with a 2.2μF ceramic capacitor..
FB	9	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{SET}=0.6\times(1+R_1/R_2)$
MODE	10	Light load operation mode selection pin. Pull this pin low for PSM operation, and pull this pin high for FCCM operation. Do not leave this pin floating.
PG	11	Power good indicator. Open drain output when the output voltage is within 92.5% to 120% of regulation point.
EN	12	Enable control. Pull this pin high to enable the IC. Do not leave this pin floating.

Block Diagram

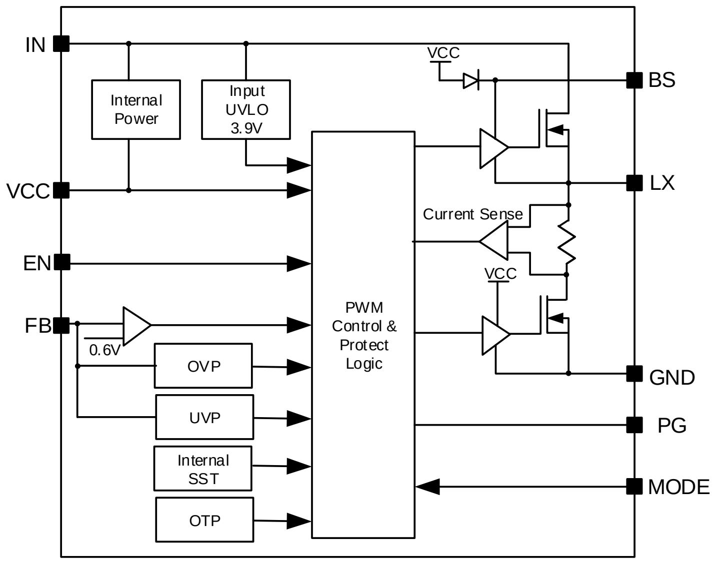


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

IN, LX, PG, EN -- 30V
BS-LX, FB, MODE, VCC--- 4V
Maximum Power Dissipation, $P_{D,MAX}$ @ T_A = 25°C QFN3×3-12 ---3.33W
Package Thermal Resistance (Note 2)
θ_{JA} ---30°C/W
θ_{JC} --- 4°C/W
Junction Temperature Range -- 150°C
Lead Temperature (Soldering, 10 sec.) -- 260°C
Storage Temperature Range --- -65°C to 150°C
Dynamic LX voltage in 50ns duration -- IN+3V to GND-4V

Recommended Operating Conditions (Note 3)

Supply Input Voltage -- 4.5V to 28V
Junction Temperature Range -- -40°C to 125°C
Ambient Temperature Range -- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, V_{OUT} =5V, C_{OUT} = 100µF, T_A = 25°C, I_{OUT} = 2A, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		28	V
Quiescent Current	I_Q	EN=1,I_{OUT}=0, MODE=Low, V_{OUT}=V_{SET}×105%		100		µA
Shutdown Current	I_{SHDN}	EN=0		6	10	µA
Feedback Reference Voltage	V_{REF}		0.594	0.6	0.606	V
FB Input Current	I_{FB}	V_{FB}=4V	-50		50	nA
Top FET $R_{DS(ON)}$	$R_{DS(ON)1}$			20		mΩ
Bottom FET $R_{DS(ON)}$	$R_{DS(ON)2}$			10		mΩ
Bottom FET Current Limit	$I_{LIM,BOT}$		12			A
Bottom FET Reverse Current Limit	$I_{LMT,RVS}$			-2.75		A
Soft-start Time	t_{SS}	V_{OUT} from 0% to 100%V_{SET}		600		µs
EN/MODE Input Voltage High	$V_{EN,H}$		1.0			V
EN/MODE Input Voltage Low	$V_{EN,L}$				0.4	V
EN Leakage Current	I_{EN}		-1		1	µA
MODE Leakage Current	I_{MODE}		-1		1	µA
Input UVLO Threshold	V_{UVLO}				3.9	V
Input UVLO Hysteresis	V_{HYS}			0.3		V
Switching Frequency	F_{SW}	V_{OUT}=5V, CCM	425	500	575	kHz
Min ON Time	$t_{ON,MIN}$	V_{IN}=$V_{IN,MAX}$		50		ns
Min OFF Time	$t_{OFF,MIN}$			180		ns
VCC Output Voltage	V_{CC}	VCC with 1mA load	3.2	3.3	3.45	V
Output Under Voltage Threshold	V_{UVP}	V_{FB} falling		33.3		%V_{REF}
Output UVP Delay Time	$t_{UVP,DLY}$			10		µs
Output Over Voltage Threshold	V_{OVP}	V_{FB} rising		120		%V_{REF}
Output OVP Delay Time	$t_{OVP,DLY}$			12		µs
Power Good Threshold	V_{PG}	V_{FB} rising (good)		92.5		%V_{REF}
Power Good Hysteresis	$V_{PG,HYS}$			2		%V_{REF}
Power Good Delay Time	$t_{PG,R}$			2.5		µs
	$t_{PG,F,}$			15		µs
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

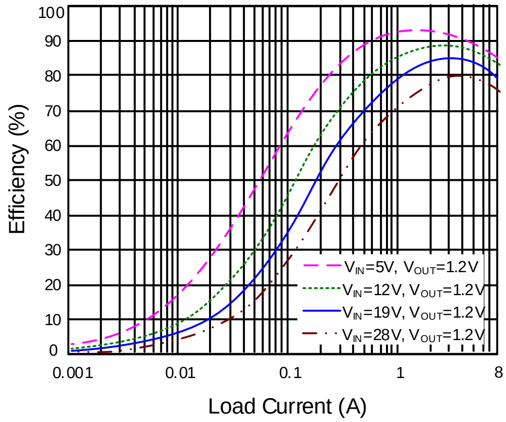
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note 2: Package thermal resistance is measured in the natural convection at T_A = 25°C on a four-layer Silergy Evaluation Board.

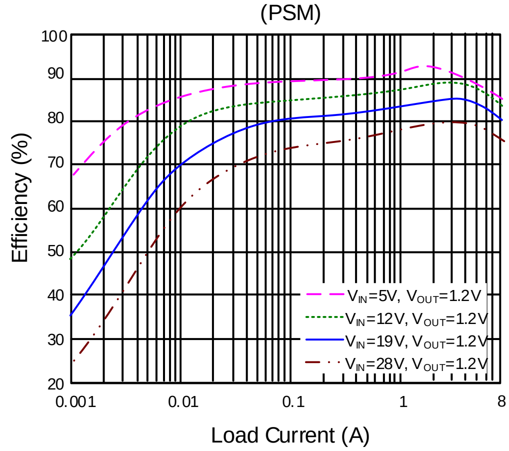
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

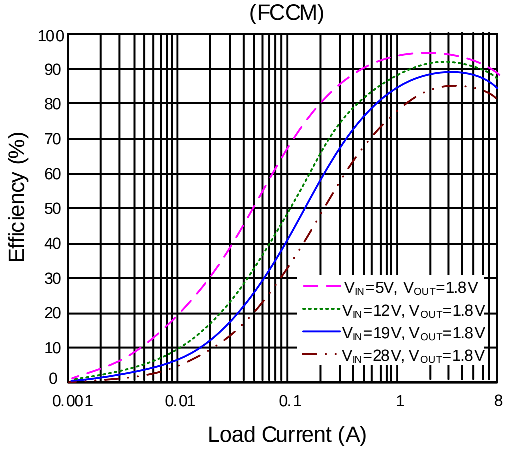
Efficiency vs. Load Current
(FCCM)



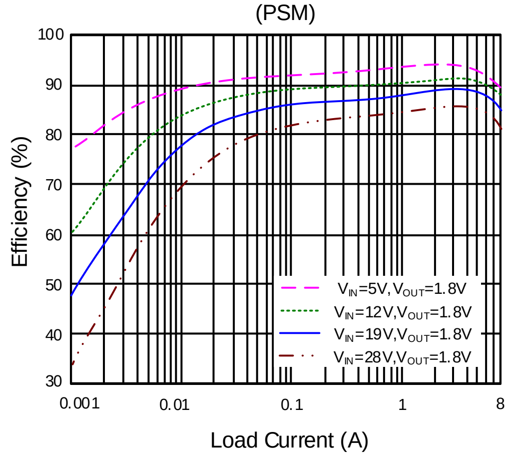
Efficiency vs. Load Current
(PSM)



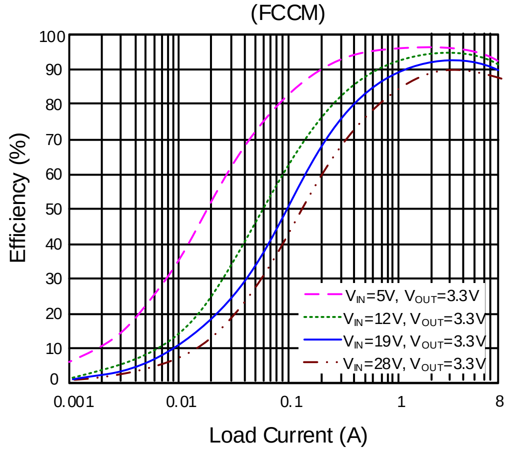
Efficiency vs. Load Current
(FCCM)



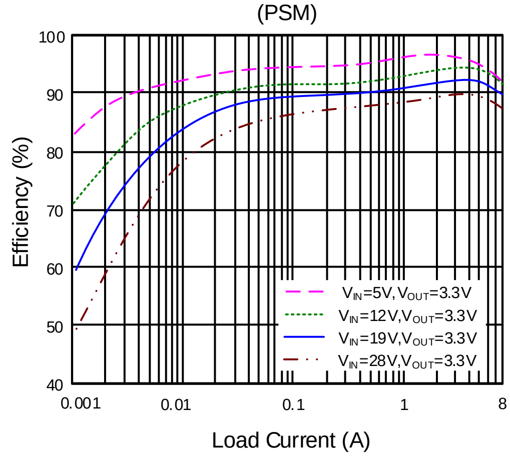
Efficiency vs. Load Current
(PSM)



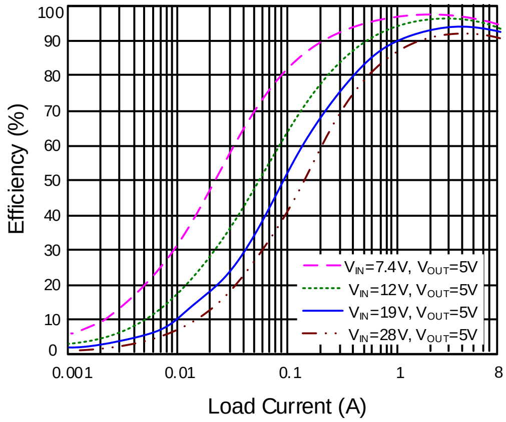
Efficiency vs. Load Current
(FCCM)



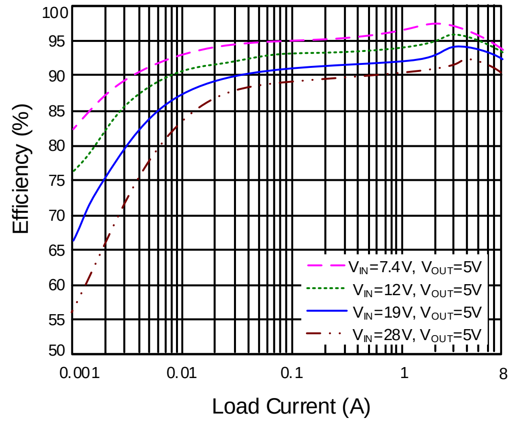
Efficiency vs. Load Current
(PSM)



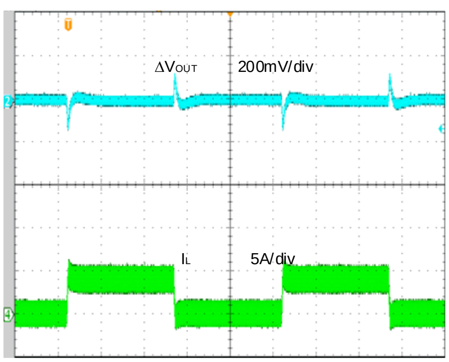
Efficiency vs. Load Current
(FCCM)



Efficiency vs. Load Current
(PSM)

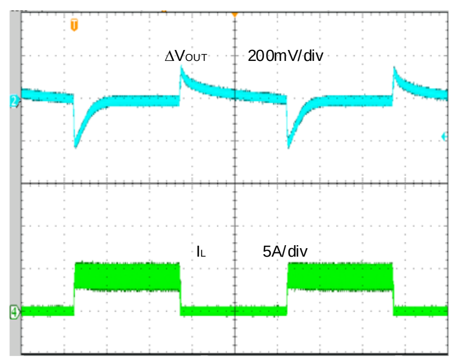


Load Transient
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0~4A, FCCM)



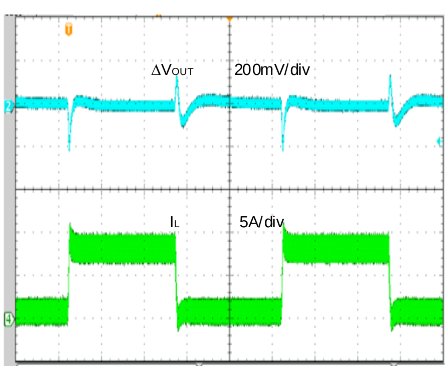
Time (200μs/div)

Load Transient
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0~4A, PSM)



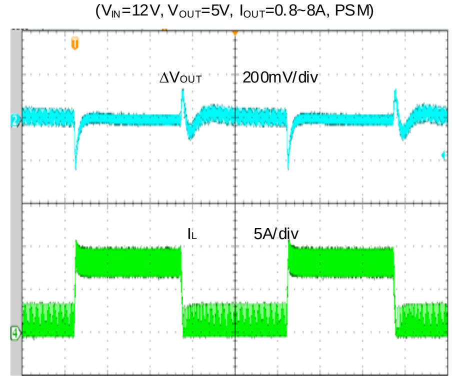
Time (200μs/div)

Load Transient
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0.8~8A, FCCM)



Time (200μs/div)

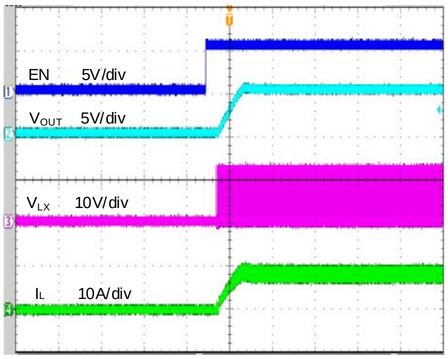
Load Transient
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0.8~8A, PSM)



Time (200μs/div)

Startup from EN

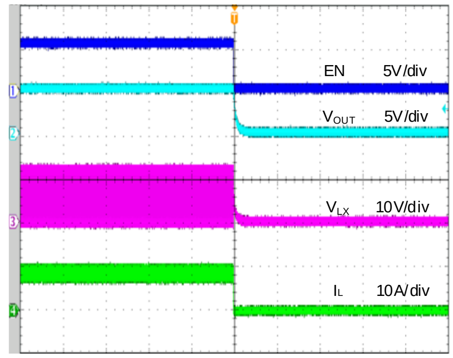
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=8A)



Time (800μs/div)

Shutdown from EN

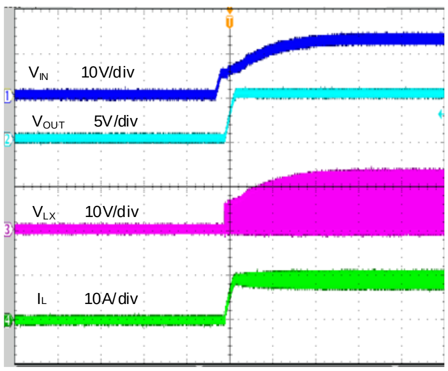
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=8A)



Time (800μs/div)

Startup from V_{IN}

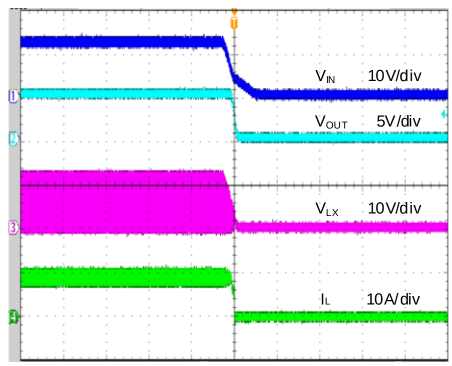
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=8A)



Time (2ms/div)

Shutdown from V_{IN}

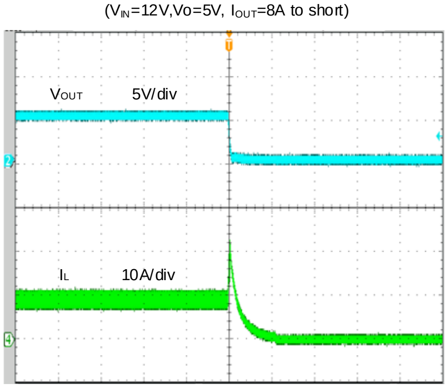
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=8A)



Time (2ms/div)

Output Short Circuit

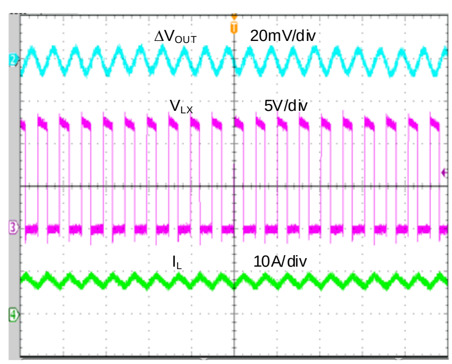
(V_{IN}=12V,Vo=5V, I_{OUT}=8A to short)



Time (200μs/div)

Output Ripple

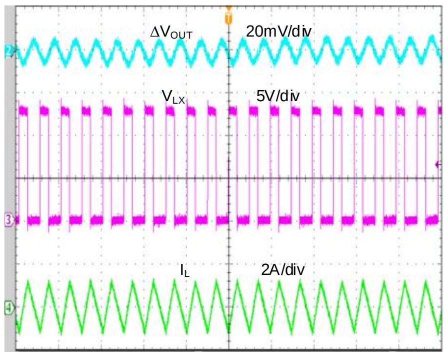
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=8A)



Time (4μs/div)

Output Ripple

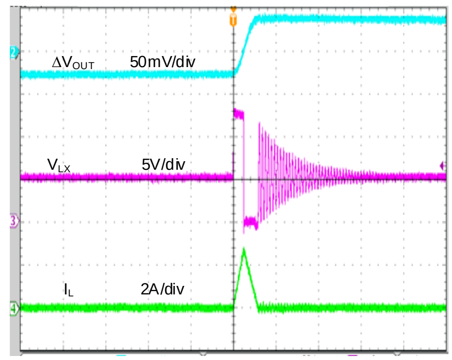
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A, FCCM)



Time (4μs/div)

Output Ripple

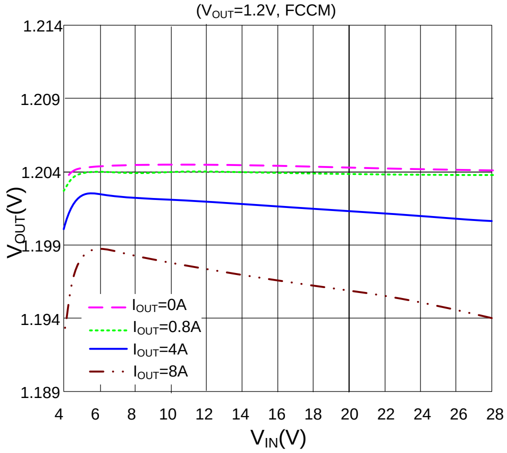
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A, PSM)



Time (4μs/div)

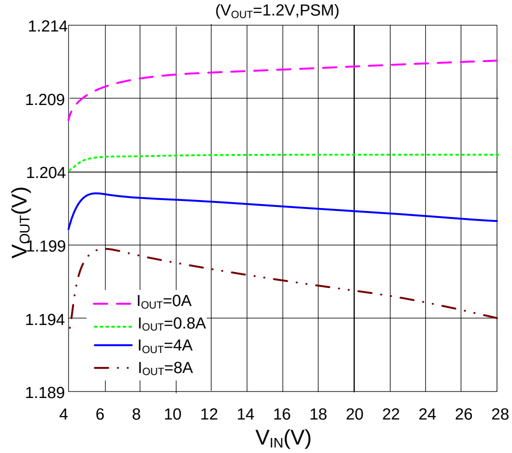
Output Voltage vs. Input Voltage

(V_{OUT}=1.2V, FCCM)

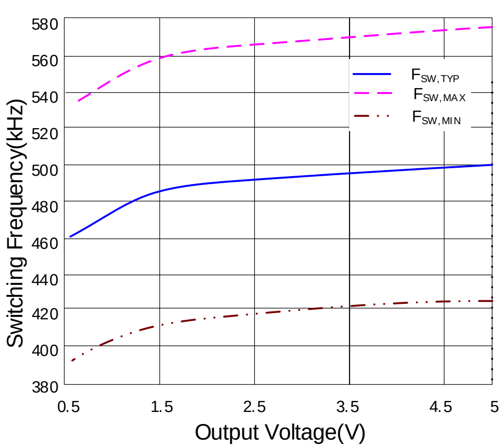


Output Voltage vs. Input Voltage

(V_{OUT}=1.2V,PSM)



Switching Frequency VS Output Voltage(I_{OUT}=3A)



Detailed Description

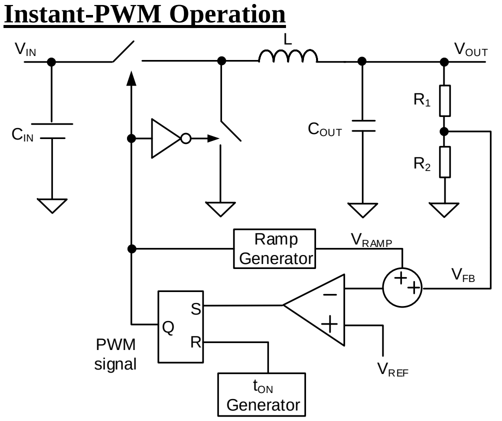
General Features

Constant-on-time Architecture

Fundamental to any constant-on-time (COT) architecture is the one-shot circuit or on-time generator, which determines how long to turn on the high-side power switch. Each on-time (t_{ON}) is a "fixed" period internally calculated to operate the converter at the desired switching frequency considering the input and output voltage ration, $t_{ON}=(V_{OUT}/V_{IN})\times(1/F_{SW})$. For example, considering that a hypothetical converter targets 5V output from a 10V input at 500kHz, the target on-time is (5V/10V)×(1/500kHz) =1μs. Each t_{ON} pulse is triggered by the feedback comparator when the output voltage as measured at FB drops below the target value. After one t_{ON} period, a minimum off-time ($t_{OFF,MIN}$) is imposed before any further switching is initiated, even if the output voltage is less than the target. This approach avoids the making any switching decisions during the noisy periods just after switching events and while the switching node (LX) is rapidly rising or falling.

In a COT architecture, there is no fixed clock, so the high-side power switch can turn on almost immediately after a load transient and subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays. Traditional current mode or voltage mode control methods must simultaneously monitor the feedback voltage, current feedback and internal ramps and compensation signals to determine when to turn off the high-side power switch and turn on the low-side synchronous rectifier. Considering these small signals in a switching environment are difficult to be noise-free after switching large currents, making those architectures difficult to apply in noisy environments and at low duty cycles.

Instant-PWM Operation



Silergy's instant-PWM control method adds several proprietary improvements to the traditional COT architecture. Whereas most legacy based on COT implementations require a dedicated connection to the output voltage terminal to calculate the t_{ON} duration, instant-PWM control method derives this signal internally. Another improvement optimizes operation with low ESR ceramic output capacitors. In many applications it is desirable to utilize very low ESR ceramic output capacitors, but legacy COT regulators may become unstable in these cases because the beneficial ramp signal that results from the inductor current flowing into the output capacitor maybe become too small to maintain smooth operation. For this reason, instant-PWM synthesizes a virtual replica of this signal internally. This internal virtual ramp and the feedback voltage are combined and compared to the reference voltage. When the sum is lower than the reference voltage, the t_{ON} pulse is triggered as long as the minimum t_{OFF} has been satisfied and the inductor current as measured in the low-side synchronous rectifier is lower than the bottom FET current limit. As the t_{ON} pulse is triggered, the low-side synchronous rectifier turns off and the high-side power switch turns on. Then the inductor current ramps up linearly during the t_{ON} period. At the conclusion of the t_{ON} period, the high-side power switch turns off, the low-side synchronous rectifier turns on and the inductor current ramps down linearly. This action also initiates the minimum t_{OFF} timer to ensure sufficient time for stabilizing any transient conditions and settling the feedback comparator before the next cycle is initiated. This minimum t_{OFF} is relatively short so that during high speed load transient t_{ON} can be retriggered with minimal delay, allowing the inductor current to ramp quickly to provide sufficient energy to the load side.

In order to avoid shoot-through, a dead time (t_{DEAD}) is generated internally between the high-side power switch off and the low-side synchronous rectifier on period or the low-side synchronous rectifier off and the high-side power switch on period.

Light Load Operation Mode Selection

PSM or FCCM light load operation is selected by MODE pin. Pull MODE pin low for PSM operation, and pull this pin high for FCCM operation.

If PSM light load operation is selected, under light load conditions, typically $I_{OUT} < 1/2\times\Delta I_L$, the current through the low-side synchronous rectifier will ramp to near zero before the next t_{ON} time. When this occurs, the low-side synchronous rectifier turns off, preventing recirculation current that can seriously reduce efficiency under these light load conditions. As load current is further reduced, and the combined feedback and ramp signals remain greater than the reference voltage, the instant-PWM control loop will not trigger another t_{ON} until needed, so the apparent operating switching frequency will correspondingly drop, further enhancing efficiency. Continuous conduction mode resumes smoothly as soon as the load current increases sufficiently for the inductor current to remain above zero at the time of the next t_{ON} cycle.

If FCCM light load operation is selected, under light load conditions, the low-side synchronous rectifier still turns on even when the inductor current crosses zero. Current flow will continue until the next t_{ON} cycle. The device always operates under continuous conditions mode.

Input Under Voltage Lock-out

To prevent operation before all internal circuitry is ready and to ensure that the power and synchronous rectifier switches can be sufficiently enhanced, instant-PWM incorporates input under voltage lock-out (UVLO) protection. The device remains in a low current state and all switching actions is inhibited until V_{IN} exceeds V_{UVLO}, the input UVLO (rising) threshold. At that time, if EN is enabled, the device will start-up by initiating a soft-start ramp. If V_{IN} falls below V_{UVLO} less than the input UVLO hysteresis, V_{HYS}, switching actions will again be suppressed.

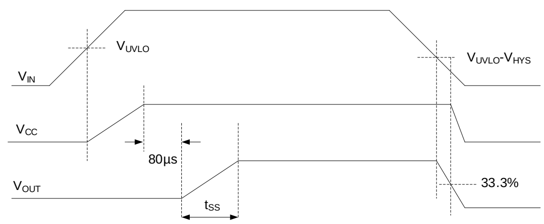
Enable Control

The EN input is a high-voltage capable input with logic-compatible threshold. When EN is driven above 1V normal device operation will be enabled. When driven < 0.4V the device will be shut down, reducing input current to < 10µA.

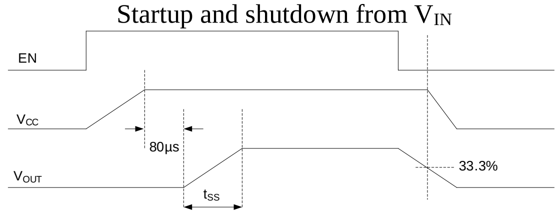
If the system connection to EN may become high-impedance during shutdown when IN is connected directly to a power source such as a Li-Ion battery, consider including a pull-down resistor (~1MΩ) from EN to GND to prevent noise or leakage from enabling the device incorrectly.

Startup and Shutdown

The SY21228L incorporates an internal soft-start circuit to smoothly ramp the output to the desired voltage whenever the device enabled. Internally, the soft-start circuit clamps the output at a low voltage and then allows the output to rise to the desired voltage over approximately 600µs, which avoids high current flow and transients during startup. The startup and shutdown sequence is shown below.



Startup and shutdown from V_{IN}



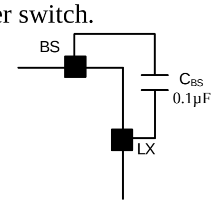
Startup and shutdown from EN

Power Good Indicator

The power-good indicator is an open drain output controlled by a window comparator connected to the feedback signal. If V_{FB} is greater than V_{PG} and less than V_{OVP} for at least the power good delay time, PG will be high-impedance.

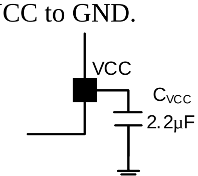
External Bootstrap Capacitor Connection

This device integrates a floating power supply for the gate driver that operates the high-side power switch. Proper operation requires a 0.1µF low ESR ceramic capacitor to be connected between BS and LX. This bootstrap capacitor provides the gate driver supply voltage for the high-side N-channel MOSFET power switch.



VCC Linear Regulator (VCC)

An internal linear regulator (VCC) produces a 3.3V supply from V_{IN} that powers the internal gate drivers, PWM logic, analog circuitry, and other blocks. Connect a 2.2µF low ESR ceramic capacitor from VCC to GND.



Fault Protection Modes

Current Limit

Instant-PWM incorporates a cycle-by-cycle "valley" current limit. Inductor current is measured in the low-side synchronous rectifier when it turns on and as the inductor current ramps down. If the current exceeds the bottom FET current limit, t_{ON} is inhibited until the current returns back to safe levels.

Output Under Voltage Protection (UVP)

If V_{OUT} < ~33.3% of the set point for approximately 10μs, the output under voltage protection (UVP) will be triggered, and the device will latch off. Recycling EN input to re-enable the device.

Output Over Voltage Protection (OVP)

This device includes output over voltage protection (OVP). If the output voltage rises above the feedback regulation level, the high-side power switch naturally remains off and the low-side synchronous rectifier turns on. If the output voltage remains high, the low-side synchronous rectifier remains on until the inductor current reaches zero when operating in PSM operation or when the reverse current limit is triggered when operating in FCCM operation. If the output voltage continues to rise and exceeds the output over voltage threshold for more than output OVP delay time, output over voltage protection (OVP) will be triggered, and the device will latch off. Recycling EN input to re-enable the device.

Over Temperature Protection (OTP)

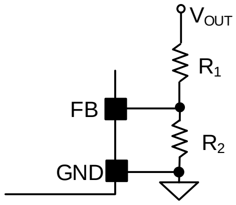
Instant-PWM includes over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 15°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the OTP threshold.

Design Procedure

Feedback Resistor Selection

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is strongly recommended for both resistors. If V_{SET} is 3.3V, R_1=100kΩ is chosen, then using following equation, R_2 can be calculated to be 22.1kΩ.

$$R_2 = \frac{0.6V}{V_{SET}\text{-}0.6V} \times R_1$$



Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage.

Instant-PWM operates well over a wide range of inductor values. This flexibility allows for optimization to find the best trade-off of efficiency, cost and size for a particular application. Selecting a low inductor value will help reduce size and cost and enhance transient response, but will increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low value inductors may help reduce DC losses and increase efficiency. On the other hand, higher inductor values tend to have higher DCR and will slow transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a ripple current (ΔI_L) about 20-50% of the desired full output load current. Start by calculating the approximate inductor value by selecting the input and output voltages, the operating frequency (F_{SW}), the maximum output current ($I_{OUT,MAX}$) and estimating a ΔI_L as some percentage of that current.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times F_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current (ΔI_L) and required peak current inductor current $I_{L,PEAK}$.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times F_{SW} \times L_1}$$

And $I_{L,PEAK}=I_{OUT,MAX} + \Delta I_L/2$

Select an inductor with a saturation current and thermal rating in excess of $I_{L,PEAK}$.

If FCCM light load operation is selected, make sure the inductor value is high enough to avoid reverse current limit is been triggered just under steady state if the load current is zero.

For highest efficiency, select an inductor with a low DCR that meets the inductance, size and cost targets. Low loss ferrite materials should be considered.

Inductor Design Example

Consider a typical design for a device providing $5V_{OUT}$ at 8A from $12V_{IN}$, operating at 500kHz and using target inductor ripple current (ΔI_L) of 30% or 2.4A. Determine the approximate inductance value:

$$L_1 = \frac{5V \times (12V - 5V)}{12V \times 500kHz \times 2.4A} = 2.43\mu H$$

Next, select the nearest standard inductance value, in this case 2.2μH, and calculate the resulting inductor ripple current (ΔI_L):

$$\Delta I_L = \frac{5V \times (12V - 5V)}{12V \times 500kHz \times 2.2\mu H} = 2.65A$$

$I_{L,PEAK}$=8A+2.65A/2=9.325A

The resulting 2.65A ripple current is 2.65A/8A is ~33.1%, well within the 20%~50% target. Finally, select an available inductor with a saturation current higher than the resulting $I_{L,PEAK}$ of 9.325A.

Input Capacitor Selection

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply and to reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X5R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current,

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D=0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

On the other hand, the input capacitor value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated by

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at D=0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times F_{SW} \times C_{IN}}$$

In most applications a single 10μF X5R capacitor is sufficient. The capacitance value is less important than the RMS current rating. Take care to locate the ceramic input capacitor as close to the device IN and GND pin as possible.

Output Capacitor Selection

Instant-PWM provides excellent performance with a wide variety of output capacitor types. Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the transient response and output voltage ripple requirements of the system.

Output Ripple

Output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitors ESR (ESR ripple) as well as the stored charge (capacitive ripple). When considering total ripple, both should be considered.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times F_{SW}}$$

Consider a typical application with ΔI_L=2.65A using three 22μF ceramic capacitors, each with an ESR of ~6mΩ for parallel total of 66μF and 2mΩ ESR.

$$V_{RIPPLE,ESR} = 2.65A \times 2m\Omega = 5.3mV$$

$$V_{RIPPLE,CAP} = \frac{2.65A}{8 \times 66\mu F \times 500kHz} = 10mV$$

Total ripple = 15.3mV. The actual capacitive ripple may be higher than calculated value because the capacitance decreases with the voltage on the capacitor.

Using a 150μF 40mΩ POS cap, the above result is

$$V_{RIPPLE,ESR} = 2.65A \times 40m\Omega = 106mV$$

$$V_{RIPPLE,CAP} = \frac{2.65A}{8 \times 150\mu F \times 500kHz} = 4.4mV$$

Total ripple = 110.4mV

Output Transient Undershoot/Overshoot

If very fast load transient must be supported, consider the affect of the output capacitor on the output transient undershoot and overshoot. Instant-PWM responds quickly to changing load conditions, however, some considerations must be needed, especially when using small ceramic capacitors which have low capacitance at low output voltages which results in insufficient stored energy for load transient. Output transient undershoot and overshoot have two causes: voltage changes caused by the ESR of the output capacitor and voltage changes caused by the output capacitance and inductor current slew rate.

ESR undershoot or overshoot may be calculated as $V_{ESR} = \Delta I_{OUT} \times ESR$. Using the ceramic capacitor example above and a fast load transient of +/-4A, V_{ESR} = +/-4A×2mΩ=+/-8mV. The POS capacitor result with the same load transient, V_{ESR} = +/-4A×40 mΩ=+/-160mV.

Capacitive undershoot (load increasing) is a function of the output capacitance, the load step, the inductor value and the input-output voltage difference and the maximum duty factor. During a fast load transient, the maximum duty factor of instant-PWM is a function of t_{ON} and the minimum t_{OFF} as the control scheme is designed to rapidly ramp the inductor current by grouping together many t_{ON} pulses in this case. The maximum duty factor D_{MAX} may be calculated by

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF,MIN}}$$

Given this, the capacitive undershoot may be calculated by

$$V_{UNDERSHOOT,CAP} = -\frac{L_1 \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times (V_{IN,MIN} \times D_{MAX} - V_{OUT})}$$

Consider a 4A load increase using the ceramic capacitor case when V_{IN} = 10V.At V_{OUT} = 5V, the result is t_{ON} = 1μs, $t_{OFF,MIN}$ = 180ns, D_{MAX} = 1000/(1000+180) = 0.84 and

$$V_{UNDERSHOOT,CAP} = -\frac{2.2\mu H \times (4A)^2}{2 \times 66\mu F \times (10V \times 0.84 - 5V)} = -78mV$$

Using the POS capacitor case, the above result is

$$V_{UNDERSHOOT,CAP} = -\frac{2.2\mu H \times (4A)^2}{2 \times 150\mu F \times (10V \times 0.84 - 5V)} = -34.5mV$$

Capacitive overshoot (load decreasing) is a function of the output capacitance, the inductor value and the output voltage where

$$V_{OVERSHOOT,CAP} = \frac{L_1 \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times V_{OUT}}$$

Consider a 4A load decrease using the ceramic capacitor case above. At V_{OUT} = 5V the result is

$$V_{OVERSHOOT,CAP} = \frac{2.2\mu H \times (4A)^2}{2 \times 66\mu F \times 5V} = 53.3mV$$

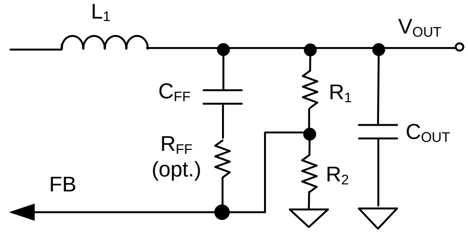
Using the POS capacitor case, the above result is

$$V_{OVERSHOOT,CAP} = \frac{2.2\mu H \times (4A)^2}{2 \times 150\mu F \times 5V} = 23.5mV$$

Combine the ESR and capacitive undershoot and overshoot to calculate the total overshoot and undershoot for a given application.

Feed-forward Compensation (R_{FF}, C_{FF})

The SY21228L is internally compensated and optimized for low duty cycle applications. However, in some applications, especially where V_{OUT} > 1.2V, the feedback divider attenuates the AC component of the output. In these cases, transient response may be improved by adding feed-forward compensation. R_{FF} = 1kΩ and C_{FF} = 220pF have been shown to perform well in most applications.



Note that when C_{OUT} > 500μF and minimum load current is low, set feed-forward values as R_{FF} = 1kΩ and C_{FF} = 10nF to provide sufficient ripple to FB for small output ripple and good transient behavior.

Thermal Design Considerations

Maximum power dissipation depends on the thermal resistance of the IC package, the PCB layout, the surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation may be calculated by:

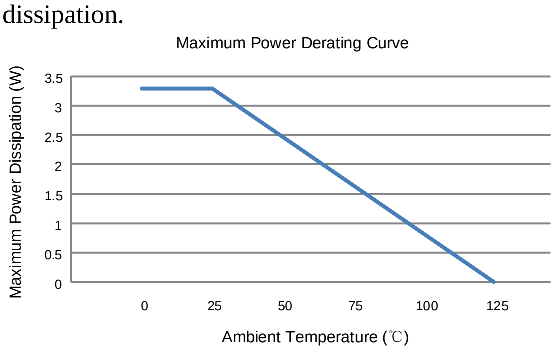
$P_{D,MAX} = (T_{J,MAX} - T_A) / \theta_{JA}$

Where, $T_{J,MAX}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

To comply with the recommended operating conditions, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For the QFN3×3-12 package the thermal resistance θ_{JA} is 30°C/W when measured on a standard Silergy four-layer thermal test board. These standard thermal test layouts have a very large area with long 2oz. copper traces connected to each IC pin and very large, unbroken 1oz. internal power and ground planes.

Meeting the performance of the standard thermal test board in a typical tiny evaluation board area requires wide copper traces well-connected to the IC's backside pads leading to exposed copper areas on the component side of the board as well as good thermal via from the exposed pad connecting to a wide middle-layer ground plane and, perhaps, to an exposed copper area on the board's solder side.

The maximum power dissipation at T_A=25℃ may be calculated by the following formula:
$P_{D,MAX} = (125℃ - 25℃) / (30℃/W) = 3.33W$
The maximum power dissipation depends on operating ambient temperature for fixed $T_{J,MAX}$ and thermal resistance θ_{JA}. Use the derating curve in figure below to calculate the effect of rising ambient temperature on the maximum power dissipation.



Layout Design

Follow these PCB layout guidelines for optimal performance.

- Keep the high current traces as short and wide as possible
- Place the input capacitor very near IN and GND minimizing the loop formed by these connections.
- Place the VCC capacitor close to VCC using short, direct connections to the device GND connection
- Place the FB components (R_1, R_2, R_{FF} and C_{FF}) as close to FB as possible. Avoid routing the FB trace near LX as it is noise sensitive.
- Connect the feedback network to C_{OUT} rather than the inductor output terminal
- The LX connection has large voltage swings and fast edges and can easily radiate noise to adjacent components. Keep its area small to prevent excessive EMI, while providing wide copper traces to minimize parasitic resistance and inductance. Keep sensitive components away from the switching node or provide ground traces between for shielding, to prevent stray capacitive noise pickup.
- The exposed GND pad should be connected to a large copper area for heat sinking and to minimize noise.
- Provide dedicated wide copper traces for the power path ground between the IC and the input and output capacitor grounds, rather than connecting each of these individually to an internal ground plane.

Avoid using vias in the power path connections that have switched currents (from C_{IN} to GND and C_{IN} to V_{IN}) and the switching node (LX).

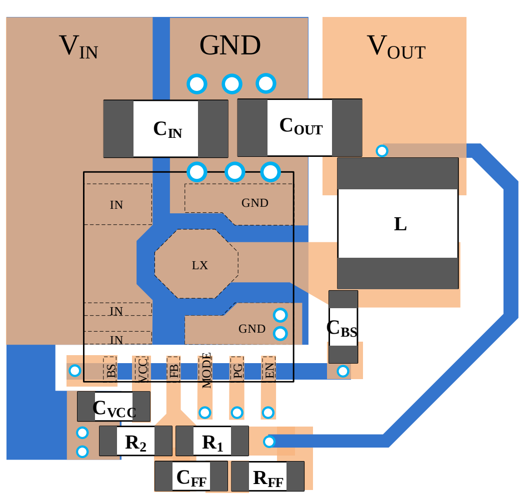
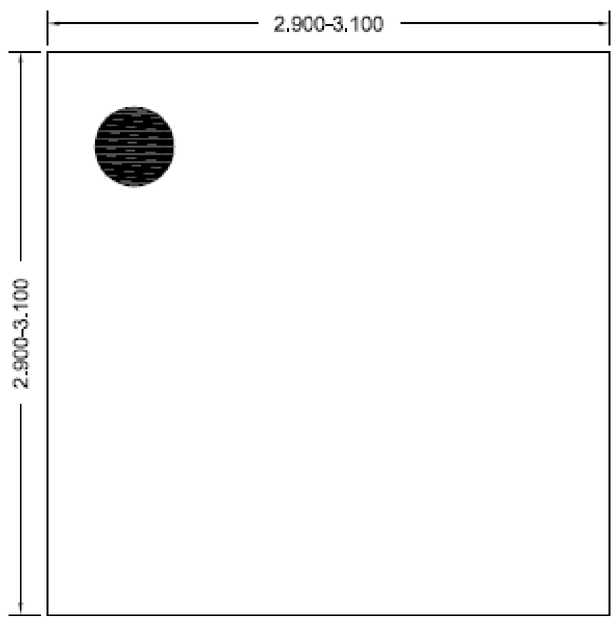
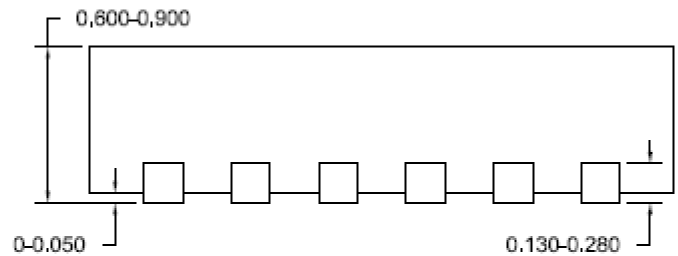


Figure4. PCB Layout Suggestion

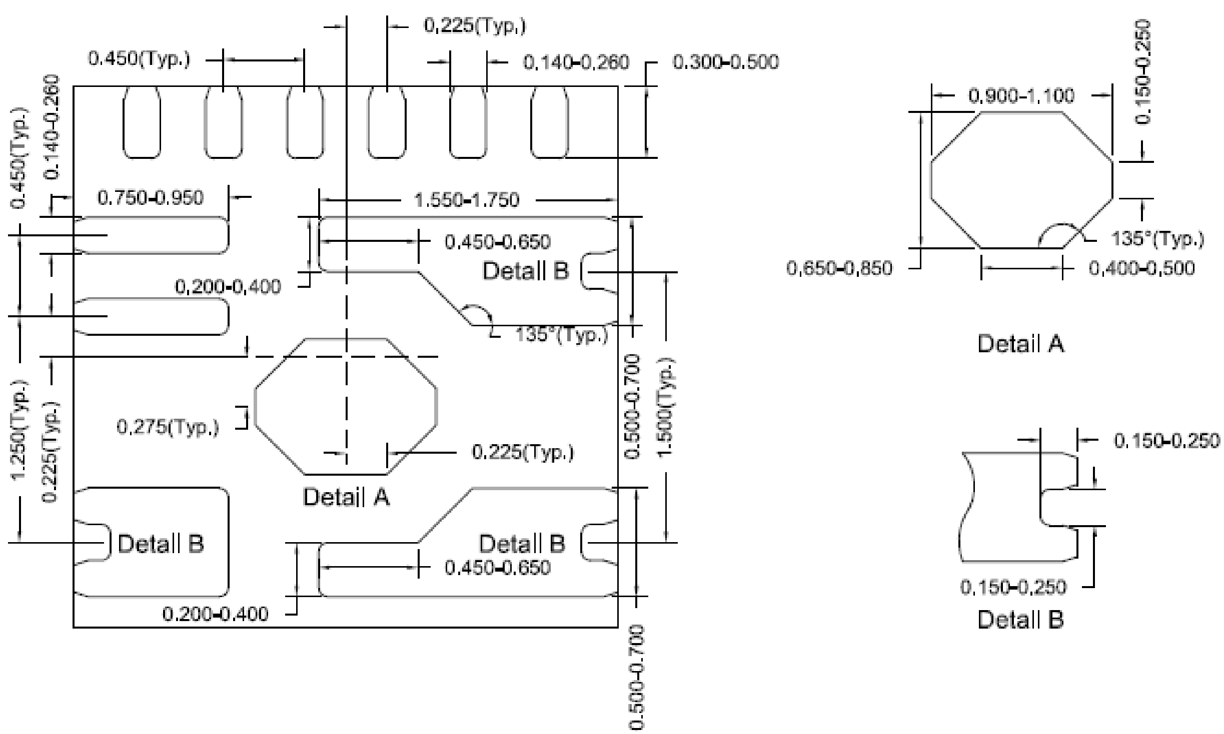
QFN3×3-12 Package Outline Drawing



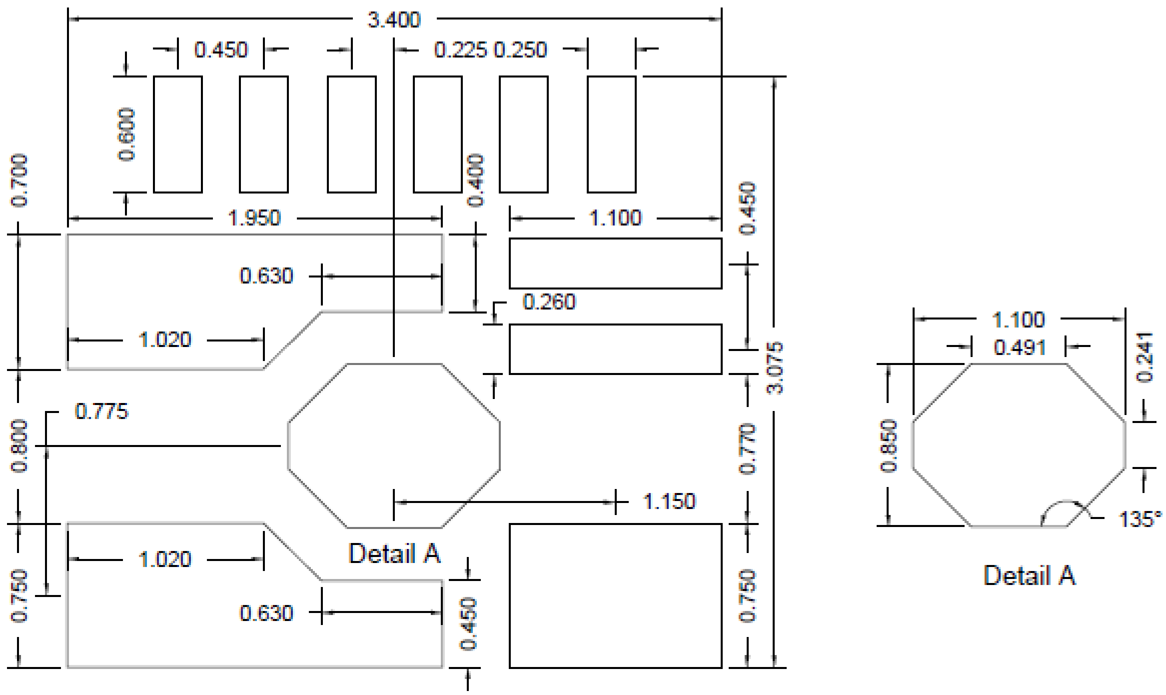
Top View



Side View



Bottom View



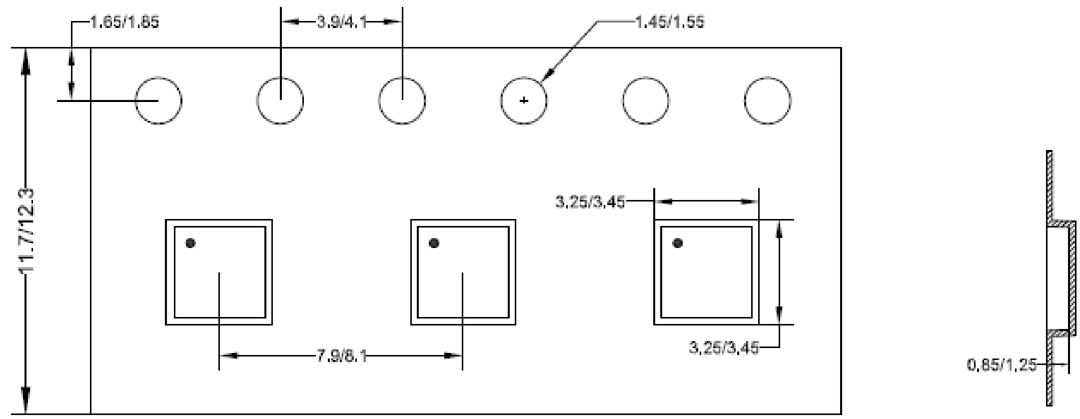
Recommended PCB layout
(Reference Only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

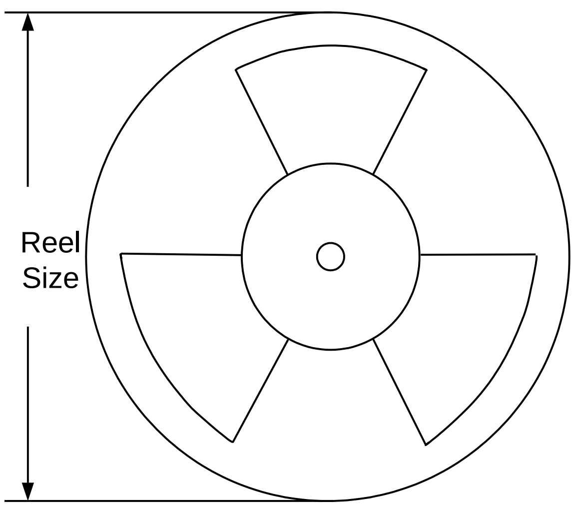
1. Taping orientation

QFN3×3



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×3	12	8	13"	400	400	5000

3. Others: NA

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