SY8088I
High Efficiency, 1.5MHz, 1A
Synchronous Step Down Regulator

General Description

SY8088I is a high efficiency 1.5MHz synchronous step down DC/DC regulator capable of delivering up to 1A output current. It can operate over a wide input voltage range from 2.5V to 5.5V and integrates main switch and synchronous switch with very low \( R_{DS(ON)} \) to minimize the conduction loss.

The low output voltage ripple, the small external inductor and the capacitor sizes are achieved with 1.5MHz switching frequency.

Features

- 2.5V to 5.5V Input Voltage Range
- 50\( \mu \)A Low Quiescent Current
- Low \( R_{DS(ON)} \) for Internal Switches (Top/Bottom) 260m\( \Omega \) /160m\( \Omega \)
- High Switching Frequency 1.5MHz Minimizes the External Components
- Internal Soft-start Limits the Inrush Current
- 100% Dropout Operation
- Reliable Short Circuit Protection
- Output Auto Discharge Function
- RoHS Compliant and Halogen Free
- Compact Package: SOT23-5

Ordering Information

<table>
<thead>
<tr>
<th>Ordering Number</th>
<th>Package type</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>SY8088IAAC</td>
<td>SOT23-5</td>
<td>--</td>
</tr>
</tbody>
</table>

Applications

- Set Top Box
- USB Dongle
- Media Player
- Smart phone

Typical Applications

![Schematic Diagram](image1.png)

![Efficiency vs. Output Current](image2.png)

Figure 1. Schematic Diagram

Figure 2. Efficiency vs. Output Current
Pinout (Top View)

Pin Name | Pin Number | Pin Description
--- | --- | ---
EN | 1 | Enable control. Pull high to turn on. Do not leave it floating.
GND | 2 | Ground pin.
LX | 3 | Inductor pin. Connect this pin to the switching node of the inductor.
IN | 4 | Input pin. Decouple this pin to the GND pin with at least a 10μF ceramic capacitor.
FB | 5 | Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: \( V_{OUT} = 0.6 \times (1 + R_H/R_L) \).

Top Mark: bPxyz (device code: bP, x=year code, y=week code, z= lot number code)

Block Diagram

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Figure2. Block Diagram
Absolute Maximum Ratings (Note 1)

Supply Input Voltage: \(-6.0\) V
EN, FB Voltage: \(-V_{IN} + 0.6\) V
LX Voltage: \(-0.3\) V\(^{(*)1}\) to \(6.0\) V\(^{(*)2}\)

Power Dissipation, \(P_D\) @ \(T_A = 25^\circ\) C: 0.77 W

Package Thermal Resistance (Note 2)
\[ \theta_{JA} = 130^\circ\) C/W \]
\[ \theta_{JC} = 28^\circ\) C/W \]

Junction Temperature Range: \(-40^\circ\) C to \(150^\circ\) C

Lead Temperature (Soldering, 10 sec.): \(-260^\circ\) C

Storage Temperature Range: \(-65^\circ\) C to \(150^\circ\) C

\(^{(*)1}\) LX Voltage Tested down to \(-3\) V\(<40\) ns
\(^{(*)2}\) LX Voltage Tested up to \(+7\) V\(<40\) ns

Recommended Operating Conditions (Note 3)

Supply Input Voltage: \(2.5\) V to \(5.5\) V
Junction Temperature Range: \(-40^\circ\) C to \(125^\circ\) C
Ambient Temperature Range: \(-40^\circ\) C to \(85^\circ\) C
Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 1.8V, L = 2.2\mu H, C_{OUT} = 10\mu F, T_A = 25^\circ C, unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>Input Voltage Range</td>
<td>V_{IN}</td>
<td></td>
<td>2.5</td>
<td></td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Input UVLO Threshold</td>
<td>V_{UVLO}</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input UVLO Hysteresis</td>
<td>V_{HYS}</td>
<td></td>
<td>150</td>
<td></td>
<td></td>
<td>mV</td>
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<tr>
<td>Quiescent Current</td>
<td>I_{Q}</td>
<td>V_{FB}=V_{REF}x105%</td>
<td>50</td>
<td></td>
<td>60</td>
<td>\mu A</td>
</tr>
<tr>
<td>Shutdown Current</td>
<td>I_{SHDN}</td>
<td>V_{EN}=0V</td>
<td>0.1</td>
<td></td>
<td>1</td>
<td>\mu A</td>
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<tr>
<td>Feedback Reference Voltage</td>
<td>V_{REF}</td>
<td>I_{OUT}=0.5A, CCM</td>
<td>591</td>
<td>600</td>
<td>609</td>
<td>mV</td>
</tr>
<tr>
<td>LX Node Discharge Resistance</td>
<td>R_{DIS}</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>\Omega</td>
</tr>
<tr>
<td>Top FET R\text{\scriptsize ON}</td>
<td>R_{DS\text{\scriptsize ON}1}</td>
<td></td>
<td>180</td>
<td>260</td>
<td>340</td>
<td>m\Omega</td>
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<tr>
<td>Bottom FET R\text{\scriptsize ON}</td>
<td>R_{DS\text{\scriptsize ON}2}</td>
<td></td>
<td>100</td>
<td>160</td>
<td>220</td>
<td>m\Omega</td>
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<td>EN Input Voltage High</td>
<td>V_{EN,H}</td>
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<td>1.2</td>
<td></td>
<td></td>
<td>V</td>
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<td>EN Input Voltage Low</td>
<td>V_{EN,L}</td>
<td></td>
<td></td>
<td></td>
<td>0.4</td>
<td>V</td>
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<tr>
<td>Min ON Time</td>
<td>I_{ON,MIN}</td>
<td>from EN high to LX start switching</td>
<td>60</td>
<td></td>
<td></td>
<td>ns</td>
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<td>Maximum Duty Cycle</td>
<td>D_{MAX}</td>
<td></td>
<td>100</td>
<td></td>
<td></td>
<td>%</td>
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<tr>
<td>Turn On Delay</td>
<td>I_{ON,DLY}</td>
<td>from EN high to LX start switching</td>
<td>300</td>
<td></td>
<td></td>
<td>\mu s</td>
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<tr>
<td>Soft-start Time</td>
<td>I_{SS}</td>
<td>V_{OUT} from 0% to 100%</td>
<td>700</td>
<td></td>
<td></td>
<td>\mu s</td>
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<tr>
<td>Switching Frequency</td>
<td>f_{SW}</td>
<td>I_{OUT}=0.5A, CCM</td>
<td>1.5</td>
<td></td>
<td></td>
<td>MHz</td>
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<tr>
<td>Top FET Current Limit</td>
<td>I_{LMT,TOP}</td>
<td></td>
<td>1.5</td>
<td></td>
<td>2.5</td>
<td>A</td>
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<tr>
<td>Thermal Shutdown Temperature</td>
<td>T_{SD}</td>
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<td>160</td>
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<td>Thermal Shutdown Hysteresis</td>
<td>T_{HYS}</td>
<td></td>
<td>20</td>
<td></td>
<td></td>
<td>\degree C</td>
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</table>

**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:** $\theta_{JA}$ of SY8088I is measured in the natural convection at $T_A = 25^\circ C$ on a 2OZ two-layer Silergy evaluation board. Pin 3 is the case position for $\theta_{JC}$ measurement.

**Note 3:** The device is not guaranteed to function outside its operating conditions.
SOT23-5 Package Outline & PCB Layout Design

Notes: All dimensions are in millimeters.
All dimensions don’t include mold flash & metal burr.
1. Taping orientation

SOT23-5

2. Carrier Tape & Reel specification for packages

<table>
<thead>
<tr>
<th>Package type</th>
<th>Tape width (mm)</th>
<th>Pocket pitch (mm)</th>
<th>Reel size (Inch)</th>
<th>Trailer length (mm)</th>
<th>Leader length (mm)</th>
<th>Qty per reel</th>
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<tbody>
<tr>
<td>SOT23-5</td>
<td>8</td>
<td>4</td>
<td>7&quot;</td>
<td>280</td>
<td>160</td>
<td>3000</td>
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3. Others: NA