SY24145S

High Performance, High Fidelity 30W Digital Audio-Power Amplifier

General Description

The SY24145S is a 2×30W, digital audio power amplifier for driving bridge-tied stereo speakers. One serial data input allows processing of up to two discrete audio channels and seamless integration to most digital audio processors. The SY24145S is an I²S slave device receiving all clocks from the external sources.

The SY24145S has the essential audio signal processing functions like dynamic range control, loudness control and parametric equalization.

Ordering Information

SY24145□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY24145SQHC	QFN6×6-40	

Applications

- LCD TV, LED TV or Monitor
- Digital Speaker, Bluetooth Speaker
- Sound Bar

Features

- 2CH Stereo(30W×2BTL)
- 2.0 BTL Mode or Single-filter PBTL Mode Support
- 4.5V to 28V PVDD Range
- 32kHz to 96kHz Sample Rate Support (LJ/RJ/I²S)
- I²C Address Selection Pin
- Independent Channel Volume Controls with 48dB to Mute
- SDATA Generator (I²S Output)
- Two DC Blocking Filters
- 18 PEQs or 12 PEQs + 6 SPEQs Each Channel for Speaker Protection and Speaker Compensation
- 3 Bands Plus a Post Dynamic Range Control
- Loudness Control
- Power Level Meter
- 3-wire I²S Digital Audio Interface without MCLK
- Thermal, Over Current, Short Circuit, Short Load, Open Load Protections and EQ/DRC Coefficients Checksum
- Support Automatic Audio Sample Rate Detection
- Surface Mount, QFN 40-Pin, 6mm×6mm

Typical Application

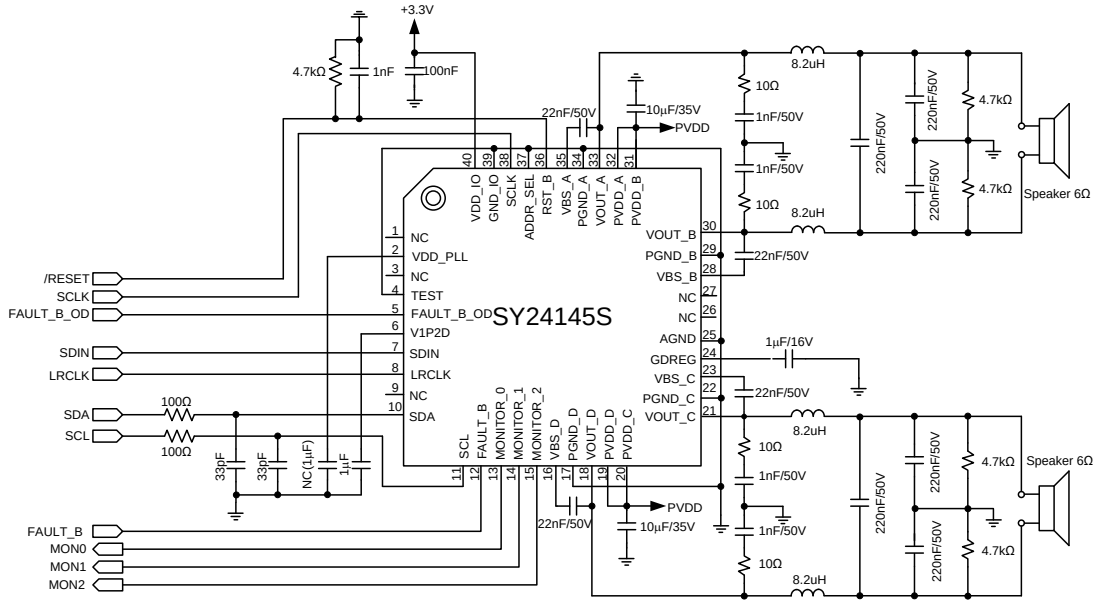
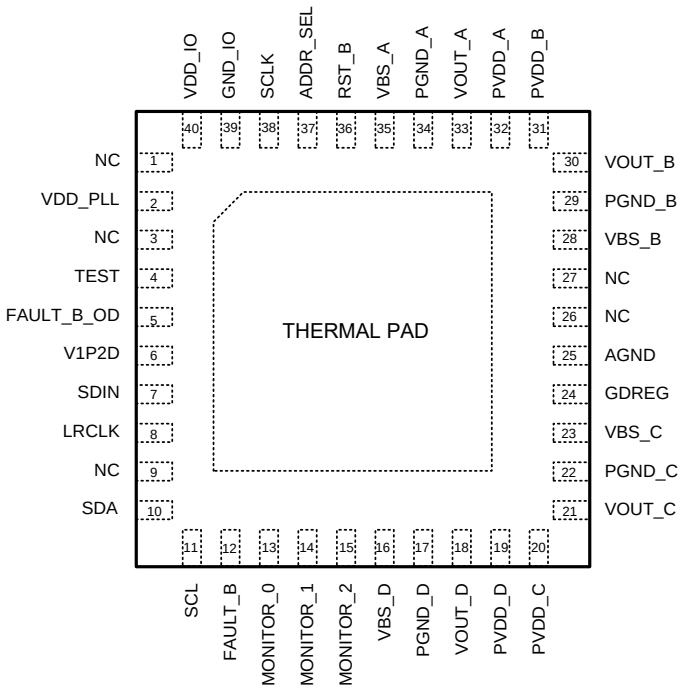


Figure1. Typical Application Circuit

Pinout (top view)



(QFN6×6-40)

Top mark: **CQN** ***xyz*** (Device code: **CQN**, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Type(1)	Termination(2)	Description
VOUT_A	33	O		Half-bridge A output.
VOUT_B	30	O		Half-bridge B output.
VOUT_C	21	O		Half-bridge C output.
VOUT_D	18	O		Half-bridge D output.
PVDD_A	32	P		Power supply for half-bridge A.
PVDD_B	31	P		Power supply for half-bridge B.
PVDD_C	20	P		Power supply for half-bridge C.
PVDD_D	19	P		Power supply for half-bridge D.
VBS_A	35	P		High side supply offset voltage for half-bridge A.
VBS_B	28	P		High side supply offset voltage for half-bridge B.
VBS_C	23	P		High side supply offset voltage for half-bridge C.
VBS_D	16	P		High side supply offset voltage for half-bridge D
GDREG	24	P		Gate driver internal regulator output. This pin must not be used to drive external devices.
GND_IO	39	P		Analog 3.3V power supply ground.
NC	1,3,9,26,27			No Connection.
VDD_IO	40	P		3.3V analog power supply.
ADDR_SEL	37	DI	Pull down	I^2C address selection pin.
V1P2D	6	P		Internal regulated 1.2V digital power supply for digital core. This pin must not be used to power external devices.
VDD_PLL	2	P		Internal regulated 1.2V digital power supply for PLL. This pin must not be used to power external devices.
FAULT_B	12	DI		Pull this pin low to turn off the PWM signal path.
FAULT_B_OD	5	DO		Output internal power-stage errors.

LRCLK	8	DI	Pull down	Serial audio data left or right clock input.
SCLK	38	DI	Pull down	Serial audio data bit clock input.
SDIN	7	DI	Pull down	Serial audio data input.
SDA	10	DIO	Pull up	I2C serial data input or output.
SCL	11	DI	Pull up	I2C serial clock input.
MONITOR_0	13	DO		Monitoring signal out from processor block / I^2S output.
MONITOR_1	14	DO		Monitoring signal out from processor block / I^2S output.
MONITOR_2	15	DO		Monitoring signal out from processor block / I^2S output.
RST_B	36	DI	Pull-up	Logic low to this pin to reset the system. When reset is pulled low, DAP restores to its default conditions, and places the PWM in the hard mute state.
TEST	4	DI	Pull down	Test pin.
AGND	25	P		Power stage analog ground.
PGND_A	34	P		Power ground for half-bridge A.
PGND_B	29	P		Power ground for half-bridge B.
PGND_C	22	P		Power ground for half-bridge C.
PGND_D	17	P		Power ground for half-bridge D.

Note: (1) Type: A =analog; D =digital; P =power/ground/decoupling; I =input; O =output; IO=inout
(2) All pull-ups and pull-downs are weak.

Block Diagram

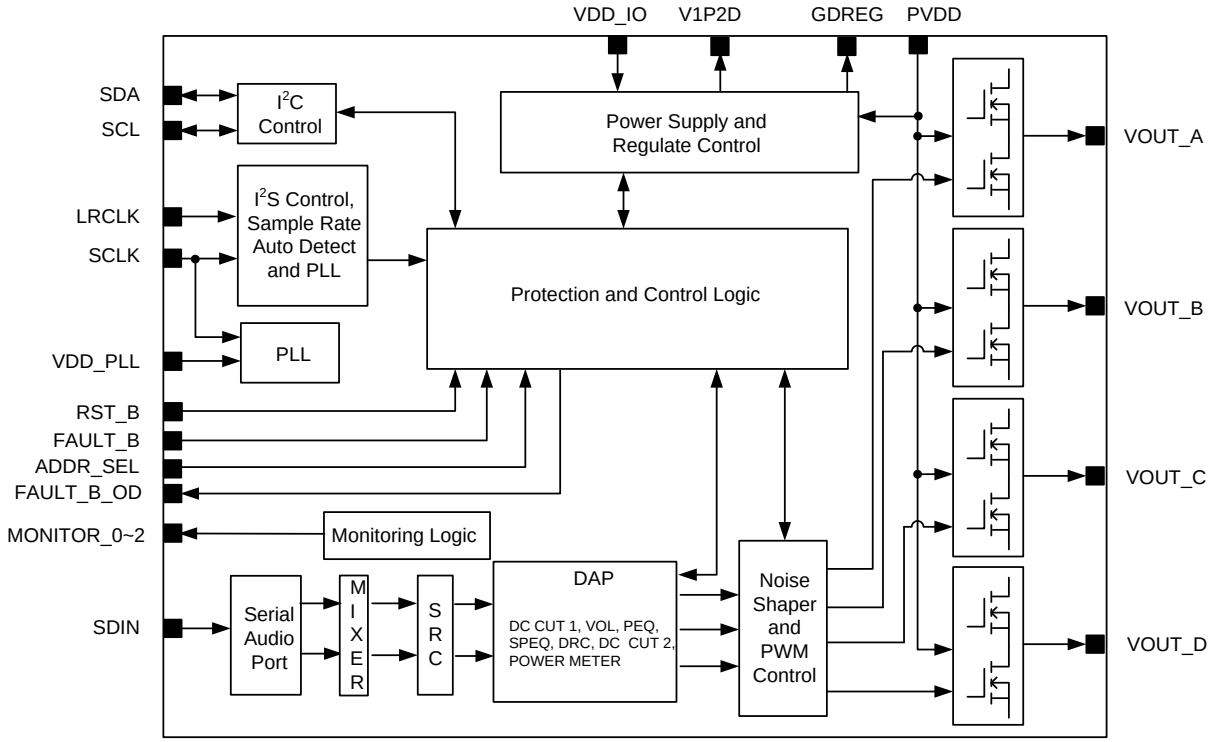


Figure2a. Block Diagram

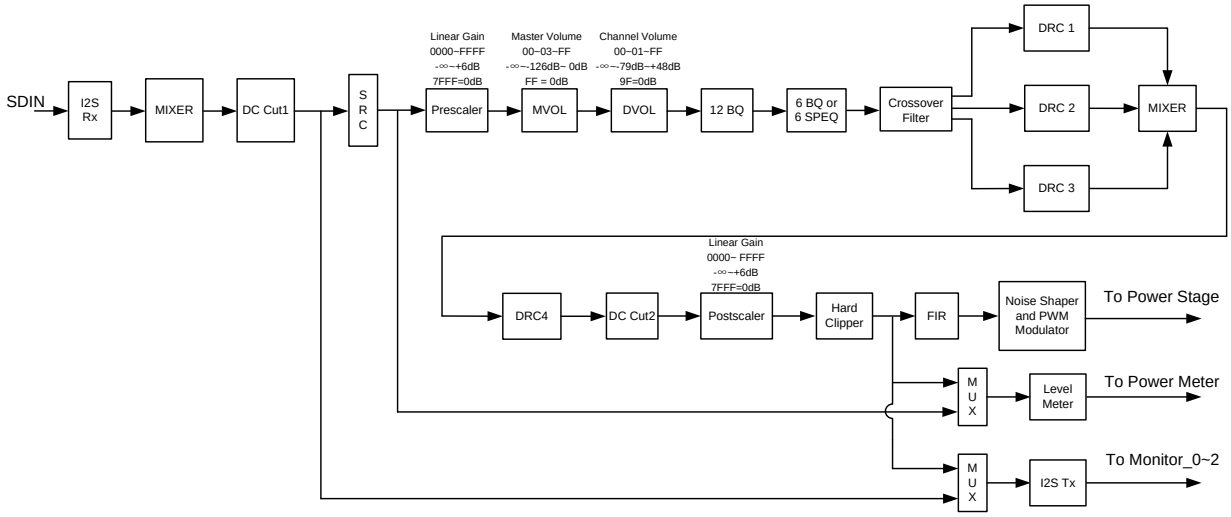


Figure2b. DAP Process Structure

Absolute Maximum Ratings (Note 1)

VDD_IO, Power Supply for Digital Interface I/O ---------- -0.3V to 3.6V
PVDD, Half-bridge Supply Voltage (Note 2) ---------- -0.3V to 30V
Digital Input ---------- -0.5V to (VDD_IO+0.5) V
VOUT_x ---------- 30V
GDREG ---------- -0.5V to 4V
VBS_x to VOUT_x ---------- -0.5V to 4V
Package Thermal Resistance (Note 3)
θ_{JA} ---------- 23°C/W
θ_{JC} (top) ---------- 15°C/W
θ_{JC} (bottom) ---------- 3°C/W
θ_{JB} ---------- 10.5°C/W
Junction Temperature Range ---------- 0°C to 150°C
Storage Temperature Range ---------- -40°C to 125°C

Recommended Operating Conditions

VDD_IO, Power Supply for Digital Interface I/O ---------- 3.3V
PVDD, Half-bridge Supply Voltage ---------- 4.5V to 28V
$R_{L(BTL)}$, Load Impedance(BTL) ---------- 8Ω
$R_{L(PBTL)}$, Load Impedance(PBTL) ---------- 4Ω
Operating Ambient Temperature Range ---------- 0°C to 85°C
Operating Junction Temperature Range ---------- 0°C to 125°C

PWM Operation Conditions

Parameter	Test Conditions	Value	Unit
Output Sample Rate	44.1kHz data rate	352.8	kHz
	32/48/96kHz data rate	384	

Electrical Characteristics

DC Characteristics

(T_A=25°C, PVDD_x=18V, VDD_IO=3.3V, R_L=8Ω, BTL Ternary Mode, f_S=48 kHz, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PVDD	Half-bridge Supply Voltage		4.5		28	V
VDD_IO	Power Supply for Digital Interface I/O		3		3.6	V
GDREG	Gate Drive Supply		3.2		3.4	V
V_{IH}	High Level Input Voltage	TEST, SDIN, LRCLK, SDA, SCL, FAULT_B, RST_B, ADDR_SEL, SCLK	2			V
V_{IL}	Low Level Input Voltage	TEST, SDIN, LRCLK, SDA, SCL, FAULT_B, RST_B, ADDR_SEL, SCLK			0.8	V
I_{IL}	Low Level Input Current	TEST, SDIN, LRCLK, SDA, SCL, FAULT_B, RST_B, ADDR_SEL, SCLK			75	μA
I_{IH}	High Level Input Current	TEST, SDIN, LRCLK, SDA, SCL, FAULT_B, RST_B, ADDR_SEL, SCLK			75	μA
I_{VDD_IO}	3.3V Supply Current	No Input, No Load		11.4		mA
		Reset(RST_B = low, FAULT_B = high)		0.75		
I_{PVDD}	No Load, Half-bridge Supply Current (Without Snubber)	Normal		23.6		mA
		Reset(RST_B = low, FAULT_B = high)		1.3		
Power MOSFET						
$R_{DS(ON)}$	High Side Drain-to-source Resistance	T_j=25°C, includes metallization resistance		110		mΩ
	Low Side Drain-to-source Resistance			110		mΩ
Load Diagnostics						
OLDT	Open-load detection threshold	Including speaker wires		100		Ω
SLDT	Short-load detection threshold	Including speaker wires		1.5		
	Resistance to detect a short from OUT pin(s) to ground				100	
	Voltage to detect a short from output pin(s) to power supply		5.5			V
Protection						
V_{UVP}	PVDD Falling			3.4		V
	PVDD Rising			4		
OVTP	Over Temperature Protection			150		°C
$OVTP_{HYST}$	Over Temperature Protection Hysteresis			30		°C
I_{OVC}	Over Current Protection			7.5		A

AC Characteristics (Note 4)

(T_A=25°C, C_{VBS}=22nF, Audio frequency=1kHz, f_S=48kHz, AES17 filter, Snubber=10Ω+1nF, BTL ternary mode, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Speaker Amplifier						
P_o	Output Power	BTL Mode, PVDD=12V, R_L=8Ω, 1%THD+N		8.1		W
		BTL Mode, PVDD=12V, R_L =8Ω, 10%THD+N		10.0		
		BTL Mode, PVDD=12V, R_L=6Ω, 1%THD+N		10.1		
		BTL Mode, PVDD=12V, R_L=6Ω, 10%THD+N		12.5		
		BTL Mode, PVDD=13.2V, R_L=6Ω, 1%THD+N		12.3		
		BTL Mode, PVDD=13.2V, R_L=6Ω,10%THD+N		15.2		
		BTL Mode, PVDD=18V, R_L=8Ω, 1%THD+N		18.2		
		BTL Mode, PVDD=18V, R_L=8Ω, 10%THD+N		22.4		
		BTL Mode, PVDD=18V, R_L=6Ω, 1%THD+N		22.9		
		BTL Mode, PVDD=18V, R_L=6Ω, 10%THD+N		28.1		
		BTL Mode, PVDD=24V, R_L=8Ω, 1%THD+N		32.2		
		BTL Mode, PVDD=24V, R_L=8Ω, 10%THD+N		39.5		
		PBTL Mode, PVDD=12V, R_L=4Ω,1%THD+N		16.2		
		PBTL Mode, PVDD=12V, R_L=4Ω,10%THD+N		20.0		
		PBTL Mode, PVDD=18V, R_L=4Ω,1%THD+N		36.4		
		PBTL Mode, PVDD=24V, R_L=4Ω,1%THD+N		64.2		
THD+N	Total Harmonic Distortion and Noise	PVDD=12V , R_L=8Ω , P_O=1W		0.035		%
		PVDD=13.2V , R_L=6Ω , P_O=1W		0.044		
		PVDD=18V , R_L=8Ω , P_O=1W		0.026		
		PVDD=20V , R_L=6Ω , P_O=1W		0.033		
		PVDD=24V , R_L=8Ω , P_O=1W		0.030		
V_n	Output Integrated Noise (rms)	PVDD=18V, R_L=8Ω, A-weighted		73.4		μV
CT	Crosstalk	PVDD=20V, P_o=1W , f =1kHz		79.6		dB
SNR	Signal to Noise Ratio	PVDD=20V, A-weighted, f=1kHz , Maximum power at THD+N <1%,		101.3		

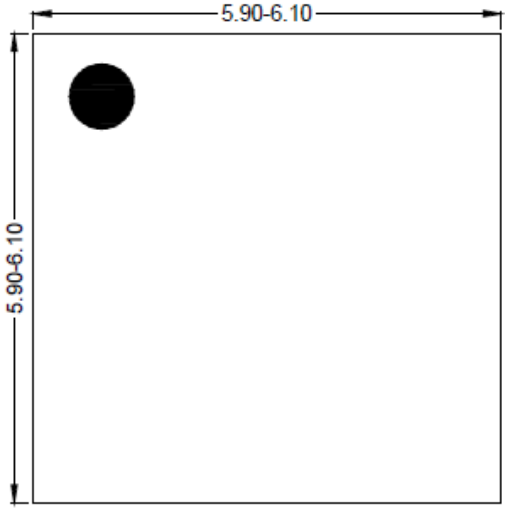
Note 1: Stresses beyond the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect the device reliability.

Note 2: DC voltage rating could be derated a little according to the possible switching spike on the switching node if the snubber is not appropriate enough.

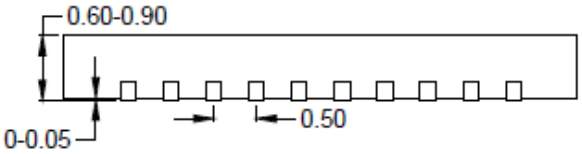
Note 3: θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective four-layer thermal conductivity test board of JEDEC 51-7.

Note 4: Typical value tested on demonstration board is guaranteed by design.

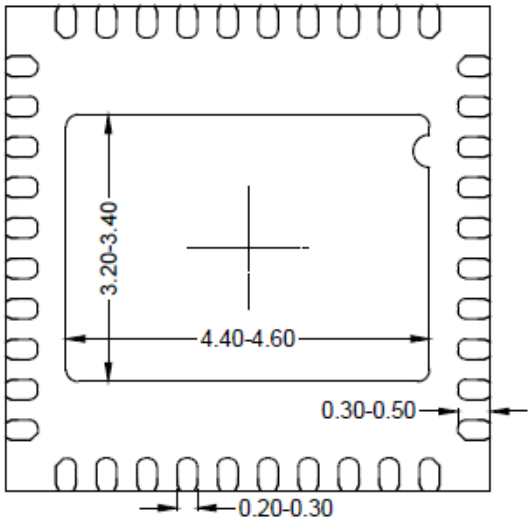
QFN6×6-40 Package Outline



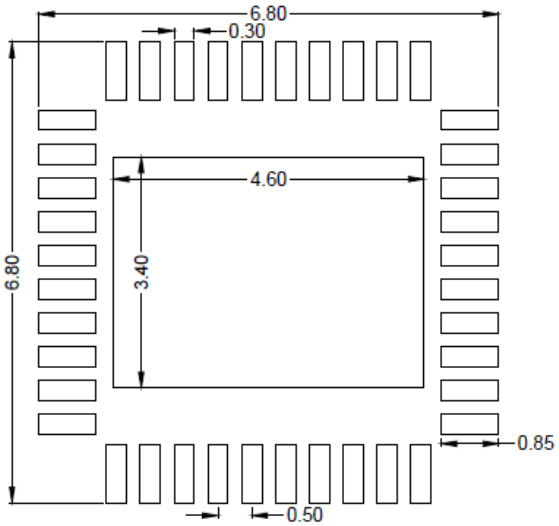
Top view



Side view



Bottom View



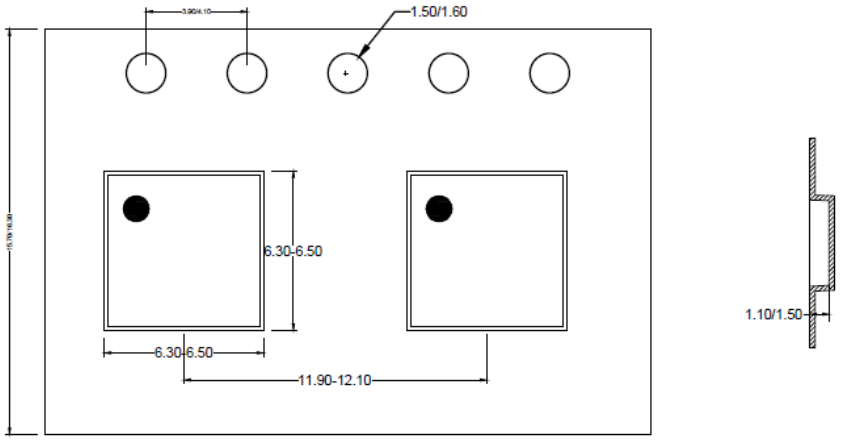
Recommended PCB Layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

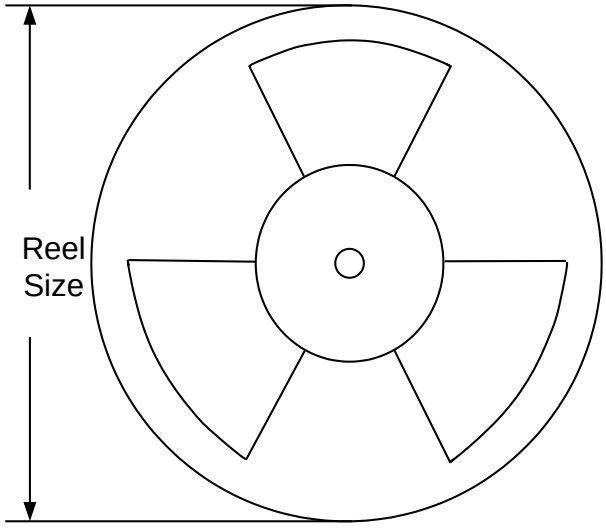
1. Taping orientation

QFN6×6



Feeding direction

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN6×6	16	12	13"	400	400	2500

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
May 30, 2023	Revision 1.0	Production Release
May 30, 2022	Revision 0.9A	Add the content of package thermal resistance.
Sept.6, 2021	Revision 0.9	Initial Release

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