SY20823

Dual Channel 4A, Ultra Low Loss Load Switch

General Description

The SY20823 is a dual 4A ultra-low loss load switch designed for intelligent power distribution in computers or portable electronics. The programmable turn-on delay facilitates proper power sequencing during mode transitions, while the programmable ramp-up time limits inrush current. Integrated over-temperature and short circuit protection enhance overall system reliability.

The SY20823 is available in a compact DFN 2mm x 2mm package.

Features

- Low $R_{DS(ON)}$ for internal MOSFETs: 28mΩ
- Maximum output current per channel: 4A
- Distribution voltages: 0.6V-BIAS
- Accurate turn-on threshold to allow programmable turn-on delay to enable power sequencing
- Programmable ramp-up time
- Latch mode overtemperature protection
- Latch mode short circuit protection
- Automatic shutdown discharge: 210Ω
- Compact: DFN2x2-8

Applications

- Notebook, Tablet, Desktop, and Net PCs
- Servers
- Set Top Boxes
- E-Book or MIDs
- Smart TVs
- Routers
- Industrial PCs

Typical Application

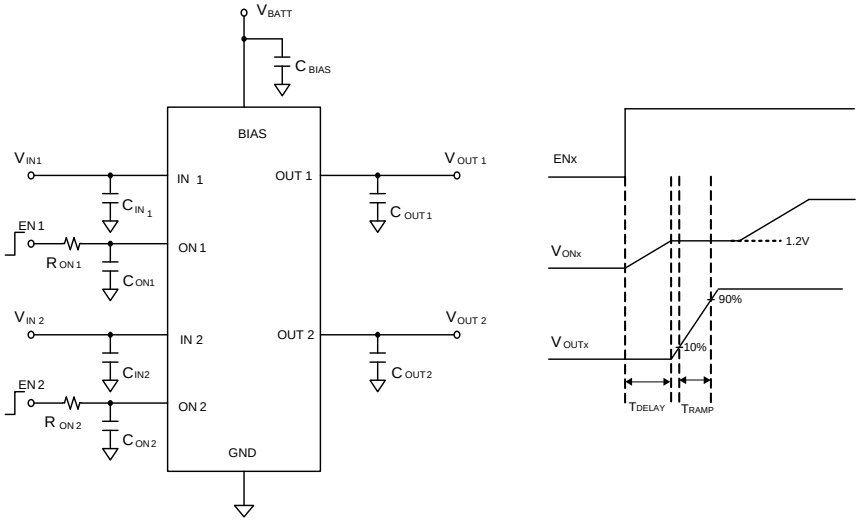

Figure 1. Schematic Diagram

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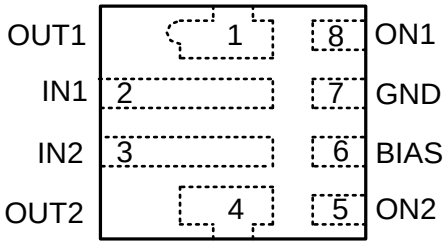
Ordering Information

Ordering Number	Package Type	Top Mark
SY20823DFC	DFN2x2-8 RoHS Compliant and Halogen Free	**WP*xyz***

Device code: WP
x=year code, y=week code, z= lot number code

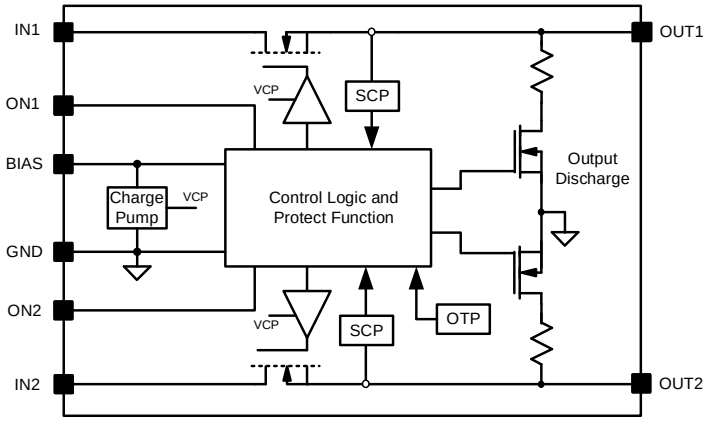
Pinout (Top View)



(DFN2x2-8)

Pin Name	Pin Number	Pin Description
IN1	2	Input pin for channel 1.
IN2	3	Input pin for channel 2.
GND	7	Ground pin
OUT1	1	Output pin for channel 1.
OUT2	4	Output pin for channel 2.
ON1	8	ON/OFF control pin for channel 1. Connect this pin to the RC circuit (as shown in Figure 1) to control the ramp-up time and turn on delay. The ramp-up time is controlled by R_{ON1}, and the delay is programmable by C_{ON1} and R_{ON1}.
ON2	5	ON/OFF control pin for channel 2. Connect this pin to the RC circuit (as shown in Figure 1) to control the ramp-up time and turn on delay. The ramp-up time is controlled by R_{ON2}, and the delay time is programmable by C_{ON2} and R_{ON2}.
BIAS	6	Device power supply input. Decouple this pin to the ground with at least 1uF MLCC.

Block Diagram



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Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
All pins		6	V
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10sec.)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	62.5	°C/W
θ_{JC} Junction-to-case Thermal Resistance	10	
P_D Power Dissipation T_A=25°C	2	W

ESD Susceptibility

Parameter	Min	Max	Unit
HBM (Human Body Mode)		2	kV
MM (Machine Mode)		200	V

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN, OUT	0.6	BIAS	V
BIAS	2.5	5.5	
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

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Electrical Characteristics

(V_{BIAS}=5V, V_{IN} = 5V, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		0.6		V_{BIAS}	V
Bias Voltage Range	V_{BIAS}		2.5		5.5	V
Bias current	I_{BIAS}	ON=3.3V, I_{OUT}=0		100		μA
Shutdown Bias Current	I_{SHDN}	ON=0			1	μA
FET R_{ON}	$R_{DS(ON)}$	I_{OUT}=1A		28		mΩ
ON clamping threshold	$V_{ON, CLP}$	R_{ON}=50k	1.1	1.2	1.3	V
BIAS UVLO Threshold	$V_{BIAS, UVLO}$				2.4	V
BIAS UVLO Hysteresis	$V_{BIAS, HYS}$			0.1		V
Output Discharge Resistance	R_{DIS}	ON=0		210		Ω
Adjustable Ramp Up Time Range		R_{ON} = 50k to 1Meg, Control Signal = 3.3V	0.5		10	ms
Minimum Turn On Delay Time	t_{DLY}			200		μs
Thermal Shutdown Temperature	T_{SD}			150		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

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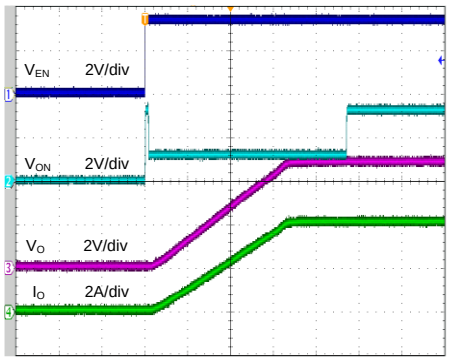
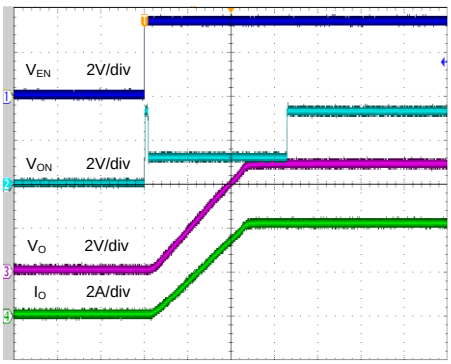
Typical Performance Characteristics

Startup from Enable
(V_{IN}=5V, V_{BIAS}=5V,EN=3.3V,I_{OUT}=4A,R_{ON}=300kΩ,C_{ON}=Null)



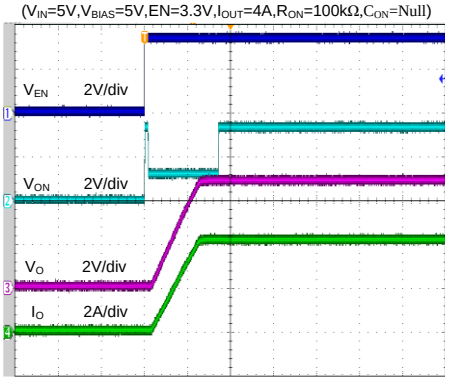
Time (1ms/div)

Startup from Enable
(V_{IN}=5V,V_{BIAS}=5V,EN=3.3V,I_{OUT}=4A,R_{ON}=200kΩ,C_{ON}=Null)



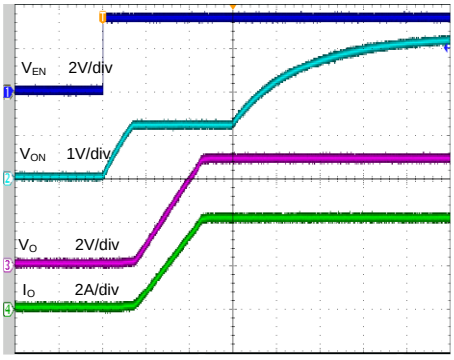
Time (1ms/div)

Startup from Enable
(V_{IN}=5V,V_{BIAS}=5V,EN=3.3V,I_{OUT}=4A,R_{ON}=100kΩ,C_{ON}=Null)



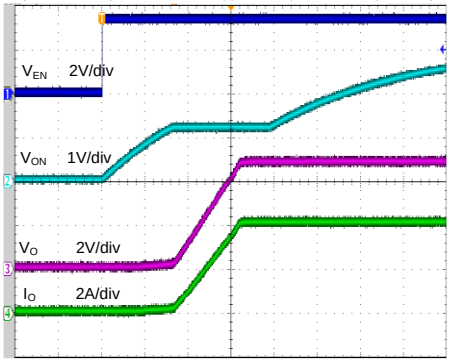
Time (1ms/div)

Startup from Enable
(V_{IN}=5V,V_{BIAS}=5V,EN=3.3V,I_{OUT}=4A,R_{ON}=300kΩ,C_{ON}=10nF)



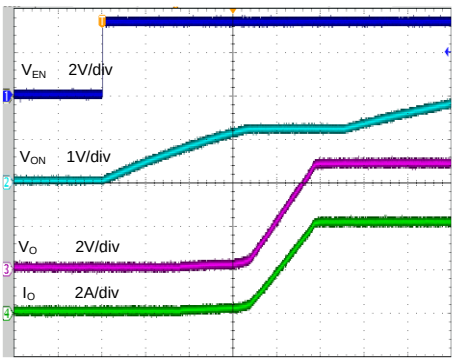
Time (2ms/div)

Startup from Enable
(V_{IN}=5V,V_{BIAS}=5V,EN=3.3V,I_{OUT}=4A,R_{ON}=300kΩ,C_{ON}=20nF)



Time (2ms/div)

Startup from Enable
(V_{IN}=5V,V_{BIAS}=5V,EN=3.3V,I_{OUT}=4A,R_{ON}=300kΩ,C_{ON}=30nF)



Time (2ms/div)

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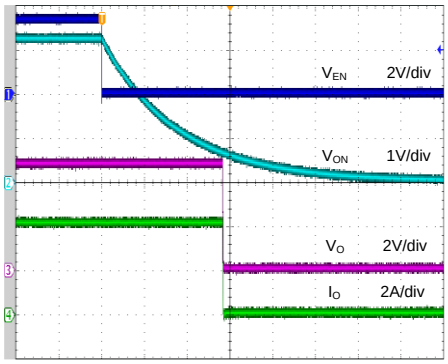
Shutdown from Enable

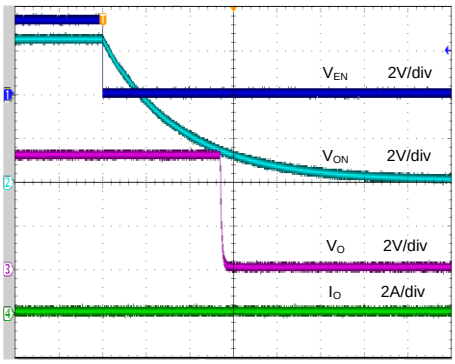
(V_{IN}=5V,V_{BIAS}=5V,EN=3.3V,I_{OUT}=4A,R_{ON}=300kΩ,C_{ON}=10nF)



Time (4ms/div)

Shutdown from Enable

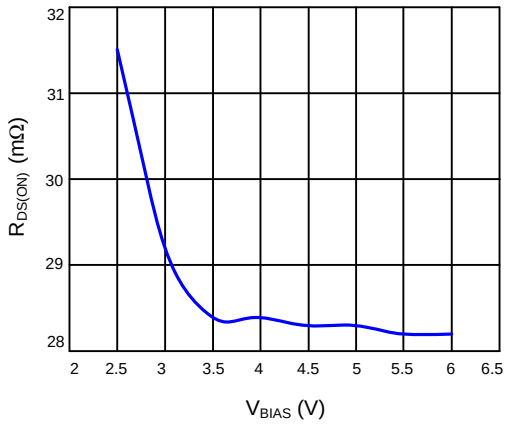
(V_{IN}=5V,V_{BIAS}=5V,EN=3.3V,I_{OUT}=0A,R_{ON}=300kΩ,C_{ON}=10nF)



Time (4ms/div)

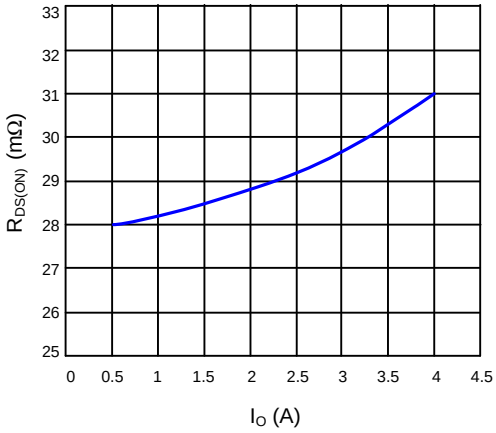
$R_{DS(ON)}$ vs. V_{BIAS}

(V_{IN}=2.5V, EN=3.3V, I_{OUT}=1A, R_{ON}=300kΩ, C_{ON}=10nF)



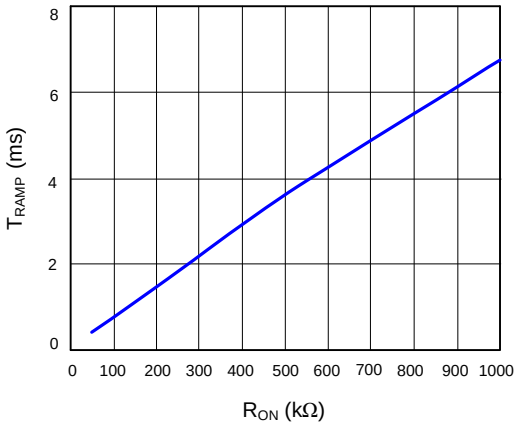
$R_{DS(ON)}$ vs. I_O

(V_{IN}=5V,V_{BIAS}=5V, EN=3.3V, R_{ON}=300kΩ, C_{ON}=10nF)



T_{RAMP} vs. R_{ON}

(V_{IN}=5V, V_{BIAS}=5V, EN=3.3V, I_{OUT}=4A, C_{ON}=10nF)



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Application Information

The SY20823 is a dual 4A, ultra-low loss load switch. The internal N-channel MOSFET bridge can support as high as 4A maximum continuous current over an input voltage range of 0.6V to V_{BIAS}. The turn on delay time and rise time can be programmed by R_{ON} and C_{ON} connected to the ON pin.

Supply Filter Capacitor:

It is recommended to place a 10μF ceramic capacitor close to the IN and GND pins. A higher value of C_{IN} can be used to further reduce the voltage drop during high current applications.

Bias Filter Capacitor:

A 1μF ceramic capacitor should be placed between the BIAS and GND pins to bypass the high-frequency noise of the bias supply.

Output Filter Capacitor:

A 10μF output ceramic capacitor is recommended to be placed close to the IC and output connector to reduce voltage drop during load transient. Higher values of C_{OUT} can be use to further reduce the voltage drop during high current application.

Output Turn-On Delay and Rise Slew Rate:

The turn-on delay time and rise time can be easily programmed using R_{ONx} and C_{ONx}. The delay time can be calculated using the following equation:

$$t_{Delay} = R_{ON} \times C_{ON} \times ln\left(\frac{V_{EN}}{V_{EN} - 1.2}\right)$$

The minimum delay time is 200μs.

The rise time slew rate can be calculated using the following equation:

$$SR = \frac{V_{EN} - 1.2}{R_{ON}} \times 0.23 \times 10^{9} \text{ (V/s)}$$

Where:

- V_{EN} is the control input voltage.
- The typical rise slew rate is 1.6V/ms when R_{ON}=300kΩ, V_{EN}=3.3V, V_{IN}=5V.

Output Discharge:

When the pass MOSFETs are off, 210Ω on-chip load resistors are connected to the outputs to quickly discharge the outputs.

Short Circuit Protection:

When V_{OUT} is lower than V_{IN}/3, a hard short condition is assumed. The device will latch off until the ON pin is reset for the respective channel.

PCB Layout Guide:

For best performance of the SY20823, the following guidelines must be strictly followed:

1. Keep all power traces as short and wide as possible. It's recommended to use a 2-layer or 4-layer board for thermal performance and better capability of current flow.
2. It is recommended to place a minimum of 6 vias around each power pin, including IN1, IN2, OUT1, and OUT2, to efficiently distribute current across different layers of the PCB.
3. Place the input capacitor close to the device, and the output capacitor close to the device and connectors for better transient performance.
4. Place the bias capacitor close to the device to reduce the noise on the bias supply.

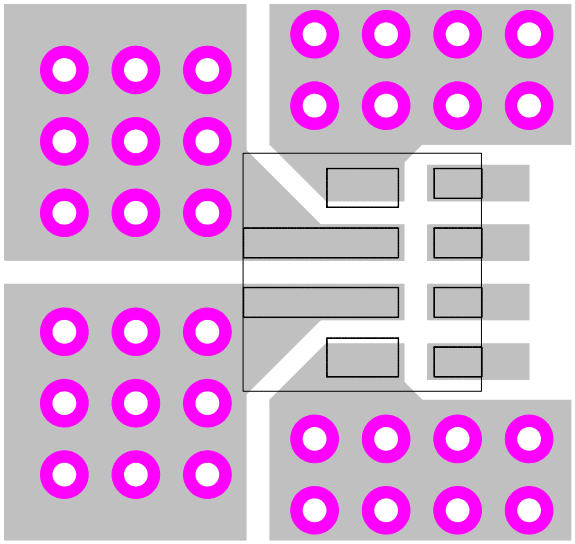

Figure 3. PCB Layout Suggestion

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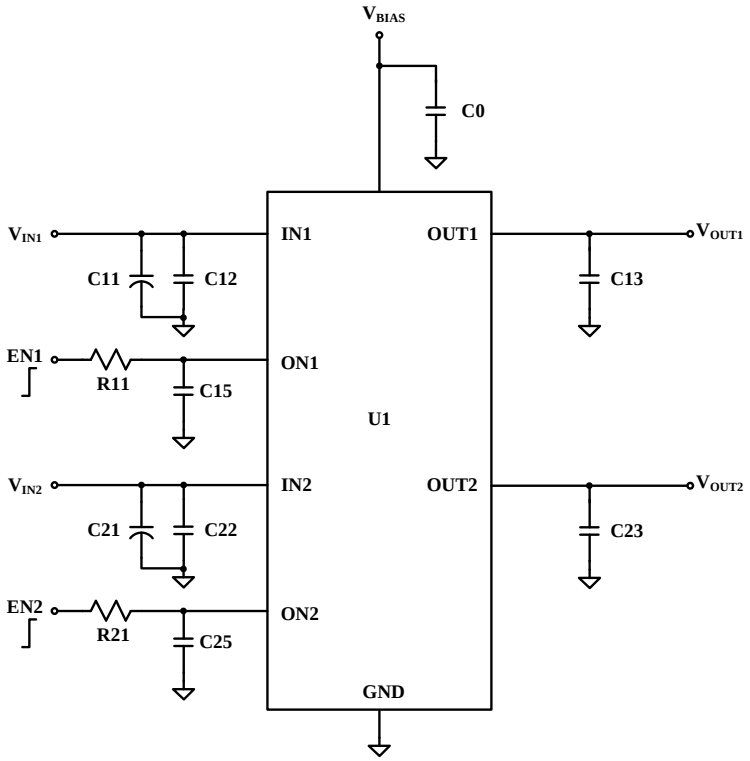
Schematic



BOM List

Reference Designator	Description	Part Number	Manufacturer
U1	Ultra Low Loss Load Switch	SY20823DFC	Silergy
C0	1uF/10V, 0603, X7R		TDK
C11, C21	NA		
C12, C13, C22, C23	10uF/6.3V, 0805, X7R	C2012X7R0J226M	TDK
C15, C25	10nF/10V, 0603, X7R	C1608X7R1H103K	TDK
R11, R21	300kΩ, 1%, 0603		

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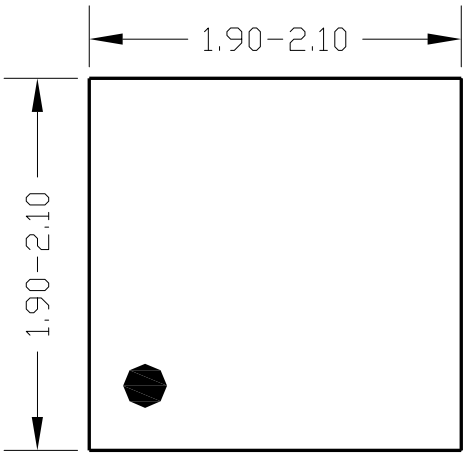
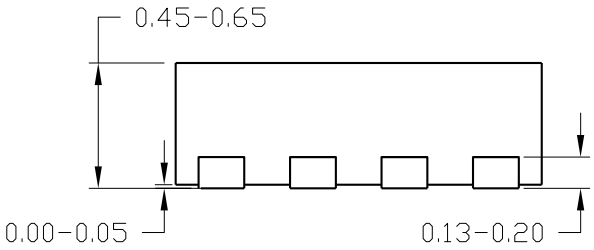
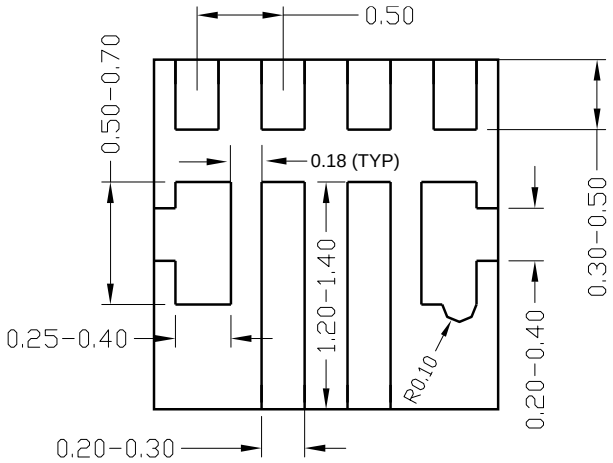
DFN2x2-8 Package Outline



Top View



Side View



Bottom View

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

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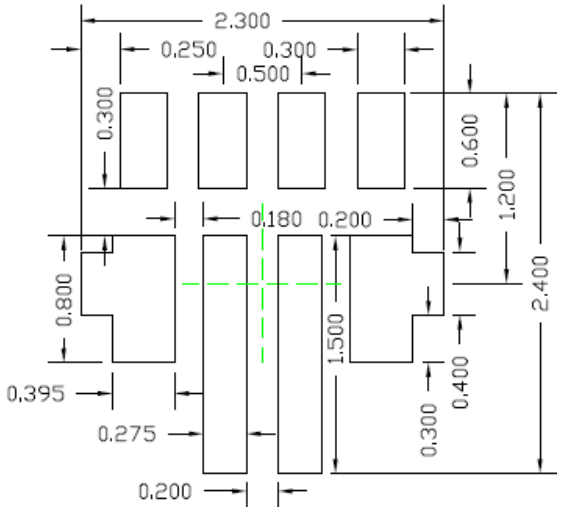
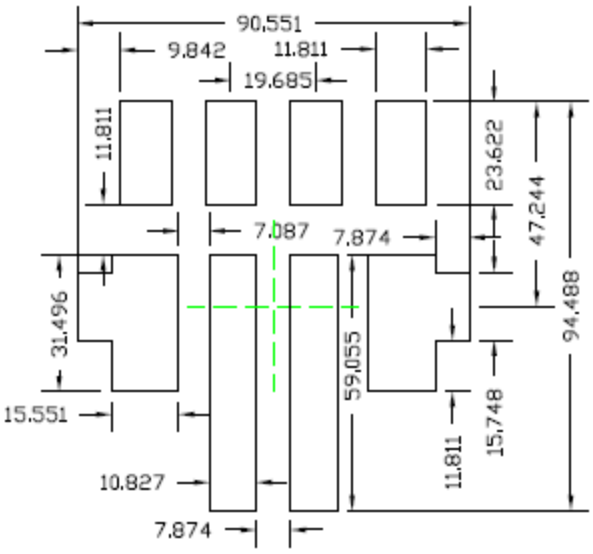


Recommended PCB Layout in Metric Units



Recommended PCB Layout in Imperial Units (mil)

Notes: All dimensions in mm except the PCB layout in Imperial units (mil).
All dimensions do not include mold flash & metal burr.

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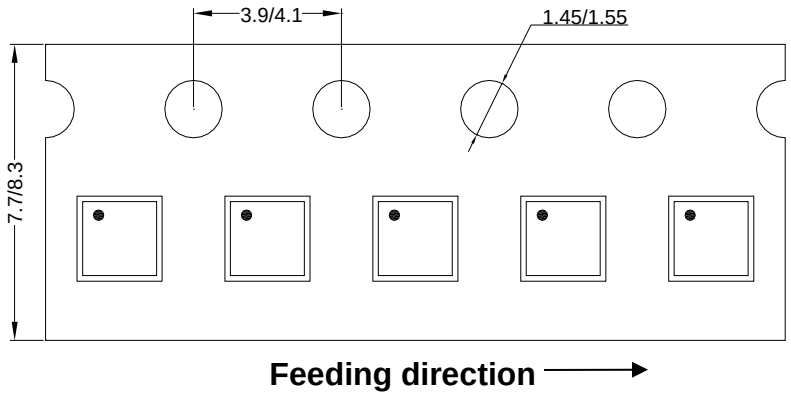
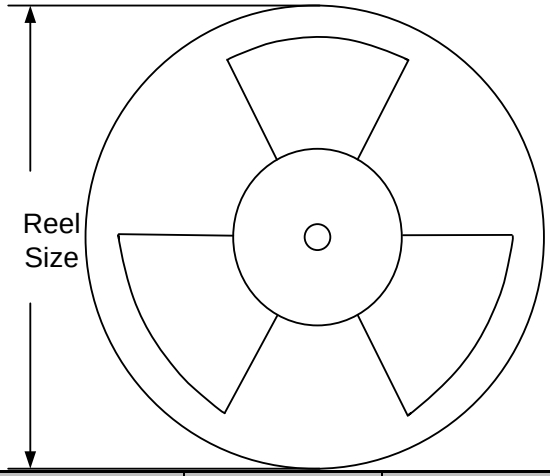
Taping & Reel Specification

DFN2x2-8 Taping Orientation



Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN2x2	8	4	7"	400	160	3000

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Mar.20, 2024	Revision 1.0	Language improvements for clarity
Apr.10, 2014	Revision 0.9	Initial Release

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