SY22686B

Flyback Regulator For LED Lighting

General Description

The SY22686B is a Flyback regulator targeting at LED lighting applications.

It integrates a 600V MOSFET to decrease physical volume. It is a primary side controller without applying any secondary feedback circuit for low cost, and drives the Flyback converter in the quasi-resonant mode to achieve higher efficiency. Proprietary self-bias technique saves the bias supply and reduces the startup time.

It integrates open/short LED protection and eliminates the need for opto-coupler or auxiliary winding, thus minimizing the component count and board size.

Features

- Integrated 600V MOSFET
- Quasi-Resonant (QR) mode to achieve low switching losses
- Primary side control to eliminate the opto-coupler
- Fast Startup (<300ms)
- No auxiliary winding for feedback
- Reliable short LED and open LED protection
- RoHS Compliant and Halogen Free
- Compact package: SOT23-5

Ordering Information

SY22686□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY22686BAAC	SOT23-5	----

Applications

- LED lighting

Recommended operating output power		
Products	90~132Vac	176~264Vac
SY22686B	4.5W	7W

Typical Applications

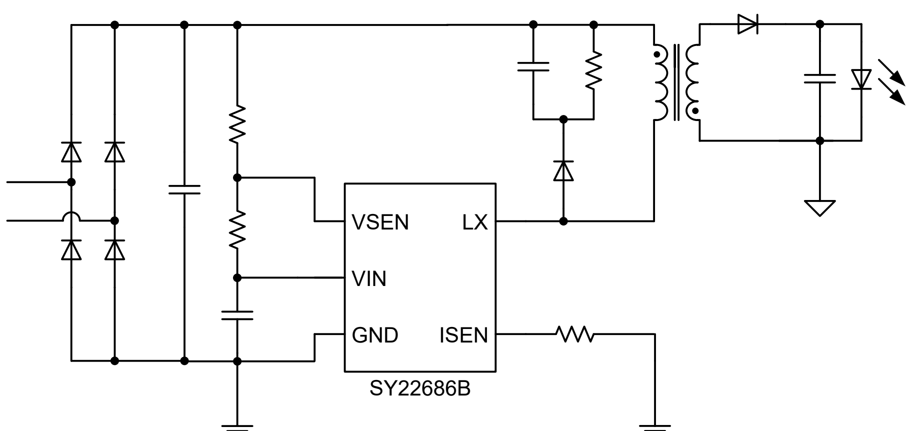
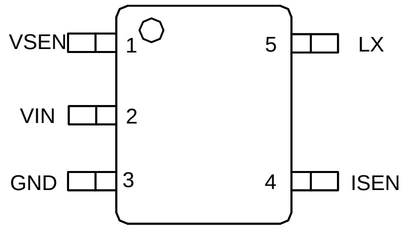


Fig.1 Schematic Diagram

Pinout (top view)



(SOT23-5)

Top Mark: Gq*xyz* (device code: Gq, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin number	Pin Description
VSEN	1	Voltage sense pin. Connect to a resistor divider from Bus to VIN to decide OVP threshold.
VIN	2	Power supply pin.
GND	3	Ground Pin.
ISEN	4	Current sense pin. Connect a resistor to program the reference output current. $I_O = \frac{V_{REF} \times N_{PS}}{2 \times R_S}$
LX	5	Internal HV MOSFET drain pin.

Absolute Maximum Ratings (Note 1)

ISEN -- -0.3V~3.6V
VIN, VSEN -- -0.3V~19V
I_{VIN}-- 20mA
LX-- 600V
Power Dissipation, @ TA = 25°C SOT23-5-- 0.6W
Package Thermal Resistance (Note 2)
SOT23-5, θ_{JA}-- 170°C/W
SOT23-5, θ_{JC}-- 130°C/W
Maximum Junction Temperature -- 150°C
Lead Temperature (Soldering, 10 sec.) -- 260°C
Storage Temperature Range -- -65°C to 150°C

Recommended Operating Conditions

Junction Temperature Range -- -40°C to 125°C

Block Diagram

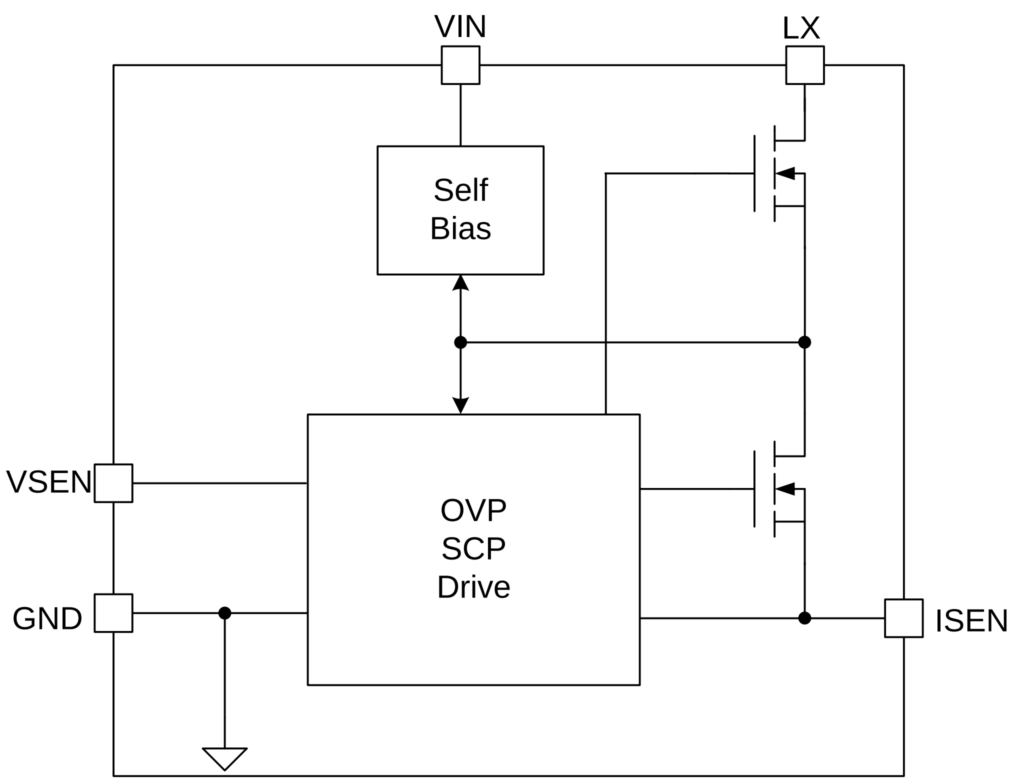


Fig.2 Simplified block diagram

Electrical Characteristics

(V_{VIN}= 12V(Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VIN turn-on threshold	$V_{VIN,ON}$			14		V
VIN turn-off threshold	$V_{VIN,OFF}$			7.6		V
Start up current	I_{ST}			2	5	μA
VSEN pin Section						
VSEN pin reference voltage	$V_{VSEN,OVP}$			160		mV
Driver Section						
Min ON Time	$t_{ON,MIN}$			400		ns
Max ON Time	$t_{ON,MAX}$			30		μs
Min OFF Time	$t_{OFF,MIN}$			2		μs
Max OFF Time	$t_{OFF,MAX}$			120		μs
Max switching frequency	f_{MAX}			180		kHz
ISEN pin Section						
Current limit threshold voltage	$V_{ISEN,OCP}$			800		mV
Current reference	V_{REF}		294	300	306	mV
Integrated MOSFET Section						
BV of HV MOSFET	V_{BV}		600			V
Thermal Section						
Thermal Shutdown Temperature	T_{SD}			150		ºC
Thermal Fold back Temperature	T_{FB}			140		ºC

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2” x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: Increase VIN pin voltage gradually higher than $V_{VIN,ON}$ voltage then turn down to 12V.

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Operation

SY22686B is a constant current Flyback regulator targeting at LED lighting applications.

The device provides primary side control to eliminate the opto-couplers or the secondary feedback circuits, which would cut down the cost of the system.

In order to reduce the switching losses and improve EMI performance, Quasi-Resonant switching mode is applied, which means to turn on the power MOSFET at valley of drain voltage.

Proprietary self-bias and OVP technique eliminates the need for auxiliary winding thus minimizes the PCB footprint and associated power loss.

Short Circuit Protection works in hiccup mode. The resulting short circuit power loss is much less than continuous working mode.

SY22686B also provides reliable protections such as Open LED Protection (OLP), Over Temperature Protection (OTP), etc.

SY22686B is available with SOT23-5 package.

Applications Information

Start up

After AC supply or DC BUS is powered on, the capacitor C_{VIN} across VIN and GND pin is charged up by BUS voltage through resistor R_{ST} and R_{OVP}(R_{ST} >> R_{OVP}). Once V_{VIN} rises up to $V_{VIN,ON}$, the internal blocks starts to work. Then IC can be supplied at every switching cycle. The supply current is balanced with IC consumption current to maintain V_{VIN} above $V_{VIN,OFF}$.

The whole start up procedure is divided into two sections shown in Fig.3. t_{STC} is the C_{VIN} charged up section, and t_{STO} is the time V_{VIN} falls to a steady state value. Usually t_{STO} is much smaller than t_{STC}.

If bias supply has more power than IC consumption, V_{VIN} is greater than $V_{VIN,Shunt}$, then a shunt current works to maintain V_{VIN} under $V_{VIN,Shunt}$.

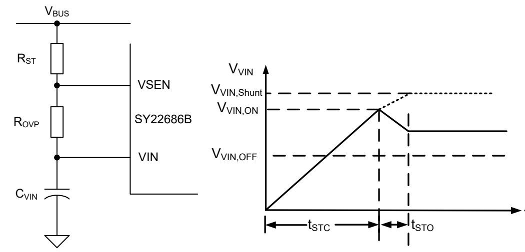


Fig.3 Start up

The start up resistor R_{ST} and C_{VIN} are designed by rules below(R_{OVP} is great smaller than R_{ST} thus it's ignored in start-up section):

(a) Preset start-up resistor R_{ST}, make sure that the current through R_{ST} is larger than I_{ST} .

$$R_{ST} < \frac{V_{BUS}}{I_{ST}} \quad (1)$$

Where V_{BUS} is the BUS line voltage.

(b) Select C_{VIN} to obtain an ideal start up time t_{ST}.

$$C_{VIN} = \frac{(\frac{V_{BUS}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}} \quad (2)$$

(c) If R_{ST} and C_{VIN} are chosen to get a very short start up time, SCP and OVP power loss will be large. Then C_{VIN} and R_{ST} time constant should be increased.

Proprietary self-bias technique allows C_{VIN} to be charged in every switching cycle. There is no need to add auxiliary winding for power supply. C_{VIN} can be chosen with small value and small package to save cost.

Shut down

After AC supply or DC BUS powered off, the energy stored in the BUS capacitor is discharged. When power supply for IC is not enough, V_{VIN} drops down. Once V_{VIN} is below $V_{VIN,OFF}$, the IC stops working.

Primary-side constant-current control

Primary side control is applied to eliminate secondary feedback circuit or opto-coupler, which reduces the circuit cost. The switching waveforms are shown in Fig.4.

The output current I_{OUT} can be represented by,

$$I_{OUT} = \frac{I_{SP}}{2} \times \frac{t_{DIS}}{t_S} \quad (3)$$

Where I_{SP} is the peak current of the secondary side; t_{DIS} is the discharge time of Flyback transformer; t_S is the switching period.

The secondary peak current is related with primary peak current, if the effect of the leakage inductor is neglected.

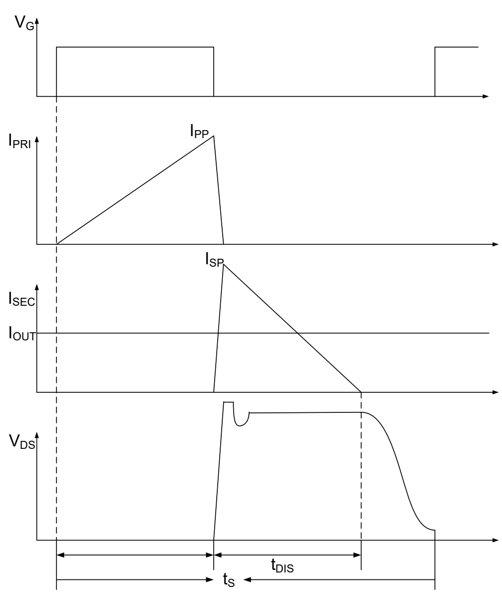


Fig.4 switching waveforms

$$I_{SP} = N_{PS} \times I_{PP} \quad (4)$$

Where N_{PS} is the turns ratio of primary to secondary of the Flyback transformer. Thus, I_{OUT} can be represented by

$$I_{OUT} = \frac{N_{PS} \times I_{PP}}{2} \times \frac{t_{DIS}}{t_S} \quad (5)$$

The primary peak current I_{PP} is detected by ISEN pin, and inductor current discharge time t_{DIS} is detected by internal circuit, which is shown in Fig.5. These singals are processed and applied to the negative input of the gain modulator. In static state, the positive and negative inputs are equal.

$$V_{REF} = I_{PP} \times R_S \times \frac{t_{DIS}}{t_S} \quad (6)$$

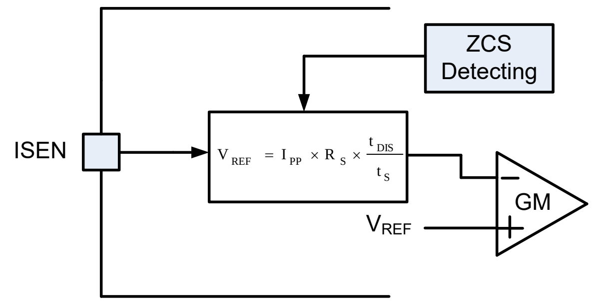


Fig.5 Output current detection diagram

Finally, the output current I_{OUT} can represented by

$$I_{OUT} = \frac{V_{REF} \times N_{PS}}{R_S \times 2} \quad (7)$$

Where V_{REF} is the internal reference voltage; R_S is the current sense resistor. I_{OUT} can be programmed by N_{PS} and R_S.

$$R_S = \frac{V_{REF} \times N_{PS}}{I_{OUT} \times 2} \quad (8)$$

Over Voltage Protection (OVP) & Open LED Protection (OLP)

When the load is null or large transient happens, the output voltage will exceed the rated value.

The resistor divider composed by R_{ST} and R_{OVP} is related with the OVP function.

$$V_{OVP} = \frac{R_{ST} + R_{OVP}}{R_{OVP}} \frac{V_{VSEN,OVP}}{N_{PS}} \quad (9)$$

Where V_{OVP} is the output over voltage specification, $V_{VSEN,OVP}$ is internal OVP reference.

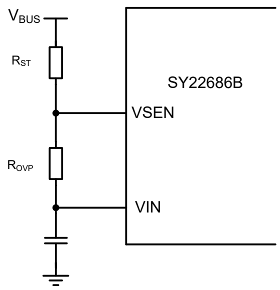


Fig.6 OVP&OLP

If over voltage protection triggered, the IC discharges V_{VIN} by an internal current source $I_{VIN,OVP}$. Once V_{VIN} is below $V_{VIN,OFF}$, the IC shuts down and be charged again by BUS voltage through start up resistor(R_{ST}). If the over voltage condition still exists, the system operates in hiccup mode.

Short Circuit Protection (SCP)

When the output is shorted, demagnetizing voltage of inductor is zero, so t_{OFF} is clamped at $t_{OFF,MAX}$, when $t_{OFF,MAX}$ lasts for 64 times, SCP is triggered and the IC discharges V_{VIN} by an internal current source $I_{VIN,SCP}$. Once V_{VIN} is below $V_{VIN,OFF}$, the IC shuts down and be charged again by BUS voltage through start up resistor. If the short circuit condition still exists, the system operates in hiccup mode.

Line regulation modification

The IC provides line regulation modification function to improve line regulation performance.

Due to the sample delay of ISEN pin and other internal delay, the output current increases with increasing input BUS line voltage. A small compensation voltage ΔV_{ISEN-C} is added to ISEN pin during ON time to improve such performance. This ΔV_{ISEN-C} is adjusted by the upper resistor of the divider connected to VSEN pin.

$$\Delta V_{ISEN,C}=\frac{(V_{BUS}-V_{VIN})}{R_{ST}}\times k_1 \qquad (10)$$

Where R_{ST} is the upper resistor of the divider; k_1 is an internal constant as the modification coefficient, $k_1=120$.

The compensation is mainly related with R_{ST}, larger compensation is achieved with smaller R_{ST}. Normally, R_{ST} ranges from 1.5MΩ~2.5MΩ.

Power Device Design

MOSFET and Diode

When the operation condition is with maximum input voltage and full load, the voltage stress of integrated MOSFET and secondary power diode is maximized;

$$V_{MOS,DS,MAX}=\sqrt{2}V_{AC,MAX}+N_{PS}(V_{OUT}+V_{D,F})+\Delta V_S \quad (11)$$

$$V_{D,R,MAX}=\frac{\sqrt{2}V_{AC,MAX}}{N_{PS}}+V_{OUT} \quad (12)$$

Where $V_{AC,MAX}$ is maximum input AC RMS voltage; N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the rated output voltage; $V_{D,F}$ is the forward voltage of secondary power diode; ΔV_S is the overshoot voltage clamped by RCD snubber during OFF time.

When the operation condition is with minimum input voltage and full load, the current stress of integrated MOSFET and power diode is maximized.

$$I_{MOS\_PK\_MAX}=I_{P\_PK\_MAX} \quad (13)$$

$$I_{MOS\_RMS\_MAX}=I_{P\_RMS\_MAX} \quad (14)$$

$$I_{D\_PK\_MAX}=N_{PS}\times I_{P\_PK\_MAX} \quad (15)$$

$$I_{D\_AVG}=I_{OUT} \quad (16)$$

Where $I_{P\text{-}PK\text{-}MAX}$ and $I_{P\text{-}RMS\text{-}MAX}$ are maximum primary peak current and RMS current, which will be introduced later.

Input capacitor C_{BUS}

Generally, the input capacitor C_{BUS} is selected by

C_{BUS} =1~3μF/W.

Or more accurately by,

$$C_{BUS}=\frac{\arcsin\left(\frac{V_{DC,MIN}}{\sqrt{2}V_{AC,MIN}}\right)+\frac{\pi}{2}}{2\pi f_{AC}V_{AC,MIN}^2\left(1-\left(\frac{V_{DC,MIN}}{\sqrt{2}V_{AC,MIN}}\right)^2\right)}\frac{P_O}{\eta} \quad (17)$$

Where $V_{DC,MIN}$ is the minimum voltage of BUS line, $V_{DC,MIN}$ usually equals 0.6~0.8 $\sqrt{2}V_{AC,MIN}$. f_{AC} is AC line frequency.

Transformer (N_{PS} and L_M)

N_{PS} is limited by the electrical stress of the internal power MOSFET:

$$N_{PS} \le \frac{V_{MOS,(BR)DS} \times 90\% - \sqrt{2}V_{AC,MAX} - \Delta V_S}{V_{OUT} + V_{D,F}} \quad (18)$$

Where $V_{MOS,(BR)DS}$ is the breakdown voltage of the integrated MOSFET.

In Quasi-Resonant mode, each switching period cycle t_S consists of three parts: current rising time t_1, current falling time t_2 and quasi-resonant time t_3 shown in Fig.7.

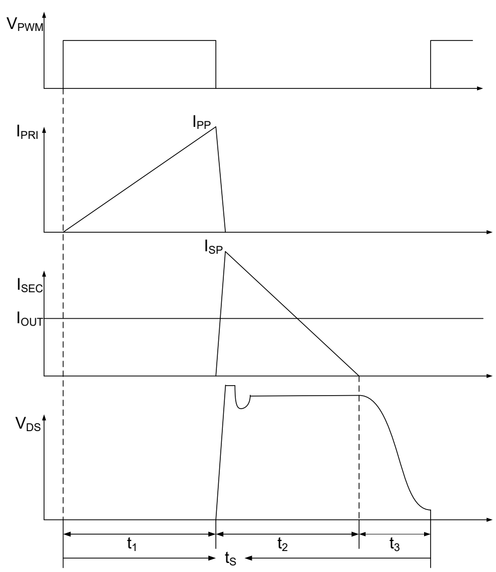


Fig.7 switching waveforms

The system operates in the peak current mode control. When the operation condition is with minimum input AC RMS voltage and full load, the ON time is maximized at valley of BUS voltage. Thus, the minimum switching frequency $f_{S,MIN}$ happens. Meanwhile, the maximum peak current through integrated MOSFET and the transformer happens.

Once the minimum frequency $f_{S,MIN}$ is set, the inductance of the transformer could be induced. The design flow is shown as below:

(a) Select N_{PS}

$$N_{PS} \le \frac{V_{MOS,(BR)DS} \times 90\% - \sqrt{2}V_{AC,MAX} - \Delta V_S}{V_{OUT} + V_{D,F}} \quad (19)$$

(b) Preset minimum frequency $f_{S,MIN}$

(c) Compute relative t_S, t_1 (t_3 is omitted to simplify the design here)

$$t_S = \frac{1}{f_{S,MIN}} \quad (20)$$

$$t_1 = \frac{t_S \times N_{PS} \times (V_{OUT} + V_{D,F})}{V_{DC,MIN} + N_{PS} \times (V_{OUT} + V_{D,F})} \quad (21)$$

(d) Design inductance L_M

$$L_M = \frac{V_{DC,MIN}^2 \times t_1^2 \times \eta}{2P_{OUT} \times t_S} \quad (22)$$

Where η is the efficiency; P_{OUT} is rated full load power.

(e) Compute t_3

$$t_3 = \pi \times \sqrt{L_M \times C_{drain}} \quad (23)$$

Where C_{Drain} is the parasitic capacitance at drain of integrated MOSFET.

(f) Compute primary maximum peak current $I_{P\text{-}PK\text{-}MAX}$ and RMS current $I_{P\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{P\_PK\_MAX} = \frac{P_{OUT}}{\eta} \times \left[\frac{1}{N_{PS}(V_{OUT} + V_{D,F})} + \frac{1}{V_{DC,MIN}}\right] + \sqrt{\left[\frac{P_{OUT}}{\eta} \times \left[\frac{1}{N_{PS}(V_{OUT} + V_{D,F})} + \frac{1}{V_{DC,MIN}}\right]\right]^2 + \frac{2P_{OUT}t_3}{L_M \eta}} \quad (24)$$

Adjust t_1 and t_S to t_1' and t_S' considering the effect of t_3.

$$t_S' = \frac{\eta \times L_M \times I_{P\_PK\_MAX}^2}{2P_{OUT}} \quad (25)$$

$$t_1' = \frac{L_M \times I_{P\_PK\_MAX}}{V_{DC,MIN}} \quad (26)$$

$$I_{P\_RMS\_MAX} = \sqrt{\frac{t_1'}{3t_S'}} \times I_{P\_PK\_MAX} \quad (27)$$

(g) Compute secondary maximum peak current $I_{S\text{-}PK\text{-}MAX}$ and RMS current $I_{S\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (28)$$

$$t_2' = t_S' - t_1' - t_3 \quad (33)$$

$$I_{S\_RMS\_MAX} = \sqrt{\frac{t_2'}{3t_S'}} \times I_{S\_PK\_MAX} \quad (29)$$

(h) Make sure that t_1', t_2' , t_3' are not out of the range given in EC table.

Transformer design (N_P,N_S,N_{AUX})

The design of the transformer is similar with ordinary Flyback transformer. the parameters below are necessary:

Necessary parameters	
Turns ratio	N_{PS}
Inductance	L_M
Primary maximum RMS current	$I_{P\text{-}RMS\text{-}MAX}$
Secondary maximum RMS current	$I_{S\text{-}RMS\text{-}MAX}$
Current limit voltage	$V_{ISEN,OCP}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e.

(b) Preset the maximum magnetic flux ΔB

$\Delta B = 0.3 \sim 0.33T$

(c) Compute primary turn N_P

$$N_P = \frac{L_M \times V_{ISEN,OCP}}{\Delta B \times A_e \times R_S} \quad (30)$$

(d) Compute secondary turn N_S

$$N_S = \frac{N_P}{N_{PS}} \quad (31)$$

(f) Select an appropriate wire diameter

With $I_{P\text{-}RMS\text{-}MAX}$ and $I_{S\text{-}RMS\text{-}MAX}$, select appropriate wire to make sure the current density ranges from $4A/mm^2$ to $10A/mm^2$.

(g) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

Output capacitor C_{OUT}

Output current ripple $\Delta I_{O,MAX}$ is,

$$\Delta I_O = \sqrt{I^2_{S\_RMS\_MAX} - I_O^2} \quad (32)$$

Choose proper output capacitor to satisfy current ripple.

RCD snubber for MOSFET

The power loss of the snubber P_{RCD} is evaluated first

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT} \quad (33)$$

Where N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the output voltage; $V_{D,F}$ is the forward voltage of the power diode; ΔV_S is the overshoot voltage clamped by RCD snubber; L_K is the leakage inductor; L_M is the inductance of the Flyback transformer; P_{OUT} is the output power.

The R_{RCD} is related with the power loss:

$$R_{RCD} = \frac{(N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S)^2}{P_{RCD}} \quad (34)$$

The C_{RCD} is related with the voltage ripple of the snubber $\Delta V_{C\text{-}RCD}$:

$$C_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{R_{RCD} f_S \Delta V_{C\_RCD}} \quad (35)$$

Thermal fold back design

If IC junction temperature rises over T_{FB}, the output current will be decreased to regulate the junction temperature around T_{FB}. If the junction temperature is over T_{SD}, IC will be shut down and won't recover unless the junction temperature drops below T_{FB}.

Design Example

A design example of typical application is shown below step by step.

#1. Identify design specification

Design Specification			
V_{AC}(RMS)	176V~264V	V_{OUT}	12V
I_{OUT}	350mA	η	85%

#2. Input Capacitor C_{BUS}

Conditions			
$V_{DC,MIN}$	150V	V_{AC-MIN}	176V
f_{AC}	50Hz		

$$C_{BUS}=\frac{\arcsin(\frac{V_{DC,MIN}}{\sqrt{2}V_{AC,MIN}})+\frac{\pi}{2}}{2\pi f_{AC}V_{AC,MIN}^2(1-(\frac{V_{DC,MIN}}{\sqrt{2}V_{AC,MIN}})^2)}\frac{P_O}{\eta}=\frac{\arcsin(\frac{150V}{\sqrt{2}\times 176V})+\frac{\pi}{2}}{2\pi\times 50\times 176V^2(1-(\frac{150V}{\sqrt{2}\times 176V})^2)}\frac{12V\times 0.35A}{0.85}=1.77\mu F$$

C_{BUS} is set to

$$C_{BUS}=2.2\mu F$$

#3. Transformer design (N_{PS}, L_M)

Refer to Power Device Design

Conditions			
$V_{DC,MIN}$	150V	V_{AC-MAX}	264V
$\triangle V_S$	50V	$V_{MOS-(BR)DS}$	600V
P_{OUT}	4.2W	$V_{D,F}$	1V
C_{Drain}	50pF	$f_{S,MIN}$	80kHz

(a) Compute turns ratio N_{PS} first

$$\begin{aligned}N_{PS}&\le\frac{V_{MOS\_(BR)DS}\times 90\%-\sqrt{2}V_{AC,MAX}-\Delta V_S}{V_{OUT}+V_{D,F}}\\&=\frac{600V\times 0.9-\sqrt{2}\times 264V-50V}{12V+1V}\\&=9\end{aligned}$$

N_{PS} is set to

$$N_{PS}=8$$

(b)$f_{S,MIN}$ is preset

$$f_{S,MIN}=80kHz$$

(c) Compute the switching period t_S and ON time t_1 at the peak of input voltage.

$$t_S = \frac{1}{f_{S,MIN}} = 12.5\mu s$$

$$\begin{aligned} t_1 &= \frac{t_S \times N_{PS} \times (V_{OUT} + V_{D,F})}{V_{DC,MIN} + N_{PS} \times (V_{OUT} + V_{D,F})} \\ &= \frac{12.5\mu s \times 8 \times 13V}{150V + 8 \times 13V} \\ &= 5.11\mu s \end{aligned}$$

(d) Compute the inductance L_M

$$\begin{aligned} L_M &= \frac{V_{DC,MIN}^2 \times t_1^2 \times \eta}{2P_{OUT} \times t_S} \\ &= \frac{150V^2 \times 5.11\mu s^2 \times 0.85}{2 \times 4.2 \times 12.5} \\ &= 4756\mu H \end{aligned}$$

Set $L_M = 4.5mH$

(e) Compute the quasi-resonant time t_3

$$\begin{aligned} t_3 &= \pi \times \sqrt{L_M \times C_{drain}} \\ &= \pi \times \sqrt{4.5mH \times 50pF} \\ &= 1.49\mu s \end{aligned}$$

(f) Compute primary maximum peak current $I_{P\text{-}PK\text{-}MAX}$

$$\begin{aligned} I_{P\_PK\_MAX} &= \frac{P_{OUT}}{\eta} \times \left[\frac{1}{N_{PS}(V_{OUT} + V_{D,F})} + \frac{1}{V_{DC,MIN}}\right] \\ &+ \sqrt{\left[\frac{P_{OUT}}{\eta} \times \left[\frac{1}{N_{PS}(V_{OUT} + V_{D,F})} + \frac{1}{V_{DC,MIN}}\right]\right]^2 + \frac{2P_{OUT}t_3}{L_M \eta}} \\ &= 0.178A \end{aligned}$$

Adjust switching period t_S and ON time t_1 to t_S' and t_1'.

$$\begin{aligned} t_S' &= \frac{\eta \times L_M \times I_{P\_PK\_MAX}^2}{2P_{OUT}} \\ &= \frac{0.85 \times 4.5mH \times 0.178A^2}{2 \times 4.2W} \\ &= 14.4\mu s \end{aligned}$$

$$\begin{aligned} t_1' &= \frac{L_M \times I_{P\_PK\_MAX}}{V_{DC,MIN}} \\ &= \frac{4.5mH \times 0.178A}{150V} \\ &= 5.34\mu s \end{aligned}$$

Compute primary maximum RMS current $I_{P\text{-}RMS\text{-}MAX}$

$$I_{P\_RMS\_MAX}=\sqrt{\frac{t_1^{'}}{3t_S^{'}}}\times I_{P\_PK\_MAX}=\sqrt{\frac{5.34}{3\times14.4}}\times0.178A=63mA$$

(g) Compute secondary maximum peak current and the maximum RMS current.

$$I_{S\_PK\_MAX}=N_{PS}\times I_{P\_PK\_MAX}=8\times0.178=1.424A \quad (32)$$
$$t_2^{'}=t_S^{'}-t_1^{'}-t_3=14.4-5.34-1.49=7.57\mu s \quad (33)$$
$$I_{S\_RMS\_MAX}=\sqrt{\frac{t_2^{'}}{3t_S^{'}}}\times I_{S\_PK\_MAX}=\sqrt{\frac{7.57}{3\times14.4}}\times1.424A=0.596A \quad (34)$$

#4. Select secondary power diode

(a) Compute the voltage and the current stress of secondary power diode

$$V_{D\_R\_MAX}=\frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}}+V_{OUT}=\frac{\sqrt{2}\times264}{8}+12=58.6V$$
$$I_{D\_PK\_MAX}=N_{PS}\times I_{P\_PK\_MAX}=8\times0.178=1.424A$$
$$I_{D\_AVG}=I_{OUT}=0.35A$$

#5. Select the output capacitor C_{OUT}

Refer to Power Device Design

Output current ripple $\Delta I_{O,MAX}$ is,

$$\Delta I_O=\sqrt{I_{S\_RMS\_MAX}^2-I_O^2}=\sqrt{0.596A^2-0.35A^2}=0.482A$$

Choose proper output capacitor to satisfy current ripple.

#6. Design RCD snubber

Refer to Power Device Design

Conditions			
V_{OUT}	12V	ΔV_S	50V
N_{PS}	8	L_K/L_M	2%
P_{OUT}	4.2W	ΔV_{C_RCD}	25V

The power loss of the snubber is

$$P_{RCD}=\frac{N_{PS}\times(V_{OUT}+V_{D,F})+\Delta V_S}{\Delta V_S}\times\frac{L_K}{L_M}\times P_{OUT}=\frac{8\times(12V+1V)+50V}{50V}\times0.02\times4.2W=0.259W$$

The resistor of the snubber is

$$R_{RCD}=\frac{(N_{PS}\times(V_{OUT}+V_{D,F})+\Delta V_S)^2}{P_{RCD}}=\frac{(8\times(12V+1V)+50V)^2}{0.259W}=91k\Omega$$

The capacitor of the snubber is

$$C_{RCD}=\frac{N_{PS}\times(V_{OUT}+V_{D,F})+\Delta V_S}{R_{RCD}f_S\Delta V_{C\_RCD}}=\frac{8\times(12V+1V)+50V}{91k\Omega\times 70kHz\times 25V}=0.97nF$$

#7. Set VIN pin

(a) R_{ST} is preset

$$R_{ST}<\frac{V_{BUS}}{I_{ST}}=\frac{250}{15\mu A}=16.7M\Omega$$

R_{ST} also acts as Feed forward compensation resistor.
R_{ST} is usually chose to 1.5MΩ to 2.5 MΩ

$$R_{ST}=2M\Omega$$

(b) Design C_{VIN}

$$C_{VIN}=\frac{\left(\frac{V_{BUS}}{R_{ST}}-I_{ST}\right)\times t_{ST}}{V_{VIN,ON}}=\frac{\left(\frac{250V}{2M\Omega}-15\mu A\right)\times 300ms}{14.3V}=2.3\mu F$$

Set C_{VIN}

$$C_{VIN}=1\mu F$$

#8. Set OVP

Known conditions at this step			
R_{ST}	2 MΩ	V_{OVP}	18V
$V_{OVP,REF}$	0.16V		

$$V_{OVP}=\frac{R_{ST}+R_{OVP}}{R_{OVP}}\frac{V_{VSEN,OVP}}{N_{PS}}$$

$$R_{OVP}=\frac{V_{VSEN,OVP}}{N_{PS}\times V_{OVP}-V_{VSEN,OVP}}R_{ST}=\frac{0.16V}{18V\times 8-0.16}\times 2M\Omega=2.22k\Omega$$

#9 Set current sense resistor to achieve ideal output current

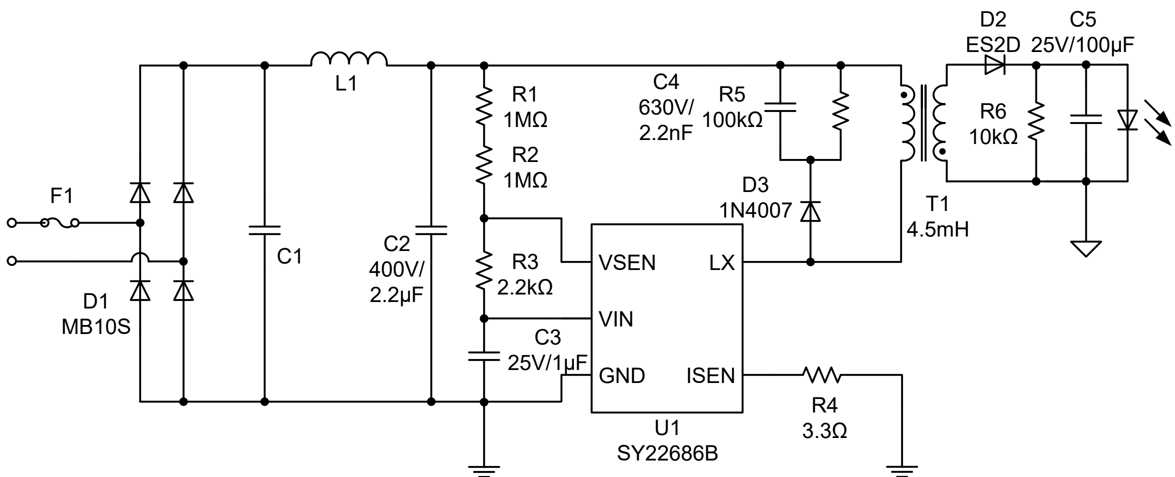
Refer to **Primary-side constant-current control**

Known conditions at this step			
N_{PS}	8	I_{OUT}	0.35A
V_{REF}	0.3V		

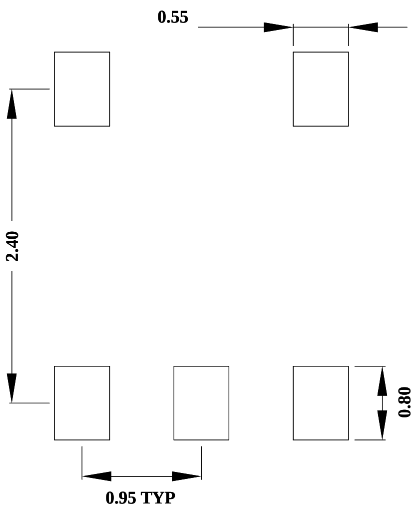
The current sense resistor is

$$R_S=\frac{V_{REF}\times N_{PS}}{I_{OUT}\times 2}=\frac{0.3V\times 8}{0.35\times 2}=3.43\Omega$$

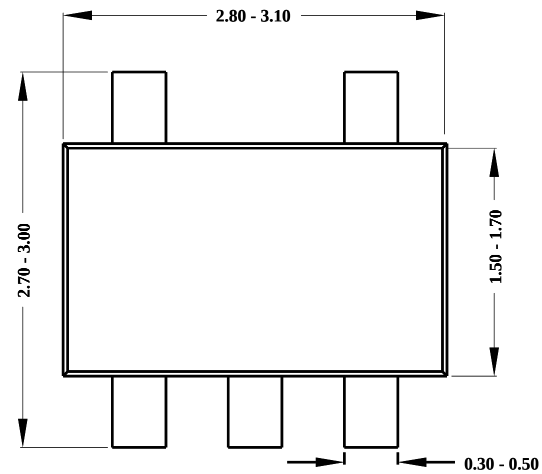
#10 Final result

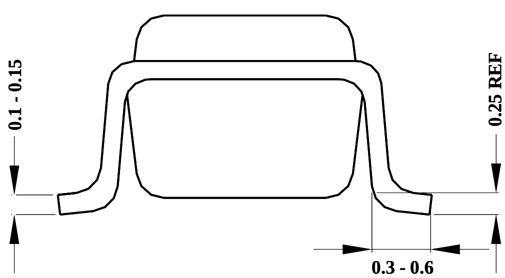

D2
ES2D
C5
25V/100μF
L1
R1
1MΩ
R2
1MΩ
C4
630V/
2.2nF
R5
100kΩ
R6
10kΩ
F1
D3
1N4007
T1
4.5mH
C1
C2
400V/
2.2μF
R3
2.2kΩ
VSEN
LX
VIN
D1
MB10S
C3
25V/1μF
GND
ISEN
R4
3.3Ω
U1
SY22686B

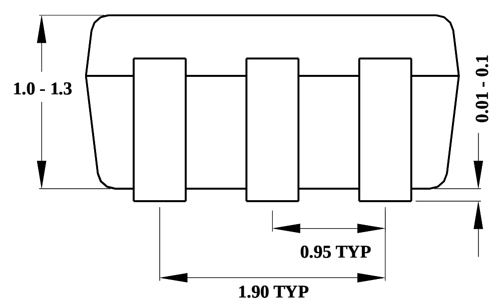
SOT23-5 Package outline & PCB layout design



Recommended Pad Layout



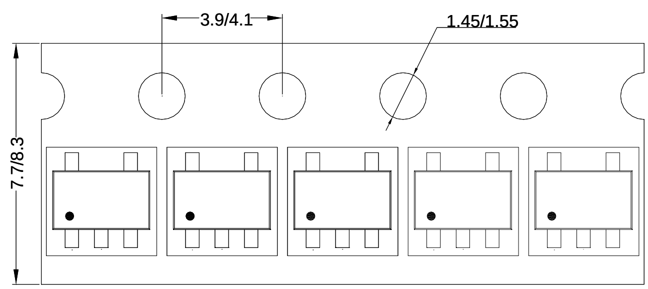




Notes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.

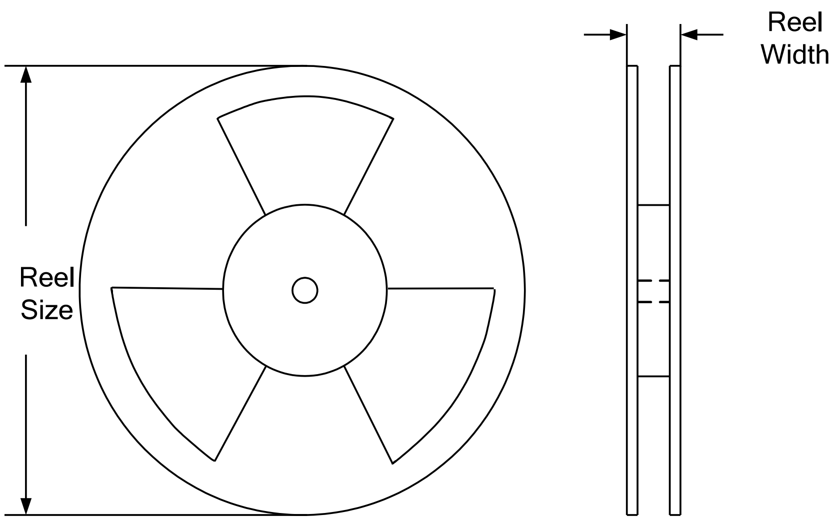
Taping & Reel Specification

1. SOT23-5 taping orientation



Feeding direction

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Reel width(mm)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-5	8	4	7"	8.4	280	160	3000

3. Others: NA

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