SY23433B

Flyback Regulator
With Primary Side CV/CC Control
for High Input Voltage Application

General Description

SY23433B is a single stage Flyback regulator targeting at high input voltage applications. It integrates 900V MOSFET to decrease physical volume. Both the output current and voltage are sensed by primary side signal process. SY23433B operates in quasi-resonant mode and adaptive PWM/PFM control for highest average efficiency. In addition, SY23433B integrates fast internal HV start up circuit to minimize no-load loss and external components. A special OVP function of VREG pin has been integrated in SY23433B to prevent the output voltage from raising too high with light load during strong magnetic field test.

Features

- Integrated 900V MOSFET
- Very Tight Primary Side CV/CC Regulation
- Quasi-resonant Mode and PWM/PFM Control for Higher Average Efficiency
- Internal CC/CV Loop Compensation
- Low Start Up Current: 5μA Max
- HV Start Up Circuit to Reduce No-load Loss
- Maximum Switching Frequency Limitation 125kHz
- VREG OVP Function for Strong Magnetic Field Test
- Reliable Protections for OCP,SCP,VCCOVP,VSEN SCP, OTP
- Compact Package: SSOP10

Ordering Information

SY23433□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY23433BFHC	SSOP10	----

Applications

- Power Supply for STB Home Appliances, Smart Power Meter and Other Appliances with High AC Input Voltage

Recommended operating output power	
Products	85~450Vac
SY23433B	7W

Typical Applications

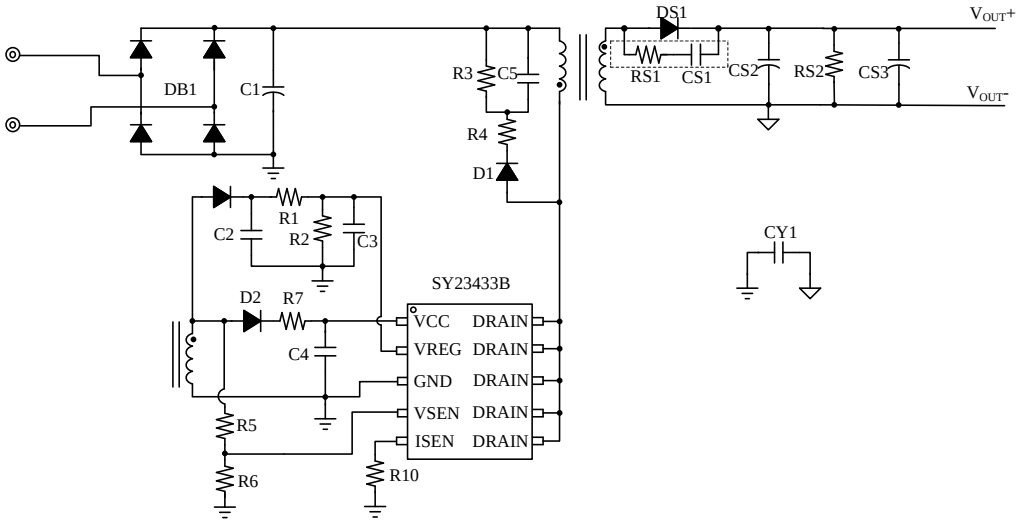
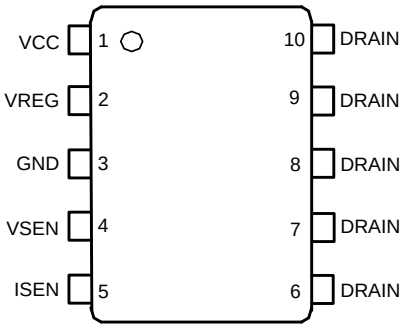


Fig.1 Schematic Diagram

© 2019 Silergy Corp. Rights Reserved.

Pinout (top view)



(SSOP10)

Top Mark: CLL*xyz* (device code: CLL, ***x=year code, y=week code, z= lot number code*****)**

Pin	Name	Description
1	VCC	Power supply pin.
2	VREG	Aux-winding voltage detection pin. Connect this pin to a voltage sensing circuit (shown in fig.1) to prevent the output voltage from raising too high with light load during strong magnetic field test.
3	GND	Ground pin.
4	VSEN	Inductor current zero-crossing detection pin. This pin receives the auxiliary winding voltage by a resistor divider and detects the inductor current zero crossing point.
5	ISEN	Current sense pin. Connect this pin to the source of the primary switch.
6~10	DRAIN	Drain of the internal power MOSFET.

© 2019 Silergy Corp. Rights Reserved.

Absolute Maximum Ratings (Note 1)

VCC ---------- -0.3V~25V
VREG ---------- -0.3V~3.3V
ISEN ---------- -0.3V~3.6V
VSEN ---------- -0.3V~V_{VCC}+0.3V
DRAIN ---------- 900V
Power Dissipation, @ TA = 25°C SSOP10 ---------- 1.1W
Package Thermal Resistance (Note 2)
SSOP10, θ_{JA} ---------- 125°C/W
SSOP10, θ_{JA} ---------- 60°C/W
Junction Temperature Range ---------- -45°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

VCC ---------- 10V~17V
ISEN ---------- 0V~1V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 105°C

Block Diagram

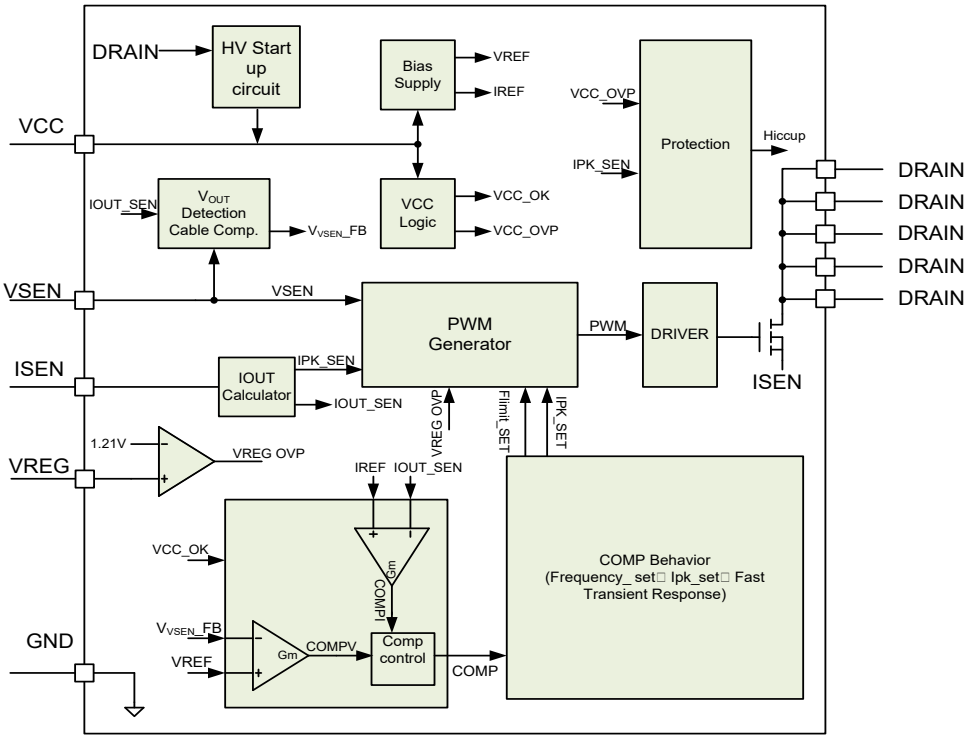


Fig.2 Block Diagram

© 2019 Silergy Corp. Rights Reserved.

Electrical Characteristics

(V_{CC} = 12V (Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VCC Operating Range	V_{VCC_RANGE}		8.5		21	V
VCC Turn-on Threshold	V_{VCC_ON}		19.4	21	22.6	V
VCC Turn-off Threshold	V_{VCC_OFF}		6.6	7.6	8.6	V
VCC OVP Voltage	V_{VCC_OVP}			24		V
Start Up Current	I_{ST}	$V_{VCC}<V_{VCC_OFF}$		2.3	5	μA
Operating Current	I_{VCC}	f=100kHz		1.5		mA
Quiescent Current	I_Q	f=2kHz	200	350	500	μA
Discharge Current in OVP Mode	I_{VCC_OVP}	V_{VCC}=12V		5		mA
Internal HV Start Up VCC Charge Current	$I_{HV_STARTUP}$			0.35		mA
Current Feedback Modulator Section						
Internal Reference Voltage for Output Current	V_{REF}		0.411	0.42	0.429	V
VREG Pin Section						
VREG Pin OVP Voltage Threshold	V_{VREG_OVP}		1.1	1.21	1.3	V
ISEN Pin Section						
Current Limit Voltage	V_{ISEN_LIM}		0.9	1	1.1	V
VSEN Pin Section						
Internal Reference Voltage	V_{REFV}		1.238	1.25	1.262	V
Integrated MOSFET Section						
Breakdown Voltage	V_{BV}	V_{GS}=0V,I_{DS}=250μA	900			V
Static Drain-Source On-Resistance	R_{DSON}	V_{GS}=12V, I_{DS}=0.1A T_A=25°C		13.4		Ω
Drain Current Continuous	I_{DS}	T_A=25°C			0.35	A
Switching Section						
Max ON Time	T_{ON_MAX}			18		μs
Min ON Time	T_{ON_MIN}			350		ns
Max OFF Time	T_{OFF_MAX}		450	550	700	μs
Min OFF Time	T_{OFF_MIN}		1.2	1.7	2.2	μs
Maximum Switching Frequency	F_{MAX}		95	120	145	kHz
Thermal Section						
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Recovery Hysteresis				30		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause perm anent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on "2 x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: Increase VCC pin voltage gradually higher than V_{VCC_ON} voltage then regulated to 12V.

© 2019 Silergy Corp. Rights Reserved.

Operation

SY23433B is a flyback regulator with several features to enhance performance of the converters.

It integrates a 900V MOSFET to handle high AC input voltage and enhance reliability of the converters.

To achieve higher efficiency and better EMI performance, SY23433B drives Flyback converters in the Quasi-Resonant mode; the maximum switching frequency is limited to 125kHz.

The output current is monitored by primary side detection technology, and the maximum output current can be programmed in Over Current Protection and Short Circuit Protection.

SY23433B can be applied in power supply for STB home appliances, smart power meter and other appliances with high AC input voltage.

A special OVP function of VREG pin has been integrated in SY23433B to prevent the output voltage from raising too high with light load during strong magnetic field test, which is special request for power meter. The OVP function should cooperate with a voltage sensing circuit shown in Fig.1.

SY23433B is available with SSOP10 package.

Applications Information

Start up

After AC supply or DC BUS is powered on, the capacitor C_{VCC} across VCC and GND pin is charged up by BUS voltage through an internal HV start up circuit. Once V_{VCC} rises up to V_{VCC-ON}, the internal blocks start to work. V_{VCC} will be pulled down by internal consumption of IC until the auxiliary winding of Flyback transformer could supply enough energy to maintain V_{VCC} above $V_{VCC-OFF}$.

The whole start up procedure is divided into two sections shown in Fig.3. t_{STC} is the C_{VCC} charged up section, and t_{STO} is the output voltage built-up section. The start up time t_{ST} composes of t_{STC} and t_{STO}, and usually t_{STO} is much smaller than t_{STC}.

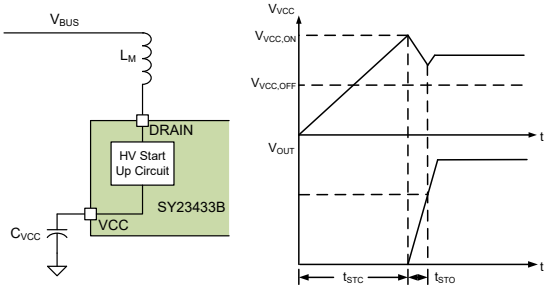


Fig.3 Start up

The C_{VCC} are designed by rules below:

Select C_{VCC} to obtain an ideal start up time $t_{ST,}$ and ensure the output voltage is built up at one time.

$$C_{VCC} = \frac{(I_{HV,Startup} - I_{ST}) \times t_{ST}}{V_{VCC_ON}} \quad (1)$$

If the C_{VCC} is not big enough to build up the output voltage at one time, increase C_{VCC} until the ideal start up procedure is obtained.

Shut down

After AC supply or DC BUS is powered off, the energy stored in the BUS capacitor will be discharged. When the auxiliary winding of Flyback transformer can not supply enough energy to VCC pin, V_{VCC} will drop down. Once V_{VCC} is below $V_{VCC-OFF}$, the IC will stop working and V_{COMP} will be discharged to zero.

Quasi-Resonant Operation

QR mode operation provides low turn-on switching losses for Flyback converter.

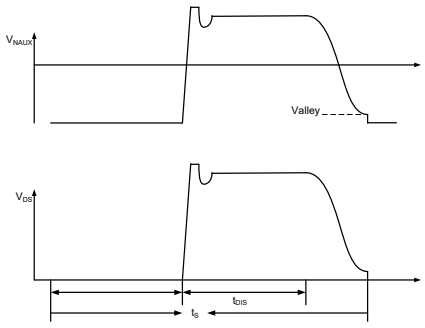


Fig.4 QR mode operation

The voltage across drain and source of the primary MOSFET is reflected by the auxiliary winding of the Flyback transformer. VSEN pin detects the voltage across the auxiliary winding by a resistor divider. When the voltage across drain and source of the primary MOSFET is at voltage valley, the MOSFET would be turned on.

© 2019 Silergy Corp. Rights Reserved.

Output Voltage Control (CV control)

In order to achieve primary side constant voltage control, the output voltage is detected by the auxiliary winding voltage.

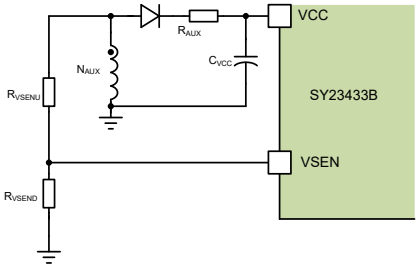


Fig.5 VSEN pin connection

As shown in Fig.5, during OFF time, the voltage across the auxiliary winding is

$$V_{AUX} = (V_{OUT} + V_{D-F}) \times \frac{N_{AUX}}{N_S} \quad (2)$$

N_{AUX} is the turns of auxiliary winding; N_S is the turns of secondary winding; V_{D-F} is the forward voltage of the power diode.

At the current zero-crossing point, V_{D-F} is nearly zero, so V_{OUT} is proportional with V_{AUX} exactly. The voltage of this point is sampled by the IC as the feedback of output voltage. The resistor divider is designed by

$$\frac{V_{VSEN-REF}}{V_{OUT}} = \frac{R_{VSEND}}{R_{VSENU} + R_{VSEND}} \times \frac{N_{AUX}}{N_S} \quad (3)$$

Where $V_{VSEN-REF}$ is the internal voltage reference.

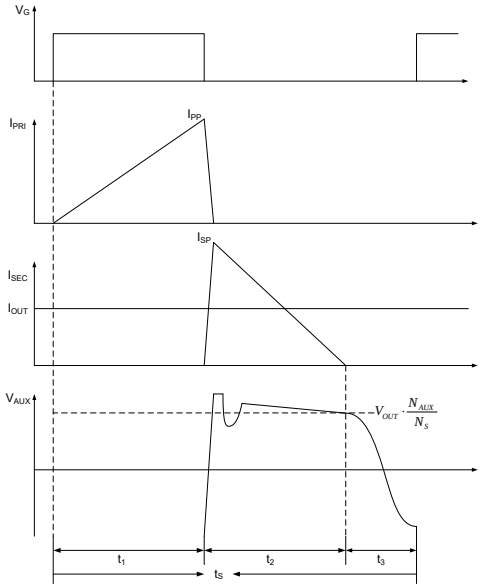


Fig.6 Auxiliary winding voltage waveforms

Output Current Control (CC control)

The output current is regulated by SY23433B with primary side detection technology, the maximum output current $I_{OUT-LIM}$ can be set by

$$I_{OUT-LIM} = \frac{k_1 \times V_{REF} \times N_{PS}}{R_S} \quad (4)$$

Where k_1 is the output current weight coefficient; V_{REF} is the internal reference voltage; R_S is the current sense resistor.

k_1 and V_{REF} are all internal constant parameters, $I_{OUT-LIM}$ can be programmed by N_{PS} and R_S.

$$R_S = \frac{k_1 \times V_{REF} \times N_{PS}}{I_{OUT}} \quad (5)$$

K_1 is set to 0.5

When over current operation or short circuit operation happens, the output current will be limited at $I_{OUT-LIM}$. The V-I curve is shown as Fig.7.

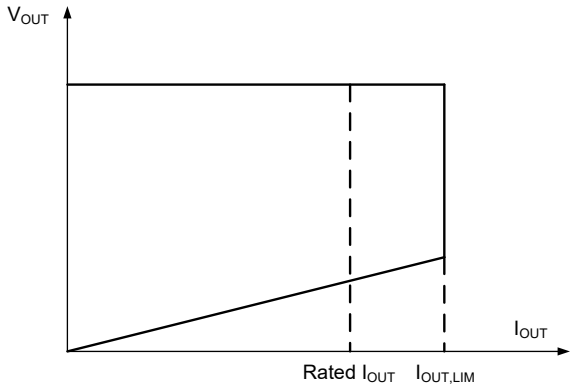


Fig.7 V-I curve

The IC provides line regulation modification function to improve line regulation performance of the output current.

Due to the sample delay of ISEN pin and other internal delay, the output current increases with increasing input BUS line voltage. A small compensation voltage ΔV_{ISEN-C} is added to ISEN pin during ON time to improve such performance. This ΔV_{ISEN-C} is adjusted by the upper resistor of the divider connected to VSEN pin.

$$\Delta V_{ISEN-C} = V_{BUS} \times \frac{N_{AUX}}{N_P} \times \frac{1}{R_{VSENU}} \times k_2 \quad (6)$$

Where R_{VSENU} is the upper resistor of the divider; k_2 is an internal constant as the modification coefficient.

© 2019 Silergy Corp. Rights Reserved.

The compensation is mainly related with R_{VSENU}, larger compensation is achieved with smaller R_{VSENU}. Normally, R_{VSENU} ranges from 50kΩ~150kΩ.

Short Circuit Protection (SCP)

There are two kinds of situations, one is the valley signal cannot be detected by VSEN, the other is the valley signal can be detected by VSEN.

When the output is shorted to ground, the output voltage is clamped to zero. The voltage of the auxiliary winding is proportional to the output winding, so valley signal cannot be detected by VSEN. There are two cases，the one is without valley detection, MOSFET cannot be turned on until maximum off time is reached. If MOSFET is turned on with maximum off-time for 64 times continuously which can not detected valley, IC will be shut down and enter into hiccup mode. The other is that IC will be shut down and enter into hiccup mode when V_{VCC} below $V_{VCC-OFF}$ within 64 times.

When the output voltage is not low enough to disable valley detection in short condition, SY23433B will operate in CC mode until VCC is below $V_{VCC-OFF}$.

In order to guarantee SCP function not effected by voltage spike of auxiliary winding, a filter resistor R_{AUX} is needed.

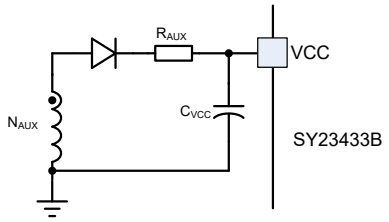


Fig. 8 Filter resistor R_{AUX}

OVP Function of VREG Pin

The aux-winding voltage is sensed by the circuit shown in Fig.9. R1 and R2 compose a voltage divider. The divided voltage is positive input of VREG OVP comparator. The OVP threshold is 1.21V. If VREG voltage exceeds 1.21V，the SY23433B will stop PWM pulse immediately. When the VREG voltage falls below 1.21V, the PWM will recover. The value of R1, R2 and C2 will determine the average output voltage when OVP occurs. C3 is a filter capacitor and usually on the order of pF.

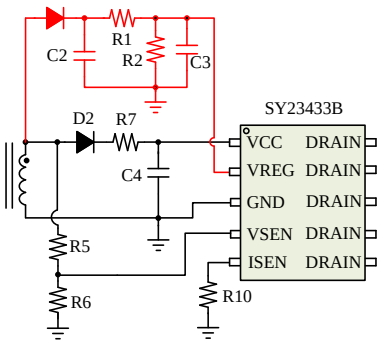


Fig. 9 circuit of VREG OVP

VSEN Pin Short Protection

The SY23433B has a protection against faults caused by a shorted VSEN pin or a shorted pull-down resistor. During start-up, the voltage on the VSEN pin is monitored. In normal situations, the voltage on the VSEN pin reaches the sense protection trigger level. When the VSEN voltage does not reach this level, the VSEN pin is shorted and the protection is activated. The IC stops switching and discharge the VCC voltage. Once V_{VCC} is below $V_{VCC-OFF}$, the IC will shut down and be charged again by HV start up. In order to ensure reliable detection, the pull-down resistor should larger than 2kΩ.

Power Device Design

MOSFET and Diode

When the operation condition is with maximum input voltage and full load, the voltage stress of MOSFET and secondary power diode is maximized.

$$V_{MOS_DS_MAX} = \sqrt{2}V_{AC_MAX} + N_{PS} \times (V_{OUT} + V_{D,F}) + \Delta V_S \quad (7)$$

$$V_{D_R_MAX} = \frac{\sqrt{2}V_{AC_MAX}}{N_{PS}} + V_{OUT} \quad (8)$$

Where $V_{AC,MAX}$ is maximum input AC RMS voltage; N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the rated output voltage; $V_{D,F}$ is the forward voltage of secondary power diode; ΔV_S is the overshoot voltage clamped by RCD snubber during OFF time.

When the operation condition is with minimum input voltage and full load, the current stress of MOSFET and power diode is maximized.

$$I_{MOS_PK_MAX} = I_{P_PK_MAX} \quad (9)$$

$$I_{MOS_RMS_MAX} = I_{P_RMS_MAX} \quad (10)$$

© 2019 Silergy Corp. Rights Reserved.

$$I_{D_PK_MAX} = N_{PS} \times I_{P_PK_MAX} \quad (11)$$

$$I_{D_AVG} = I_{OUT} \quad (12)$$

Where $I_{P\text{-}PK\text{-}MAX}$ and $I_{P\text{-}RMS\text{-}MAX}$ are maximum primary peak current and RMS current, which will be introduced later.

Transformer (N_{PS} and L_M)

N_{PS} is limited by the electrical stress of the power MOSFET:

$$N_{PS} \le \frac{V_{MOS_(BR)DS} \times 90\% - \sqrt{2} V_{AC_MAX} - \Delta V_S}{V_{OUT} + V_{D_F}} \quad (13)$$

Where $V_{MOS_(BR)DS}$ is the breakdown voltage of the power MOSFET; $V_{AC,MAX}$ is maximum input AC RMS voltage.

In Quasi-Resonant mode, each switching period cycle t_S consists of three parts: current rising time t_1, current falling time t_2 and quasi-resonant time t_3 shown in Fig.10.

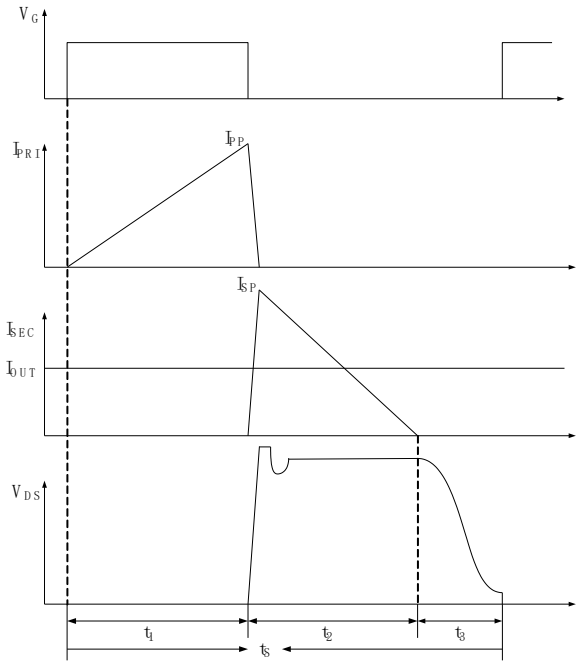


Fig.10 switching waveforms

When the operation condition is with minimum input AC RMS voltage and full load, the switching frequency is minimum frequency, the maximum peak current through MOSFET and the transformer happens.

Once the minimum frequency f_{S_MIN} is set, the inductance of the transformer could be induced. The design flow is shown as below:

(a) Select N_{PS};

$$N_{PS} \le \frac{V_{MOS_(BR)DS} \times 90\% - \sqrt{2} V_{AC_MAX} - \Delta V_S}{V_{OUT} + V_{D_F}} \quad (14)$$

(b) Preset minimum frequency $f_{S,MIN}$;

(c) Compute inductor L_M and maximum primary peak current $I_{P_PK_MAX}$;

$$I_{P,PK,MAX} = \frac{2P_{OUT}}{\eta \times V_{DC,MIN}} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D,F})} + \pi \sqrt{\frac{2P_{OUT}}{\eta} \times C_{Drain} \times f_{S,MIN}} \quad (15)$$

$$L_M = \frac{2P_{OUT}}{\eta \times I_{P,PK,MAX}^2 \times f_{S,MIN}} \quad (16)$$

Where C_{Drain} is the parasitic capacitance at drain of MOSFET; η is the efficiency; P_{OUT} is rated full load power; V_{DC_MIN} is minimum input DC RMS voltage.

(d) Compute current rising time t_1 and current falling time t_2;

$$t_1 = \frac{L_M \times I_{P,PK,MAX}}{V_{DC,MIN}} \quad (17)$$

$$t_2 = \frac{L_m \times I_{P,PK}}{N_{PS} \times (V_{OUT} + V_{D,F})} \quad (18)$$

$$t_S = \frac{1}{f_{S,MIN}} \quad (19)$$

(e) Compute primary maximum RMS current $I_{P\text{-}RMS\text{-}MAX}$ for the transformer fabrication;

$$I_{P,RMS,MAX} = \frac{\sqrt{3}}{3} I_{P,PK,MAX} \sqrt{\frac{t_1}{t_S}} \quad (20)$$

(f) Compute secondary maximum peak current $I_{S\text{-}PK\text{-}MAX}$ and RMS current $I_{S\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{S_PK_MAX} = N_{PS} \times I_{P_PK_MAX} \quad (21)$$

$$I_{S,RMS,MAX} = \frac{\sqrt{3}}{3} N_{PS} \times I_{P,PK,MAX} \times \sqrt{\frac{t_2}{t_S}} \quad (22)$$

Transformer Design (N_P , N_S , N_{AUX})

The design of the transformer is similar with ordinary Flyback transformer. The parameters below are necessary:

© 2019 Silergy Corp. Rights Reserved.

Necessary parameters	
Turns ratio	N_{PS}
Inductance	L_M
Primary maximum current	$I_{P\text{-}PK\text{-}MAX}$
Primary maximum RMS current	$I_{P\text{-}RMS\text{-}MAX}$
Secondary maximum RMS current	$I_{S\text{-}RMS\text{-}MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e;

(b) Preset the maximum magnetic flux ΔB;

ΔB=0.22~0.26T

(c) Compute primary turn N_P;

$$N_p = \frac{L_M \times I_{P_PK_MAX}}{\Delta B \times A_e} \quad (23)$$

(d) Compute secondary turn N_S;

$$N_S = \frac{N_P}{N_{PS}} \quad (24)$$

(e) Compute auxiliary turn N_{AUX};

$$N_{AUX} = N_S \times \frac{V_{VCC}}{V_{OUT}} \quad (25)$$

Where V_{VCC} is the working voltage of VCC pin (11V~13V is recommended);

(f) Select an appropriate wire diameter;

With $I_{P\text{-}RMS\text{-}MAX}$ and $I_{S\text{-}RMS\text{-}MAX}$, select appropriate wire to make sure the current density ranges from 4A/mm^2 to 10A/mm^2.

(g) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

Input capacitor C_{BUS}

Generally, the input capacitor C_{BUS} is selected by

C_{BUS}=2~3μF/W

Or more accurately by

$$C_{BUS} = \frac{\arcsin\left(1-\frac{V_{DC,MIN}}{\sqrt{2}V_{AC,MIN}}\right)+\frac{\pi}{2}}{\pi} \frac{P_{OUT}}{\eta} \frac{1}{2f_{IN}V_{AC,MIN}^2\left(1-\frac{V_{DC,MIN}}{\sqrt{2}V_{AC,MIN}}\right)^2} \quad (26)$$

Where V_{DC_MIN} is the minimum voltage of BUS line; f_{IN} is AC line frequency;

RCD Snubber for MOSFET

The power loss of the snubber P_{RCD} is evaluated first.

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D_F}) + \Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT} \quad (27)$$

Where N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the output voltage; $V_{D\text{-}F}$ is the forward voltage of the power diode; ΔV_S is the overshoot voltage clamped by RCD snubber; L_K is the leakage inductor; L_M is the inductance of the Flyback transformer; P_{OUT} is the output power.

The R_{RCD} is related with the power loss:

$$R_{RCD} = \frac{\left[N_{PS} \times (V_{OUT} + V_{D_F}) + \Delta V_S\right]^2}{P_{RCD}} \quad (28)$$

The C_{RCD} is related with the voltage ripple of the snubber $\Delta V_{C\text{-}RCD}$:

$$C_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D_F}) + \Delta V_S}{R_{RCD} \times f_S \times \Delta V_{C_RCD}} \quad (29)$$

Layout

(a) To achieve better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit;

(b) The ground of the BUS line capacitor, the ground of the current sample resistor and the signal ground of the IC should be connected in a star connection;

(c) The circuit loop of all switching circuit should be kept small: primary power loop, secondary loop and auxiliary power loop.

© 2019 Silergy Corp. Rights Reserved.

Design Example

A design example of multiple output power supply of smart power meter y is shown below step by step.

#1. Identify Design Specification

Design Specification			
$V_{AC,MIN}$	85V	$V_{AC,MAX}$	300V
V_{OUT1}	16V	I_{OUT1}	0.2A
V_{OUT2}	16V	I_{OUT2}	0.2A
$P_{OUT,Total}$	6.4W	η	75%
$f_{IN,MIN}$	60KHz		

#2. Transformer Design （N_{PS} and L_M）

Refer to Power Device Design

Conditions			
$V_{AC,MIN}$	85V	V_{AC-MAX}	300V
P_{OUT}	6.4W	f_{S-MIN}	60kHz
Parameters designed			
$V_{MOS-(BR)DS}$	900V	ΔV_S	80V
C_{Drain}	100pF	$V_{D,F}$	0.7V

(a) Compute turns ratio N_{PS} first;

$$N_{PS} \le \frac{V_{MOS_(BR)DS} \times 90\% - \sqrt{2} V_{AC_MAX} - \Delta V_S}{V_{OUT} + V_{D,F}}$$

$$= \frac{900V \times 0.9 - \sqrt{2} \times 300V - 80V}{16V + 0.7V}$$

$$= 18.3$$

N_{PS} is set to

$$N_{PS} = 7$$

(b)f_{S_MIN} is preset ;

$$f_{S_MIN} = 60kHz$$

(c) Compute inductor L_M and maximum primary peak current $I_{P_PK_MAX}$;

$$I_{P,PK,MAX} = \frac{2P_{OUT}}{\eta \times \left(\sqrt{2} V_{AC,MIN} - \Delta V_{BUS}\right)} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D,F})} + \pi \sqrt{\frac{2P_{OUT}}{\eta} \times C_{Drain} \times f_{S,MIN}}$$

$$= \frac{2 \times 6.4W}{0.75 \times (\sqrt{2} \times 85V - 0.3 \times \sqrt{2} \times 85V)} + \frac{2 \times 6.4W}{0.75 \times 7 \times (16V + 0.7V)} + \pi \times \sqrt{\frac{2 \times 6.4W}{0.75} \times 100pF \times 60KHz}$$

$$= 0.381A$$

© 2019 Silergy Corp. Rights Reserved.

$$L_m = \frac{2P_{OUT}}{\eta \times I_{P,PK,MAX}^2 \times f_{S,MIN}}$$
$$= \frac{2 \times 6.4W}{0.75 \times (0.381A)^2 \times 60KHz}$$
$$= 1.96mH$$

Set

L_M=1.96mH

(d) Compute current rising time t_1 and current falling time t_2;

$$t_1 = \frac{L_M \times I_{P,PK,MAX}}{V_{BUS}} = \frac{1.96mH \times 0.381A}{\sqrt{2} \times 85V} = 6.21\mu s$$

$$t_2 = \frac{L_m \times I_{P,PK,MAX}}{N_{PS} \times (V_{OUT} + V_{D,F})} = \frac{1.96mH \times 0.381A}{7 \times (16V + 0.7V)} = 6.39\mu s$$

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}} = \pi \times \sqrt{1.96mH \times 100pF} = 1.39\mu s$$

$$t_S = t_1 + t_2 + t_3 = 6.21\mu s + 6.39\mu s + 1.39\mu s = 13.99\mu s$$

(e) Compute primary maximum RMS current $I_{P\text{-}RMS\text{-}MAX}$ for the transformer fabrication;

$$I_{P,RMS,MAX} = \frac{\sqrt{3}}{3} I_{P,PK,MAX} \times \sqrt{\frac{t_1}{t_S}} = \frac{\sqrt{3}}{3} \times 0.381A \times \sqrt{\frac{6.21\mu s}{13.99\mu s}} = 0.147A$$

(f) Compute secondary maximum peak current $I_{S\text{-}PK\text{-}MAX}$ and RMS current $I_{S\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{S_PK_MAX} = N_{PS} \times I_{P_PK_MAX} = 7 \times 0.381A = 2.667A$$
$$I_{S,RMS,MAX} = N_{PS} \times \frac{\sqrt{3}}{3} I_{P,PK,MAX} \times \sqrt{\frac{t_2}{t_S}} = 7 \times \frac{\sqrt{3}}{3} \times 0.381A \times \sqrt{\frac{6.39\mu s}{13.99\mu s}} = 1.041A$$

#3. MOSFET and Diode Design

Conditions			
$V_{AC\text{-}MAX}$	300V	N_{PS}	7
V_{OUT1}	16V	$V_{D\text{-}F}$	0.7V
V_{OUT2}	16V	N_{PS2}	7
ΔV_S	80V	η	75%

(a) Compute the voltage and the current stress of MOSFET:

$$V_{MOS_DS_MAX} = \sqrt{2} V_{AC_MAX} + N_{PS} \times (V_{OUT} + V_{D_F}) + \Delta V_S$$
$$= \sqrt{2} \times 300V + 7 \times (16V + 0.7V) + 80V$$
$$= 621V$$

$$I_{MOS_PK_MAX} = I_{P_PK_MAX} = 0.381A$$

© 2019 Silergy Corp. Rights Reserved.

$I_{MOS_RMS_MAX}=I_{P_RMS_MAX}=0.147A$

(b) Compute the voltage and the current stress of secondary power diode

$$V_{D1_R_MAX}=V_{D2_R_MAX}=\frac{\sqrt{2}V_{AC_MAX}}{N_{PS}}+V_{OUT}=\frac{\sqrt{2}\times 300V}{7}+16V=76.6V$$

$I_{D1_AVG}=I_{OUT1}=I_{OUT2}=0.2A$

#4. Select the input capacitor C_{IN}

Refer to input capacitor C_{IN} Design

Known conditions at this step			
$V_{AC,MIN}$	85V	ΔV_{BUS}	30% $V_{AC,MIN}$

$$C_{BUS}=\frac{\arcsin(1-\frac{\Delta V_{BUS}}{\sqrt{2}V_{AC_MIN}})+\frac{\pi}{2}}{\pi}\times\frac{P_{OUT}}{\eta}\times\frac{1}{2f_{IN}V_{AC_MIN}^2[1-(1-\frac{\Delta V_{BUS}}{\sqrt{2}V_{AC_MIN}})^2]}$$

$$=\frac{\arcsin(1-\frac{0.3\times\sqrt{2}\times 85V}{\sqrt{2}\times 85V})+\frac{\pi}{2}}{\pi}\times\frac{6.4W}{0.75}\times\frac{1}{2\times 50Hz\times 85V^2\times[1-(1-\frac{0.3\times\sqrt{2}\times 85V}{\sqrt{2}\times 85V})^2]}$$

$=12.4\mu F$

Set C_{BUS} = 12μF

The rated voltage of BUS E-cap is 450V or 500V

Where ΔV_{BUS} is the voltage ripple of BUS line.

#5. Set current sense resistor to achieve ideal output current

Refer to **Primary-side constant-current control**

Known conditions at this step			
k_1	0.5	N_{PS}	7
V_{REF}	0.42V	$I_{OUT,LIM}$	0.5A

The current sense resistor is

$$R_S=\frac{k_1\times V_{REF}\times N_{PS}}{I_{OUT}}$$

$$=\frac{0.5\times 0.42V\times 7}{0.5A}$$

$=2.94\Omega$

Set Rs=3Ω

© 2019 Silergy Corp. Rights Reserved.

#6. Set VSEN pin

Refer to V_{OUT}

First identify R_{VSENU} need for line regulation.

Parameters Designed			
R_{VSENU}	43kΩ		

Then compute R_{VSEND}

Conditions			
V_{OUT}	16V	V_{VSEN_REF}	1.25V
R_{VSENU}	43kΩ		

Set $N_{AUX}=N_S$

$$R_{VSEND}=\frac{R_{VSENU}}{\frac{V_{OUT}N_{AUX}}{V_{VSEN_REF}N_S}-1}=\frac{43K}{(\frac{16V}{1.25V}-1)}=3.64K$$

$R_{VSEND}=3.6k\Omega$

#7. Design output voltage OVP point during strong magnetic field test

First identify the maximum output voltage is 20V.

Set $R_{VREG1}=22k\Omega$

$$R_{VREG2}=\frac{R_{VREG1}}{\frac{V_{O,OVP}}{V_{REG,OVP}}-1}$$

$$=\frac{22}{\frac{20}{1.2}-1}$$

$$=1.4k$$

Set $R_{VREG2}=1.5k\Omega$

#8. Design RCD snubber

Refer to Power Device Design

Conditions			
V_{OUT}	16V	ΔV_S	80V
N_{PS}	7	L_K/L_M	3%
P_{OUT}	6.4W		

The power loss of the snubber is

© 2019 Silergy Corp. Rights Reserved.

$$P_{RCD}=\frac{N_{PS}\times(V_{OUT}+V_{D_F})+\Delta V_S}{\Delta V_S}\times\frac{L_K}{L_M}\times P_{OUT}$$
$$=\frac{7\times(16V+0.7V)+80V}{80V}\times 0.03\times 6.4W$$
$$=0.47W$$

The resistor of the snubber is

$$R_{RCD}=\frac{\left[N_{PS}\times(V_{OUT}+V_{D_F})+\Delta V_S\right]^2}{P_{RCD}}$$
$$=\frac{\left[7\times(16V+0.7V)+80V\right]^2}{0.47W}$$
$$=82k\Omega$$

The capacitor of the snubber is

$$C_{RCD}=\frac{N_{PS}\times(V_{OUT}+V_{D_F})+\Delta V_S}{R_{RCD}f_{S,MIN}\Delta V_{C_RCD}}$$
$$=\frac{7\times(16V+0.7V)+80V}{82k\Omega\times 60kHz\times 70V}$$
$$=571pF$$

#9. Final Result

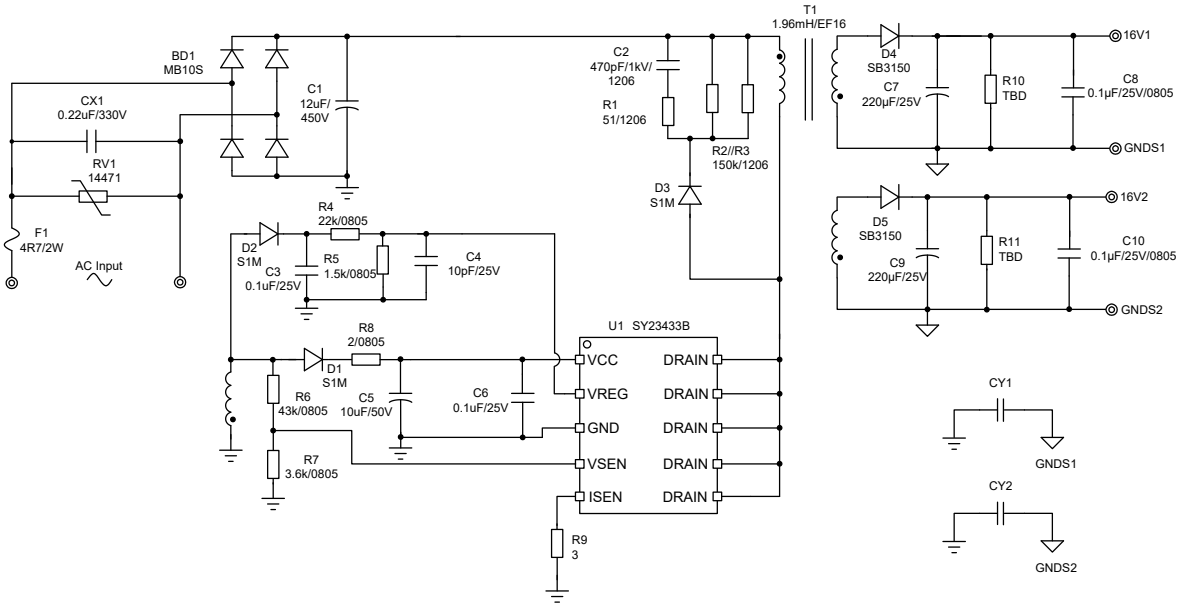
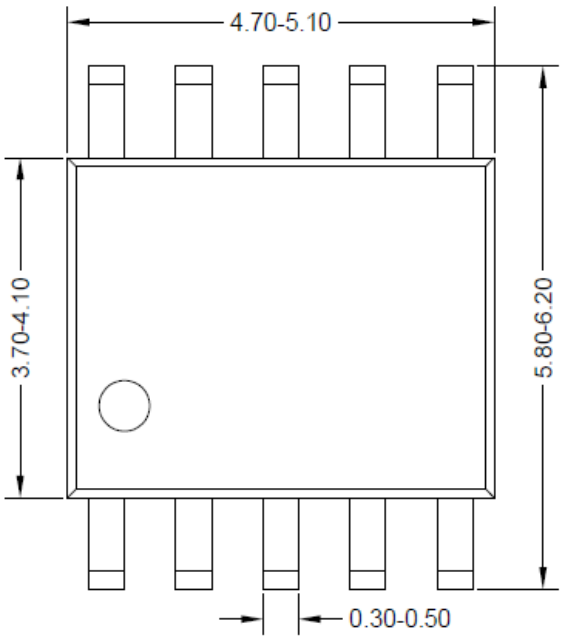


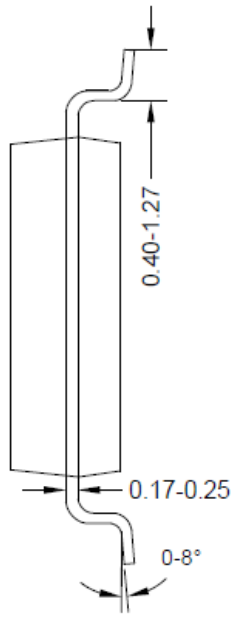
Fig.11 Final Result

© 2019 Silergy Corp. Rights Reserved.

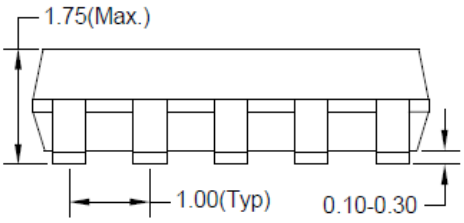
SSOP10 Package Outline Drawing



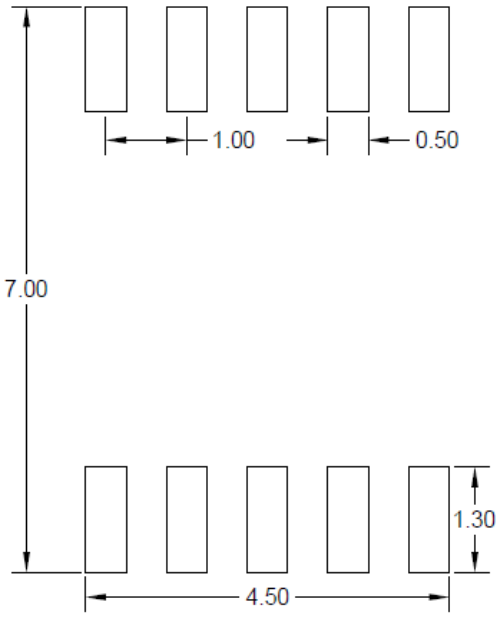
Top view



Side view



Front view



Recommended PCB layout

(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

© 2019 Silergy Corp. Rights Reserved.

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
March 6, 2019	Revision 0.9	Initial Release

© 2019 Silergy Corp. Rights Reserved.

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. Applications. Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com

© 2019 Silergy Corp. **All Rights Reserved.**

© 2019 Silergy Corp. Rights Reserved.