SY26172

High Efficiency, 16V/12A Synchronous Step-down Regulator

General Description

The SY26172 is a high-efficiency synchronous step-down DC-DC regulator featuring internal power and synchronous rectifier switches capable of delivering 12A of continuous output current over a wide input voltage range, from as low as 2.7V up to 16V. The output voltage is adjustable from 0.6V to 5.5V.

Silergy's proprietary Instant-PWM™ fast-response, constant-on-time (COT) PWM control method supports high input/output voltage ratios (low duty cycles) and responds to load transients within ~100ns while maintaining a near constant operating frequency over line, load and output voltage ranges. This control method provides stable operation without complex compensation, even with low ESR ceramic output capacitors.

The stable internal reference (V_{REF}) provides ±1% accuracy over T_J= -40°C to 125°C, and the differential input sense configuration allows the feedback sensing at the most relevant load point.

Internal 12.6mΩ power and 4.3mΩ synchronous rectifier switches provide excellent efficiency for a wide range of applications, especially for low output voltages and low duty cycles. Cycle-by-cycle current limit, input under-voltage lock-out, internal soft-start, output under- and over-voltage protection, and thermal shutdown provide safe operation in all operating conditions.

The SY26172 is available in a compact QFN3×4 package.

Features

- Wide Input Voltage Range: 3.6-16V, and as Low as 2.7V with External VCC Applied
- Internal 12.6mΩ Power Switch and 4.3mΩ Synchronous Rectifier
- Accurate Feedback Set Point: 0.6V ±1%
- Differential Remote Sense
- Fast Transient Response
- 600kHz, 800kHz and 1000kHz Operating Frequency
- Selectable Automatic High-efficiency Discontinuous Operating Mode at Light Loads
- Programmable Valley Current Limit
- Reliable Built-in Protections:
  - Automatic Recovery for Input Under-voltage (UVLO), Output Under-voltage (UVP) and Over-temperature (OTP) Conditions
  - Cycle-by-cycle Valley and Peak Current Limit (OCP)
  - Cycle-by-cycle Reverse Current Limit
- Internal, Adjustable Soft-Start Limits Inrush Current
- Smooth Pre-biased Startup
- Power Good Output Monitor for Under-voltage and Over-voltage

Applications

- Telecom and Networking Systems
- Servers
- High Power Access Points
- Storage Systems
- Cellular Base Stations

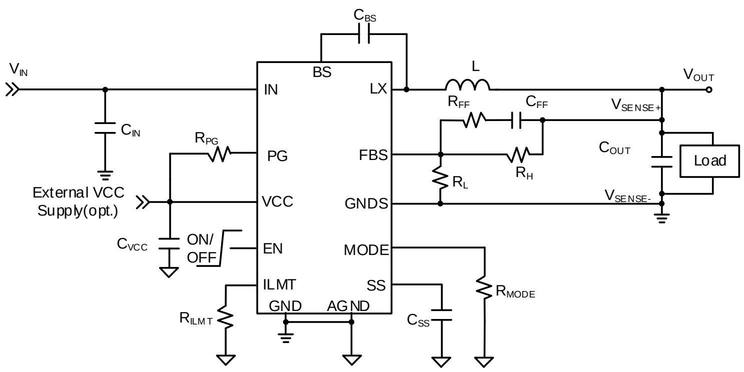


Figure1. Typical Application Circuit

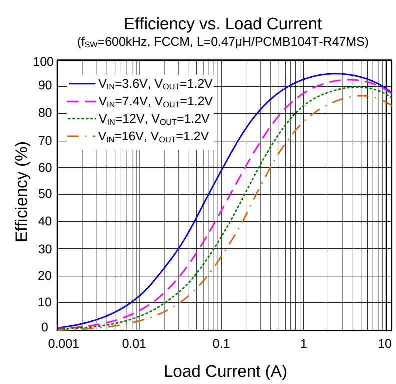


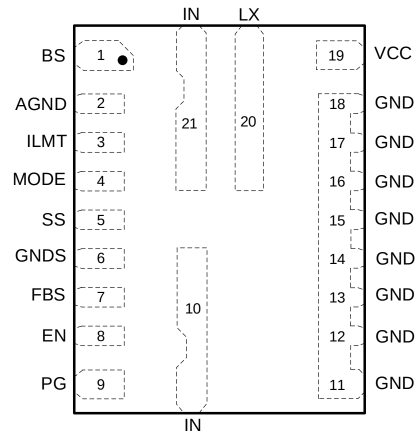
Figure2. Efficiency vs. Load Current

Ordering Information

Ordering Part Number	Package type	Top Mark
SY26172TXQ	QFN3×4-21 RoHS Compliant and Halogen Free	**EAB***xyz*

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin No	Pin Name	Pin Description
1	BS	Boot-strap supply for the high side gate driver. Connect a 0.1μF ceramic capacitor between the BS and the LX pin.
2	AGND	Analog ground.
3	ILMT	Synchronous rectifier current limit setting. Connect a resistor to AGND to set the inductor valley current limit value. See detailed description.
4	MODE	Operation mode selection. Program MODE to select FCCM/DCM, and the operating switching frequency. See table 1.
5	SS	External soft-start setting. Optionally adjust the soft-start time by adding an appropriate external capacitor between this pin and AGND pin. See detailed description.
6	GNDS	Remote ground sense. Connect this pin directly to the negative side of the preferred voltage sense point. Short to AGND if remote sense is not used.
7	FBS	Remote feedback sense. Connect this pin to the center point of the output resistor divider to program the output voltage. See design procedure.
8	EN	Enable input. Pull low to disable the device, high to enable. Do not leave this pin floating. May be used for increasing startup voltage or sequencing. See Detailed Description.
9	PG	Power good indicator. Open drain output when the output voltage is within 93.5% to 120% of the regulation set point.
10, 21	IN	Power input. Decouple this pin to GND pin with at least a 20μF ceramic capacitor.
11, 12, 13, 14, 15, 16, 17, 18	GND	Power ground.
19	VCC	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuits. Decouple this pin to GND with at least a 1μF ceramic capacitor. Use short, direct connections and avoid the use of vias. May be driven by an external bias supply. See detailed description.
20	LX	Inductor pin. Connect this pin to the switching node of the inductor.

Block Diagram

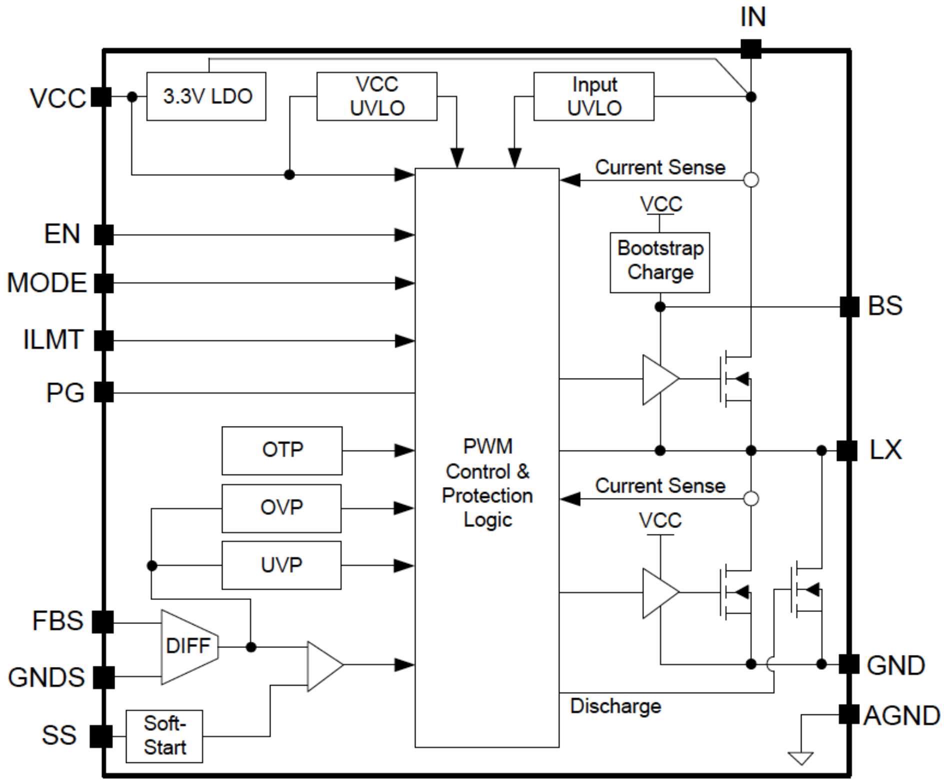


Figure 3. Block Diagram

Absolute Maximum Ratings (1)	Min	Max	Unit
IN	-0.3	18	V
ILMT, EN, MODE, SS, LX	-0.3	IN + 0.3	
LX, 10ns duration	-5	IN + 5	
BS	LX - 0.3	LX + 4	
FBS, GNDS, AGND, VCC, PG	-0.3	4	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering,10sec.)		260	
Storage Temperature	-65	150	

Thermal Information (2)	Min	Max	Unit
θ_{JA} Junction-to-ambient Thermal Resistance		25	°C/W
θ_{JC} Junction-to-case Thermal Resistance		5	
P_D Power Dissipation T_A=25°C		4	W

Recommended Operating Conditions (3)	Min	Max	Unit
IN	2.7	16	V
Output Voltage	0.6	5.5	
GNDS	-0.2	0.2	
Output Current		12	A
Output Current Limit Setting		14	
Peak Inductor Current		17	
Junction Temperature	-40	125	°C

Electrical Characteristics V_{IN} = 12V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise specified (4)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage	V_{IN}		2.7		16	V
	UVLO, rising	$V_{IN,UVLO}$		2.52	2.6	2.68	V
	UVLO, Hysteresis	$V_{IN,HYS}$			200		mV
	Shutdown Current	I_{SHDN}	V_{EN}=0V, T_J=25°C		3	5	μA
	Quiescent Current	I_Q	V_{EN}=2V, V_{FBS} = 0.65V, DCM mode, No Switching		650	850	μA
VCC	UVLO, Rising	$V_{VCC,UVLO}$				2.5	V
	UVLO, Hysteresis	$V_{VCC,HYS}$			100		mV
	Output	V_{CC}	I_{VCC}=0mA	3.1	3.25	3.4	V
	Load regulation	$V_{CC,REG}$	I_{VCC}=25mA		1.8		%
FBS	Reference Voltage	V_{REF}	GNDS = 0V	0.594	0.600	0.606	V
	Error Amp Offset	V_{OS}		-3		3	mV
	Input Current	I_{FBS}	V_{EN}=2V, V_{FBS} = 1V	-50	0	50	nA
Power Switch	On resistance	$R_{DS(ON)HS}$	V_{BS-LX} = 3.3V, T_J=25°C		12.6	18.9	mΩ
	Current Limit	$I_{LMT,HS}$		14	15.5	17	A
Synchronous Rectifier	On resistance	$R_{DS(ON)LS}$	V_{CC} = 3.3V, T_J=25°C		4.3	6.5	mΩ
	Reverse current	$I_{LMT,RVS}$		3.5	4.5	6.6	A
		$t_{RCL,BLK}$		40	60		ns
	Forward current	$I_{LMT,BOT}$	R_{ILMT} = 4.5kΩ		13.3		A
ILMT Pin Output Voltage		V_{ILMT}		0.77	0.8	0.83	V
ILMT Ratio		$I_{ILMT}/I_{LMT,BOT}$	$I_{LMT,BOT}$>5A	12	13.3	14.6	μA/A
Discharge FET Resistance		R_{DIS}			60		Ω
Enable (EN)	Rising Threshold	$V_{EN,R}$		1.16	1.21	1.26	V
	Threshold Hysteresis	$V_{EN,HYS}$			0.23		V
	Input Current	I_{EN}	V_{EN}=2V		0		μA
Soft Start (SS)	Charging current	I_{SS1}	V_{SS}=0V		42		μA
	Discharge current	I_{SS2}	V_{SS}=1V		34		mA
	Min soft-start time	$t_{SS,MIN}$			1		ms
Overvoltage Protection Threshold		V_{OVP}		110	120	130	%V_{FBS}
Undervoltage Protection	threshold	V_{UVP}		45	50	55	%V_{FBS}
	Delay	$t_{UVP,DLY}$			20		μs
UVP/OCP Hiccup ON Time		$t_{HICCUP,ON}$	C_{SS} open		3		ms
UVP/OCP Hiccup OFF Time		$t_{HICCUP,OFF}$	C_{SS} open		15		ms
Power Good	Thresholds	V_{PG}	V_{FBS} falling, fault	76	79	82.5	%V_{FBS}
			V_{FBS} rising, good	88	93.5	97	%V_{FBS}
			V_{FBS} rising, fault	110	120	130	%V_{FBS}
			V_{FBS} falling, good	100	103.5	107.5	%V_{FBS}
	Delay	$t_{PG,R}$	V_{FBS} rising, good		0.8		ms
		$t_{PG,F}$	V_{FBS} falling, fault		20		μs
	Output low voltage	$V_{PG,LOW}$	V_{IN}=0V, 100kΩ from PG to 3.3V		550	750	mV
			V_{IN}=0V, 10kΩ from PG to 3.3V		660	850	mV
			V_{EN} = 2V, V_{FBS} = 0V, I_{PG}=10mA			0.4	V
	Output low leakage	$I_{PG,LKG}$	V_{PG} = 3.3V		3	5	μA

Electrical Characteristics (cont.) V_{IN} = 12V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise specified (4)						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Switching Frequency	f_{SW}	R_{MODE}=0Ω, I_{OUT}=0A, FCCM, V_{OUT}=1V, T_J=25°C	500	600	700	kHz
		R_{MODE}=30.1kΩ, I_{OUT}=0A, FCCM, V_{OUT}=1V, T_J=25°C	710	800	890	
		R_{MODE}=60.4kΩ, I_{OUT}=0A, FCCM, V_{OUT}=1V, T_J=25°C	900	1000	1100	
Min ON Time	$t_{ON,MIN}$	I_{OUT}=3A		55		ns
Min OFF Time	$t_{OFF,MIN}$	I_{OUT}=3A		150		
Thermal Shutdown Temperature	T_{SD}		140	160		˚C
Thermal Shutdown Hysteresis	T_{HYS}			30		

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Package thermal resistance is measured in the natural convection at T_A=25˚C on an 8.5cm×8.5cm size four-layer Silergy Evaluation Board.

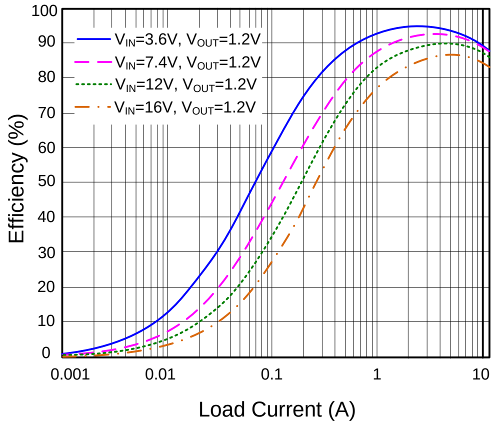
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Production testing is performed at 25˚C; limits at -40°C to +125°C are guaranteed by design, test or statistical correlation.

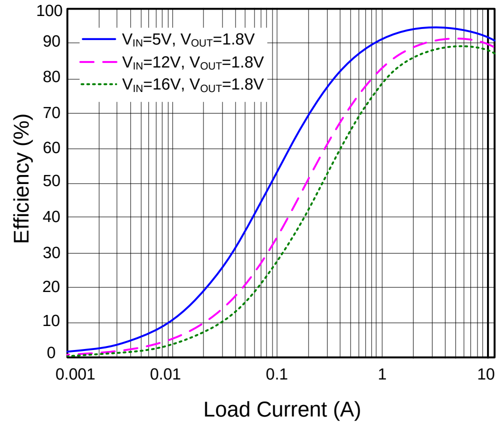
Typical Performance Characteristics

(T_A=25°C, V_{IN}=12V, V_{OUT}=1.2V, L=0.47μH, C_{OUT}=44μF, f_{SW}=600kHz, R_{ILMT}=4.5kΩ, C_{SS}=0.22μF, unless otherwise noted)

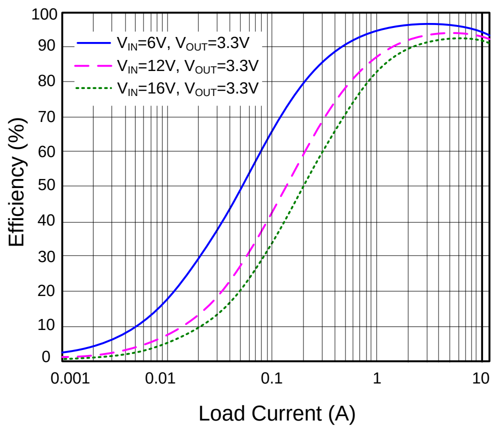
Efficiency vs. Load Current
(f_{SW}=600kHz, FCCM, L=0.47μH/PCMB104T-R47MS)



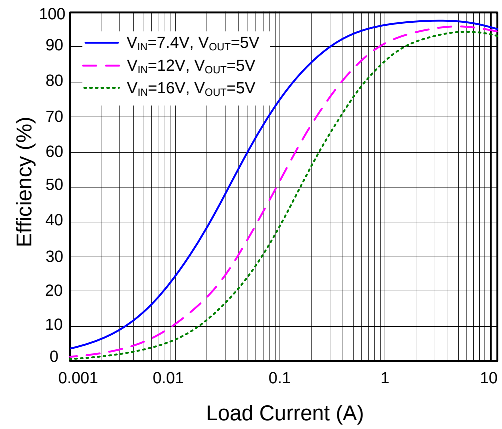
Efficiency vs. Load Current
(f_{SW}=600kHz, FCCM, L=0.47μH/PCMB104T-R47MS)



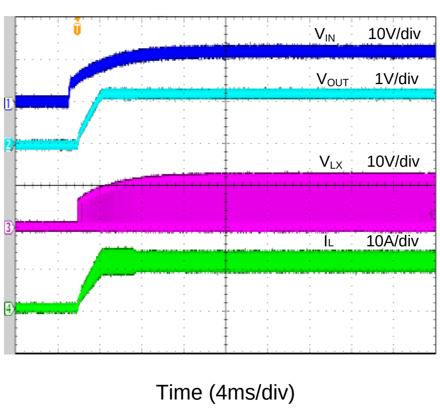
Efficiency vs. Load Current
(f_{SW}=600kHz, FCCM, L=0.68μH/PCMB104T-R68MS)



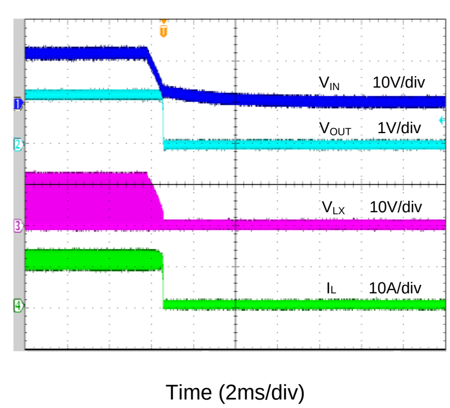
Efficiency vs. Load Current
(f_{SW}=600kHz, FCCM, L=1.0μH/PCMB104T-1R0MS)



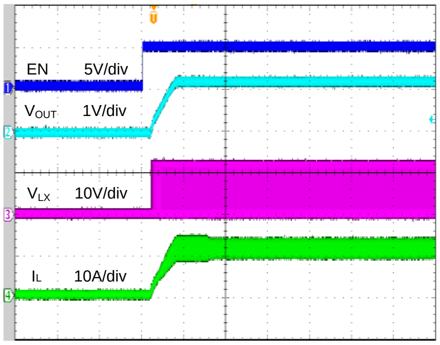
Startup from V_{IN}
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=12A)



Shutdown from V_{IN}
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=12A)

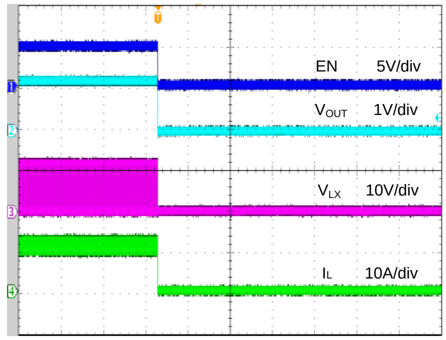


Startup from EN
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=12A)



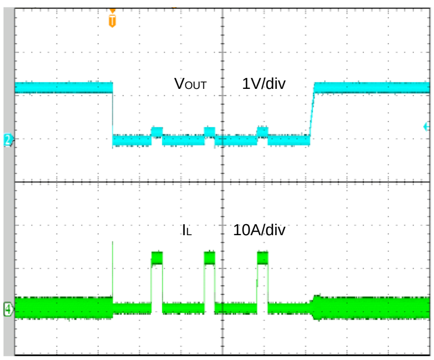
Time (4ms/div)

Shutdown from EN
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=12A)



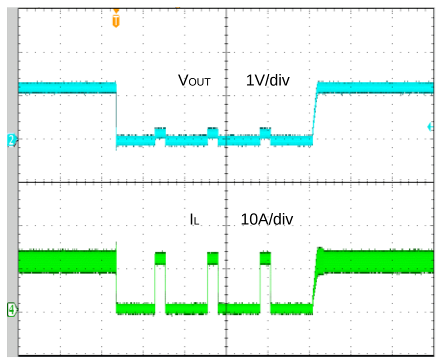
Time (4ms/div)

Short Circuit Protection
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=0A~short, R_{ILMT}=4.5kΩ, FCCM)



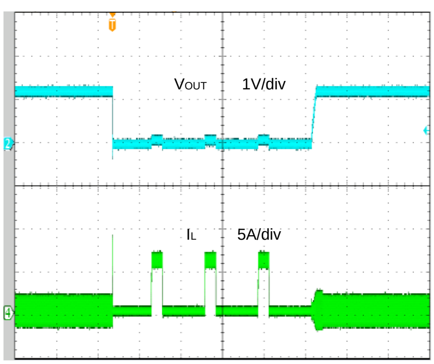
Time (20ms/div)

Short Circuit Protection
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=12A~short, R_{ILMT}=4.5kΩ, FCCM)



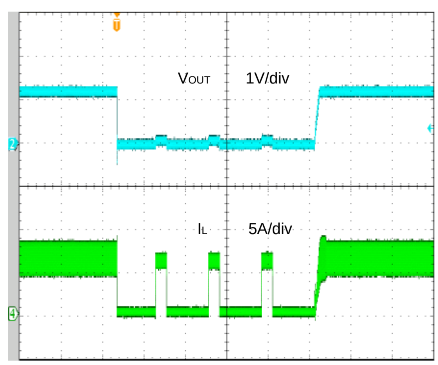
Time (20ms/div)

Short Circuit Protection
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=0A~short, R_{ILMT}=10kΩ, FCCM)



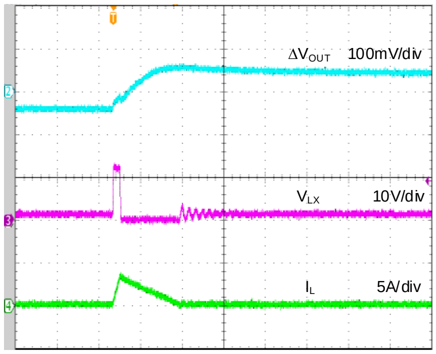
Time (20ms/div)

Short Circuit Protection
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=6A~short, R_{ILMT}=10kΩ, FCCM)



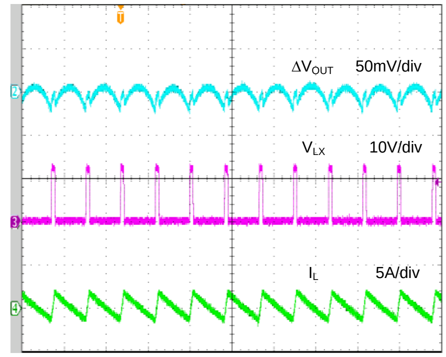
Time (20ms/div)

Output Ripple
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=0A, DCM)



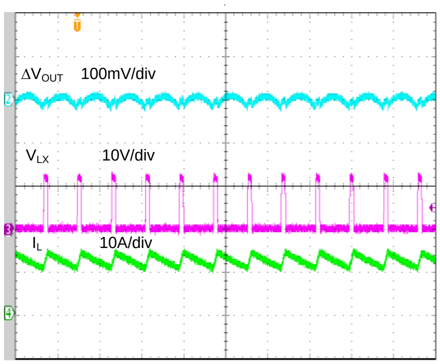
Time (1μs/div)

Output Ripple
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=0A, FCCM)



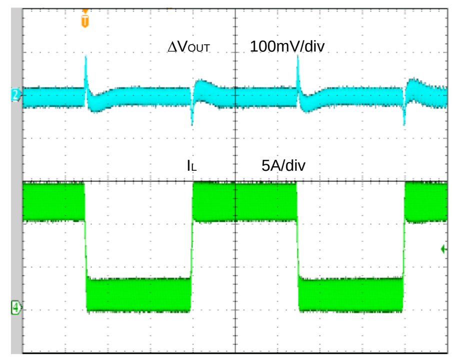
Time (2μs/div)

Output Ripple
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=12A)



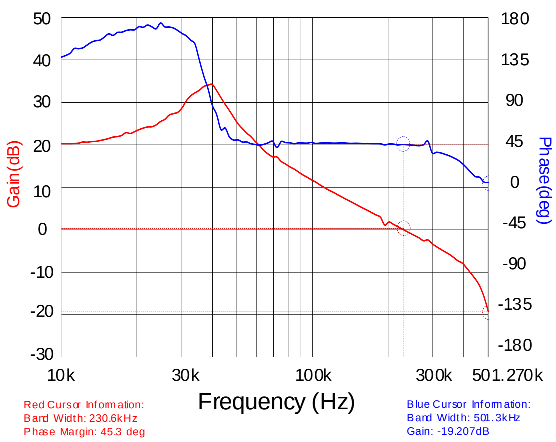
Time (2μs/div)

Load Transient
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=1.2~12A, FCCM)

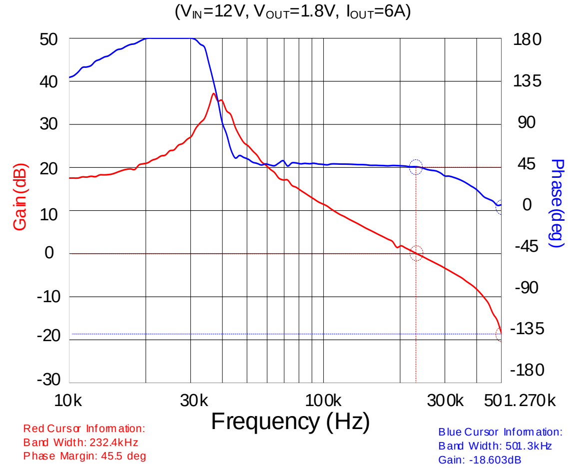


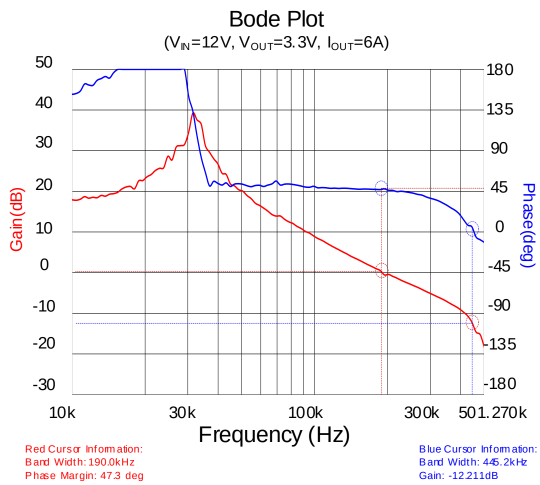
Time (200μs/div)

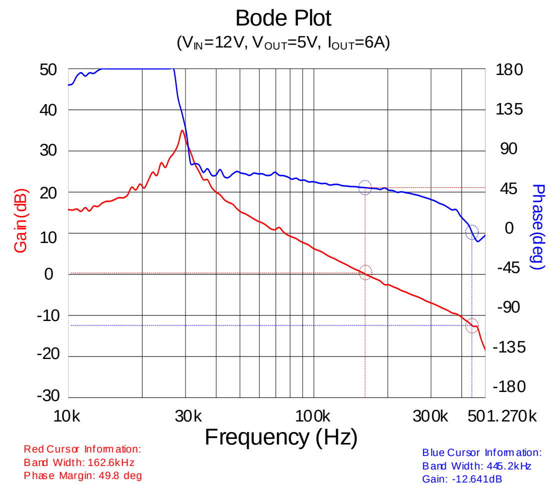
Bode Plot
(V_{IN}=12V, V_{OUT}=1.2V, I_{OUT}=6A)



Bode Plot
(V_{IN}=12V, V_{OUT}=1.8V, I_{OUT}=6A)




Bode Plot
(VIN=12V, VOUT=3.3V, IOUT=6A)
Gain (dB)
Phase(deg)
Frequency (Hz)
Red Cursor Information:
Band Width: 190.0kHz
Phase Margin: 47.3 deg
Blue Cursor Information:
Band Width: 445.2kHz
Gain: -12.211dB


Bode Plot
(VIN=12V, VOUT=5V, IOUT=6A)
Gain (dB)
Phase(deg)
Frequency (Hz)
Red Cursor Information:
Band Width: 162.6kHz
Phase Margin: 49.8 deg
Blue Cursor Information:
Band Width: 445.2kHz
Gain: -12.641dB

Detailed Description

General Features

Constant-on-time Architecture

Fundamental to any constant-on-time (COT) architecture is the one-shot circuit or on-time generator, which determines how long to turn on the high-side power switch. Each on-time (t_{ON}) is a "fixed" period internally calculated to operate the step down regulator at the desired switching frequency considering the input and output voltage ration, $t_{ON}=(V_{OUT}/V_{IN})\times(1/f_{SW})$. For example, consider a hypothetical converter targeting 1.2V output from a 12V input at 600kHz. The target on-time is (1.2V/12V)×(1/600kHz)=167ns. Each t_{ON} pulse is triggered by the feedback comparator when the output voltage as measured at FB drops below the target value. After the t_{ON} period, a minimum off-time ($t_{OFF,MIN}$) is imposed before any further switching is initiated, even if the output voltage is less than the target. This approach avoids making any switching decisions during the noisy periods when the switching node (LX) is rapidly rising or falling.

In a COT architecture, there is no fixed clock, so the high-side power switch can turn on almost immediately after a load transient and subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays. Traditional current- or voltage-mode control methods must simultaneously monitor the feedback voltage, current feedback and internal ramps and compensation signals to determine when to turn off the high-side power switch and turn on the low-side synchronous rectifier. Considering these small signals in a switching environment makes those methods difficult to apply in noisy environments and at low duty cycles.

Instant-PWM Operation

Silergy's instant-PWM control method adds several proprietary improvements to the traditional COT architecture. Whereas most legacy based on COT implementations require a dedicated connection to the output voltage terminal to calculate the t_{ON} duration, instant-PWM derives this signal internally. Another improvement optimizes operation with low ESR ceramic output capacitors. In many applications it is desirable to utilize very low ESR ceramic output capacitors, but legacy COT regulators become unstable in these cases because the beneficial ramp signal that results from the inductor current flowing into the output capacitor may be too small to maintain smooth operation. For this reason, instant-PWM synthesizes a virtual replica of this signal internally. This internal virtual ramp and the feedback voltage are combined and compared to the reference voltage. When the sum is lower than the reference voltage, the t_{ON} pulse is triggered as long as the minimum t_{OFF} has been satisfied and the inductor current as measured in the low-side synchronous rectifier is lower than the current limit. As the t_{ON} pulse is triggered, the low-side synchronous rectifier is turned off if necessary and the high-side power switch is turned on. Inductor current then ramps up linearly during t_{ON}. At the conclusion of t_{ON}, the high-side power switch is turned off, the low-side synchronous rectifier is turned on and the inductor current ramps down linearly. This action also initiates the minimum t_{OFF} timer to ensure sufficient time for stabilizing any transient conditions and settling the feedback comparator before the next cycle is initiated. This minimum t_{OFF} is relatively short so that during fast load transient t_{ON} can be retriggered with minimal delay, allowing the inductor current to ramp quickly to provide sufficient energy to the load.

To avoid shoot-through current, a dead time (t_{DEAD}) is generated internally to ensure that only one switch is on at any time.

Frequency-locked Loop (FLL)

Although COT provides a relatively constant operating frequency over variations in line and load conditions, Silergy's FLL improves the operating frequency performance by comparing the actual operating frequency with an internal reference frequency. The signal that results is used to adjust $t_{ON,}$ resulting in a stable and predictable operating frequency. Note that the FLL is disabled during soft-start and during discontinuous inductor current mode (DCM) conditions. In these cases the operating frequency will be slightly lower than the target.

Light-load Operating Modes

This device supports two user-selectable light load operating modes, set with the MODE input (see table 1). Light load occurs at ~ $I_{OUT} < ½\times\Delta I_L$, when the current through the low-side synchronous rectifier will ramp to near zero before the next t_{ON} time.

Forced continuous inductor current mode (FCCM). In this operating mode, the low-side synchronous rectifier remains on until the next $t_{ON,}$ cycle, allowing continuous current flow in the inductor. The inductor current ramps below zero, recirculating current from the output to the input. This allows the device to maintain a relatively constant switching frequency over the output current range. This reduces efficiency at light loads, but is often desirable in equipment that is sensitive to low frequency operations, such as audio or RF systems.

Discontinuous inductor current mode (DCM). In this operating mode, the low-side synchronous rectifier is turned off when the inductor current reaches zero and remains off, preventing recirculation current that can seriously reduce efficiency under these light load conditions. As load current is further reduced, and the combined feedback and ramp signals remain greater than the reference voltage, the instant-PWM control loop will not trigger another t_{ON} until needed, so the apparent operating switching frequency will drop, further enhancing efficiency. Continuous inductor current mode (CCM) resumes smoothly as soon as the load current increases sufficiently for the inductor current to remain above zero at the time of the next t_{ON} cycle. This threshold of load current may be determined with

$$I_{OUT\_CTL} = \frac{\Delta I_L}{2} = \frac{V_{OUT} \times (1-D)}{2 \times f_{SW} \times L_1}$$

Note that the operating frequency of the device in DCM can be quite low, and may not be desirable in equipment that is sensitive to low frequency operations, such as audio or RF systems.

Switching Frequency

This device supports three user selectable operating frequencies: 600kHz, 800kHz and 1,000kHz. See table 1.

MODE Input

The MODE pin is an input that provides user selectable operating frequency and light-load operating modes. See table 1 for configuration details. Note that this input is evaluated during startup of the device, and changes to the configuration after startup will not change the device operation. Any change in the the configuration requires a restart of the device.

Table 1

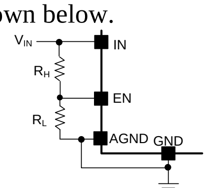
MODE Pin Connection	Light-Load Mode	Switching Frequency
VCC	DCM	600kHz
240kΩ(±20%) to GND	DCM	800kHz
120kΩ(±20%) to GND	DCM	1000kHz
GND	FCCM	600kHz
30kΩ(±20%) to GND	FCCM	800kHz
60kΩ(±20%) to GND	FCCM	1000kHz

Input Under Voltage Lock-out (UVLO)

To prevent operation before all internal circuitry is ready and to ensure that the power and synchronous rectifier switches can be sufficiently enhanced, instant-PWM incorporates UVLO. The device remains in a low current state and all switching actions are inhibited until V_{IN} exceeds the UVLO (rising) threshold. At that time, if EN is enabled, the device will start-up by initiating a soft-start ramp. If V_{IN} subsequenctly falls below $V_{IN,UVLO}$ less the UVLO hysteresis, switching actions will again be suppressed. In some systems, it may be desirable to ensure that the device remains in shutdown until Vin is even higher. See EN input description.

Enable Control (EN)

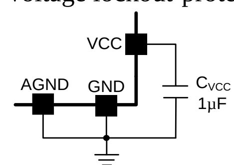
The EN input is a high-voltage capable input with an accurate logic-compatible threshold voltage. In many systems, pulling EN high from Vin to enable the device is sufficient. However, EN may be used to more precisely control startup by taking advantage of the accurate threshold, $V_{EN,R}$ by means of a resistor divider as shown below.



When EN is driven below ~ 0.4V the VCC regulator will be shut down. It is not recommended to connect EN and IN directly. A resistor in a range of 1kΩ to 1MΩ should be used if EN is pulled high by IN.

VCC Linear Regulator

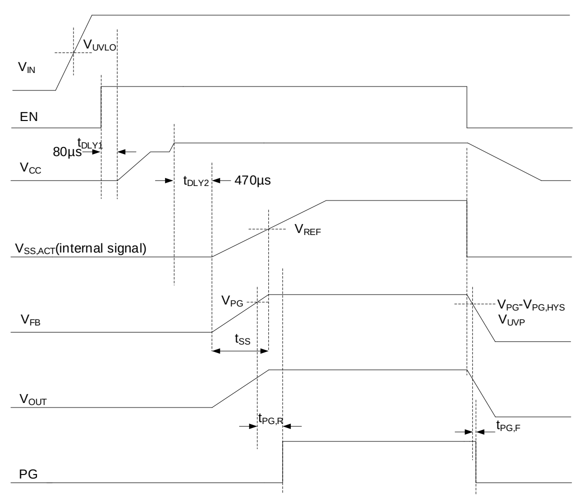
An internal linear regulator (VCC) produces a 3.3V supply from VIN that powers the internal gate drivers, PWM logic, analog circuitry, and other blocks. Connect a 1μF low ESR ceramic capacitor from VCC to GND. This regulator incorporates under-voltage lockout-protection $V_{VCC,UVLO}$.



VCC may also be used to apply an external 3.3V power source, if available. This external bias will allow device operation with V_{IN} as low as 2.9V

Startup and Shutdown

An internal soft-start circuit smoothly ramps the output to the desired voltage whenever the device is enabled. Internally, the soft-start circuit clamps the output at a low voltage and then allows it to rise to the desired voltage over approximately one soft-start time, T_{SS}, which avoids high current flow and transients during startup. The startup and shutdown sequence are shown below.

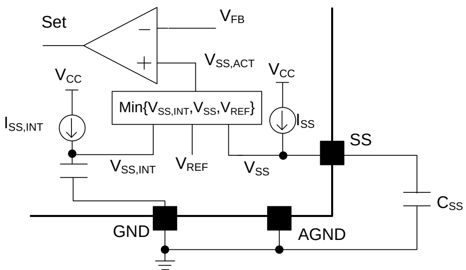


Programmable Soft-start Time and On-time Pre-bias Function

The soft-start time is a minimum of 1ms but may be extended by connecting a capacitor between the SS and AGND pins. The soft-start time equation is:

$$t_{SS}(ms)=\frac{C_{SS}(nF)\times V_{REF}}{I_{SS}(\mu A)}$$

where I_{SS} ~ 42μA.



Increasing t_{SS} with an external capacitor also increases $t_{HICCUP,ON}$ and $t_{HICCUP,OFF}$ proportionally.

During startup where the output is greater than zero, a pre-biased condition, switching will be disabled until the voltage on the internal soft start circuit voltage $V_{SS,ACT}$ exceeds the sensed output voltage at FB. Before switching is initiated, the on-time generator will set t_{ON} to match the pre-bias output voltage.

Note that in a pre-biased scenario, if the BS-LX voltage is lower than 1.8V, the low-side synchronous rectifier will be turned on for one narrow pulse. Any drop in the pre-biased output level as a result is negligible.

GNDS Differential Output Remote Ground Sense

To improve output voltage accuracy at the load, a dedicated remote ground sense pin GNDS is provided. Connect this pin directly to the negative side of the preferred voltage sense point. Short to AGND if remote sense is not used.

Output Discharge Function

An internal ~ 120Ω discharge FET is turned on whenever the shutdown logic is triggered, discharging the output through the inductor. Although only active during the shutdown process, this brings the output to a low voltage state until the device is once again enabled.

Power Good Indicator (PG)

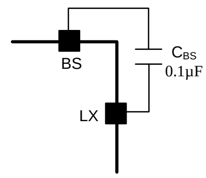
PG is an open drain output controlled by a window comparator connected to the feedback signal. PG allows system monitoring of the device. If V_{FB} is greater than $V_{PG,R}$ and less than V_{OVP} for at least $t_{PG,R}$, PG will be high-impedance.

Connect PG with a resistor in the range 10kΩ~100kΩ to VCC or another voltage source less than 4V. During startup, PG is pulled to GND. After V_{FB} reaches $V_{PG,R}$, PG becomes high-impendance in ~ 800μs, indicating that the output is good. If V_{FB} drops below $V_{PG,F}$, or rises above V_{OVP}, PG is pulled low, if the condition remains for at least the appropriate PG delay. See the Electrical Characteristics table.

PG functionality is active even in the absence of VIN orr VCC, as long as the pull-up power source is available.

External Bootstrap Capacitor Connection

This device integrates a floating power supply for the gate driver that operates the high-side power switch. Proper operation requires a 0.1μF low ESR ceramic capacitor to be connected between BS and LX. This bootstrap capacitor provides the gate driver supply voltage for the high-side N-channel MOSFET power switch.



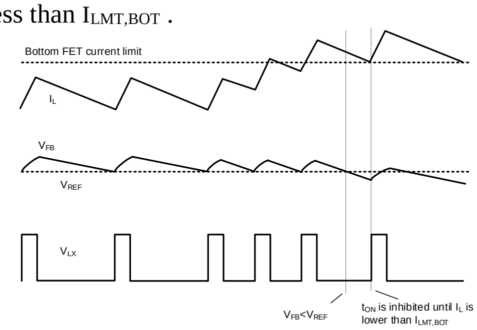
Fault Protection

Over Current Protections (OCP)

Three cycle-by-cycle over-current protections are integrated in this device to prevent excessive current flow. Although current limit protections will not force a shutdown of the device, continuous operation in these conditions are expected to result in the output voltage dropping below the under-voltage protection threshold, or for the junction temperature to rise above the thermal protection limit, which will shut down the device. See UVP and OTP sections.

Valley Current Limit

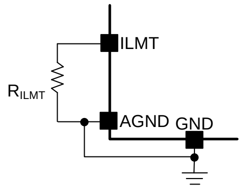
Inductor current is measured in the low-side synchronous rectifier when it turns on and as the inductor current ramps down. If the current exceeds $I_{LMT,BOT}$ the synchronous rectifier is turned off and t_{ON} is inhibited until the current is less than $I_{LMT,BOT}$.



$I_{LMT,BOT}$ may be adjusted by selecting R_{ILIMIT} as follows

$$I_{BOT,LMT}=\frac{V_{ILMT}}{G_{MIRROR}\times R_{ILMT}(\Omega)}$$

where, V_{ILMT} is 0.8V and the low-side synchronous rectifier mirror ratio G_{MIRROR} is ~ 13.3μA/A.



Peak Current Limit

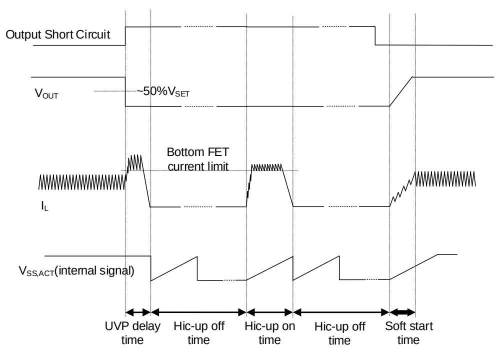
During t_{ON}, and after $t_{ON,MIN}$, if the high-side power switch current exceeds $I_{LMT,HS}$, the switch is turned off, the low-side synchronous rectifier is turned on and t_{ON} is inhibited until the low-side synchronous rectifier current is below $I_{LMT,BOT}$. Peak current limit is disabled during initial t_{ON} at startup.

Reverse Current Limit Protection

In FCCM mode, if the low-side synchronous rectifier current exceeds $I_{LMT,RVS}$ for more than $t_{RCL,BLK}$, the low-side synchronous rectifier is turned off and the high-side power switch is turned on. Reverse current limit is disabled during initial t_{OFF} at startup.

Output Under Voltage Protection (UVP)

After startup, if VBS drops below V_{UVP} for more than $t_{UVP,DLY}$ UVP will be triggered, and the device will shut down for $t_{HICCUP,OFF}$, after which the device will restart with a complete soft start cycle. If the fault condition remains after $t_{HICCUP,ON}$ this 'hiccup' cycle of startup and shutdown will continue unless the junction temperature exceeds T_{SD}. If the fault condition is resolved, the device will resume normal operation

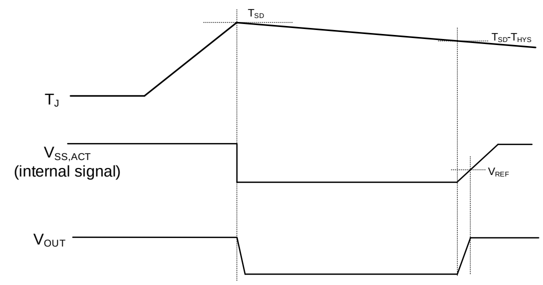


Output Over Voltage Protection (OVP)

If FBS exceeds V_{OVP}, the low-side synchronous rectifier will be turned on in an attempt to bring the FBS below V_{OVP}. If DCM operation has been selected, the low-side synchronous rectifier will remain on until the inductor current reaches zero. If FBS still exceeds V_{OVP}, the operating mode will be changed to FCCM, with the low-side synchronous rectifier remaining on at a very high duty factor, pulling the inductor current as low as $I_{LMT,RVS}$. This continues until FBS is again in regulation or until the junction temperature exceeds T_{SD}.

Over Temperature Protection (OTP)

The over temperature protection (OTP) circuitry prevents overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds T_{SD}. Once the junction temperature cools down by approximately 30°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the T_{SD}.

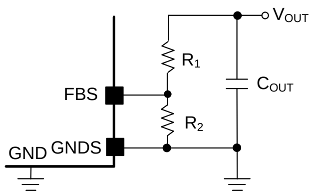


Design Procedure

Feedback Resistor Selection

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is strongly recommended for both resistors. If V_{SET} is 1.2V, R_1=100kΩ is chosen, then using following equation, R_2 can be calculated to be 100kΩ.

$$R_2 = \frac{0.6V}{V_{SET}\text{-}0.6V} \times R_1$$



Input Capacitor Selection

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply and to reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X5R or X7R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current,

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

On the other hand, the input capacitor value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated by

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1\text{-}D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications two22µF X5R capacitors is sufficient. Take care to locate the ceramic input capacitor as close to the device IN and GND pin as possible.

Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage.

Instant-PWM operates well over a wide range of inductor values. This flexibility allows for optimization to find the best trade-off of efficiency, cost and size for a particular application. Selecting a low inductor value will help reduce size and cost and enhance transient response, but will increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low value inductors may help reduce DC losses and increase efficiency. On the other hand, higher inductor values tend to have higher DCR and will slow transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a ripple current (ΔI_L) about 20% ~ 50% of the desired full output load current. Start calculating the approximate inductor value by selecting the input and output voltages, the operating frequency (f_{SW}), the maximum output current ($I_{OUT,MAX}$) and estimating a ΔI_L as some percentage of that current.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current (ΔI_L) and required peak current inductor current $I_{L,PEAK}$.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L_1}$$

And $I_{L,PEAK} = I_{OUT,MAX} + \Delta I_L/2$

Select an inductor with a saturation current and thermal rating in excess of $I_{L,PEAK}$.

If FCCM light load operation is selected, make sure the inductor value is high enough to avoid reverse current limit is been triggered just under steady state if the load current is zero.

For highest efficiency, select an inductor with a low DCR that meets the inductance, size and cost targets. Low loss ferrite materials should be considered.

Inductor Design Example

Consider a typical design for a device providing $1.2V_{OUT}$ at 12A from $12V_{IN}$, operating at 600kHz and using target inductor ripple current (ΔI_L) of 50% or 6A. Determine the approximate inductance value at first:

$$L_1 = \frac{1.2V \times (12V - 1.2V)}{12V \times 600kHz \times 6A} = 0.3\mu H$$

Next, select the nearest standard inductance value, in this case 0.33μH, and calculate the resulting inductor ripple current (ΔI_L):

$$\Delta I_L = \frac{1.2V \times (12V - 1.2V)}{12V \times 600kHz \times 0.33\mu H} = 5.45A$$

$I_{L,PEAK}$ =12A + 5.45A/2 =14.725A

The resulting 5.45A ripple current is 5.45A/12A is ~45.4%, well within the 20% ~ 50% target.

$I_{L,PEAK,RVS}$ = 5.45A/2 =2.725A < $I_{LIM,RVS}$

Finally, select an available inductor with a saturation current higher than the resulting $I_{L,PEAK}$ of 14.725A.

Output Capacitor Selection

Instant-PWM provides excellent performance with a wide variety of output capacitor types. Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the transient response and output voltage ripple requirements of the system.

Output Ripple

Output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitors ESR (ESR ripple) as well as the stored charge (capacitive ripple). When considering total ripple, both should be considered.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Consider a typical application with ΔI_L = 5.45A using two22μF ceramic capacitors, each with an ESR of ~5mΩ for parallel total of 44μF and 2.5mΩ ESR.

$$V_{RIPPLE,ESR} = 5.45A \times 2.5m\Omega = 13.6mV$$

$$V_{RIPPLE,CAP} = \frac{5.45A}{8 \times 44\mu F \times 600kHz} = 25.8mV$$

Total ripple = 39.4mV. The actual capacitive ripple may be higher than calculated value because the capacitance decreases with the voltage on the capacitor.

Using a 150μF 40mΩ POS cap, the above result is

$$V_{RIPPLE,ESR} = 5.45A \times 40m\Omega = 218mV$$

$$V_{RIPPLE,CAP} = \frac{5.45A}{8 \times 150\mu F \times 600kHz} = 7.56mV$$

Total ripple =225mV

Output Transient Undershoot/Overshoot

If very fast load transient must be supported, consider the effect of the output capacitor on the output transient undershoot and overshoot. Instant-PWM responds quickly to changing load conditions, however, some considerations must be needed, especially when using small ceramic capacitors which have low capacitance at low output voltages which results in insufficient stored energy for load transient. Output transient undershoot and overshoot have two causes: voltage changes caused by the ESR of the output capacitor and voltage changes caused by the output capacitance and inductor current slew rate.

ESR undershoot or overshoot may be calculated as $V_{ESR}=\Delta I_{OUT} \times ESR$. Using the ceramic capacitor example above and a fast load transient of ±6A, V_{ESR} = ±6A × 2.5mΩ = ±15mV. The POS capacitor result with the same load transient, V_{ESR} = ±6A × 40mΩ = ±240mV.

Capacitive undershoot(load increasing) is a function of the output capacitance, the load step, the inductor value and the input-output voltage difference and the maximum duty factor. During a fast load transient, the maximum duty factor of instant-PWM is a function of t_{ON} and the minimum t_{OFF} as the control scheme is designed to rapidly ramp the inductor current by grouping together many t_{ON} pulses in this case. The maximum duty factor D_{MAX} may be calculated by

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF,MIN}}$$

Given this, the capacitive undershoot may be calculated by

$$V_{UNDERSHOOT,CAP} = -\frac{L_1 \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times (V_{IN,MIN} \times D_{MAX} - V_{OUT})}$$

Consider a 6A load increase using the ceramic capacitor case when V_{IN} = 12V.At V_{OUT} = 1.2V, the result is t_{ON} = 167ns, $t_{OFF,MIN}$ = 150ns, D_{MAX} = 167 / (167 + 150) =0.526 and

$$V_{UNDERSHOOT,CAP} = -\frac{0.33\mu H \times (6A)^2}{2 \times 44\mu F \times (12V \times 0.526 - 1.2V)} = -26.4mV$$

Using the POS capacitor case, the above result is

$$V_{UNDERSHOOT,CAP} = -\frac{0.33\mu H \times (6A)^2}{2 \times 150\mu F \times (12V \times 0.526 - 1.2V)} = -7.7mV$$

Capacitive overshoot (load decreasing) is a function of the output capacitance, the inductor value and the output voltage.

$$V_{OVERSHOOT,CAP} = \frac{L_1 \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times V_{OUT}}$$

Consider a 6A load decrease using the ceramic capacitor case above. At V_{OUT} = 1.2V the result is

$$V_{OVERSHOOT,CAP} = \frac{0.33\mu H \times (6A)^2}{2 \times 44\mu F \times 1.2V} = 112.5mV$$

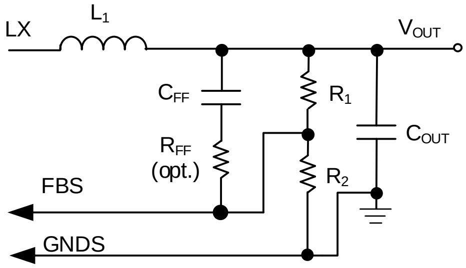
Using the POS capacitor case, the above result is

$$V_{OVERSHOOT,CAP} = \frac{0.33\mu H \times (6A)^2}{2 \times 150\mu F \times 1.2V} = 33mV$$

Combine the ESR and capacitive undershoot and overshoot to calculate the total overshoot and undershoot for a given application.

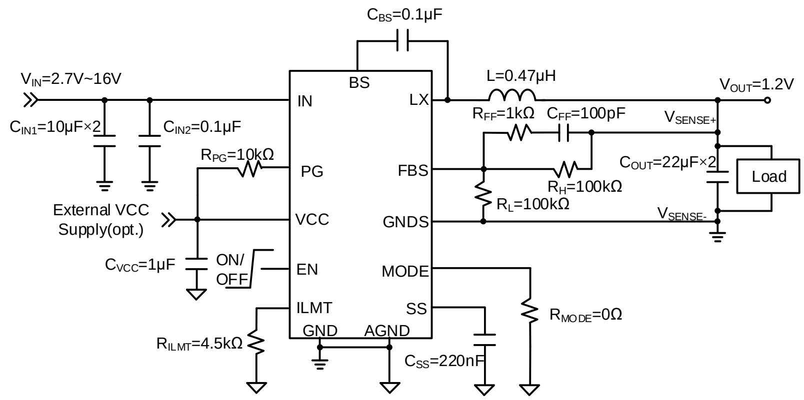
Load Transient Considerations:

The SY26172 adopts the instant PWM architecture to achieve good stability and fast transient responses. In applications with high step load current, adding an RC feed-forward compensation network R_{FF} and C_{FF} may further speed up the load transient responses. R_{FF} = 1kΩ and C_{FF} = 220pF have been shown to perform well in most applications. Increase C_{FF} will speed up the load transient response if there is no stability issue.



Note that when C_{OUT}> 500μF and minimum load current is low, set feed-forward values as R_{FF} = 1kΩ and C_{FF}> 2.2nF to provide sufficient ripple to FB for small output ripple and good transient behavior.

Application Schematic (V_{OUT}=1.2V)



BOM List

Designator	Description	Part Number	Manufacturer
C_{IN1}	10µF/25V/X5R,1206	GRM21BR61E106MA73L	mµRata
C_{IN2}	0.1µF/50V/X5R, 0603	GRM188R61H104KA93D	mµRata
C_{FF}	100pF/50V/C0G,0603	GRM1885C1H101JA01D	muRata
C_{OUT}	22µF/10V/X5R, 1206	GRM31CR61A226ME19L	mµRata
C_{SS}	220nF/50V/X5R, 0603	GRM188R61H224KAC4	mµRata
C_{BS}	0.1µF/50V/X5R, 0603	GRM188R61H104KA93D	mµRata
C_{VCC}	1.0µF/25V/X5R, 0603	GRM155R61E105KE11D	mµRata
L	0.47µH, inductor	PCMB104T-R47MS	CYNTEC
R_H	100kΩ, 1%, 0603		
R_L	100kΩ, 1%, 0603		
R_{PG}	10kΩ, 1%, 0603		
R_{MODE}	0Ω, 1%, 0603		
R_{ILMT}	4.5kΩ, 1%, 0603		
R_{FF}	1kΩ, 1%, 0603		

Recommend Table for Typical Applications

V_{OUT}(V)	R_H(kΩ)	R_L(kΩ)	C_{FF}(pF)	L/(Rated/Saturating Current)	C_{OUT}
1.2	100	100	100	0.47µH/(18A/20A)	22µF×2/10V/X7R,1206
1.8	100	49.9	100	0.47µH/(18A/20A)	22µF×2/10V/X7R,1206
3.3	100	22.1	220	0.68µH/(18A/20A)	22µF×2/10V/X7R,1206
5	100	13.7	220	1.0µH/(18A/20A)	22µF×2/10V/X7R,1206

Thermal Design Considerations

Maximum power dissipation depends on the thermal resistance of the IC package, the PCB layout, the surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation may be calculated by:

$P_{D,MAX} = (T_{J,MAX} - T_A) / \theta_{JA}$

Where, $T_{J,MAX}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

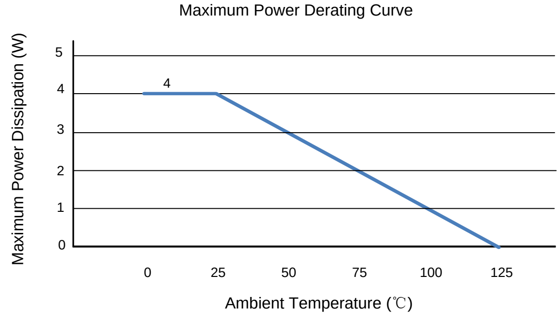
To comply with the recommended operating conditions, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For the QFN3×4-21 package the thermal resistance θ_{JA} is 25°C/W when measured on a standard Silergy four-layer thermal test board. These standard thermal test layouts have a very large area with long 2oz. copper traces connected to each IC pin and very large, unbroken 1oz. internal power and ground planes.

Meeting the performance of the standard thermal test board in a typical tiny evaluation board area requires wide copper traces well-connected to the IC's backside pads leading to exposed copper areas on the component side of the board as well as good thermal via from the exposed pad connecting to a wide middle-layer ground plane and, perhaps, to an exposed copper area on the board's solder side.

The maximum power dissipation at T_A=25℃ may be calculated by the following formula:

$P_{D,MAX}$ = (125℃ − 25℃) / (25℃/W) = 4W

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J,MAX}$ and thermal resistance θ_{JA}. Use the derating curve in figure below to calculate the effect of rising ambient temperature on the maximum power dissipation.



Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation.

- Place the major MLCC capacitors (C_{IN}, C_{OUT}, C_{VCC}) on the same layer as the device.
- Place the input capacitor very near IN and GND, minimizing the loop formed by these connections. Avoid using direct vias connection in the power trace between the input capacitors and IN 、GND to reduce parasitic inductance.
- Place one smaller package input MLCC capacitor at the reach out port of pin21. This capacitor can be connected with GND by vias.
- Place the VCC capacitor close to VCC using short, direct connections instead of vias connection to device GND pins.
- Make one Kelvin connection between AGND and GND at the C_{VCC} negative sides.
- Place the feedback components (R_1, R_2, R_{FF} and C_{FF}) as close to the FBS pin as possible. Avoid routing the remote output sense line and remote GND sense (GNDS) line near LX, BS or other high frequency signal as they are noise sensitive.
- Make the feedback sampling point Kelvin connect with C_{OUT} rather than the inductor output terminal.
- Guarantee the C_{OUT} negative sides are connected with GND pin by wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.
- The LX connection has large voltage swings and fast edges and can easily radiate noise to adjacent components. Keep its area small to prevent excessive EMI, while providing wide copper traces to minimize parasitic resistance and inductance. Keep sensitive components away from the switching node or provide ground traces between for shielding, to prevent stray capacitive noise pickup.
- Place the BS capacitor on the same layer as the device; keep the BS voltage path (BS, LX and C_{BS}) as short as possible.
- It is not recommended to connect control signals and IN directly. A resistor in a range of 1kΩ to 1MΩ should be used if they are pulled high by IN.
- Provide dedicated wide copper traces for the power path ground between the IC and the input and output capacitor grounds, rather than connecting each of these individually to an internal ground plane.
- The exposed GND pad should be connected to a large copper area and place several GND vias on it for heat sinking and to minimize noise.
- A four-layer layout is strongly recommended to achieve better thermal performance. 8.5cm × 8.5cm, four-layer PCB with 2-oz copper used as example.
- Keep the high current traces (IN, GND, LX and OUT trances) as short and wide as possible.
- The top layer and bottom layer should place power IN and GND copper plane as wide as possible. Middle1 layer should place all GND layer for conducting heat and shielding middle2 layer signal line from top layer crosstalk. Place signal lines on middle2 layer instead of other layers to avoid top and bottom GND layer be cut apart.

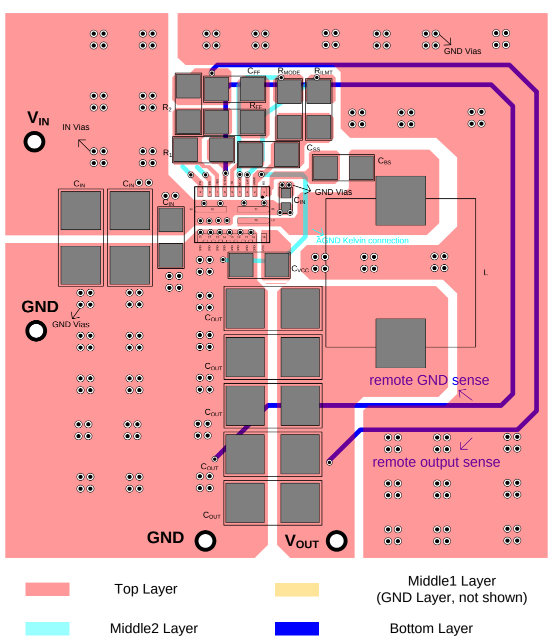
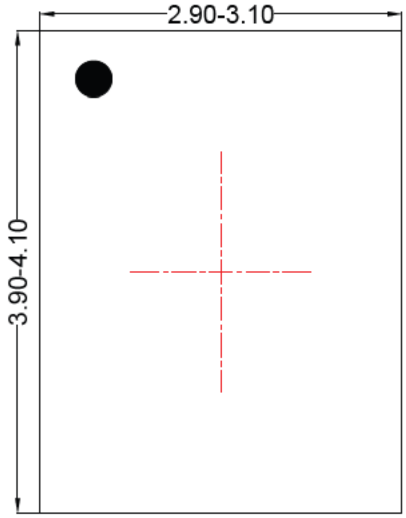
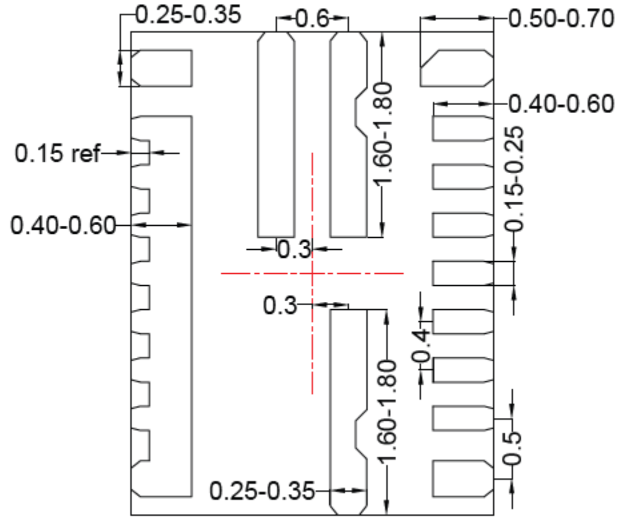


Figure4. PCB Layout Suggestion

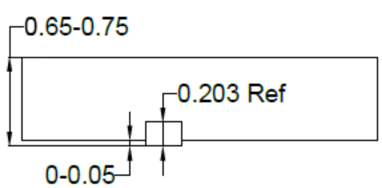
QFN3×4-21 Package Outline Drawing



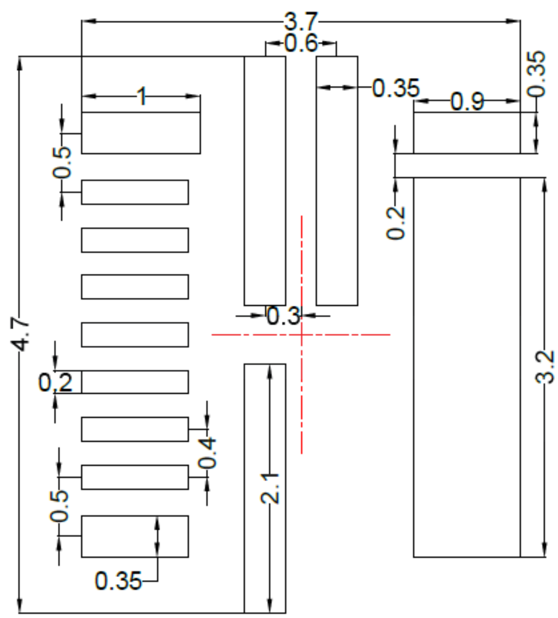
Top View



Bottom View



Front View

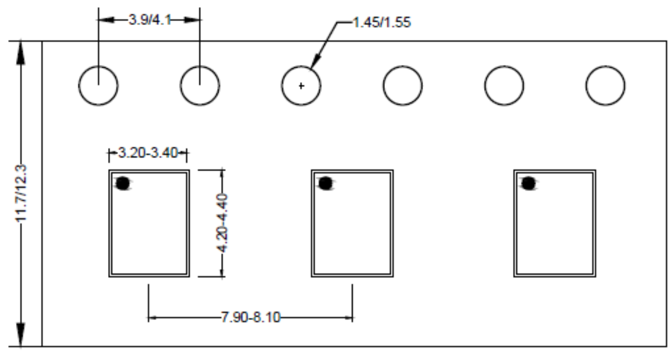


Recommended PCB layout (Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr;center line refers chip body center.

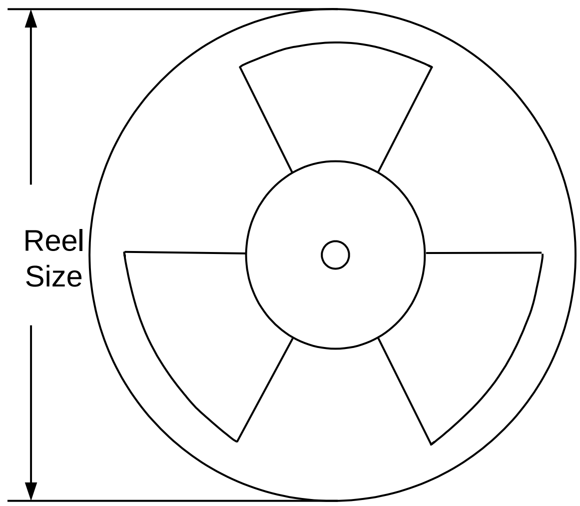
Taping & Reel Specification

1. Package orientation



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length (mm)	Leader length (mm)	Qty per reel
QFN3×4	12	8	13"	400	400	5000

Revision History

Revision Number	Revision Date	Description	Pages changed
0.9	06/01/2021	Initial Release	-
0.9A	09/24/2021	The Absolute Maximum Ratings of the Supply Input Voltage changes from (-0.3V to 17V) to (-0.3V to 18V).	Page 3
0.9B	06/15/2022	Update the package outline drawing (Bottom View)	Page 18
1.0	03/07/2023	Upgrade the version code to Rev1.0 (No change in specification)	-

Revision history is for reference only and may not be comprehensive or complete.

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