SY24105B

Analog Class-D Audio IC

General Description

The SY24105B is a Class-D audio power amplifier with analog input and high-power efficiency for driving bridged-tied mono speaker with up to 60W/4Ω. The high efficiency of the SY24105B eliminates the need for an external heat sink when playing music.

The SY24105B advanced oscillator/PLL circuit employs a multiple switching frequency option to avoid AM interference, this is achieved together with an option of Master and Slave synchronization, making it possible to synchronize multiple devices.

The SY24105B is fully protected against faults including short circuit, over temperature, DC error, under voltage and over voltage. The short circuit, over temperature and DC error protection includes an auto-recovery feature. The under voltage and over voltage protection with hysteresis can be self-cleared.

Ordering Information

SY24105 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY24105BQEC	QFN5×5-32	

Features

- 60W into a 4Ω Load @ 10% THD+N from a 24V Supply
- Wide Supply Voltage Range from 5.6V to 26 V
- Differential and Single-ended Inputs
- Internal Feedback Control with High PSRR
- High Efficient Class-D Operation Eliminates Need for Heat Sinks
- AM Avoidance
- Master/Slave Mode Synchronization
- Four Fixed-gain Controlled: 20dB, 26dB, 32dB and 36dB
- Selectable BD Mode and 1SPW Mode Modulation
- Integrated Protection Circuits Including Over Voltage, Under Voltage, Over Temperature, DC Error, and Short Circuit
- Comprehensive Click and Pop Suppression
- Space-Saving Surface Mount 32-Pin QFN 5mmx5mm Package

Applications

- Powered Speakers
- Music Instruments
- Boom Box
- Consumer Audio Applications

Typical Application

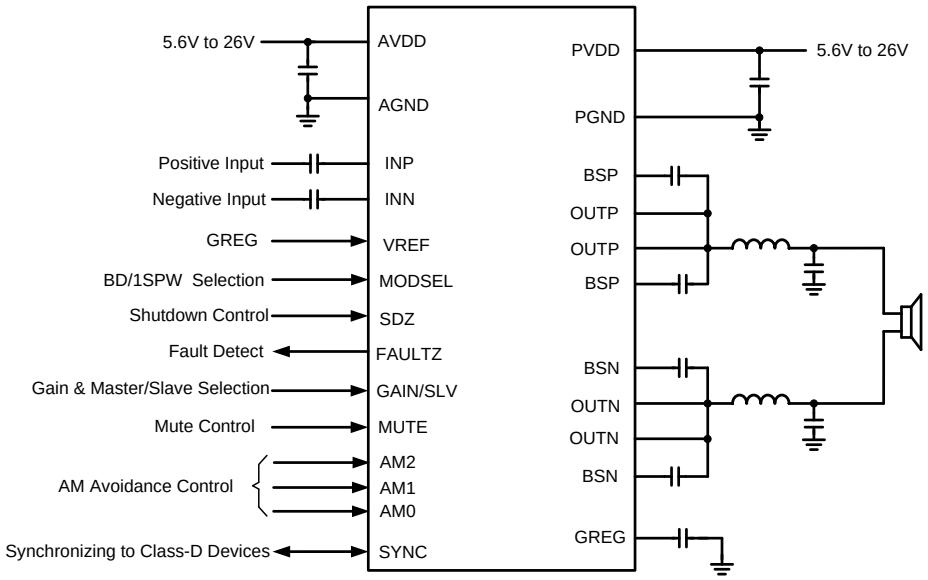
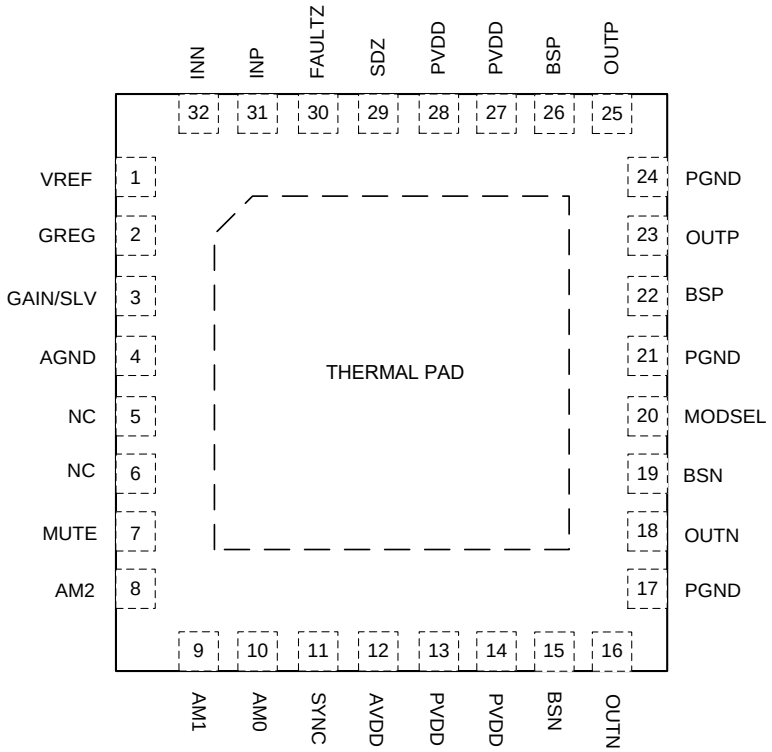


Figure 1. Typical Application Circuit

Pin out (Top View)



(QFN5×5-32)

Top Mark: ENA*xyz* (device code: ENA, ***x=year code, y=week code, z= lot number code)***

Name	No.	Description
VREF	1	Internal reference pin. Connect to GREG directly.
GREG	2	Gate drive supply. Nominal voltage is 3.4V.
GAIN/SLV	3	Gain & Master/Slave mode selection depending on voltage divider from GREG to GND.
AGND	4	Analog Ground.
NC	5	Not Connected.
NC	6	Not Connected.
MUTE	7	Mute pin (high=mute, low=unmute), TTL logic levels with compliance to AVDD.
AM2	8	AM avoidance frequency selection.
AM1	9	AM avoidance frequency selection.
AM0	10	AM avoidance frequency selection.
SYNC	11	Clock input/output for synchronizing other Class-D devices. Determined by Gain/SLV pin.
AVDD	12	Analog power supply. Not internally connected to PVDD.
PVDD	13,14,27, 28	Power supply.
BSN	15,19	Bootstrap for negative high-side FET.
OUTN	16,18	H-bridge negative output.
PGND	17,21,24	Power Ground.
MODSEL	20	Mode selection (low=BD, high=1SPW), TTL logic levels with compliance to AVDD
BSP	22,26	Bootstrap for positive high-side FET.
OUTP	23,25	H-bridge positive output.

SDZ	29	Shutdown pin (low = enter shutdown, high = exit shutdown). TTL logic levels with compliance to AVDD.
FAULTZ	30	Open drain output used to display general fault, including SCP, OTP, DCP fault status (low=fault, high=normal).
INP	31	Positive audio input. Biased at 1.7V.
INN	32	Negative audio input. Biased at 1.7V
Thermal Pad	33	Connect to GND for best system performance.

Block Diagram

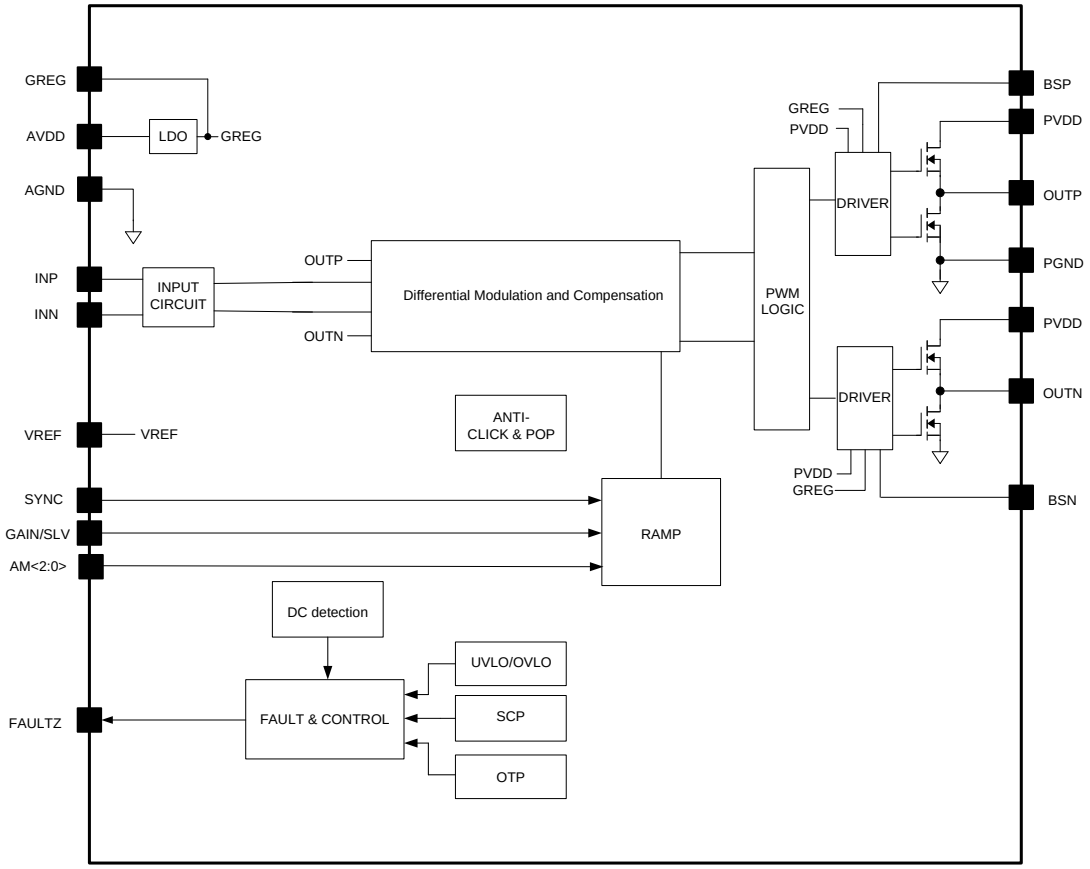


Figure 2. Block Diagram

Absolute Maximum Ratings (Note 1)

AVDD, PVDD ---------- -0.3V to 30V
INP, INN ---------- -0.3V to 3.6V
MODSEL, SDZ, MUTE, AM2, AM1, AM0 ---------- -0.3V to PVDD + 0.3V
VREF, GAIN/SLV, SYNC ---------- -0.3V to GREG+0.3V
Minimum Load Resistance Output Configuration ---------- 2.5Ω
Junction Temperature (T_J) ---------- -40°C to +150°C
Storage Temperature ---------- -40°C to +125°C
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 22°C/W
θ_{JC} ---------- 8°C/W

Recommended Operating Conditions

Supply Voltage Range ---------- 5.6V to 26V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(T_A = 25°C, V_{DD}=18V, R_L=4Ω, Gain=26dB, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DC Characteristics						
AVDD, PVDD	V_{DD}		5.6		26	V
Quiescent Supply Current	I_Q	SDZ=high, no load or filter (Note 4)		28.5		mA
		SDZ=high,with snubber and LC:10μH+680nF(Note 4)		37.7		
		SDZ=Low, no load		100	122	μA
High-level Input Voltage	V_{IH}	SDZ, SYNC, MUTE, AM2, AM1, AM0	2.05			V
		MODSEL (Note 4)		1.75		
Low-level Input Voltage	V_{IL}	SDZ, SYNC, MUTE, AM2, AM1, AM0			0.75	V
		MODSEL (Note 4)		1		
Low-level Output Voltage	V_{OL}	FAULTZ, $R_{PULL-UP}$=100k, PVDD=26V		0.22		V
High-level Input Current	I_{IH}	MODESEL, MUTE, AM2, AM1, AM0, V_I= 2V	-0.1		0.1	μA
		SDZ, V_I= 2V	4	6	8	
Drain-Source On-State Resistance	$R_{DS(ON)}$			60		mΩ
Gain(Master)	G	R1=Open, R2=5.6kΩ, no load (Note 4)		20		dB
		R1=100kΩ, R2=20kΩ, no load	25.5	26	26.5	
		R1=100kΩ, R2=39kΩ, no load (Note 4)		32		
		R1=75kΩ, R2=47kΩ, no load (Note 4)		36		
Gain(Slave)	G	R1=51kΩ, R2=51kΩ, no load (Note 4)		20		dB
		R1=47kΩ, R2=75kΩ, no load (Note 4)		26		
		R1=39kΩ, R2=100kΩ, no load (Note 4)		32		
		R1=16kΩ, R2=100kΩ, no load	35.5	36	36.5	
Turn-on Time(Note 4)	t_{ON}	SDZ=High		45		ms
Turn-off Time(Note 4)	t_{OFF}	SDZ=Low		1		μs
Output Offset Voltage	$\|V_{OS}\|$	V_{IN}=0Vrms, Measured Differentially at V_{DD} =18V		1.5	15	mV
Gate Drive Supply	GREG	SDZ=2V, V_{IN}=0Vrms	3.2	3.4	3.6	V
PWM Frequency	f_{PWM}	AM2=0,AM1=0,AM0=0	350	400	428	kHz
		AM2=0,AM1=0,AM0=1	437.5	500	535	
		AM2=0,AM1=1,AM0=0	525	600	642	
		AM2=0,AM1=1,AM0=1	875	1000	1070	
		AM2=1,AM1=0,AM0=0	1050	1200	1284	
		AM2=1,AM1=0,AM0=1	Reserved			
		AM2=1,AM1=1,AM0=0	Reserved			
		AM2=1,AM1=1,AM0=1	Reserved			
AC Characteristics(Note 4)						
Output Integrated Noise	V_n	20Hz to 22kHz, A-weighted filter, Gain=20dB		65		μV
Signal to Noise Ratio	SNR	Max output at THD+N<1%, V_{DD}=6V, f=1kHz, Gain=20dB, A-weighted		96		dB

		Max output at THD+N<1%, V_{DD}=12V, f=1kHz, Gain=20dB, A-weighted		102		
		Max output at THD+N<1%, V_{DD}=18V, f=1kHz, Gain=20dB, A-weighted		106		
		Max output at THD+N<1%, V_{DD}=24V, f=1kHz, Gain=20dB, A-weighted		108		
		Max output at THD+N<1%, VDD=18V, f=1kHz, Gain=20dB, A-weighted, R_L=8Ω		106		
Total Harmonic Distortion + Noise	THD+N	V_{DD}=6V, f=1kHz, Po=1W		0.04		%
		V_{DD}=12V, f=1kHz, Po=1W		0.033		
		V_{DD}=12V, f=1kHz, Po=7.8W		0.07		
		V_{DD}=18V, f=1kHz, Po=1W		0.028		
		V_{DD}=18V, f=1kHz, Po=17W		0.279		
		V_{DD}=24V, f=1kHz, Po=1W		0.025		
		V_{DD}=24V, f=1kHz, Po=30W		0.456		
		V_{DD}=18V, f=1kHz, R_L=8Ω, Po=1W		0.012		
		V_{DD}=18V, f=1kHz, R_L=8Ω, Po=9.5W		0.059		
Output Power	P_O	V_{DD}=6V, f=1kHz, 1% THD+N		3.9		W
		V_{DD}=6V, f=1kHz, 10% THD+N		4.9		
		V_{DD}=12V, f=1kHz, 1% THD+N		15.6		
		V_{DD}=12V, f=1kHz, 10% THD+N		19.7		
		V_{DD}=18V, f=1kHz, 1% THD+N		35		
		V_{DD}=18V, f=1kHz, 10% THD+N		43.7		
		V_{DD}=24V, f=1kHz, 1% THD+N		61		
		V_{DD}=18V, R_L=8Ω, f=1kHz, 1% THD+N		19.3		
		V_{DD}=18V, R_L=8Ω, f=1kHz, 10% THD+N		24		
Power Supply Rejection Ratio	PSRR	200mV_{PP} ripple, f=1kHz, Gain=20dB		-64.5		dB
Protection						
V_{DD} Under Voltage Lockout Voltage	V_{UVLO_RISE}	V_{DD} Rising		5.5	5.6	V
	V_{UVLO_FALL}	V_{DD} Falling	4.9	5.2	5.3	V
V_{DD} Over Voltage Lockout Voltage	V_{OVLO_RISE}	V_{DD} Rising		31	32.5	V
	V_{OVLO_FALL}	V_{DD} Falling	26.5	28		V
Short Circuit Protection Current Limit (Note 4)	I_{SC}			28		A
Thermal Shutdown Temperature (Note 4)	T_{SD}			150		℃

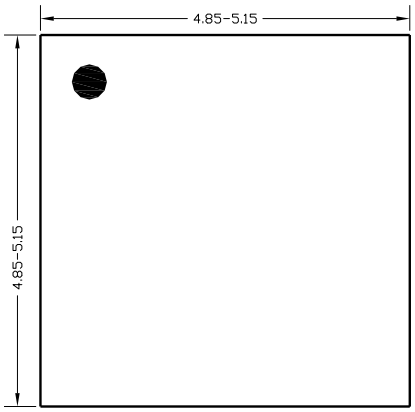
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: DC voltage rating could be derated a little according to the possible switching spike on switching node if the snubber is not appropriate enough.

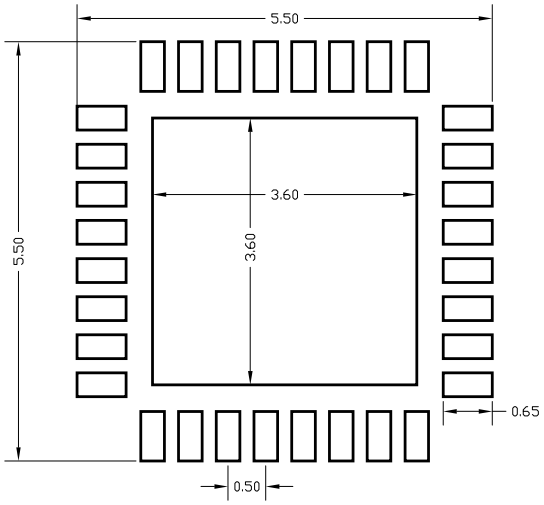
Note 3: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4: Typical test value on demonstration board, guarantee by design.

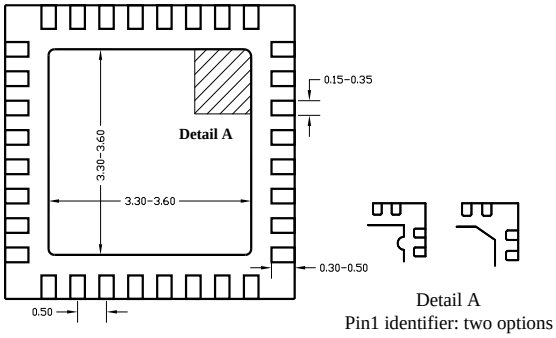
QFN5×5-32 Package Outline & PCB Layout



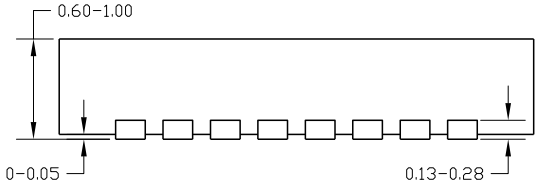
Top View



PCB layout (Recommended)



Bottom View

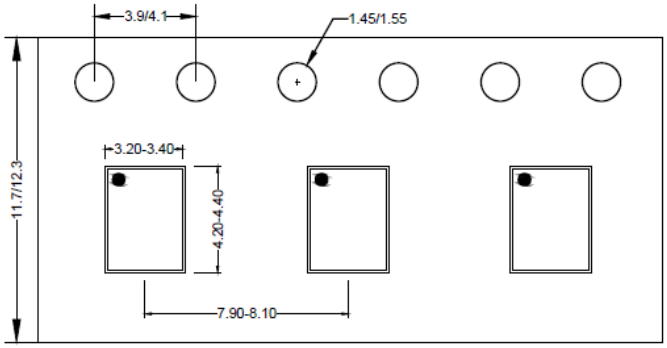


Side View

Notes: All dimension in millimeter and exclude mold flash & metal burr

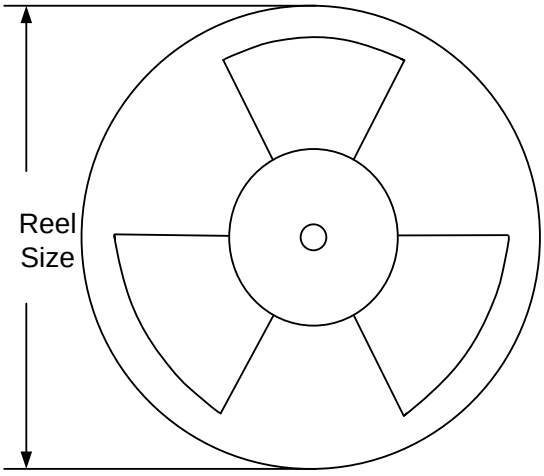
Taping & Reel Specification

1. QFN5×5 taping orientation



Feeding direction

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN5x5	12	8	13"	400	400	5000

Others: NA.

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Apr.25, 2023	Revision 1.0	Production Release
Apr.25, 2022	Revision 0.9A	1. modify the MUTE PIN description as: Mute pin (High=mute, Low=unmute), TTL logic levels with compliance to AVDD. 2. modify the SDZ PIN description as: Shutdown pin (low = enter shutdown, high = exit shutdown). TTL logic levels with compliance to AVDD.
Jan. 5, 2017	Revision 0.9	Initial Release

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